High-Performance Data Readout and the HGCAL Electronics

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Contribution to the
CALICE Collaboration Meeting

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Karlsruhe Institute of Technology

Institute for Data Processing and Electronics

CMS High Granularity Calorimeter

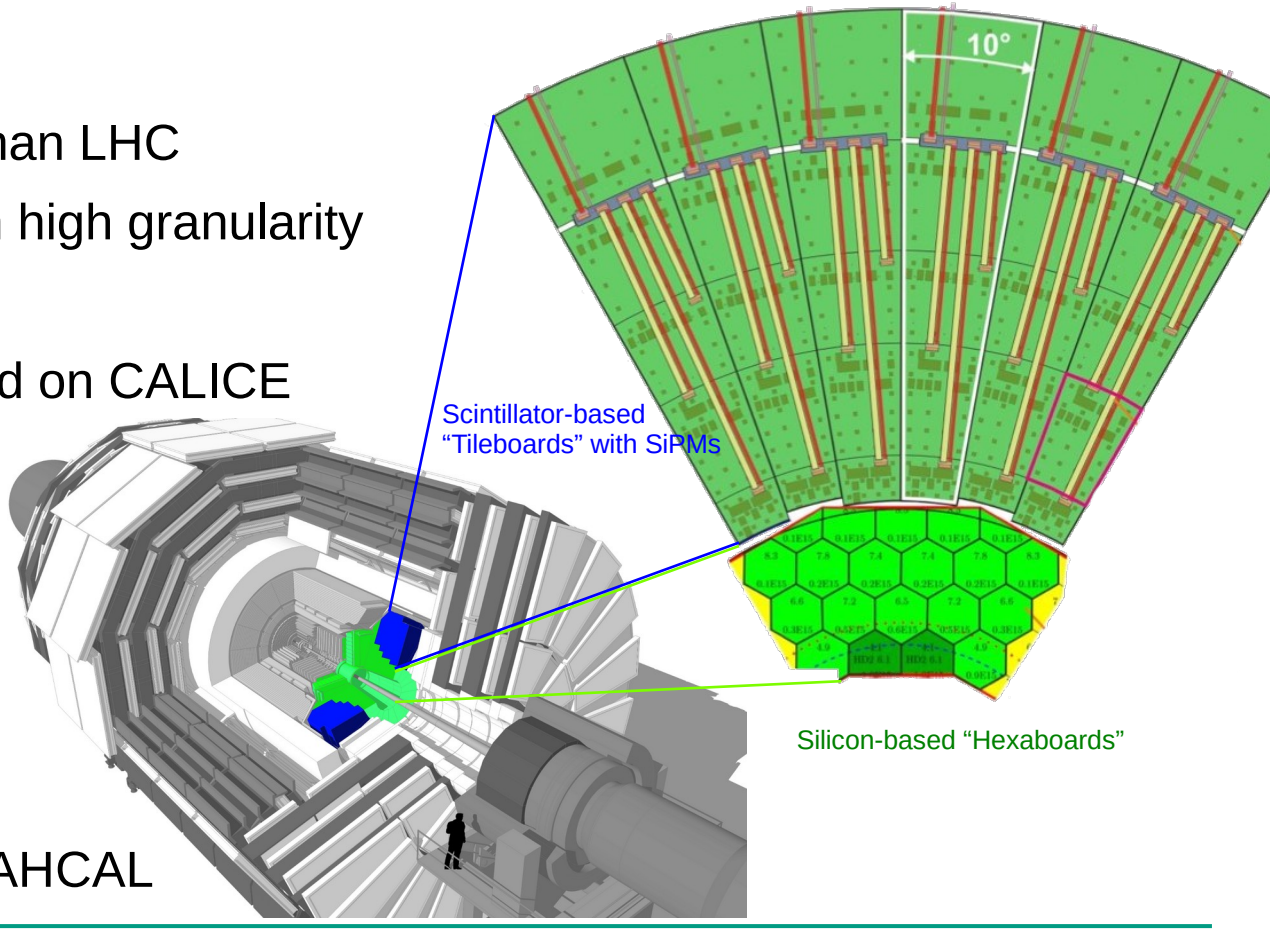
Karlsruhe Institute of Technology

Two main challenges:

- Event pileup 3-5 times higher than LHC
  - → Particle flow calorimeter with high granularity
  - → > 6 Mio channels

  3D shower reconstruction based on CALICE research
- Radiation environment
  - → Silicon-based „hexaboards“ for high-radiation environment
  - → SiPM-on-Tile „tileboards“ for lower-radiation environment

  Technology based on CALICE AHCAL



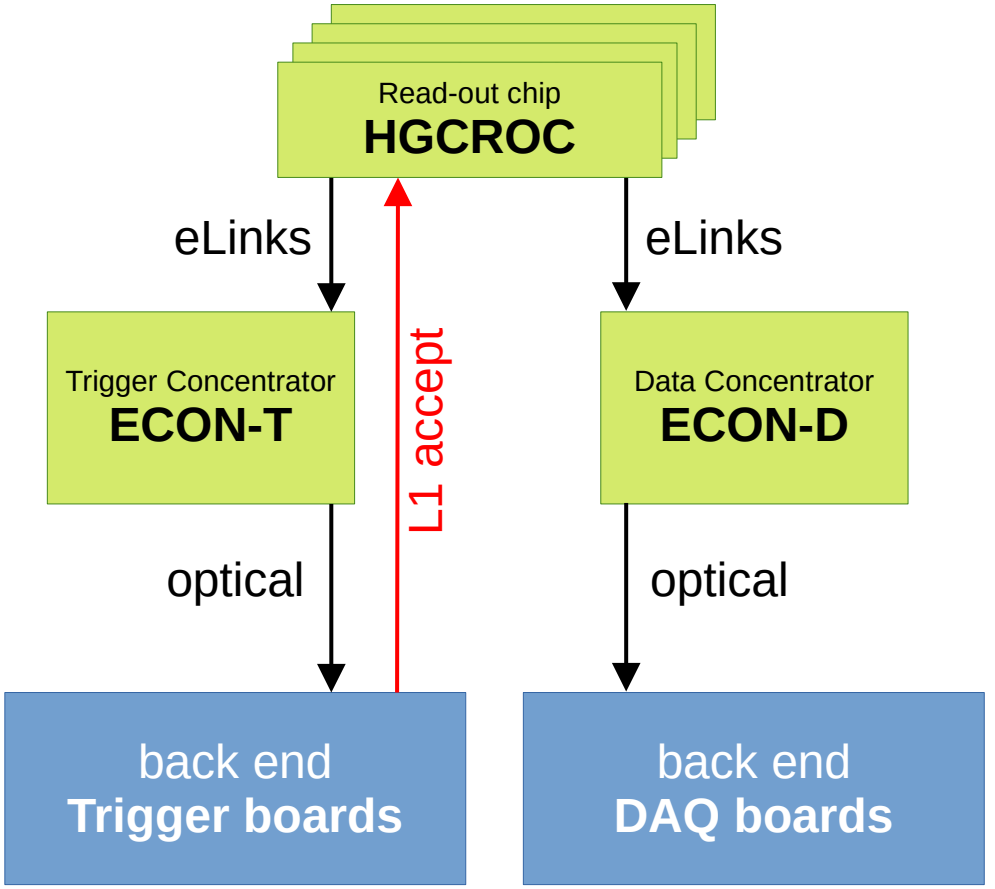
Front End Challenges

- Total of approx. 6M channels (hexaboards) + 240k channels (tileboards)
  - Full event size 2.5 – 3.5 MB (both endcaps)
  - Separate between trigger and data path
  - Event buffer in ROC > 12.5µs latency for L1 trigger decision
- Active CO_2 cooling to -30°C to mitigate effects of radiation damage
  - Power budget limited by cooling power (electronics will dissipate ~125kW)
- High density of readout channels and electronics (especially for hexaboards)
  - Silicon sensor cell size 0.5...1cm²

→ **Scale and density of front end poses an engineering challenge!**

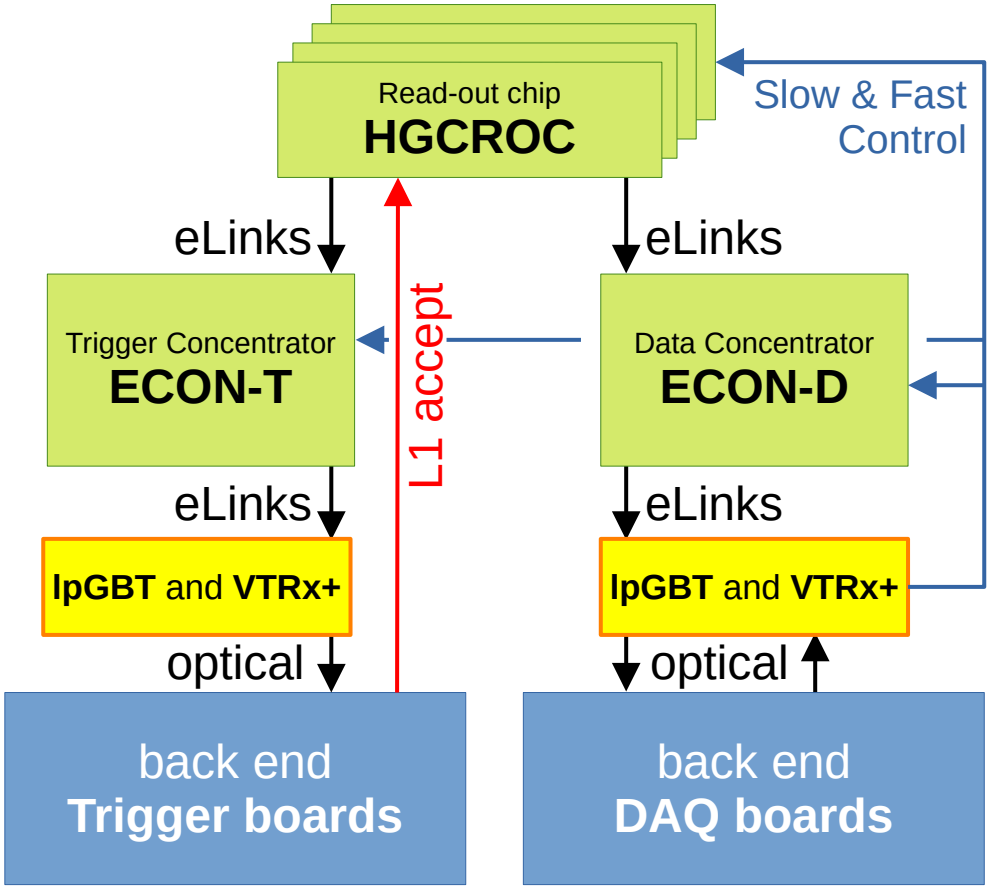
How to get the data out of the detector

- Approx. 100k HGCROCs
- Separate DAQ and Trigger path, approx. 8000 optical links to FE *each*
- Trigger Path:
  - Total average event rate 40Tb/s
- DAQ Path:
  - 12Tb/s at 750kHz L1 accept rate
- Additional components: lpGBT, GBT-SCA, DC/DC, fan-out, …
- (Almost) same FE for hexaboards and tileboards → same backend



The Versatile Link plus Environment

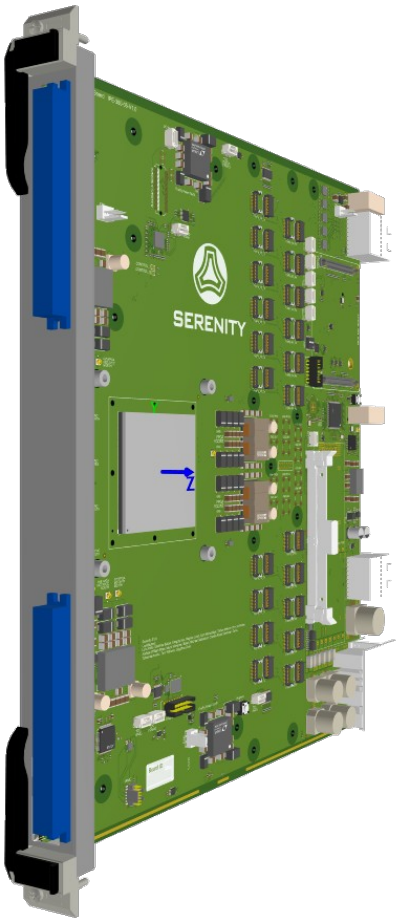
- Common ASICs for phase II of CMS and ATLAS
  - Dev. boards + tech support at CERN
  - Radiation hard, wide temperature range
- **VTRx+** → optical transceiver
  - 4x 10Gb/s uplink
  - 1x 2.56 Gb/s downlink
- **lpGBT** (low power gigabit transceiver) fans out to eLinks, clocks, slow and fast control
  - 10Gb/s uplink, 2.56Gb/s downlink
- **GBT-SCA** → Slow control adapter
  - Only used in tileboards



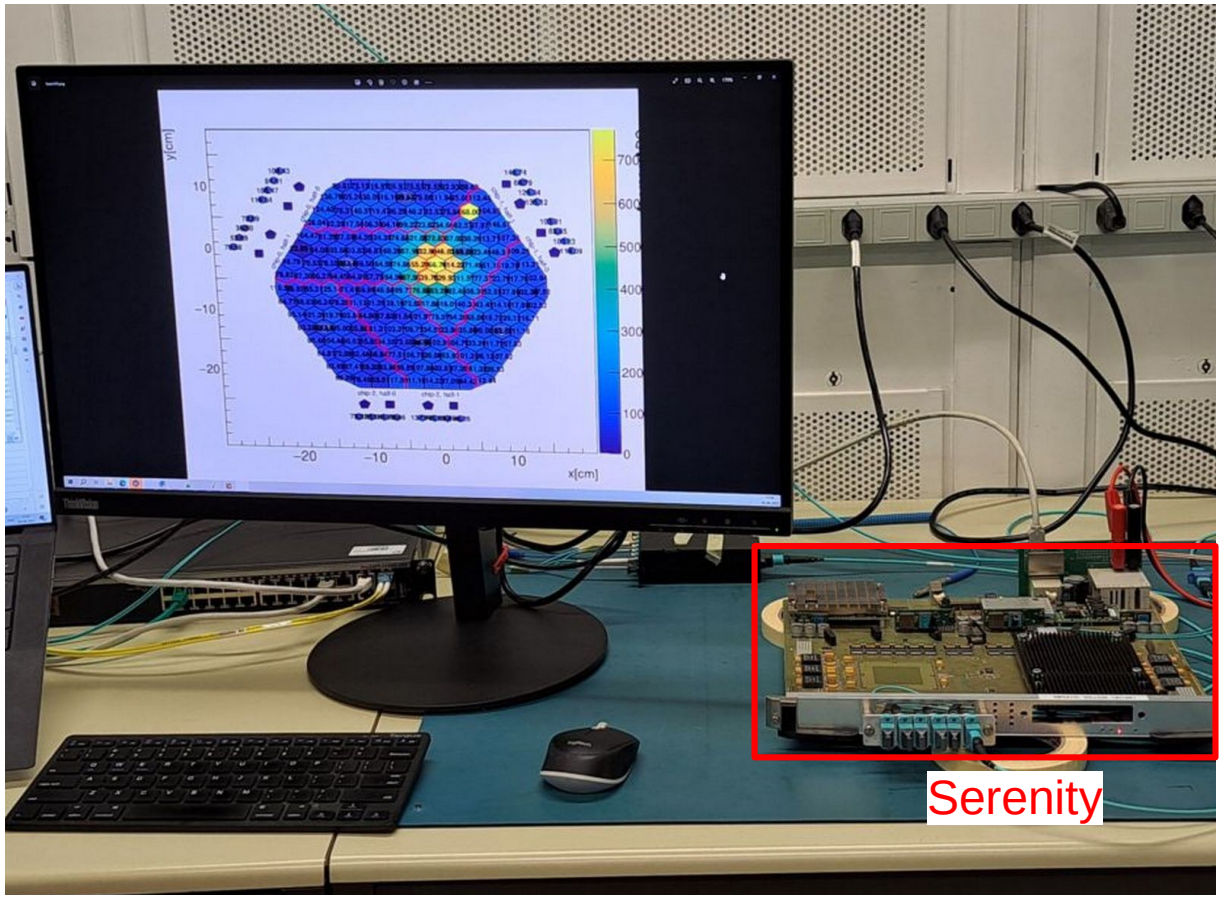
What to do with the data on the other side?

Serenity-S1 FPGA card:

- Generic readout card for various CMS subsystems
  - Links, FPGA and firmare configurable for each use case
- More than 700 cards will be used in HL-LHC upgrade
  - Approx. 300 for HGCAL (for Trigger and DAQ)
- Each Serenity board houses
  - VU9P or VU13P FPGA
  - 124 fiber optical links up to 25Gb/s (Rx and Tx each)
  - Zynq Kria System-on-Module
- Developed in collaboration between KIT and Imperial College London



The Serenity in action...



Two beam tests at SPS this year:

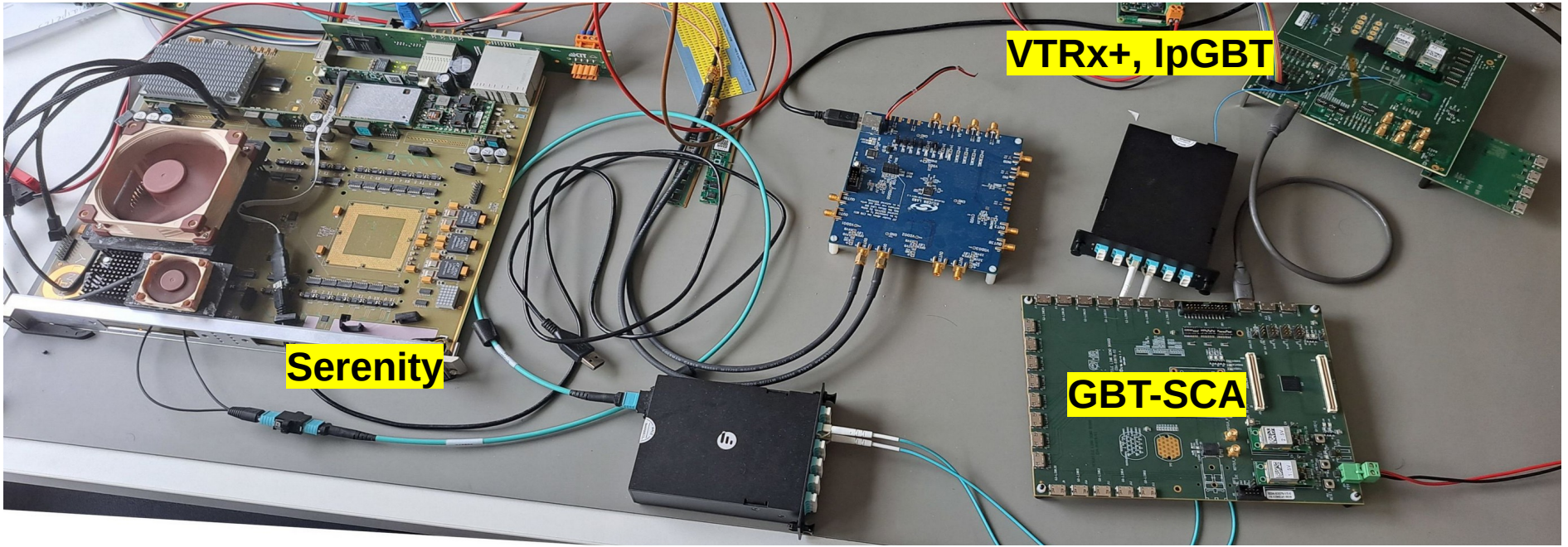
- Two hexaboards with the complete pre-series front end
- Full readout chain until the Serenity
- First time this system was in a beam test!

→ a huge success for HGCAL!

...requires a large team to get working!

HGCAL activities at IPE / KIT

- Building a test stand for the full readout chain: tileboard → Serenity
- Currenlty preparing FW and SW for slow control using VLDB(+) boards
- Close collaboration with DESY (front end), CERN and ICL (back end)



CALICE plans at IPE / KIT

- Simulations on future detectors and development of reconstruction algorithms
  - Determine performance requirements for the new AHCAL readout chain
  - Which performance parameters drive energy resolution? e.g. timing, granularity, …
- Develop a new readout chain & local powering for the AHCAL
  - Fit for linear and circular colliders
  - Which readout electronics? Data rates? Triggering capabilities required?
- IPE has extensive expertise in development of digital and analog electronics, System-on-Chip and firmware