UNIVERSITAT DE BARCELONA

LA SALLE
Universitat Ramon Llull

R&D on pixel sensors at ILC

ILC Workshop - November 2006 – Valencia

I. Interest on R&D on pixel sensors

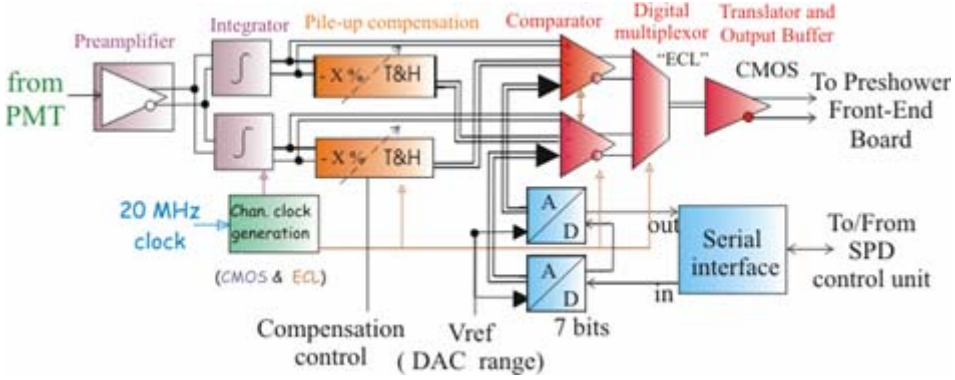
- **A previous collaboration worked well in front end electronics for LHC :**
  - HEP experimental group of the ECM department of the Physics School (Universitat de Barcelona): physicists and electronic engineers (HEP instrumentation and μelectronics design).
  - Microelectronics design group of the electronics department of the Physics School (Universitat de Barcelona): analog and mixed μelectronics design, smart sensors, μrobotics and cameras (APS).
  - Instrumentation group of the the electronics department of Enginyeria La Salle (Universitat Ramon Llull): instrumentation, test, VHDL/Verilog, fast serial links (optical, copper-LVDS)

- **Start R&D on silicon sensors and its front end electronics.**
- **From the point of view of instrumentation we are interested in pixel sensor application at ILC:**
  - Vertexing
  - Tracking
  - Others: Scintillator-Silicon pads…
- **The technologies we are currently interested in are DEPFETs and CMOS MAPs.**
- **Study the possibility to join one (or more?) of the current research projects.**
- **Final goal is to acquire the know-how on pixel sensor construction.**
- **A collaboration with other Spanish institutes with experience on (or interested in) silicon detectors would be essential to make the project feasible.**

II. Experience on HEP: Amplifier, Shaper and Discriminator

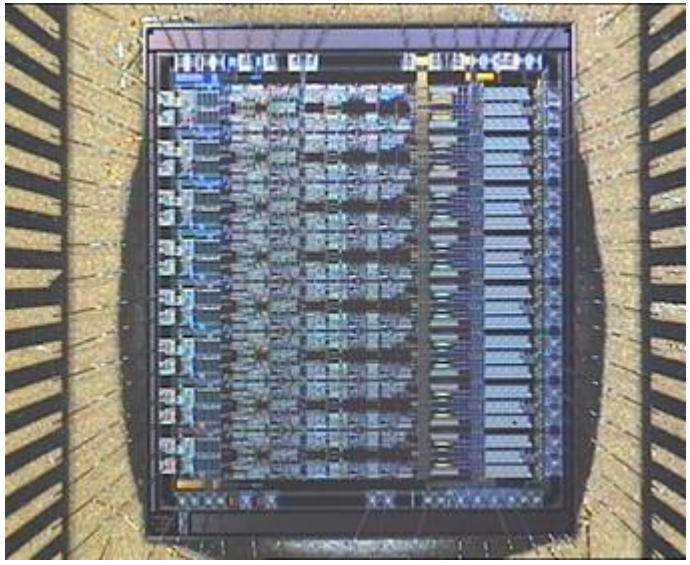
Designed in collaboration with the electronics department (UB)

- ***Analog Processing + Digital Control***
- ***Signal range: 1 pC*** (1 V)
  (1 MIP ~ 30-100 fC)
- ***Electronics resolution 2 fc***
- ***Radiation tolerant design***
  - Guard rings for SEL prevention
  - Triple Voting Register (TVR) for SEU.

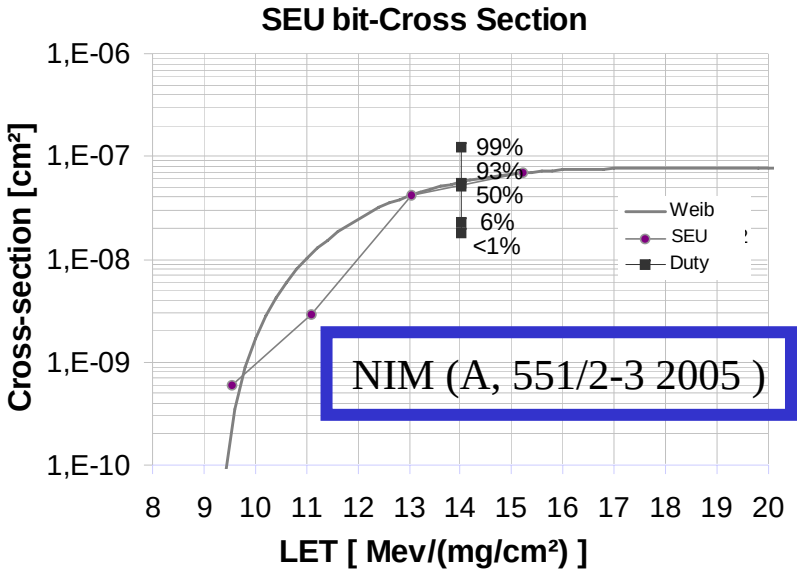


Radiation qualification:

Using a krypton beam we have qualified this ASIC
- Expected total dose (tested up to 200 Gy = 20krad)
- The rate of SEU is acceptable
- No SEL

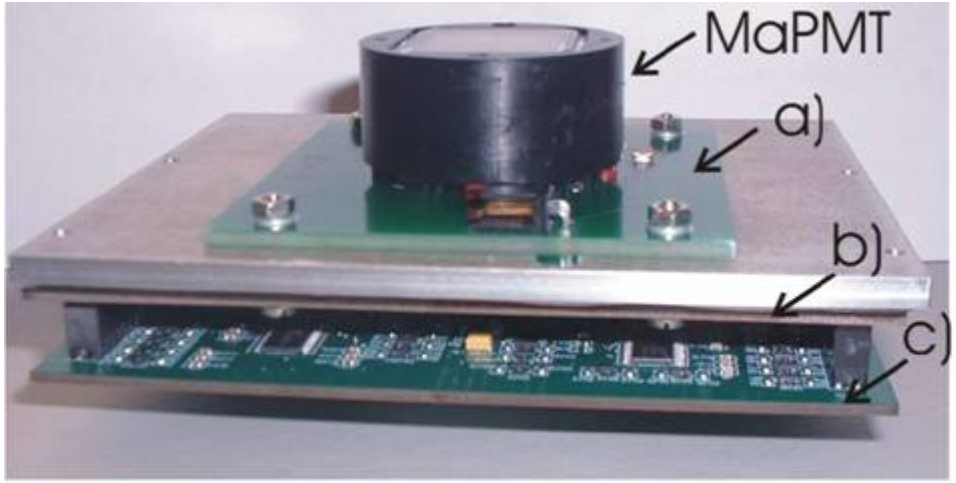


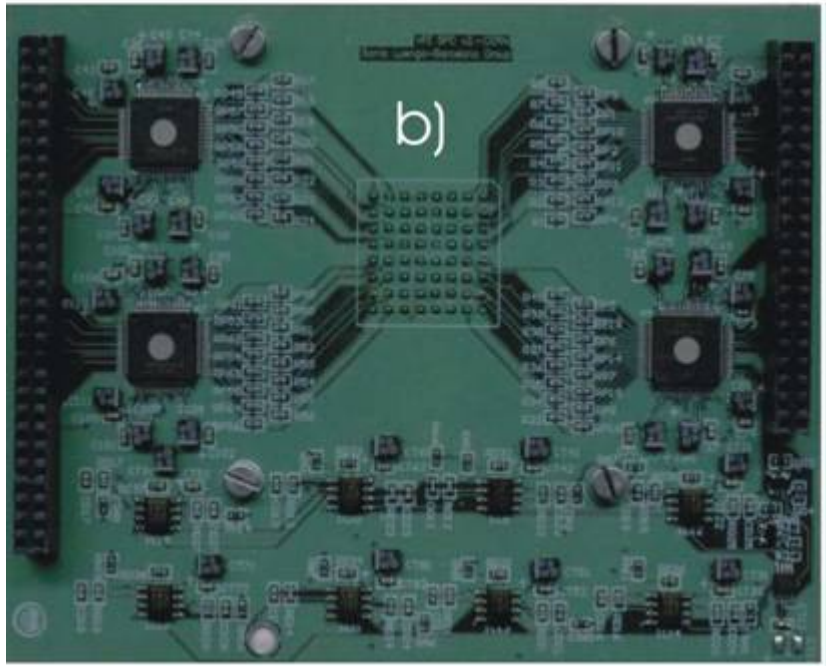
AMS BiCMOS 0.8μm - 8 dual channels – 30mm²

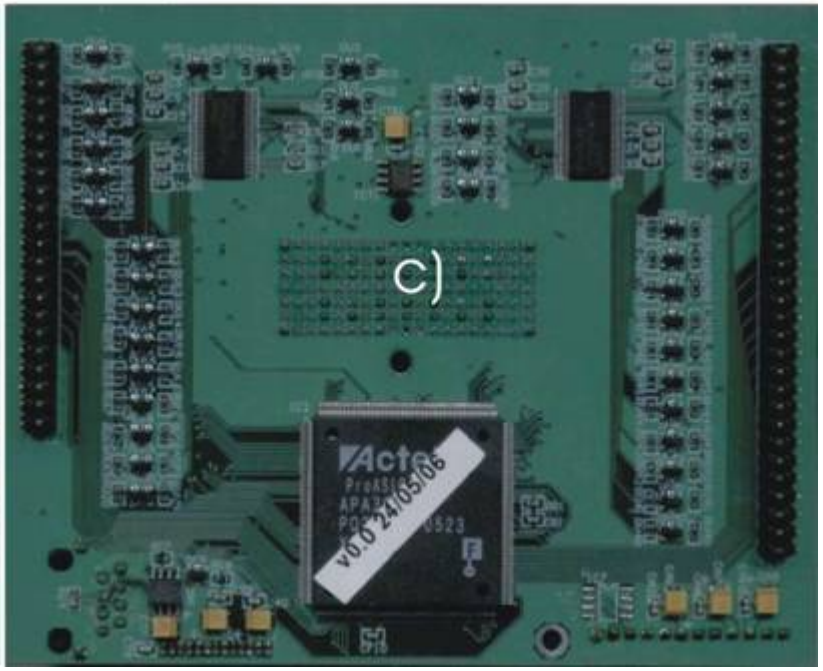


II. Experience on HEP : VFE board

Designed in collaboration with the La Salle School of Egineering

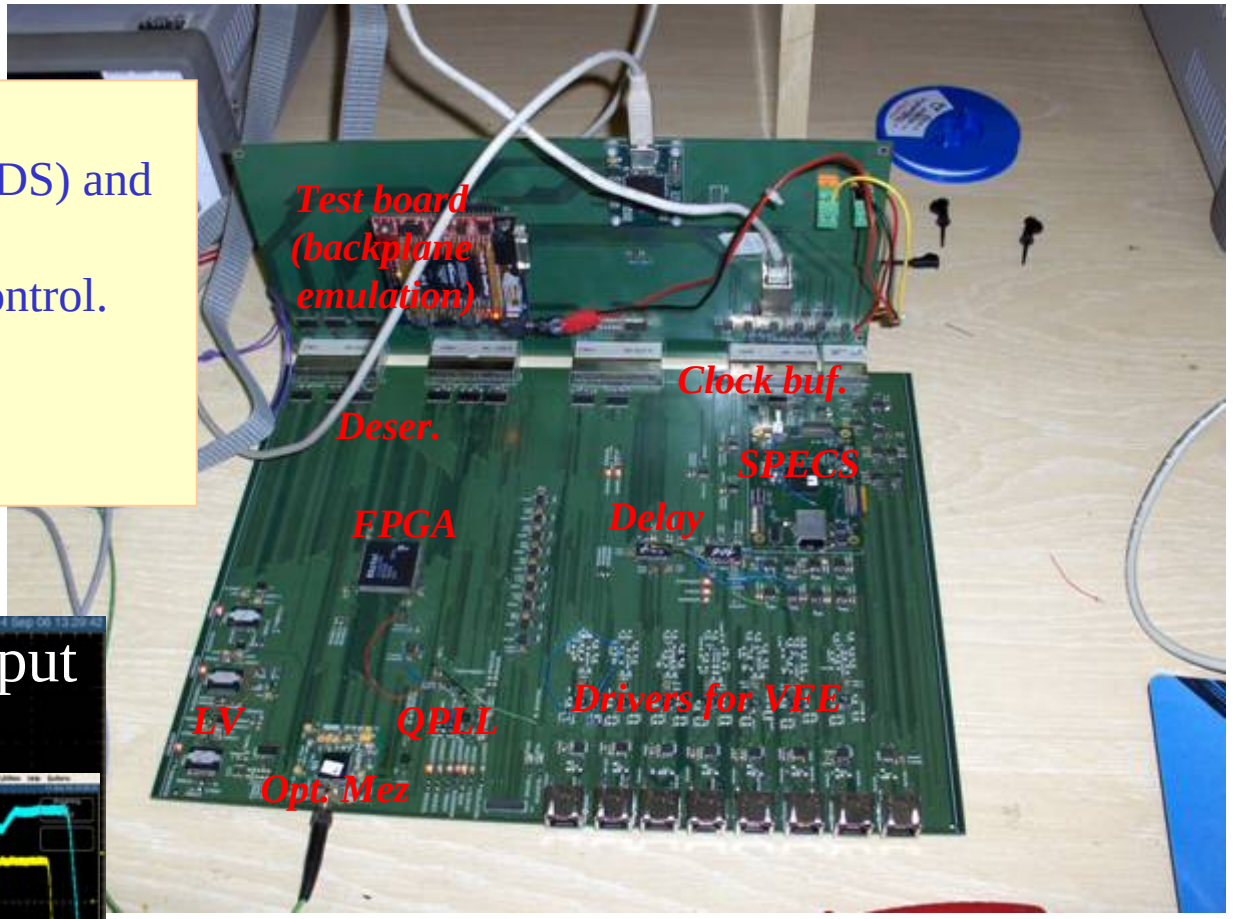


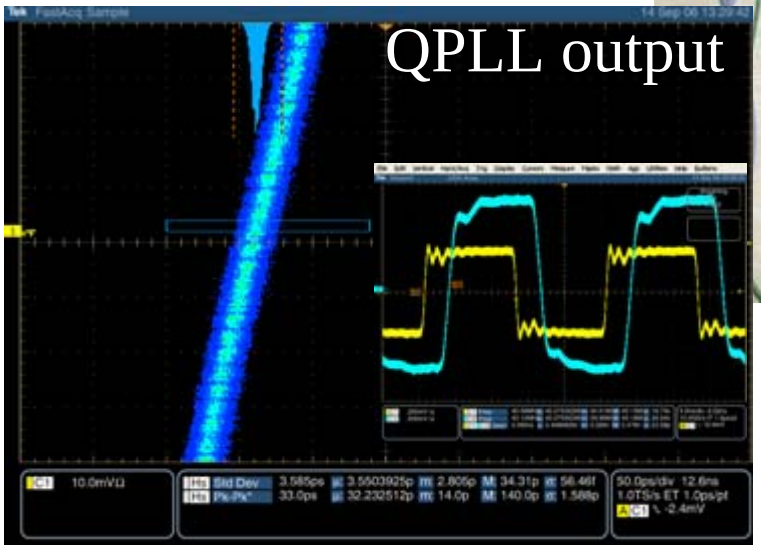




II. Experience on HEP: Control Board

- First level trigger processing
- Fast serial links: copper (LVDS) and optical (Gigabits/s)
- Interface for slow and fast control.
- SPY RAM (debug).
- 40 MHz clock distribution.
- Radiation tolerance

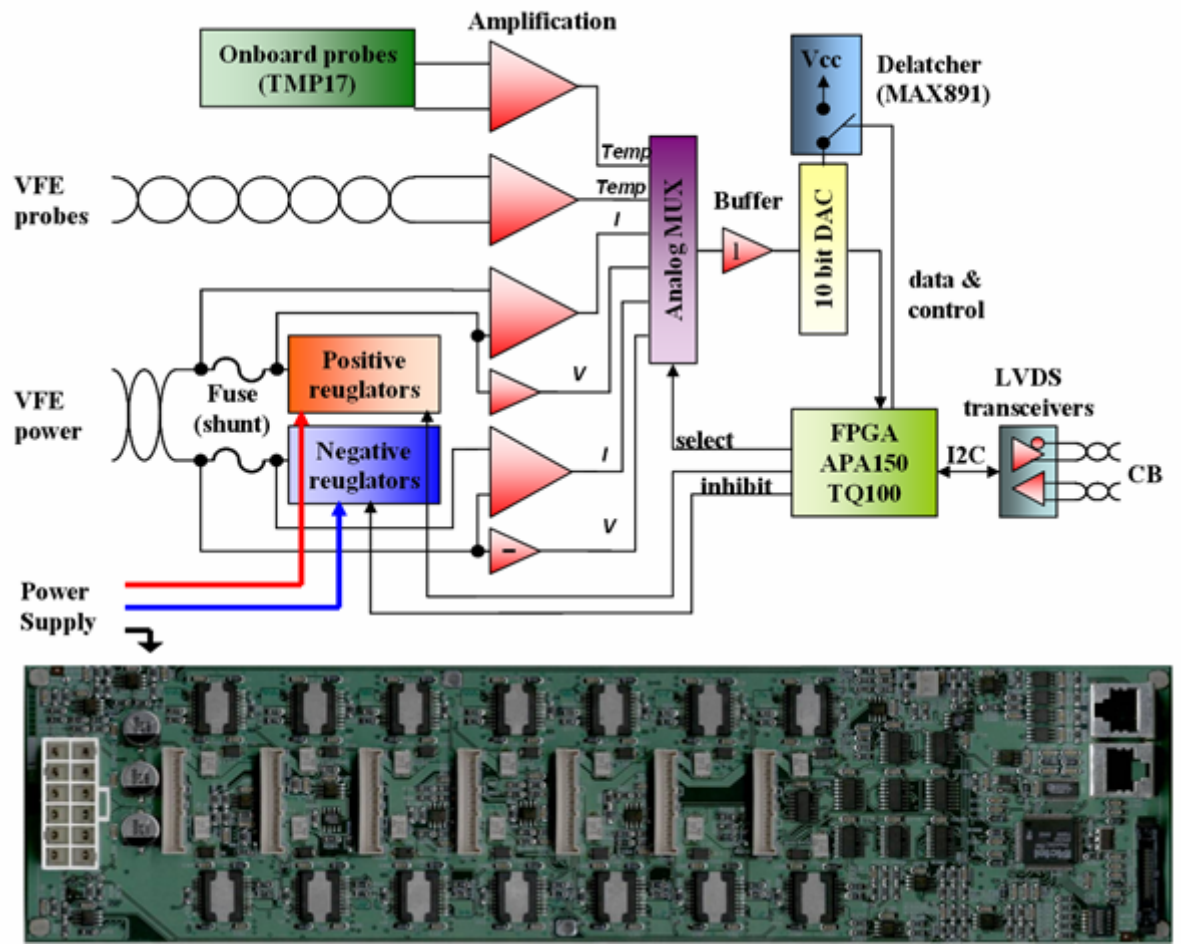




Designed in collaboration with the La Salle School of Egineering

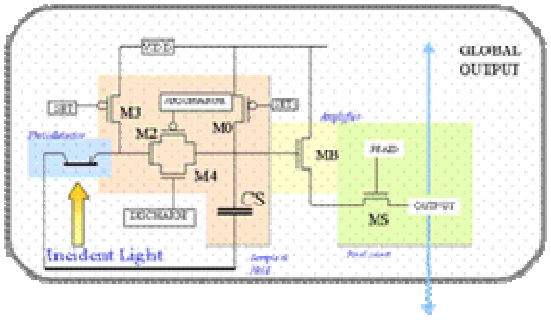
II. Experience on HEP: low voltage regulation

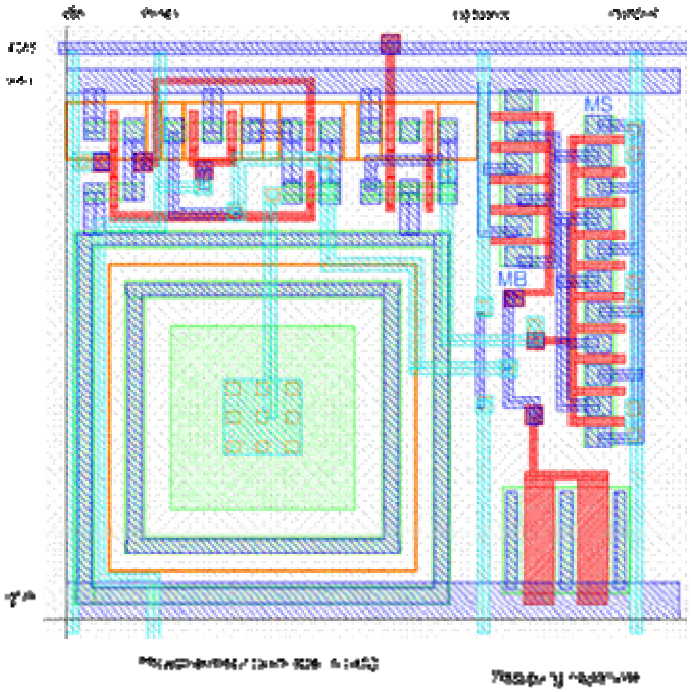
- Each powers up to 7 VFE cards
- Several regulators per card
- Regulators shared between VFE cards (26 per LV card).
- Monitoring: V, I and Temperature (on board, on VFE board and external)
- SEL possible (although very rare) in VFE serializers: real time monitoring + fast fuses.
- All the cards pass BURN IN cycling.

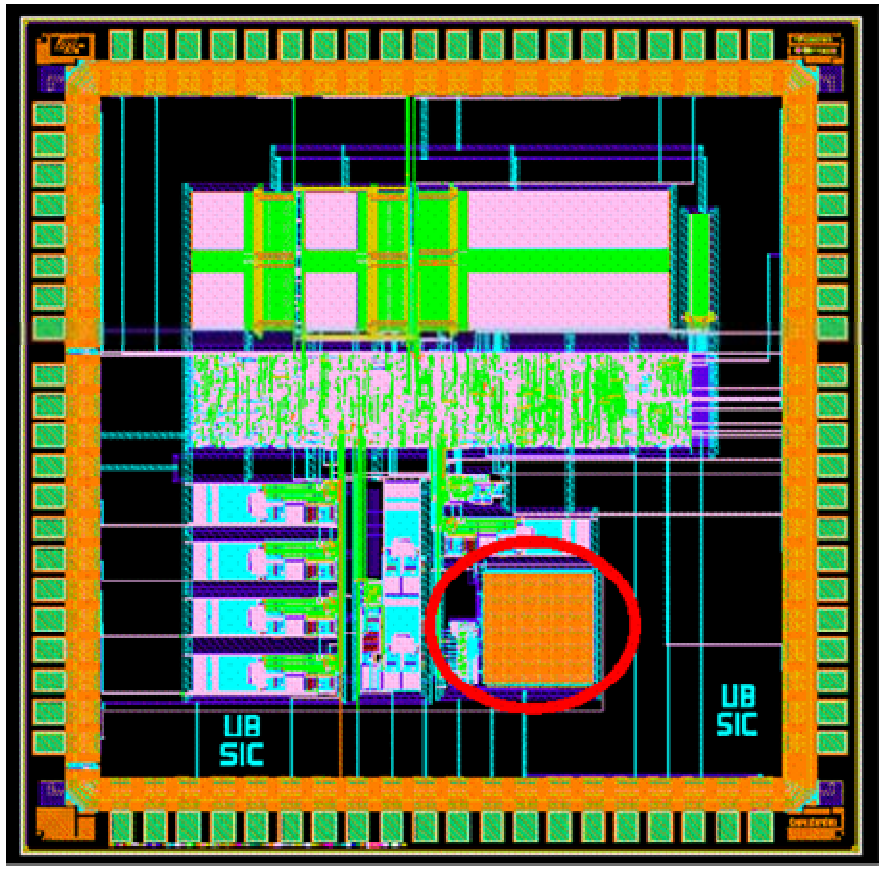


III. Other experience in microelectronics: APSs

32 x 32 pixels CMOS sensor in 0.13 STMicroelectronics technology







Departament d' Electrònica
Universitat de Barcelona

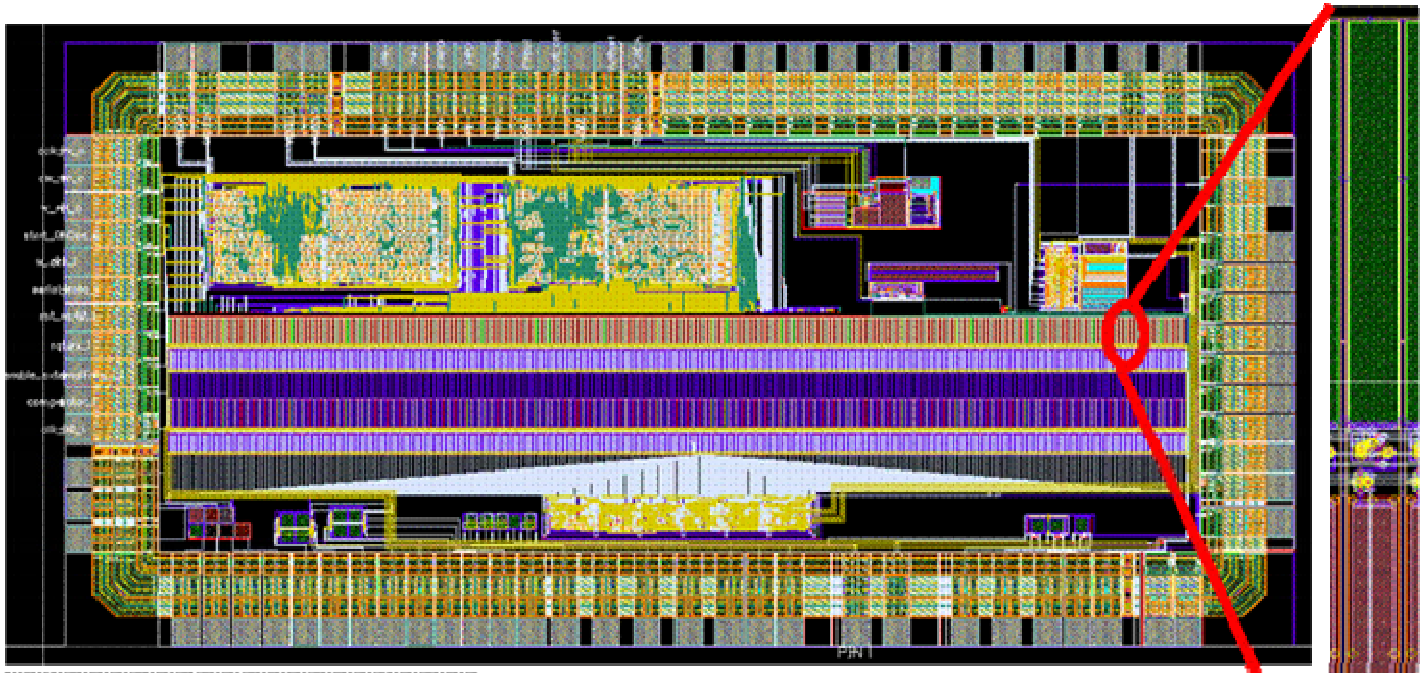
UNIVERSITAT DE BARCELONA

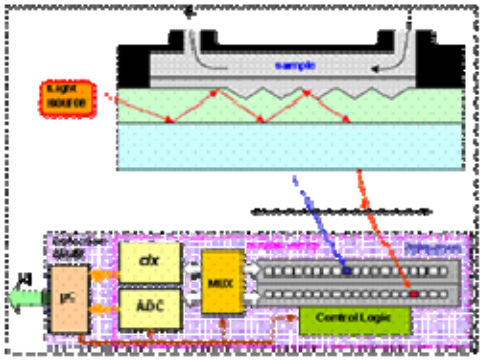
SIC
Instrumentation and Communications Systems

CONTACT: dieguez@el.ub.es

III. Other experience in microelectronics: APSs

0.35µm CMOS 256 Pixels Double Array with AD Conversion and Derivative output for Biosensing Applications





Departament d' Electrònica
Universitat de Barcelona

UNIVERSITAT DE BARCELONA

SIC
Instrumentation and Communications Systems

CONTACT: dieguez@el.ub.es