CMOS Monolithic Sensors with Sparsified Readout and Time Stamping Capabilities for Vertexing Applications at the ILC

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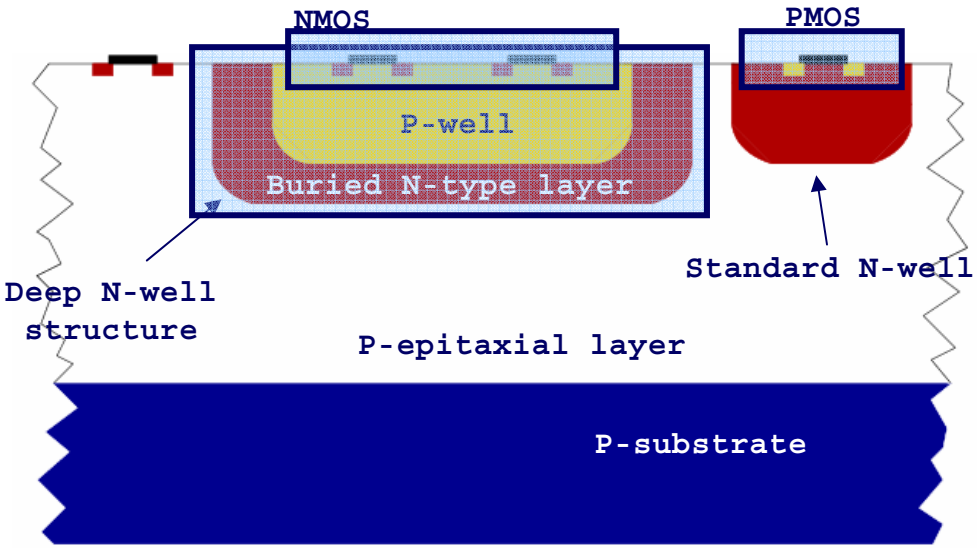
MAPS for vertexing applications

- Tracking and vertexing systems in future high luminosity colliders (ILC, SLHC, Super B-Factory) will be operated at high rate with low material budget to optimize position and momentum resolution
- Monolithic active pixel sensors (MAPS) may provide the required low mass and high granularity
- An ambitious goal is to design MAPS with similar readout functionalities as in hybrid pixels (sparsification, time stamping, e.g. FPIX)
- A readout architecture with data sparsification would be a new feature which could give some advantages with respect to existing MAPS implementations
  - flexibility in dealing with possible luminosity and background changes during the experiment lifespan
  - decouple modularity from readout speed
  - reduce digital power dissipation
- Modern VLSI CMOS processes (130 nm and below) could be exploited to increase the functionality in the elementary cell

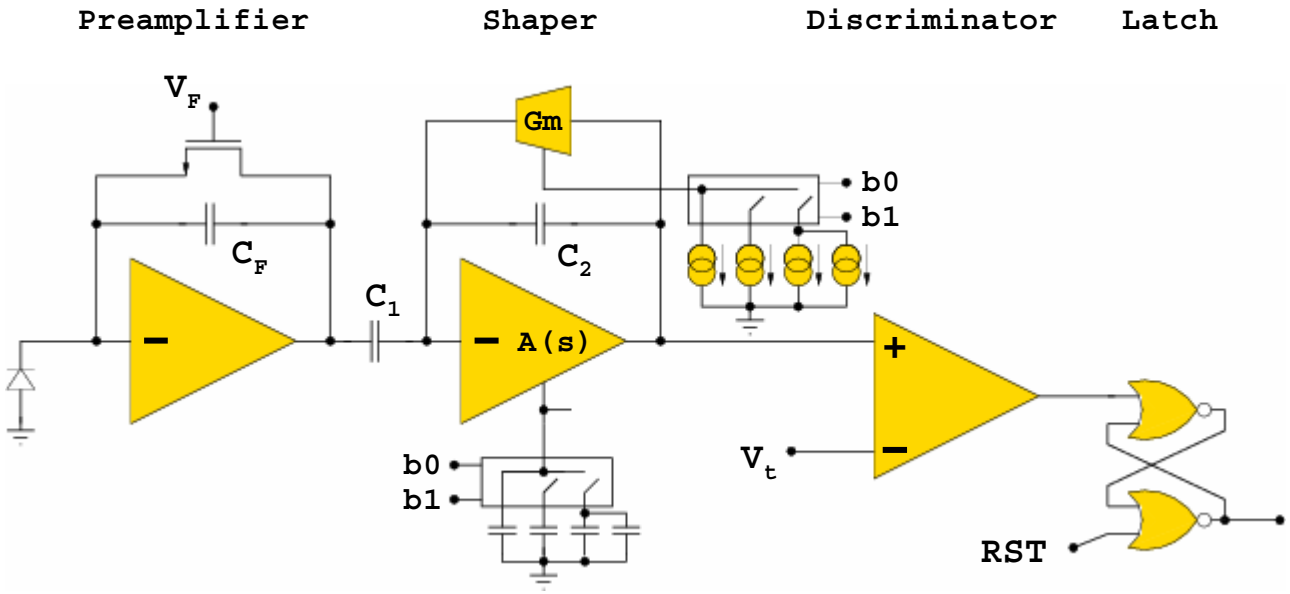
Deep N-well MAPS concept



- In triple-well CMOS processes a deep N-well is used to isolate N-channel MOSFETs from substrate noise
- Such features were exploited in the development of **deep N-well (DNW) MAPS** devices

- A DNW is used to collect the charge released in the epitaxial layer
- A readout channel for capacitive detectors is used for Q-V conversion → gain decoupled from electrode capacitance
- NMOS devices of the analog section are built in the deep N-well
- Using a large detector area, PMOS devices may be included in the front-end design → charge collection inefficiency depending on the ratio of the DNW area to the area of all the N-wells (deep and standard)

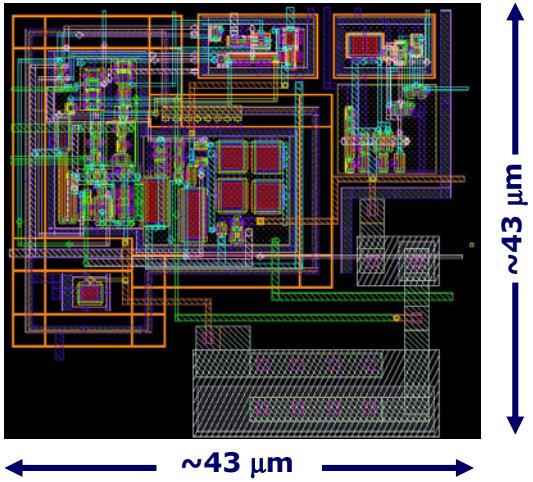
Pixel level processor (Apsel family)



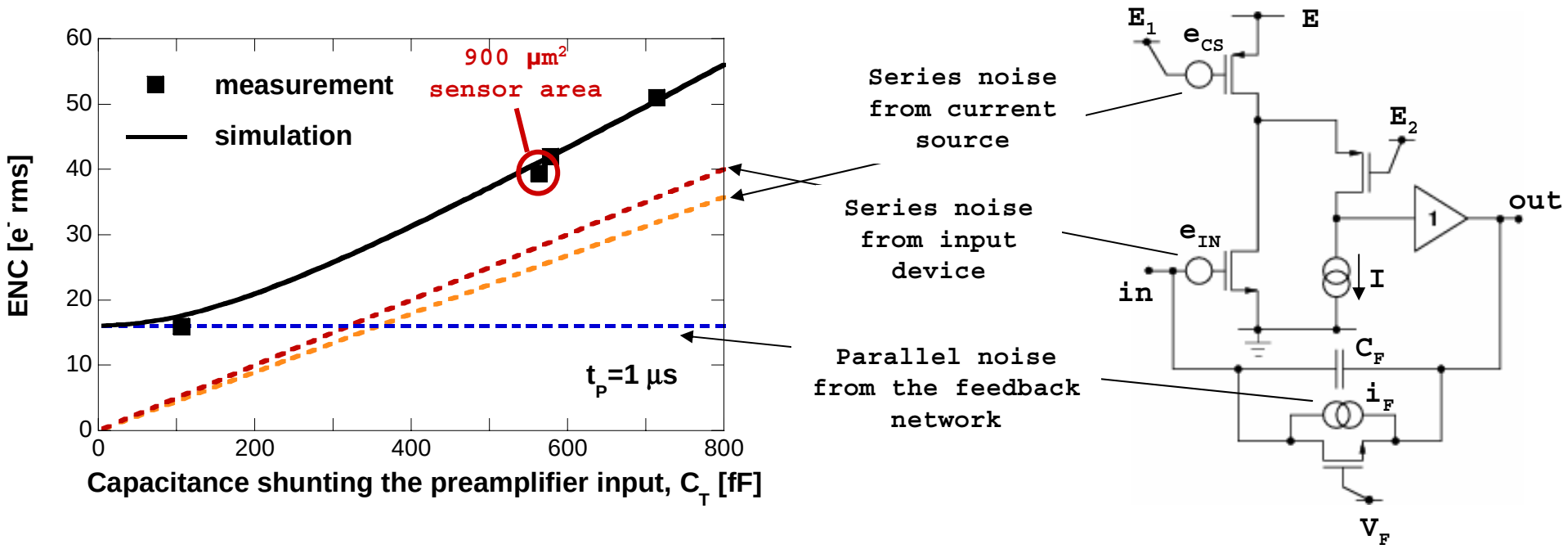
- High sensitivity charge preamplifier with continuous reset
- RC-CR shaper with programmable peaking time (0.5, 1 and 2 μs)
- A threshold discriminator is used to drive a NOR latch featuring an external reset

- A couple of test structures were fabricated in a 130 nm, triple well, epitaxial layer CMOS technology by STM
- The first prototypes proved the capability of the sensor to collect charge from the epitaxial layer

(G. Rizzo et al., "A novel monolithic active pixel detector in 0.13 μm triple well CMOS technology with pixel level analog processing", *NIMA* vol. 565, pp. 195-201, 2006)



Analog performances



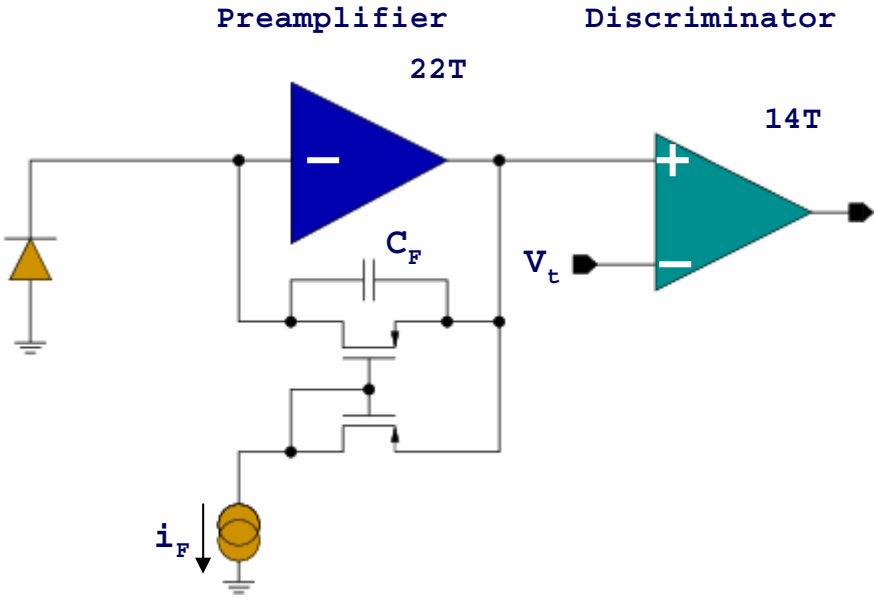
- Two chips recently submitted to study charge spreading in the epi-layer and charge collection efficiency (130 nm CMOS process by STM)
  - ENC=40 e^- rms @C_D=320 fF (900 µm^2 sensor area)
  - Threshold dispersion about 40 e^- rms
  - Power dissipation about 60 µW (although decreasing the input device current by a factor of three does not change significantly the noise performances)

DNW MAPS for vertexing at the ILC

- ILC is expected to feature a beam structure with 2820 crossings per train (1 ms), with a duty-cycle of 0.5%
  - Maximum hit occupancy is assumed to be 0.03 particles/crossing/mm^2
  - 3 hits/particle yield a hit rate of about 250 hits/train/mm^2
- Chance of a single cell being hit twice in a bunch train is ≤ 1% for 20 μm x 20 μm or smaller pixels → pipeline with a depth of one is sufficient to record ≥ 99% of events with no ambiguity → data can be readout all together during the intertrain interval
- Although the occupancy is quite small, a time stamp may prove useful to complement information from other detectors and reconstruct hit patterns
- Sparsification reduces the amount of data sent off the chip and digital power dissipation
- A DNW MAPS sensor for ILC is being designed based on a token passing readout scheme suggested by R. Yarema

(R. Yarema, "Fermilab Initiatives in 3D Integrated Circuits and SOI Design for HEP", *ILC VTX Workshop at Ringberg*, May 2006)

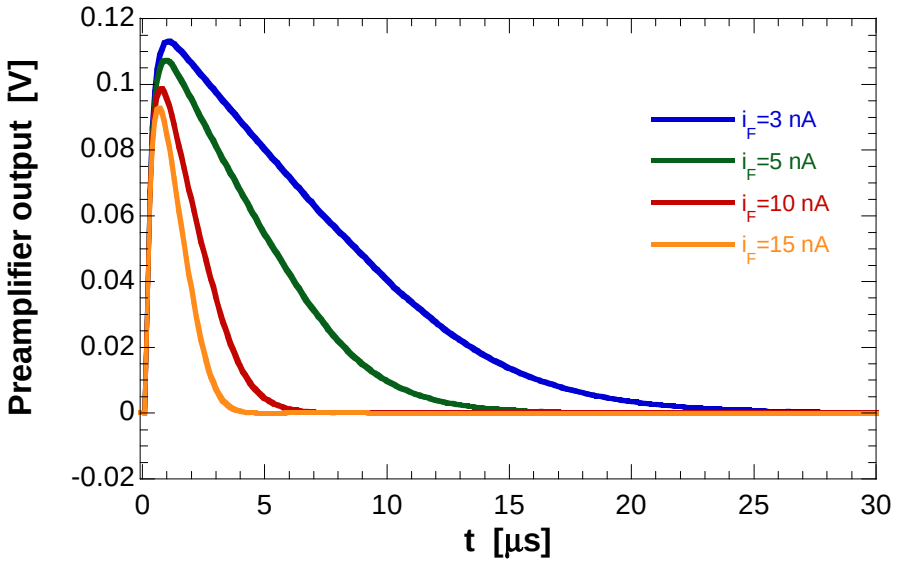
Cell analog front-end



- Threshold dispersion: about **30 e⁻ rms**
- Features power-down capabilities for power saving

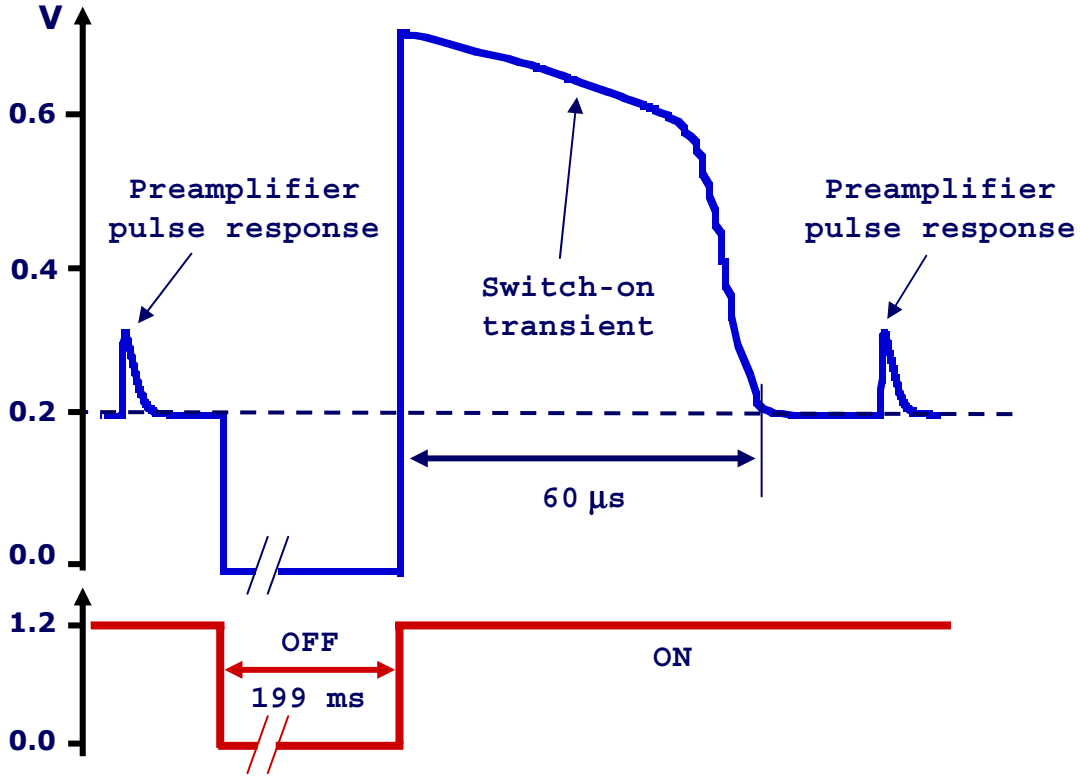
- Smaller area than in the Apsel prototypes → smaller detector capacitance
- ENC=**25 e⁻ rms@C_D=100 fF**
- Power consumption: about **5 µW**

Preamplifier response to an 800 e⁻ pulse



Power cycling

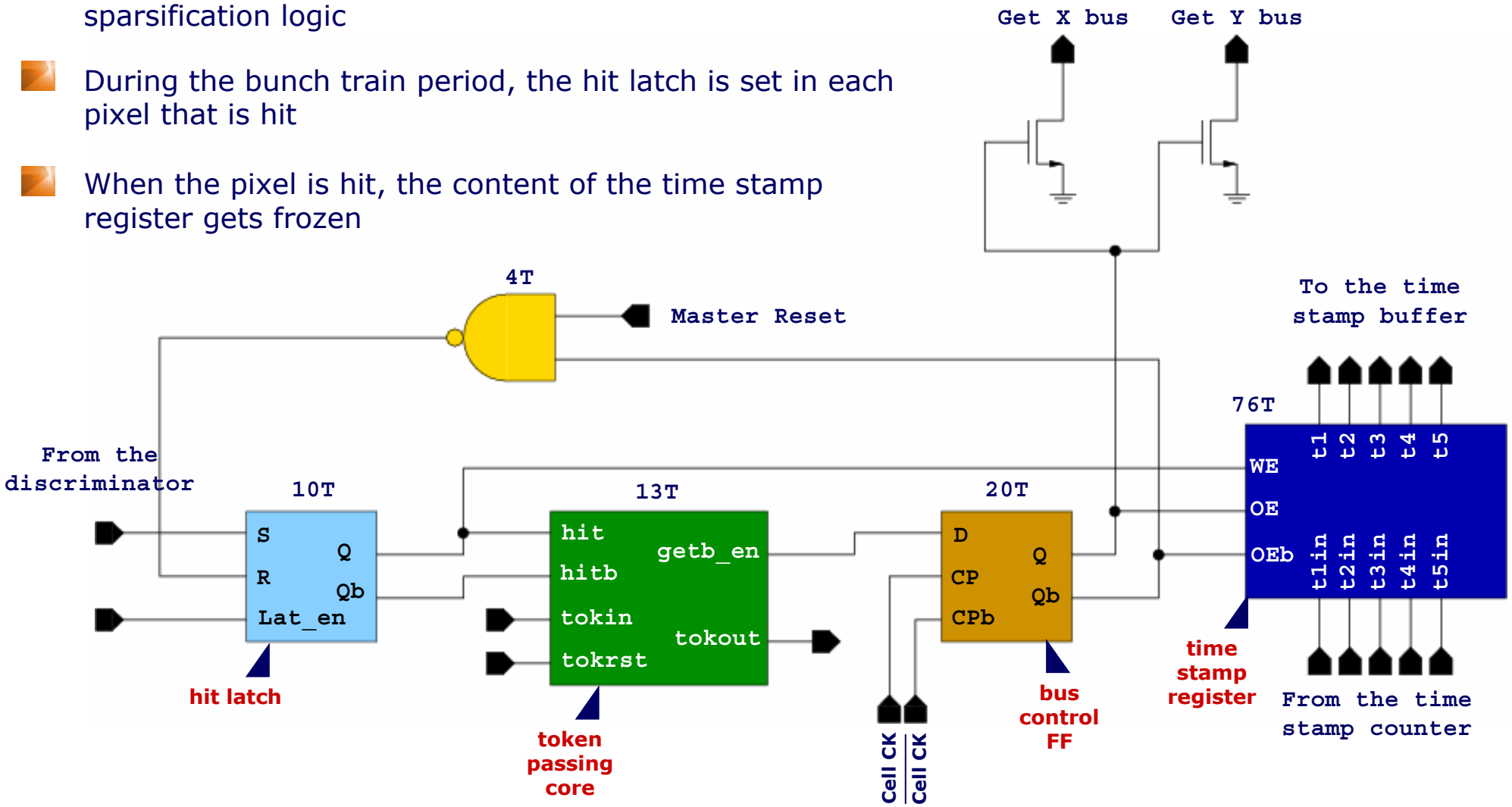
- The analog section in the elementary cell can be switched off during the intertrain interval in order to save power (analog power is supposed to be predominant over digital)



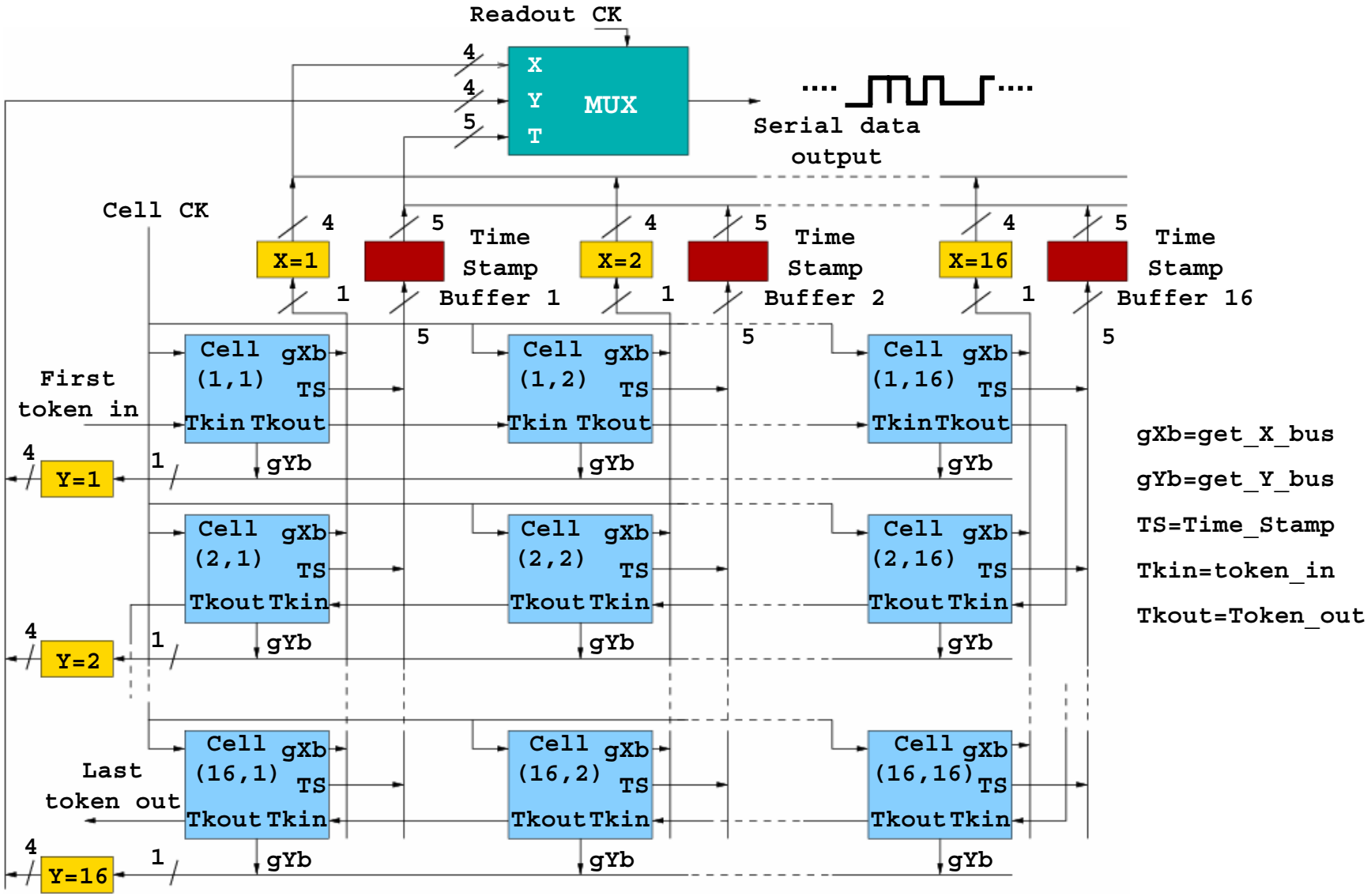
- Based on circuit simulations, power cycling with at least **1% duty-cycle** seems feasible
- Considering the **power available** for the ILC vertex detector (**20 W**) and the **vertex barrel area** (about **170000 mm^2**), the available **power/cell** is ≥**4.7 µW** for a pitch of 20 µm or larger, compatible with the power dissipation features of the analog front-end

Cell digital section

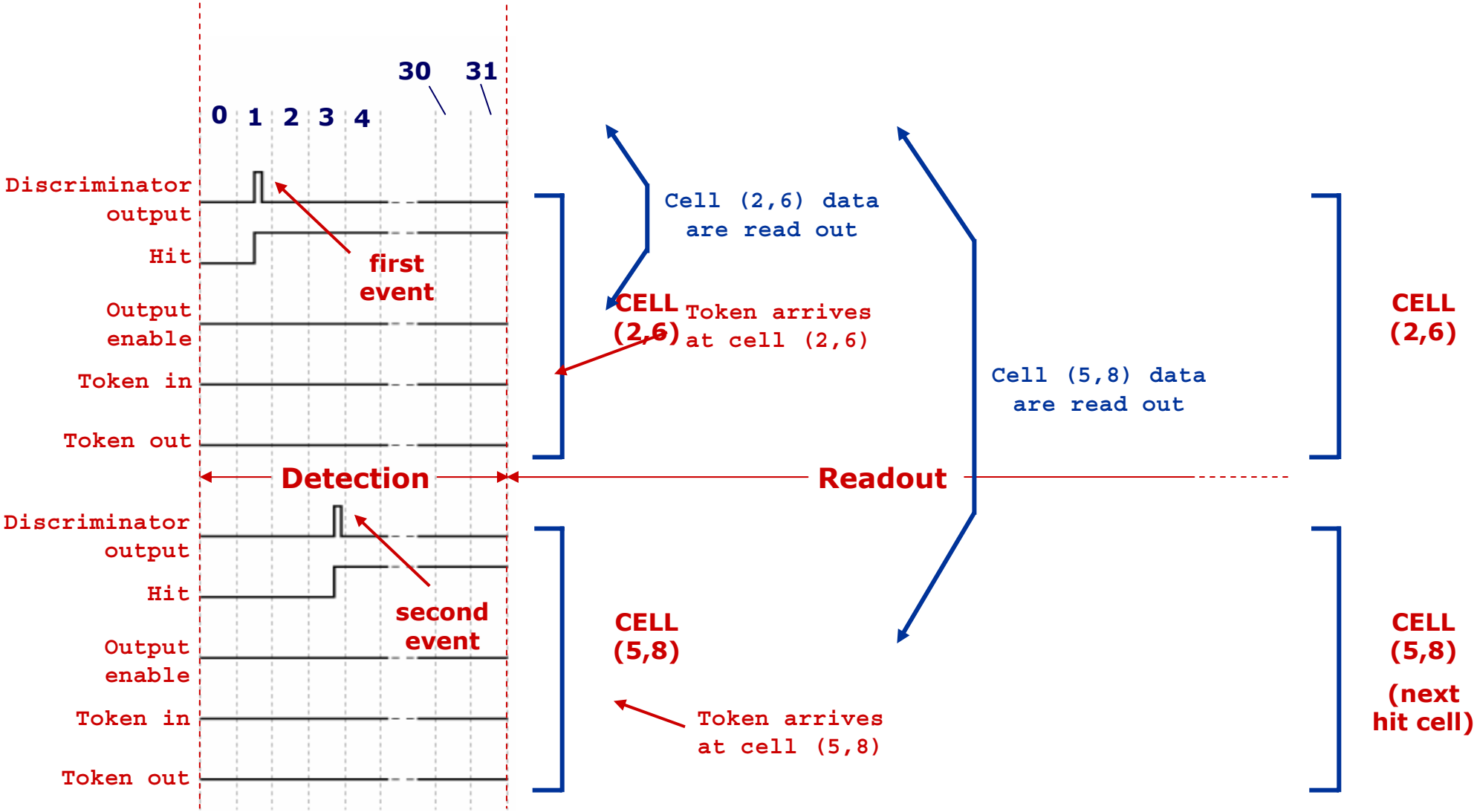
- Includes a 5 bit time stamp register and the data sparsification logic
- During the bunch train period, the hit latch is set in each pixel that is hit
- When the pixel is hit, the content of the time stamp register gets frozen



Digital readout scheme

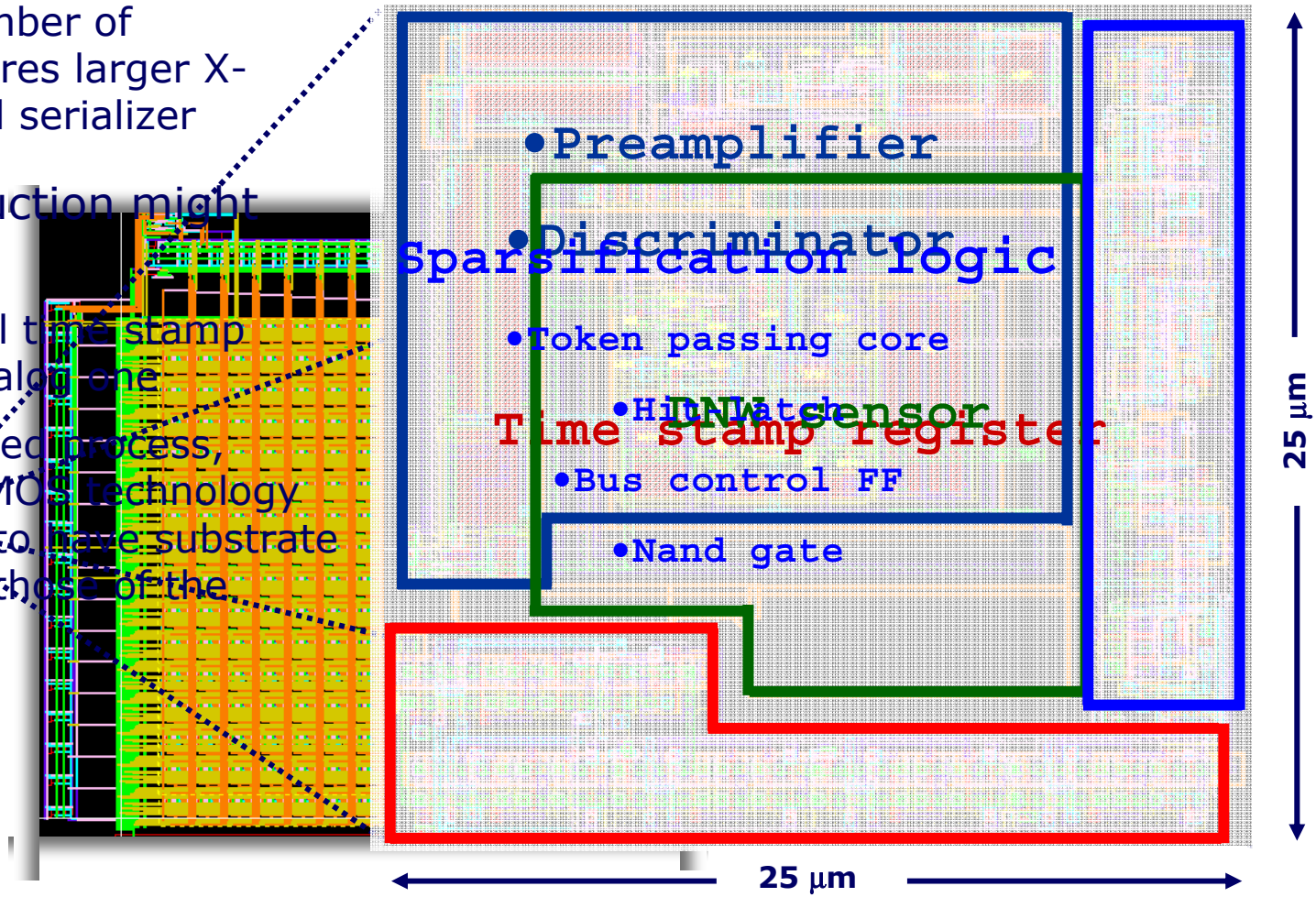


Timing diagram



ILC DNW MAPS demonstrator

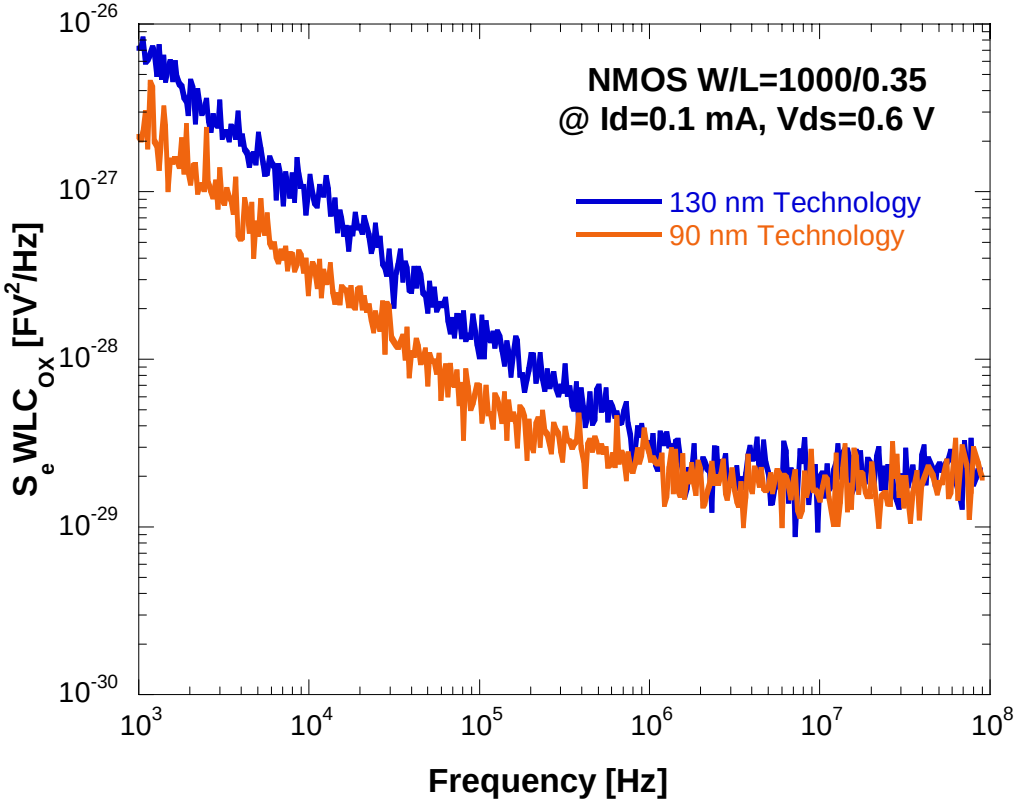
- A 16x16 MAPS demonstrator chip is being designed in the 130 nm bulk CMOS technology by STM
  - Increase in the number of elements just requires larger X- and Y-registers and serializer
- Further pitch reduction might be achieved by:
  - replacing the digital time stamp register with an analog one
  - using a further scaled process, namely a 90 nm CMOS technology by STM, supposed to have substrate features similar to those of the 130 nm process



DNW MAPS in 90 nm CMOS

- A 90 nm CMOS process might provide some advantages in the design of DNW MAPS with respect to the 130 nm process
  - about a factor of two reduction in silicon area occupation
  - better power/channel thermal noise trade off
  - better 1/f noise performances
  - smaller dispersion in device parameters
  - be careful with gate currents
- Experimental characterization of test structures in 90 nm CMOS process will provide useful information as to the design of DNW MAPS

Normalized power spectral densities for NMOS devices belonging to the STM 130 and 90 nm processes



Conclusions

- A DNW MAPS demonstrator aimed at vertexing applications at the ILC is being designed in a 130 nm bulk CMOS technology
  The chip is capable of
- The chip is capable of sparsified readout, time stamp generation and is compatible with power cycling operation
- Simulations show good noise and threshold dispersion performances at a power dissipation close to the ILC vertex specifications
- Further activities are under way to optimize the elementary cell size and geometry, including
  - simplification of the pixel cell logic
  - MAPS development in a 90 nm CMOS technology
  - physical device simulations