Status on CMOS sensors

on behalf of
DAPNIA-Saclay, LPSC-Grenoble, LPC-Clermont-Ferrand, JINR-Dubna, DRS/IPHC-Strasbourg

- Status of the main R&D directions
- Engineering Run in AMS-0.35 OPTO Technology
- Progress on ADC developments
- Plans for the coming years
- Summary

Status of the Main R&D Directions

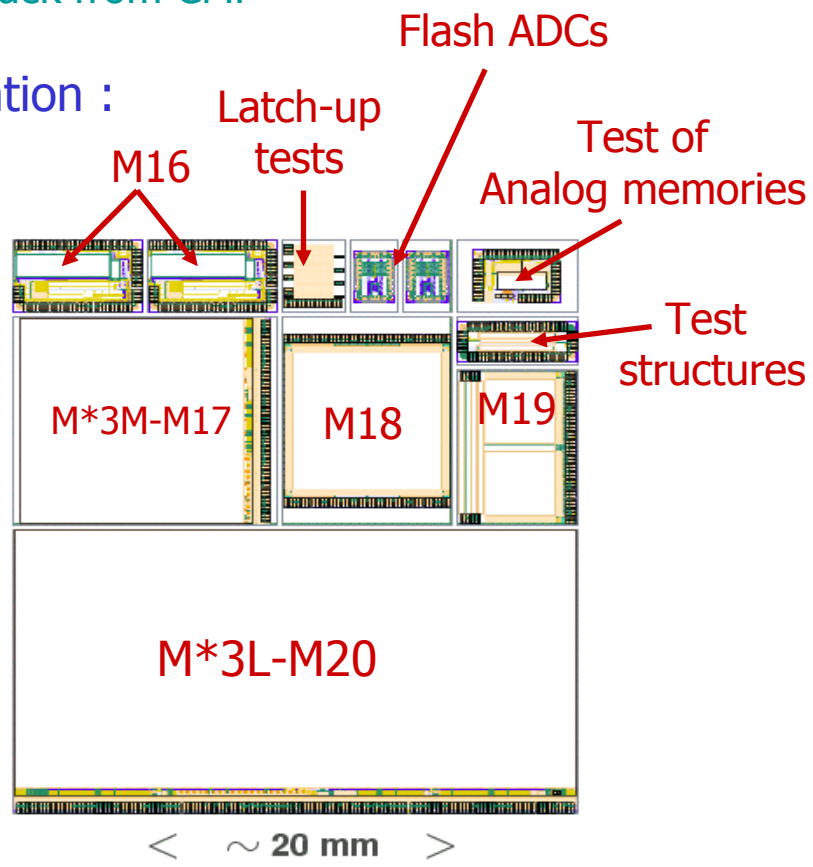
Status of the Main R&D Directions : Overview

- Engineering run (MIMOSA-16/-20, ADC, test structures) in AMS - 0.35 OPTO
- Fast read-out sensor with // processing of columns of pixels:
  - MIMOSA-8 (integ. discri.; TSMC-0.25) tested at CERN-SPS
    - spatial resolution (binary encoding) ~≤ 7 µm
  - MIMOSA-16 = AMS-0.35 OPTO version of MIMOSA-8
    - manufactured in Summer (engin. run)
  - Development of fast integrated ADC :
    - several different architecture prototypes fabricated
- Vertex Detector data size :
  - Study of efficiency vs fake hits
    - constraints on design features and performances
- Other on-going activities:
  - Industrial thinning
    - individual chips of ~ 5 x 5 mm^2 (MIMOSA-10) to 50 μm
  - MIMO* development
    - data taking with heavy ion collisions at the corner
  - EUDET : beam telescope demonstrator made of MIMOSA sensors
    - should start data taking in 2007

Engineering Run
in AMS-0.35 OPTO Technology

AMS-0.35 OPTO Engineering Run

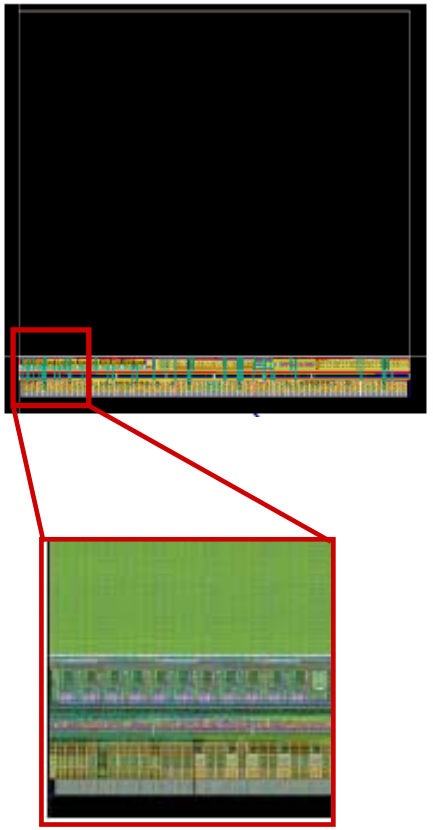
- AMS 0.35 OPTO engineering run (submitted end of June):
  - 2 + 4 wafers (8"⇨50 reticles/wafer) → just came back from CMP
  - 2 epitaxy thicknesses : ~ 11 and 16 µm
- Triggered by MIMO*-3 (= MIMOSA-20) fabrication :
  - 200 kpixels, ~ 2 cm^2, 2 // outputs, $t_{r.o.}$ ~≤ 4 ms
- includes 8 other chips :
  - MIMOSA-16 : fast col. // archi. like MIMOSA-8
  - MIMOSA-17 (MIMO-3M) :
    - rad.tol.
    - EUDET beam telescope arms
  - MIMOSA-18 (IMAGER) :
    - 10 µm pitch, precision 1 µm (EUDET: DUT)
  - MIMOSA-19 bio-med. imaging:
    - special diode shape
  - test structures :
    - in-pixel amplification, discrimination, ...
  - ADCs: flash from LPCC
- Time line :
  - 2 wafers back from foundry to CMP
    - Just received (diced) in Strasbourg
- First test results expected:
  - End of 2006 : fab. yield
  - 2007 : chip performances (also inclined tracks), performances of ~16 µm epitaxy



Advent of New Macro-Sensor : MIMOSA-17 = MIMO-3M

- Will equip EUDET telescope demonstrator (e.g. 2 arms of 3 planes)
  - Commissionning in Summer 2007 at DESY

- Medium size copy of STAR final sensor prototype :
    - (65 000 pixels instead of 205 000)
  - Manufactured in AMS 0.35 µm OPTO techno.
    - with 11 µm and ~ 16 µm epitaxial thickness
  - Tests foreseen at DESY, INFN, IPHC early 2007
  - Ionising rad. hard pixel design (validated with MIMOSA-11/-14)
  - 4 matrices of 64 x 256 pixels treated in //
    - 30 µm pitch
    - active area of ~ 8 x 8 mm^2
  - 4 parallel analog outputs at 10 (or 20) MHz
    - frame r.o. time = 1.6 ms (or 800 µs)
    - ~ 10 times faster than M5
  - Integrated JTAG logic for steering
  - Works at room temperature

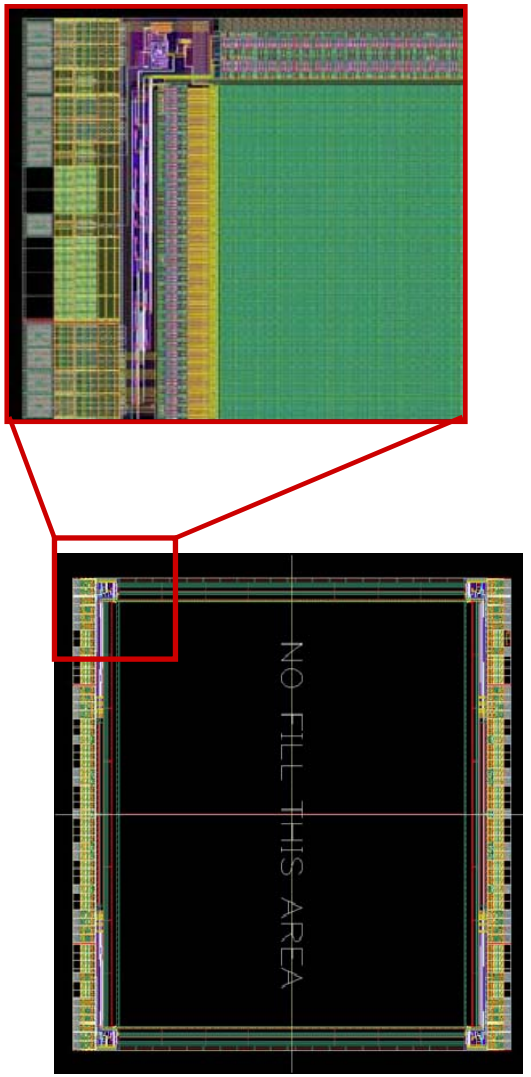


- Will equip various other devices
  - Beam telescopes (LBL-FNAL, INFN, etc.), CBM MVD demonstrator
    - allows new studies: inclined tracks, DAQ of combined sensor planes, etc.

High Resolution Sensor: MIMOSA-18

- May equip DUT surface (EUDET)
  - Provide high resol. despite mult. scattering
  - Commissionning in Summer 2007 at DESY (?)

- Design close to MIMOSA-17 with smaller pitch :
  - (260 000 pixels instead of 65 000)
  - Manufactured in AMS 0.35 µm OPTO techno.
    - with 11 µm and ~16 µm epitaxial thickness
  - Tests foreseen at IPHC Nov. '06
  - 4 matrices of 256 x 256 pixels treated in //
    - 10 µm pitch
    - active area of ~5 x 5 mm^2
  - 4 parallel analog outputs at 10 (or 20) MHz
    - frame r.o. time = 6.4 ms (or 3.2 ms)
  - Works at room temperature



High Read-Out Speed Architecture: MIMOSA-16

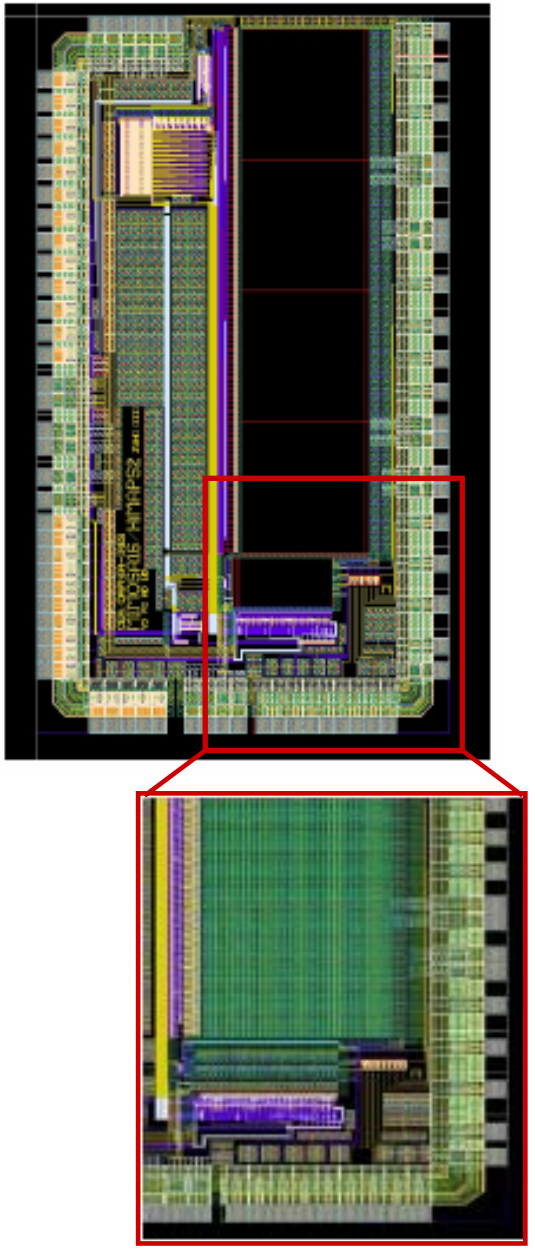
- MIMOSA-16 design features :
  - AMS-0.35 OPTO translation of MIMOSA-8
    - 11–16 µm epitaxy instead of ~ 7 µm
  - 32 // columns of 128 pixels (pitch: 25 µm)
  - On-pixel CDS (repeated at end of each column)
  - Discriminator at end of each column
  - 4 sub-arrays :
    - 2 alike MIMOSA-8

    On pixel CDS validated with M15 (2 different pitches)
    - 1 with ionising radiation tol. pixels
    - 1 with enhanced in-pixel amplification

    (against noise of read-out chain)

- Next steps :
  - lab tests in November 2006
  - beam tests Summer 2007

- Next generations :
  - Large prototype
    - 320 columns of 256 pixels
    - 15–20 µm pitch
    - integrated ⌀ micro-circuits ???
  - Small prototypes with ADCs replacing discriminators



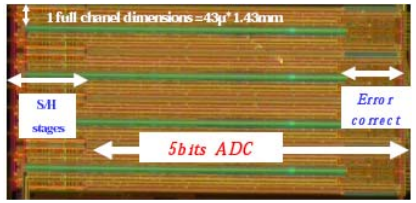
Progress on ADC developments

Progress on ADC developments and plans

- Several different ADC architectures under development
  - LPCC (Clermont) : flash 4+1.5-bit ADC
    - 1st proto tested, 2nd proto back from foundry
  - LPSC (Grenoble): Ampli + semi-flash (pipe-line) 5-bit ADC
    - 1st proto tested, 2nd proto under test
  - DAPNIA (Saclay) : Ampli + Suc.App.R (4- and) 5-bit ADC
    - 1st proto under test
  - IPHC (Strasbourg) : SAR 4-bit and Wilkinson 5-bit ADCs:
    - 1st proto submitted end October 06

LPCC, new comparator

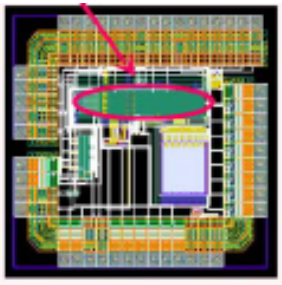
LPSC, 5-bit ADC



- Present outcome of development :
  - Typical differences between architectures :
    - ~ factor 2 in power & speed
  - Observed pbs: loss of 1–2 bits

  (e.g. due to offset dispersion between columns)
    - solutions under study
    - ⇨ include enhanced signal amplification before ADC

DAPNIA, 6 ADC in //



- Next steps :
  - Final ADC designs expected to come out in 2007
  - Submission of 1st col. // pixel array proto equipped with ADCs & ∅ end 2007

Vertex Detector Data Flow

- Raw data flow (in absence of any signal):
  - total = 5 Gpixels / train ⇨ 25 Gpixels / s
  - 3 Bytes / pixel (20 address bits + 5–4 charge bits) ⇨ **raw data flow ⇨ 75 GB/ s**

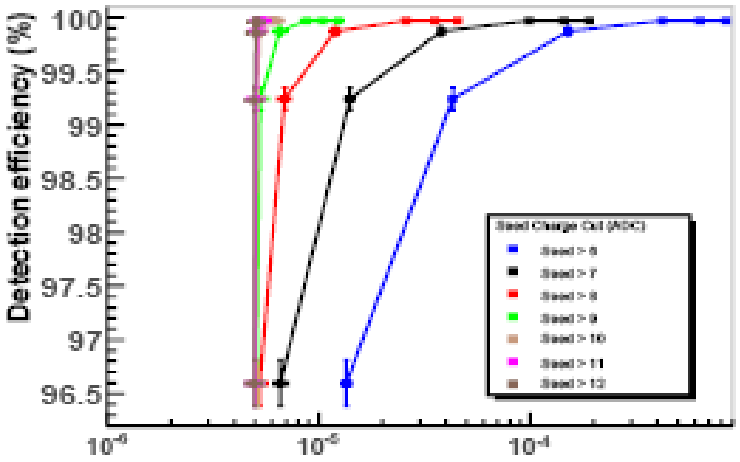
- Signal data size dominated by $e^{\pm}_{BS}$:

  ≥~ 10^3 hits / BX ⇨ $3 \cdot 10^6$ hits / train
  - Assuming 5 pixels / cluster : $15 \cdot 10^6$ pix / train ⇨ 45 MB/ train
  - Uncertainties on beamstrahlung rate prediction
    - (factor 3 - 5) ⇨ 135–225 MB/train ⇨ 0.7–1.1 GB/ s

- Efficiency vs rate of fake clusters
  - studied on real (MIMOSA-9) beam test data:

- Eff_{det} ~ 99.9 % for fake rate ~ 10^{-5}
- Electronic noise ~≤ 1–10 MB/s after sparsification ⇨ negligible

Efficiency vs fake rate



Plans for the coming years

Mid-Term Objectives of CMOS Sensor Development

- 2006 :
  - Production (engineering run) :
    - STAR demonstrator final proto., EUDET Beam Telescope demonstrator
    - studies : yield, "20 μm" option, thinning, perfo. with inclined tracks, ...
  - Prototyping :
    - various ADCs, col. // discri. archi., high-resol. array, ...
- 2007 :
  - Production (engineering run):
    - final chip for STAR demonstrator (analog output)
  - Prototyping :
    - small array with integ. ADC/col. , medium size fast array with integ. discri., Ø μcircuits, new fab. techno., stitching (?)
- 2008 :
  - Production (engineering run):
    - EUDET Beam Telescope final sensor (digital output)
  - Prototyping :
    - medium size pixel array with integ. ADC & Ø, new fab. techno., 1st ladder equipped with fast sensors (?), ...
- 2009 :
  - Production (engineering run):
    - final STAR-HFT sensors (digital output), etc.

Summary

Summary

- Engineering run in AMS 0.35 OPTO technology completed (triggered by STAR HFT):
  - 6 wafers fabricated (5 different sensors, 1 ADC, test structures)
    - Tests Nov. 2006 - Summer 2007 + fabrication yield + ~16 µm epitaxy option
  - New generation of real size sensors (still with analog output)
    - 2 for EUDET beam tel. demonstrator ; 1 for CBM demonstrator ; 1 final STAR proto.

- Fast column parallel architecture with digitised output :
  - Small proto. of binary output architecture fabricated in AMS 0.35 OPTO
    - Next step (2007 ?) : real size (e.g. 320 x 256 pixels, 15 µm pitch) proto. ?
  - ADC devt progressing steadily final architectures expected in 2007
    - Next step (2007 ?) : small sensor proto. with integ. ADC instead of discri. at end of each column

- Sensors will soon be operated in real experimental conditions :
  - 2007 : EUDET tele. demonstrator ; MIMO*-2 ladder inside STAR-DAQ
  - 2008 : STAR HFT : 2 layers of 60 + 180 sensors (~100 MPix) ; CBM demonstrator

Back up

Mid-Term Applications of CMOS Sensor

- CMOS sensors will be operated in real (less demanding) experiments before end of decade
  - Opportunity to assess their performances for the ILC running conditions
- MIMOSA sensors will equip STAR Heavy Flavour Tagger:
  - 2008: analog output, 4 ms frame r.o. time
  - 2011: digital output, 200 µs frame r.o. time
- Similar sensors will equip EUDET beam telescope:
  - 2007: demonstrator with analog output
  - 2008: final device with digital output
- Other applications of STAR-HFT sensors :
  - Beam telescopes at LBL-FNAL
  - INFN demonstrator of CBM Micro-Vertex-Detector

data flow

- L0 : 25 Mpixels read 40 times / train = 1 Gpixels / train
- L1 : 50 MPixels read 20 times / train = 1 Gpixels / train
- L2 + L3 + L4 : ~≤300 Mpixels read ~≤10 times /train = 3 Gpixels / train
  - total = 5 Gpixels / train ⇨ 25 Gpixels / s
  - 3 Bytes / pixel (20 address bits + 5–4 charge bits) ⇨ **raw data flow ⇨ 75 GB/ s**

Integration issues

- Thinning of individual chips smaller than a reticle :
  - 5 copies of MIMOSA-10 ($\sim$ 4 x 5 mm^2) thinned to 50 µm
    - no visible damage
  - 50 µm thin MIMOSA-5 (3.5 cm^2) chips being characterised on ALS beam (1.5 GeV e$^-$) by LBNL team
  - several copies of MIMOSA-5 (3.5 cm^2) sent to Dalian Univ. (μelectronics Depmt) for dedicated thinning (etching).

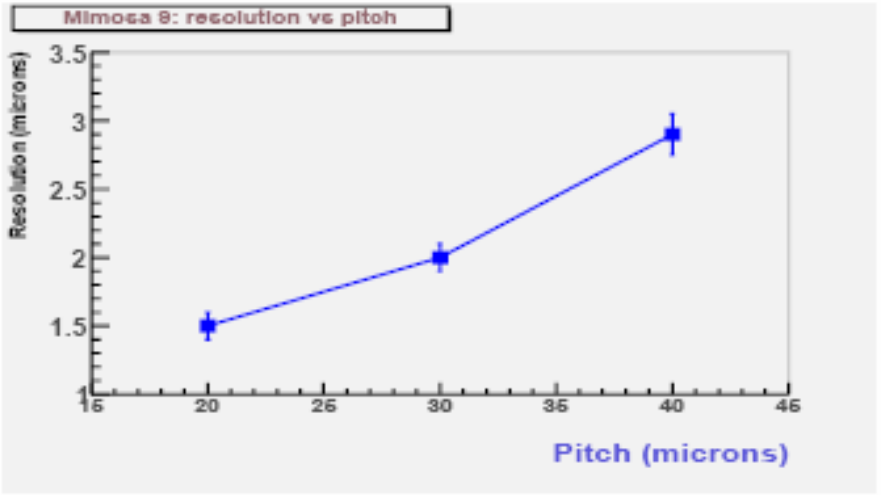
- Development of mechanical supports and chip servicing :
  - 50 µm thin MIMO-2 chips being mounted on ladder and installed inside STAR
    - real condition tests (within STAR DAQ)
  - MIMOSA-5 chips (thinned to 50 µm) sent to RAL-Liverpool for mounting tests on ultra light (0.1 % X0 ?) mechanical supports developed by LCFI coll.

plans

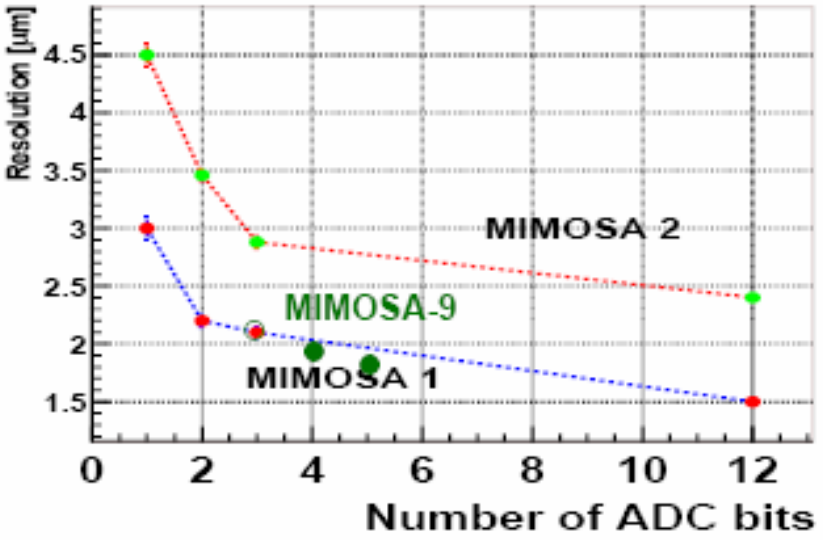
Application	version	2006	2007	2008	2009	2010	2011
STAR	HFT-1	proto. final	Prod.				
	HFT-2	R&D	R&D	proto final	Prod.		
EUDET	BT-1	2 Prod.					
	BT-2	R&D	proto final ?	Prod.			
Imagerie		R&D	proto final	Prod. ?			
Thèmes génériques							
Capteurs rapides :	○ architecture	R&D	R&D	R&D +	R&D ++	proto ILC	proto CBM
	○ ADC	R&D	proto final	↗			
	○ numérique	pré-étude	R&D	proto final	↗		
Tolérance aux rayonnements		R&D	R&D	R&D	R&D	↗	
Technologies de fabrication		R&D	R&D	R&D	R&D	↗ ???	
Amincissement		R&D	R&D	R&D	OK ???		
Aboutement		–	pré-étude	R&D	R&D	OK ???	

AMS-0.35 OPTO Perfomances : Spatial Resolution

- **Single point resolution versus pixel pitch:**
  - clusters reconstructed with eta-function, exploiting charge sharing between pixels
  - $\sigma_{sp} \sim 1.5\ \mu m$ (20 μm pitch)
    $\rightarrowtail \sigma_{sp} \lesssim 2\ \mu m$ (30 μm pitch)
  - obtained with signal charge encoded on 12 bits



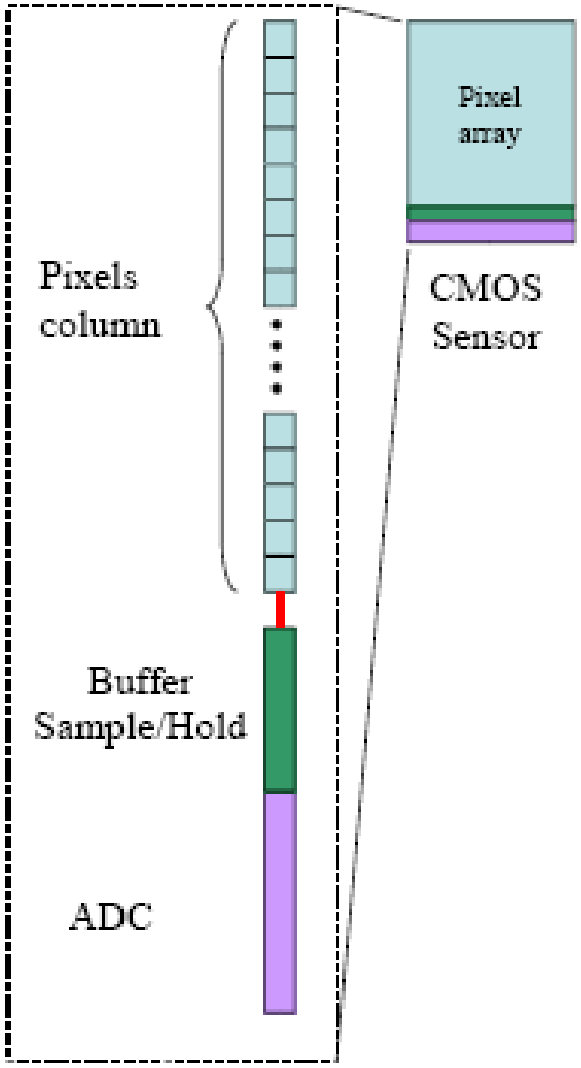
- σ_{sp} dependence on ADC granularity:
  - minimise number of ADC bits
    $\rightarrowtail$ minimise dimensions, $t_{r.o.}$ & P_{diss}
  - effect simulated on real MIMOSA data
    (20 μm pitch ; 120 GeV/c π^- beam)



- $\sigma_{sp} < 2\ \mu m$ (4 bits) $\rightarrowtail$ 1.7–1.6 μm (5 bits)
  (MIMOSA-9 : 20 μm pitch; T= + 20°C)

- Warning : results based on simple pixel (N $\lesssim$ 10 e^- ENC)
  $\Rightarrow$ rad. tol. pixel integrating CDS (N $\lesssim$ 15 e^- ENC) not yet evaluated

Development of ADC at IPHC



Successive Approximation ADC

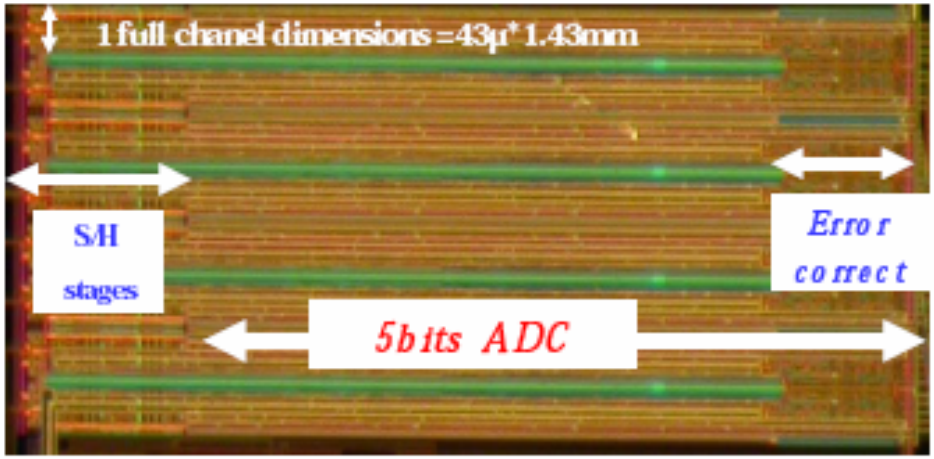
- Process : 0.35 µm AMS , Hi-Res Substrate
- 4 bits ADC (LSB = 7,8 mV)
- Analog input dynamic : 125 mV
- Core area : 25 µm × 920 µm.
- Conversion speed : 7.1 MS/s and 6.25 MS/s
- Static power dissipation : 330µW

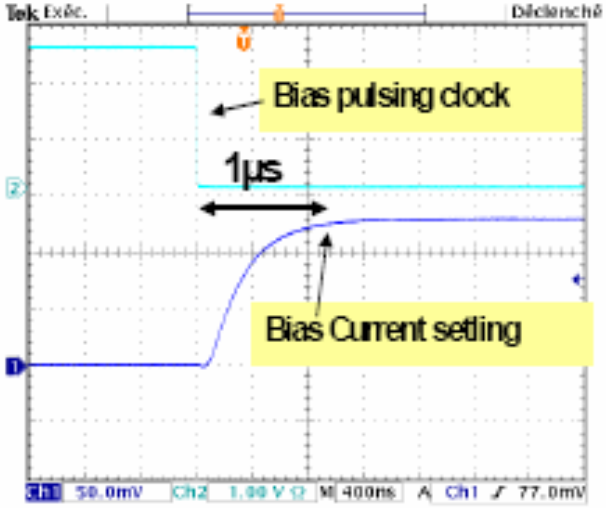
Double Scale Wilkinson ADC

- Process : 0.35µm AMS , Hi-Res substrate.
- 4 bits ADC (LSB = 7,8 mV)
- Analog input dynamic : 125 mV
- Core area : 25 µm × 840 µm.
- Conversion speed : 10 MS/s and 6.67 MS/s
- Static power dissipation : 250µW

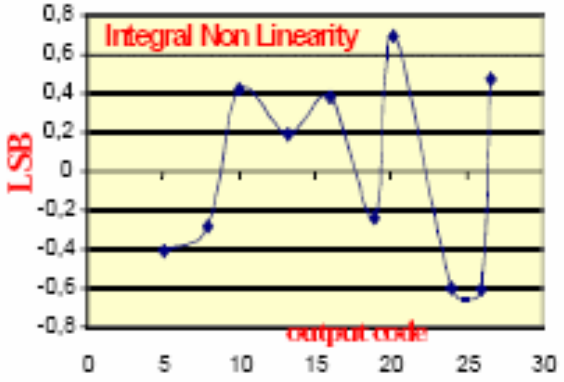
Submission of 2 chips : 24 October 2006

S/H & 5 bits Pipe line ADC =>(LPSC)

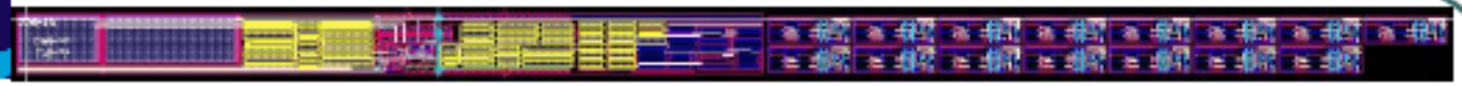




	Sample & Hold	5 bits ADC
Frequency	25Mhz	25Mhz
Dimensions	43µ *250µ	43µ *1200µ
Power@3.3V	0.413 mW	1.287 mW
Power@2.5V	0.313 mW	0.975 mW



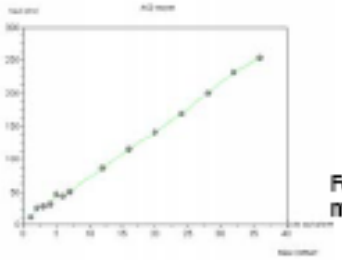
Status of R&D at LPC-Clermont



VADC juin 06 1100x45 µm²

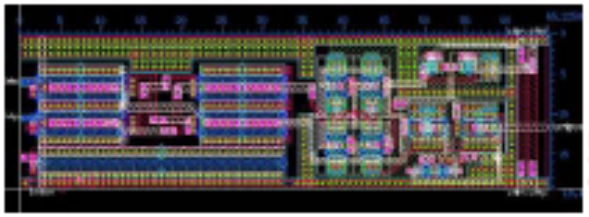
Flash ADC 20 Mhz, 2 mW, 4 bits/300 mV pour ILC VDET (collaboration LPC-IRES)

- Septembre 05
  - Version 3.3 V
  - Consommation x20 !
  - Offsets comparateurs > lsb (= 15 mV)

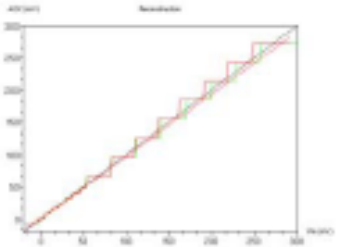


Fonction de transfert moyenne non monotone

- Juin 06
  - Version **2.5 V**
  - Fonderie le 26 juin
  - Nouveau comparateur d'offset réduit
  - Double étage d'entrée (gain x3)
  - Répartition non linéaire des points de basculement
  - 20 MHz (taille et consommation double, 1 pour 2 voies)
  - Echelle résistive compensée pour une charge de 1 pF

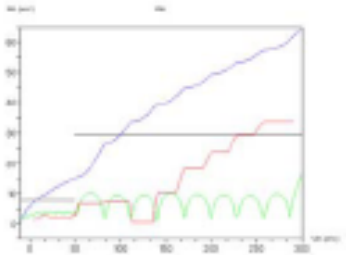


Nouveau Comparateur 65x15 µm²



Fonction de transfert

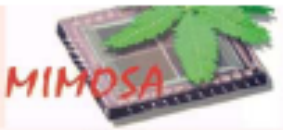
Idéal (vert)
Simulé (rouge)



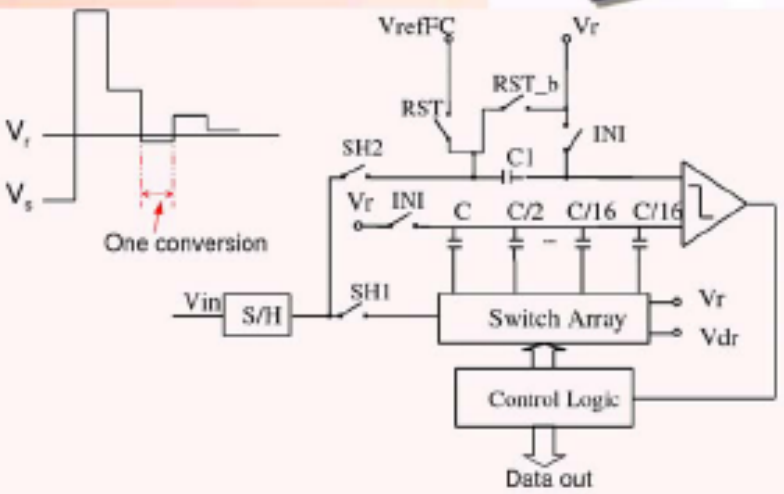
INL

Status of R&D at DAPNIA

ADC à approximation successive (DAPNIA)

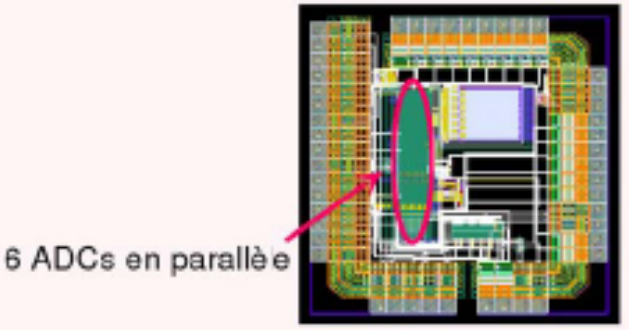


- Type : Approximation successive
- Discrimination intégrée pour limiter la puissance dissipée
- Dimensions: 25 µm x 1 mm (comprenant le S&H et le sérialiseur)
- Deux versions : 5-bit et 4-bit
- Temps de conversion : ~250 ns
- Puissance dissipée :
  Vin < VrefFC → ~350µW (diss. statique)
  Vin > VrefFC → >350µW (statique+dynamique)



- Tests en cours

- Fonctionnel mais bits manquants (pour les faibles dynamiques) à cause des couplages dus au layout
- Refaire le layout & intégrer un amplificateur entre le pixel et l'ADC?



Layout du prototype soumis en mars 2006
(Techno : AMS CMOS 0.35µm Opto)