Status Report
DEPFET Active Pixel Sensors for the ILC

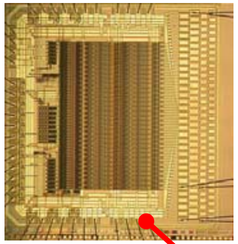
Laci Andricek

for the DEPFET Collaboration
(www.depfet.org)

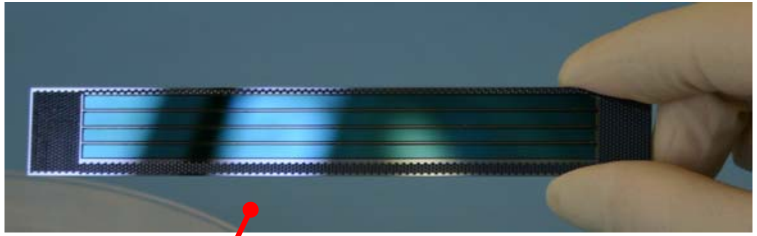
The DEPFET ILC VTX Project

mpi halbleiterlabor

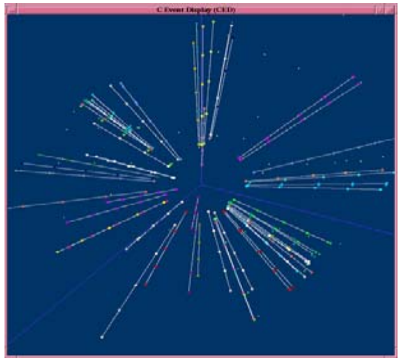
✓ steering chips Switcher



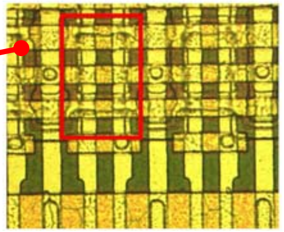
✓ thinning technology

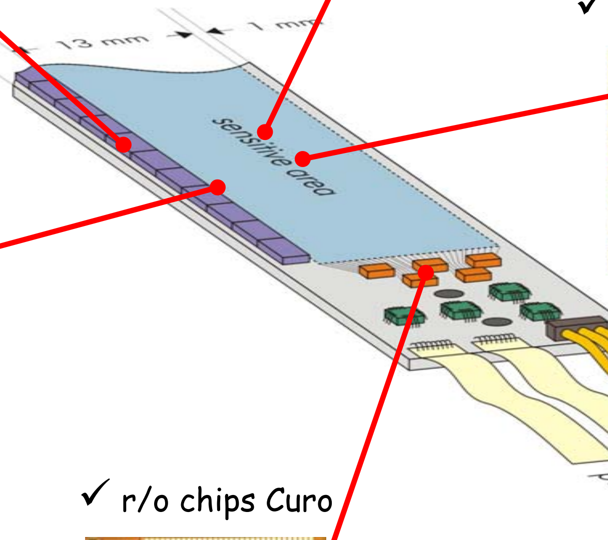


✓Simulation

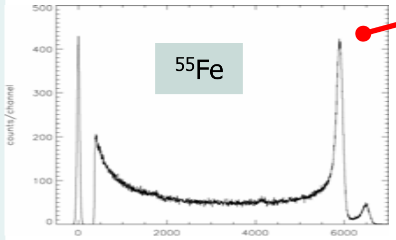


✓sensor development

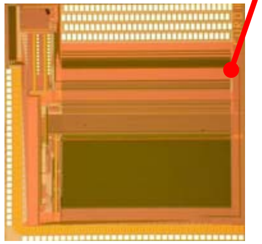




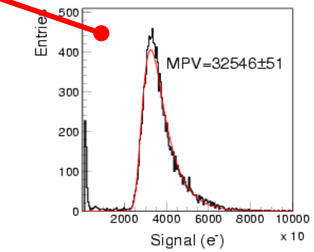
✓ radiation tolerance



✓ r/o chips Curo



✓beam test

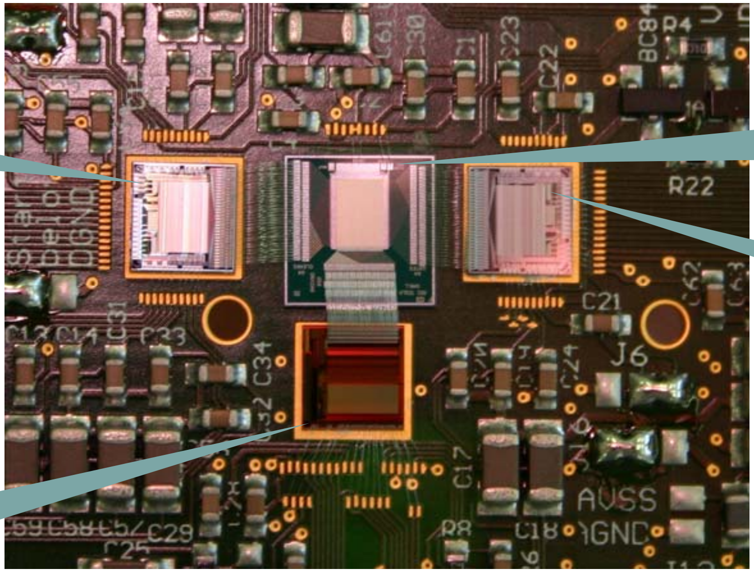


Outline

- The new Switcher
- System Performance - Beam Test
- Improving the DEPFET Pixel Cell - New Production
- Thinning Technology - Latest Results

- Summary

ILC Prototype System



Gate Switcher

DEPFET Matrix
64x128 pixels, 33 x 23.75µm^2

Clear Switcher

- 2 analog MUX outputs with
- 64 channels each
- Can switch up to 25 V
- 0.8µm AMS HV technology

radhard version submitted
→ P.Fischer @ Vertex06

Current Readout
CUROII

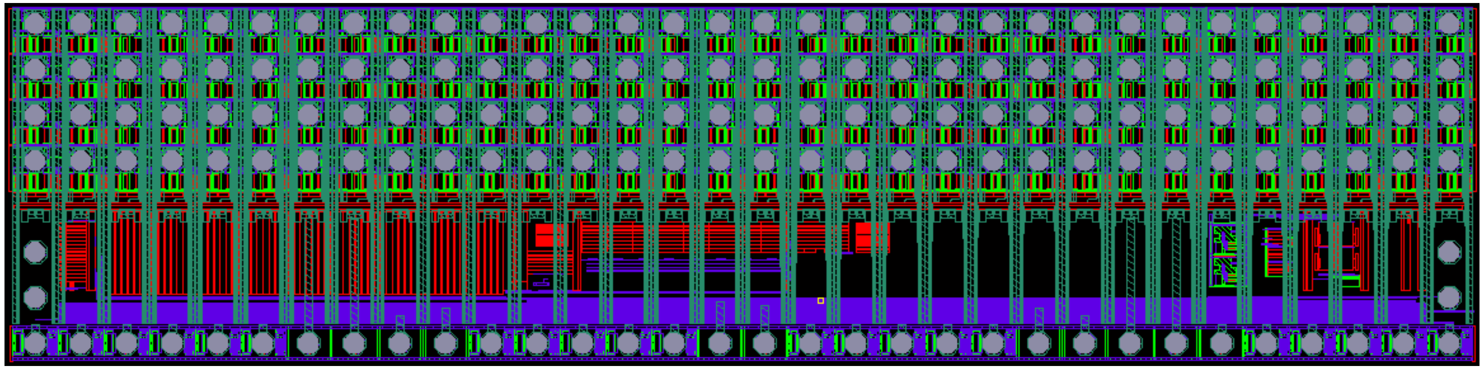
- current based 128 channel readout chip
- 50 MHz band width in the f/e
- On-chip pedestal subtraction by switched current technique (CDS)
- Real time hit finding and zero suppression
- 0.25µm CMOS technology (radhard design)

Switcher 3 Layout (submitted 16.8.06)

Main features:

- 128 channels
- Radiation Hardness ⇒ use ≤ 0.35µm technology (‘3.3V’) with enclosed layouts etc.
- 10V swing ⇒ use stacked transistors
- ‘zero’ standby current ⇒ use ac coupling in ‘level shifters’

- Flexible sequencer
- Pad geometry for bump bonding (gold stud for prototypes)
- Minimum number of control / power signals

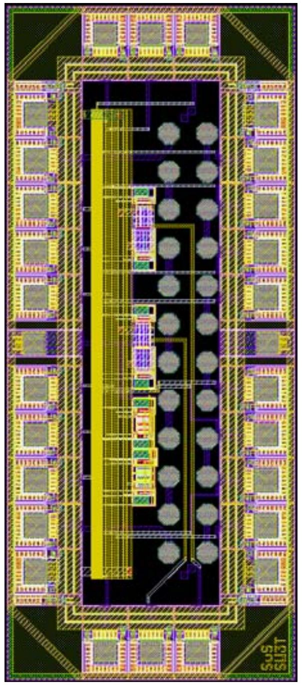


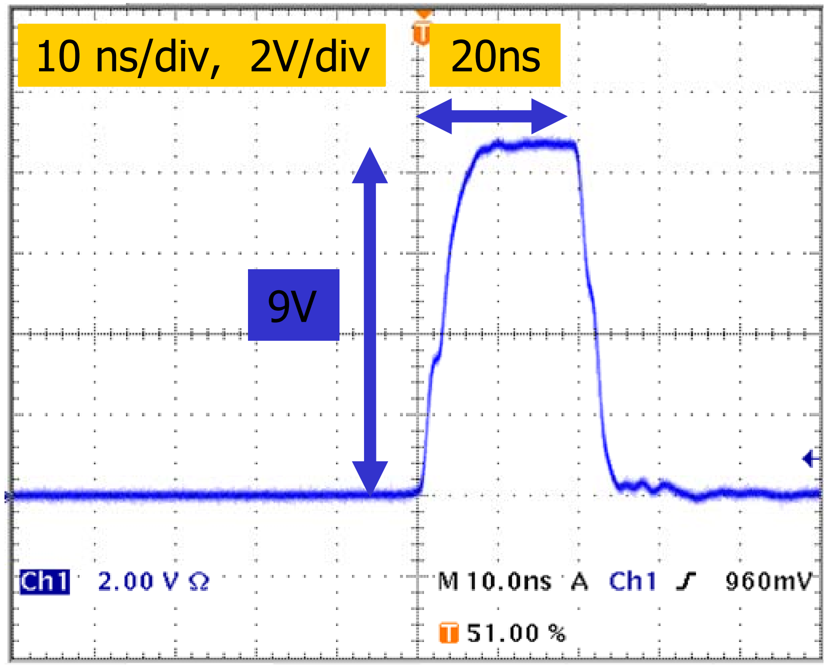
full chip:
5.8 x 1.24 mm^2

slim enough to fit on
the "balcony" of the ladder

Results of Test Chip SW3T

- Test chip with various switch designs has been submitted and tested.
- High voltage technology (AMS H35, 4M) has been used to separate wells.

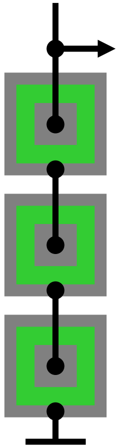




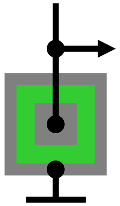
Supply = 3+3+3 = 9V, C_{load} ~ 15pF

First Irradiation Results: Test Chip SW3T

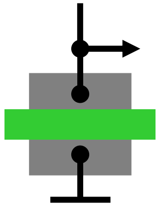
X-ray irradiation (as Switcher 2) up to ~600 krad, (V_{GS} = 3V)



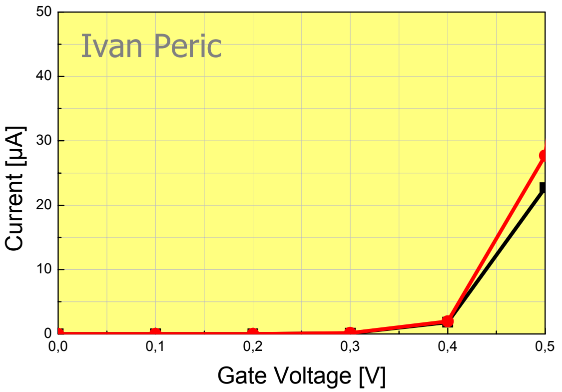
stacked 'normal' annular NMOS

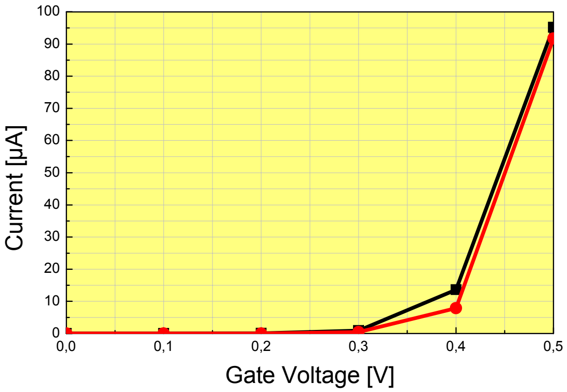


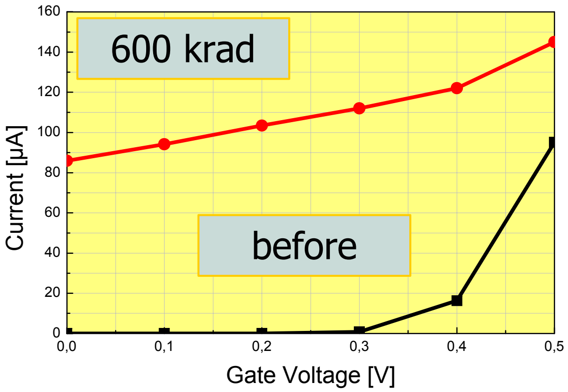
'HV' NMOS:
thin gate oxide,
extended thick drain,
enclosed gate



'HV' NMOS,
normal layout







No (significant) threshold shift or leakage current for annular structures!!

Test Beam(s)

:- 5 test beam periods have been done in the past

3 x @ DESY (1-6 GeV e^-) – spatial resolution limited by multiple scattering to ~6μm for us.

2 x @ CERN (120 GeV π) – August and October 2006. Analysis in progress...

:- Reference system is the 4 layer Silicon strip telescope (Bonn)
(double sided strip detectors, 50 μm pitch)

:- Sensors are

450μm thick (mip = 36ke)

min. pixel size = **33x23.75μm²**

various DEPFET variations have been studied

:- Speed:

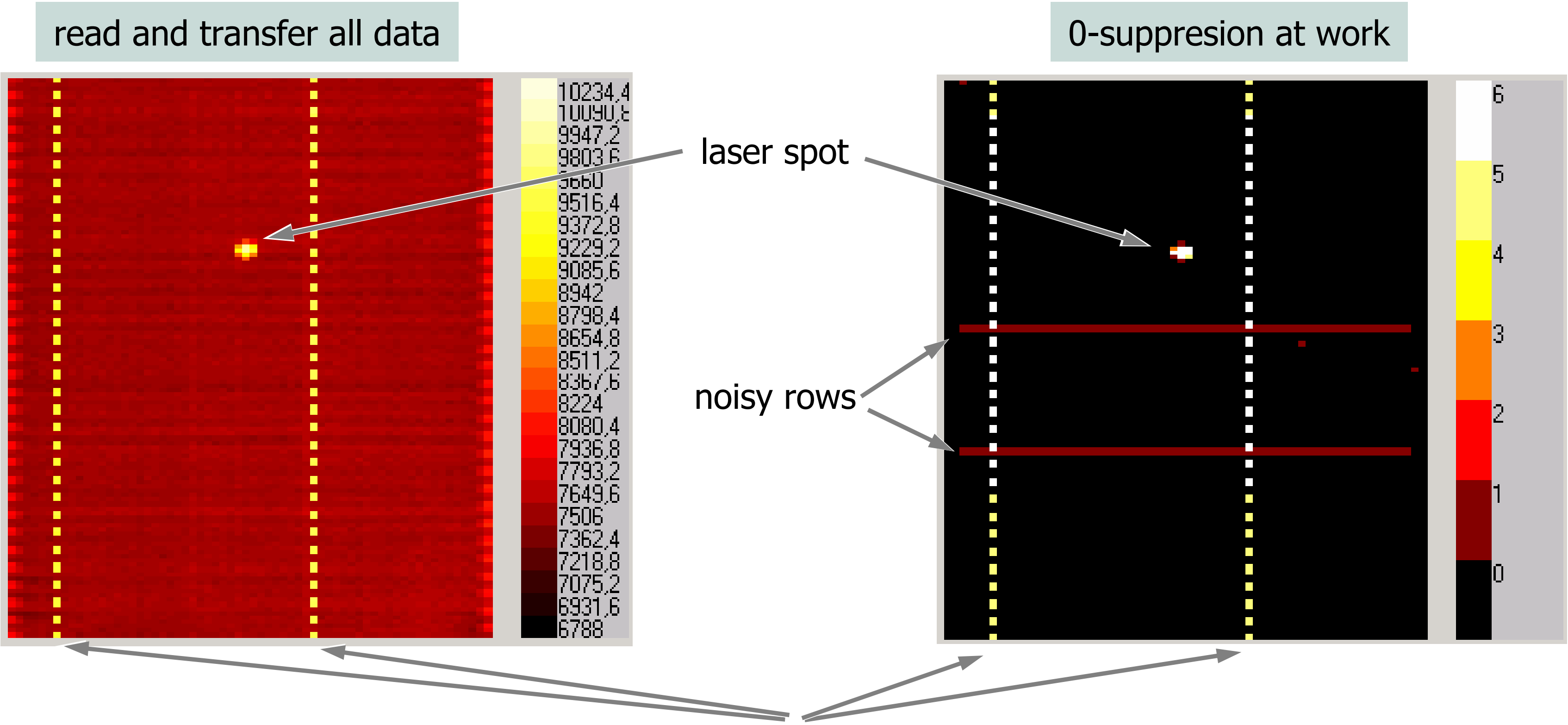
Clearing in 20ns

Sample-clear-sample in CURO: ~ 240 ns (This would give a 4 MHz row rate)

Non-zero suppressed readout (mostly)~ 800 μs/frame (128 rows) → ~ 6 μs/row

In the recent CERN test beam, a **beam telescope of 5 DEPFET planes** has been successfully operated!

Zero suppression



read and transfer all data

0-suppresion at work

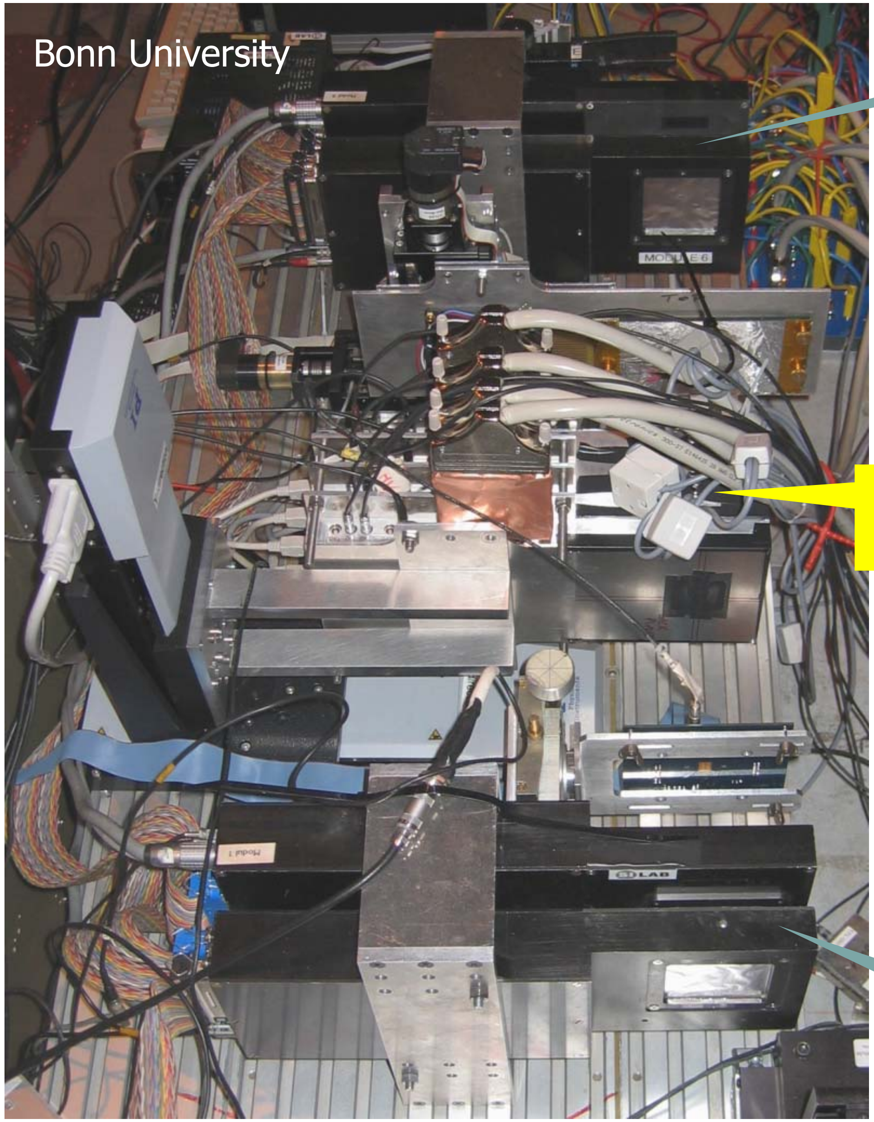
laser spot

noisy rows

test pulses, current injected in the front end

...well... it works!!
Has been used in the CERN test beams, let's wait for the results...

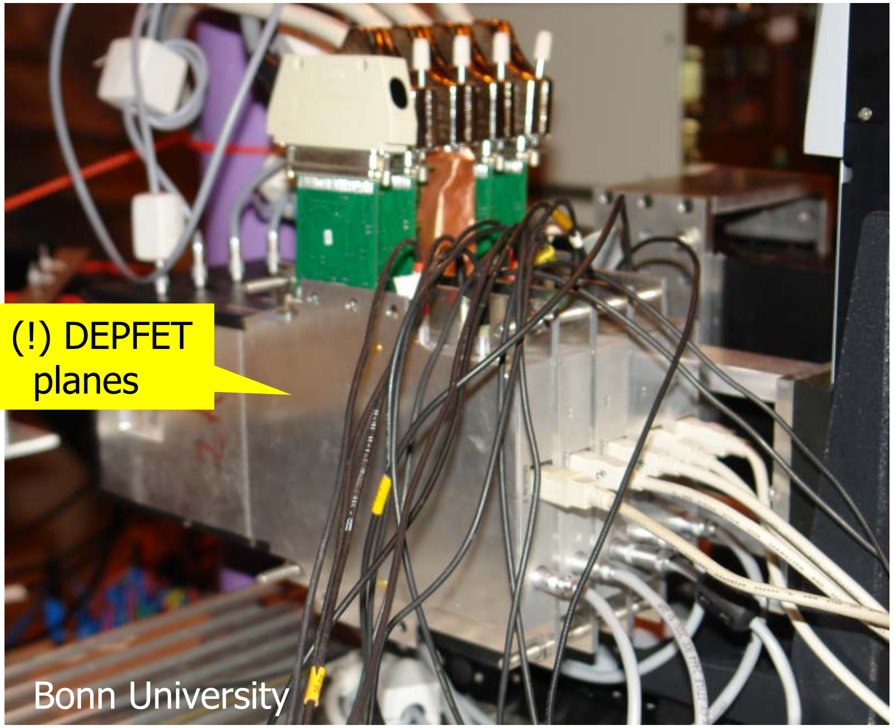
Test Beam Setup (at CERN)



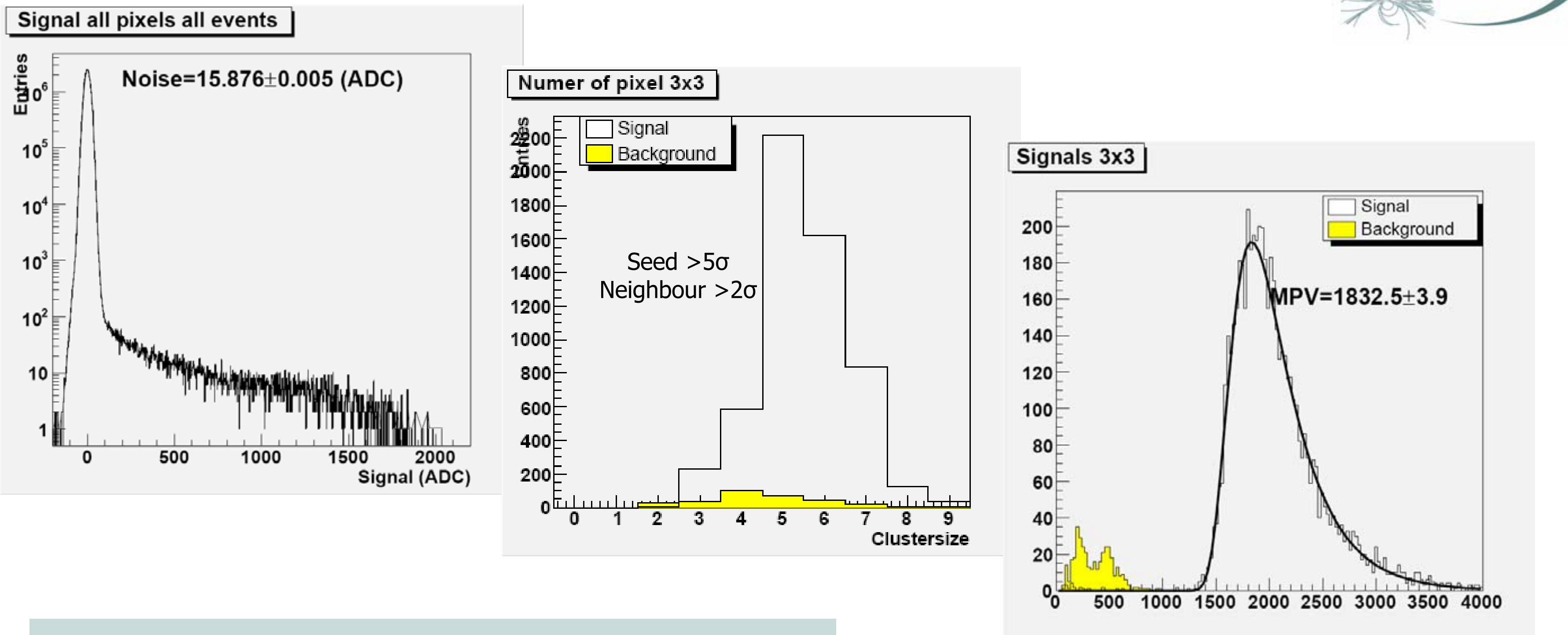
2 strip planes

5 (!) DEPFET planes

2 strip planes



Test Beam at DESY, Jan. '06



(Jaap Velthuis)

- Noise is determined from pedestal variations
- Seed pixel has signal >5 σ in central area
- Add neighbours if signal ≥2σ
- charge mostly confined in 3x3 cluster

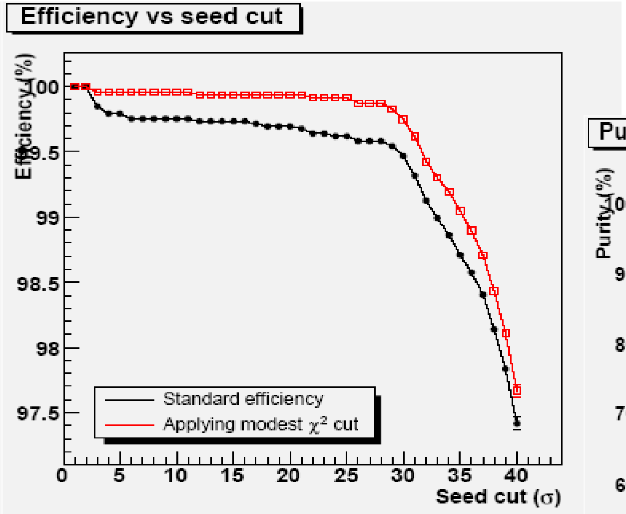
- S/N ≈ 110..115 (for 450 µm sensor!)
- Noise about 230 - 300 e- ENC

Usual suspects: system x-talk

CURO, external I2V converter…

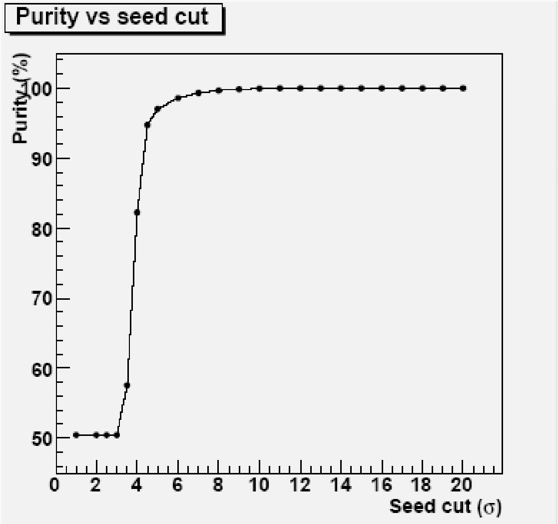
There is still room for improvement

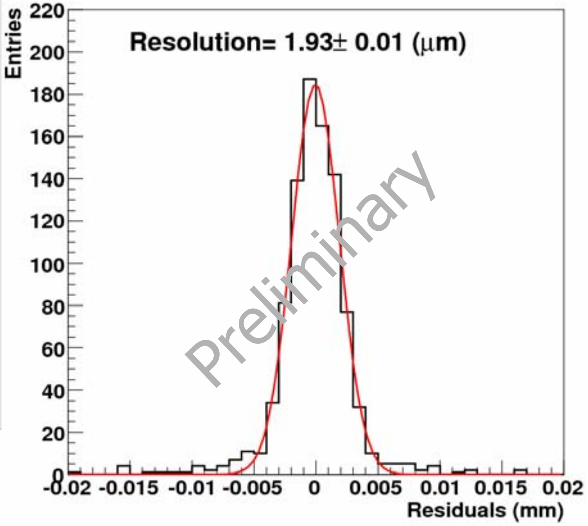
Efficiency & Position resolution



$$\text{Efficiency} = \frac{\text{Number of tracks with cluster}}{\text{Total number of tracks}}$$

$$\text{Purity} = \frac{\text{Number of clusters with tracks}}{\text{Total number of clusters}}$$





(Jaap Velthuis)

For 5 σ seed cut

- Efficiency ≈ 99.96%
- Purity ≈ 99.6 %

First preliminary result from CERN test beam,

129 GeV π, 33x23.75 μm² pixels

position resolution ≈ 2 μm

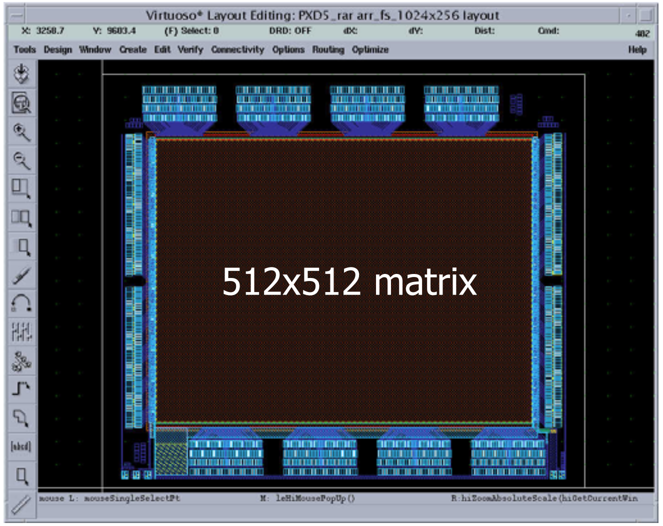
New DEPFET Generation ‘PXD5’

- Mostly use ‘baseline’ linear DEPFET geometry

- Build **larger matrices**
  Long matrices (full ILC drain length)
  Wide matrices (full Load for Switcher Gate / Clear chips)

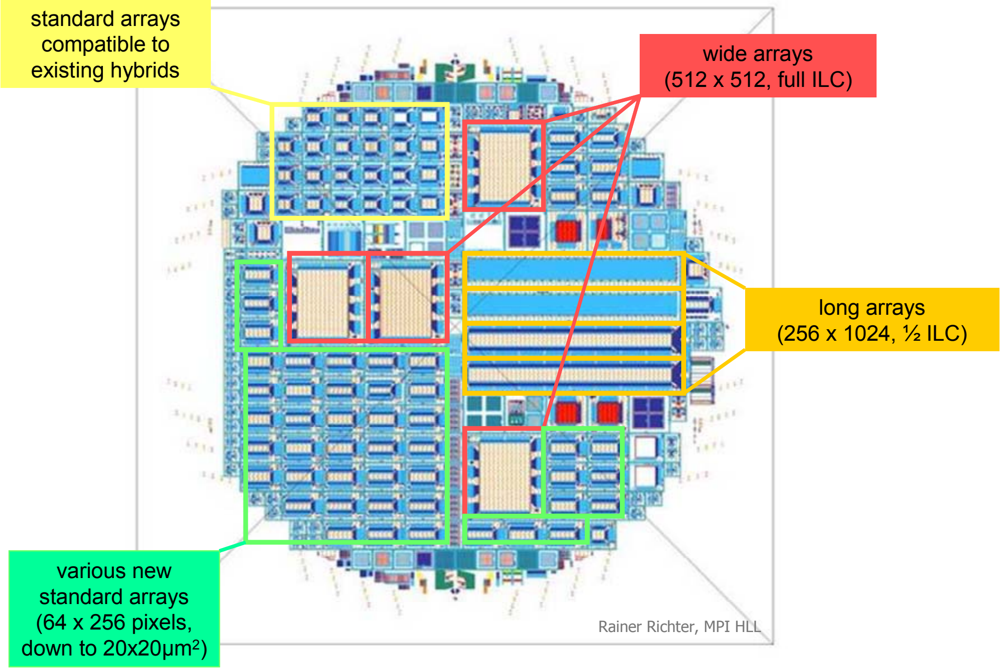
- Try new DEPFET variants:
  reduce **clear voltages** (modified implantations, modified geometry)
  Very **small** pixels (20µm x 20µm)
    - Increase internal **amplification** (g_q)

- Add some bump bonding test structures


Virtuoso® Layout Editing: PXD5_rar arr_fs_1024x256 layout

X: 3258.7 Y: 9603.4 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd: 402

mouse L: mouseSingleSelectPt M: leHiMousePopUp() R:hiZoomAbsoluteScale(hiGetCurrentWin


standard arrays compatible to existing hybrids

wide arrays (512 x 512, full ILC)

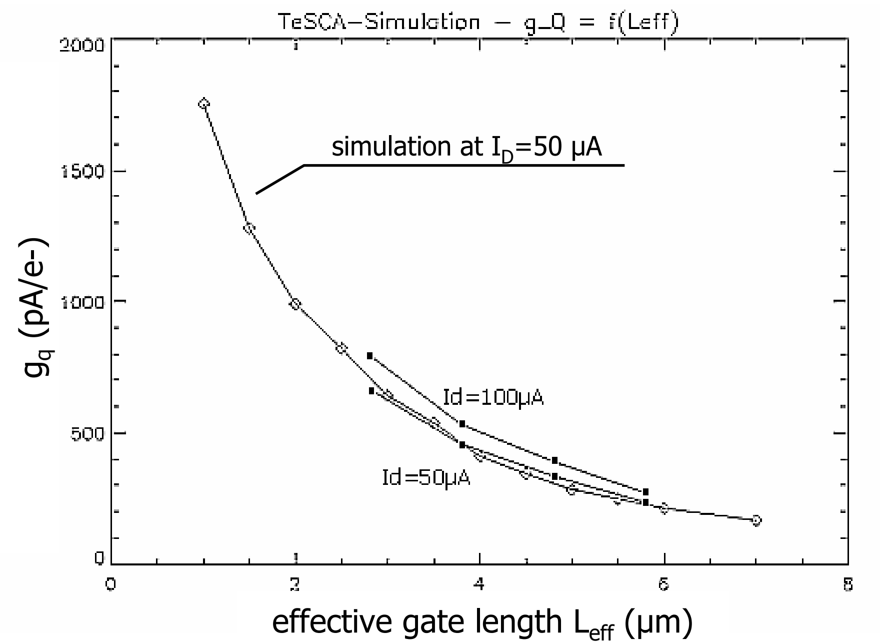
long arrays (256 x 1024, ½ ILC)

various new standard arrays (64 x 256 pixels, down to 20x20µm²)

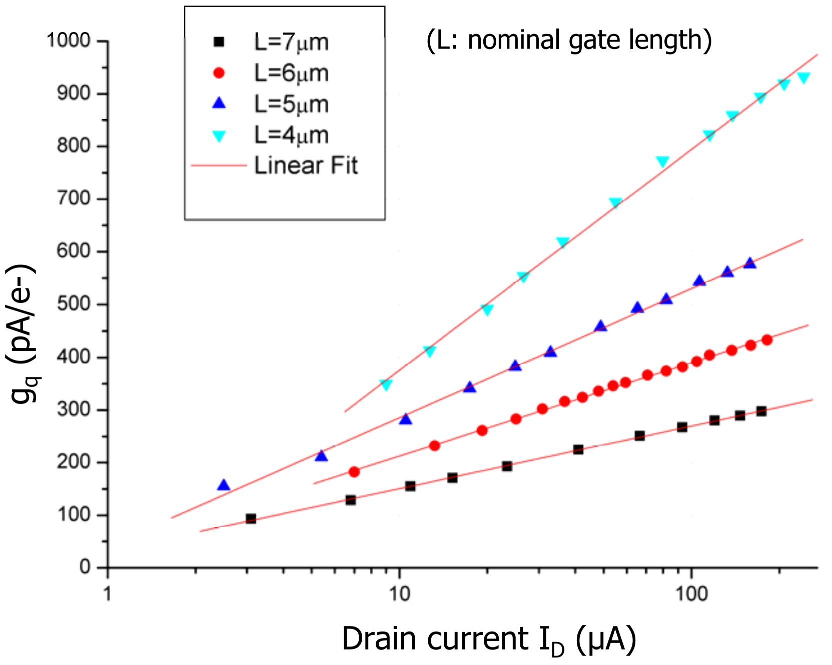
Rainer Richter, MPI HLL

Internal amplification g_q

$$g_q = \frac{dI_D}{dQ} = -\frac{\mu_p}{L^2}(V_{GS} - V_{th})$$ (neglecting short channel effects)



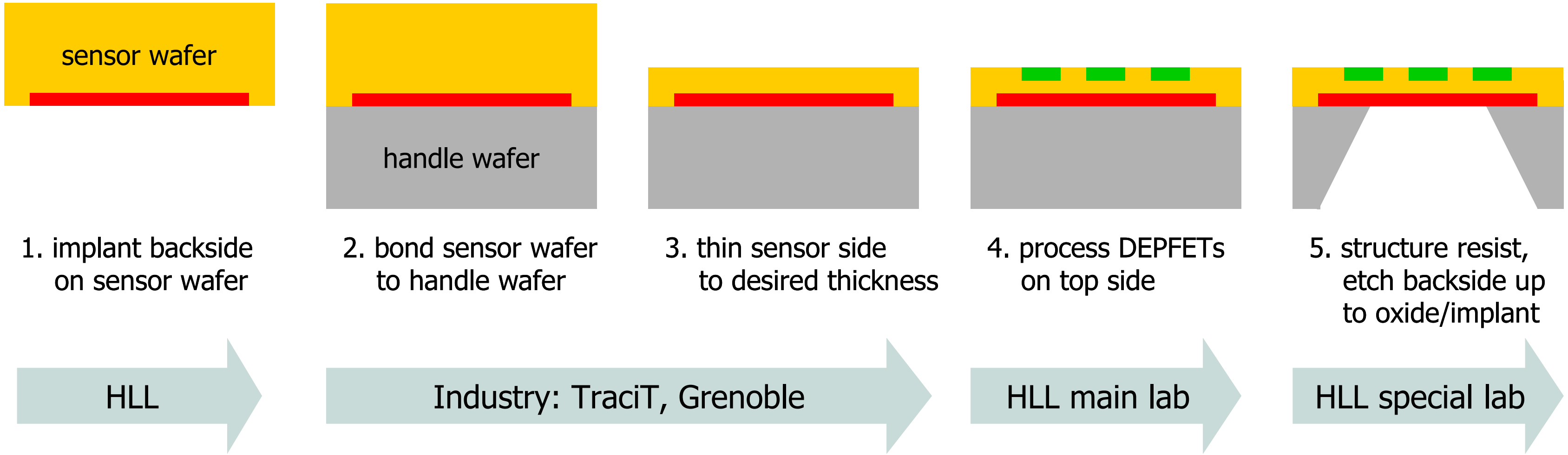
L_{eff} = L - 2 x under etching of 1.2µm



As long as noise is dominated by r/o chip → S/N linear with g_q

PXD4 has L=6µm, some matrices in PXD5 have now L=4µm → expect factor 2 better S/N

Thinning Technology



1. implant backside on sensor wafer
2. bond sensor wafer to handle wafer
3. thin sensor side to desired thickness
4. process DEPFETs on top side
5. structure resist, etch backside up to oxide/implant

HLL → Industry: TraciT, Grenoble → HLL main lab → HLL special lab

New: **150mm Ø** wafers!

New: Wafer bonding and thinning in **industry**

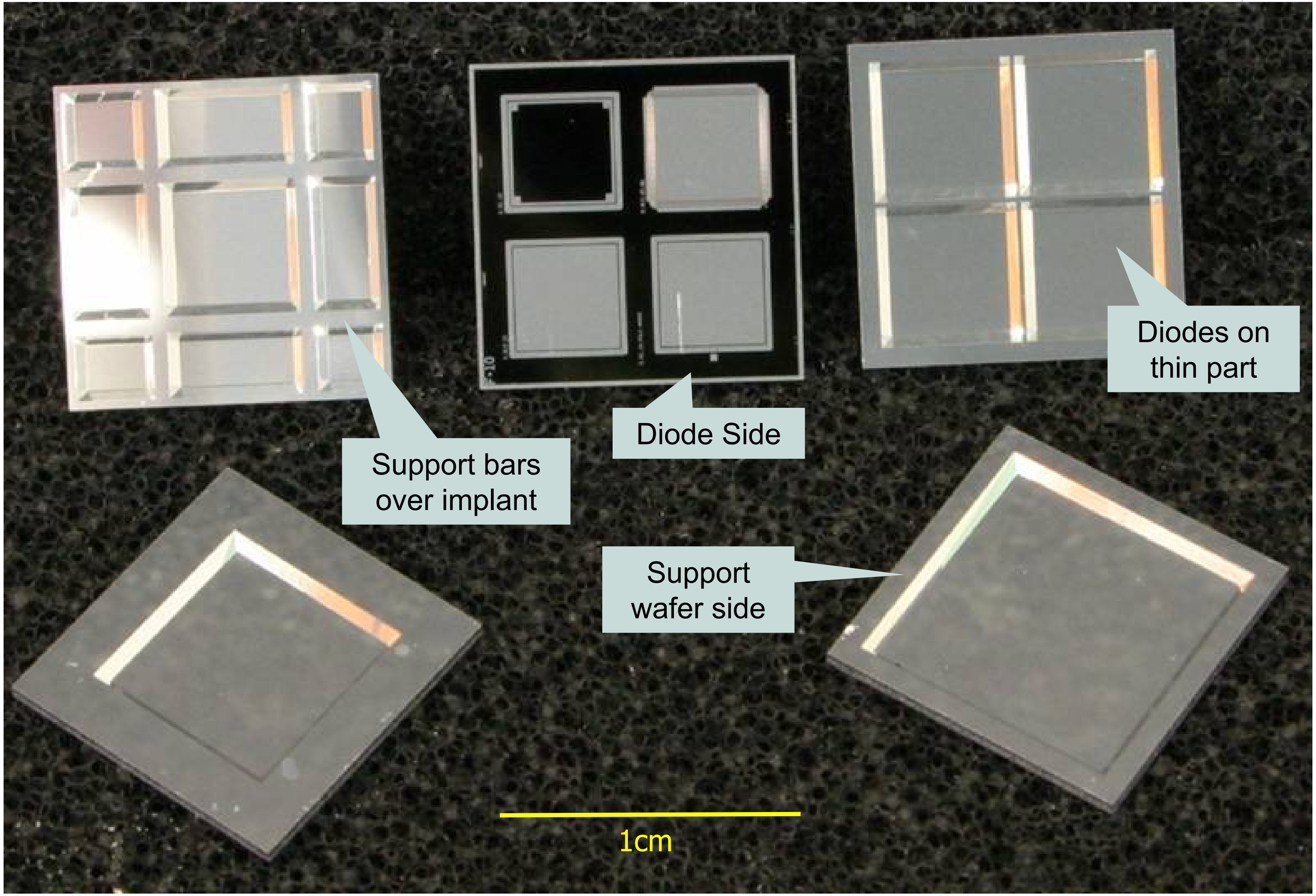
New: Processing in **HLL main lab**

Still in R&D phase:

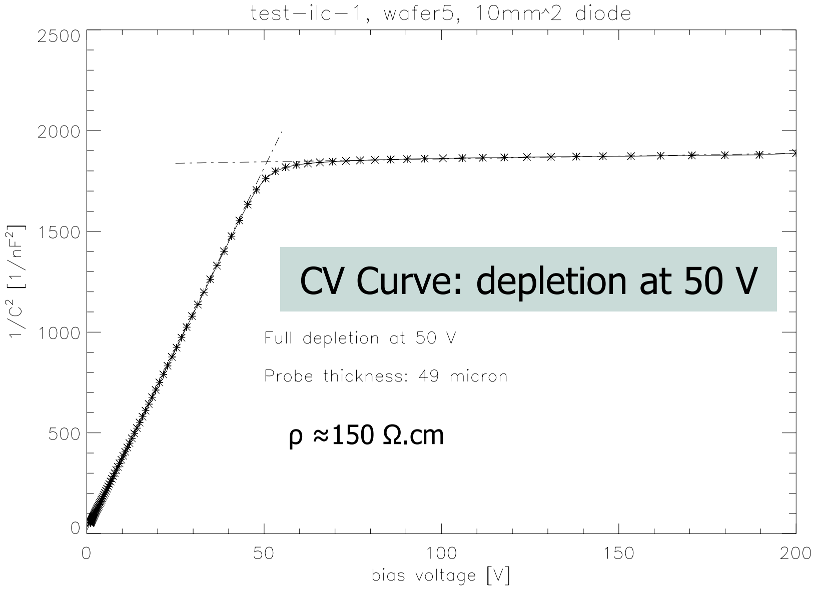
1: process test structures on SOI wafers

2: mechanical samples

PiN Diodes with Different Support Sides



PiN Diodes on thin Silicon

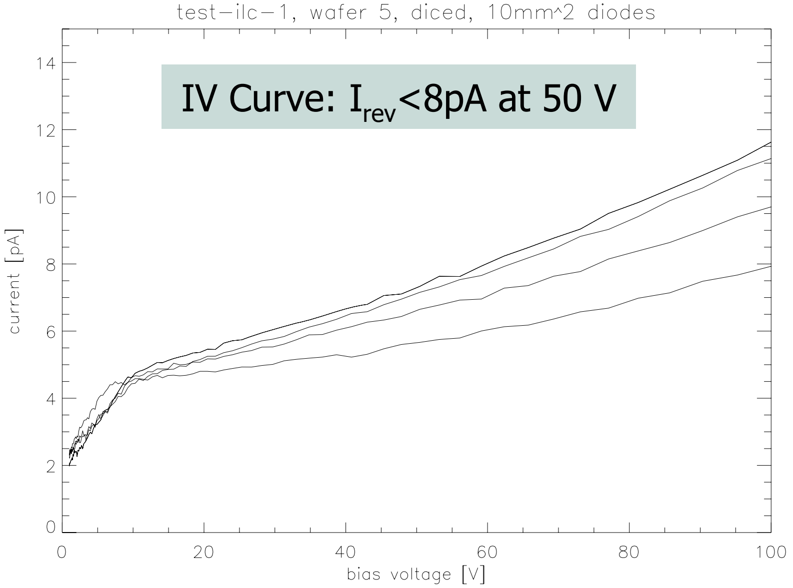


CV Curve: depletion at 50 V

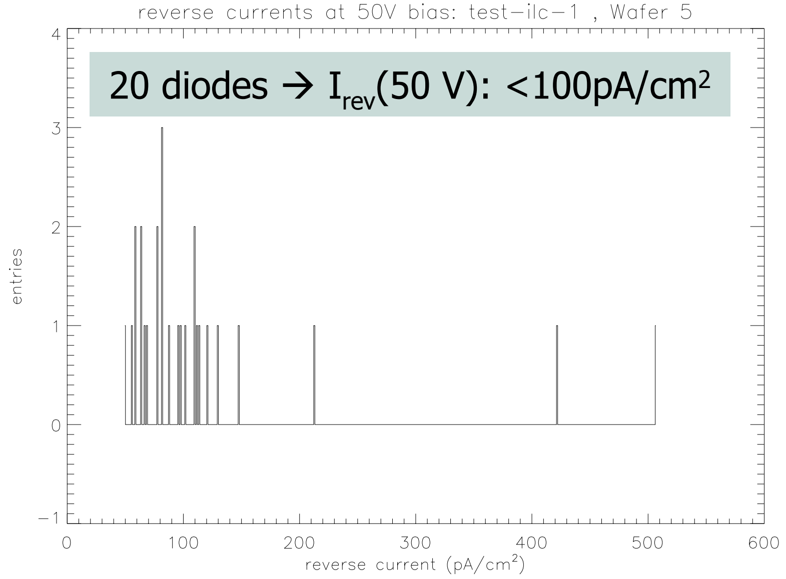
ρ ≈150 Ω.cm

Thin diodes have **excellent** leakage currents.

Processing of the SOI wafers and removal of handle wafer
does not degrade devices!



IV Curve: I_{rev}<8pA at 50 V

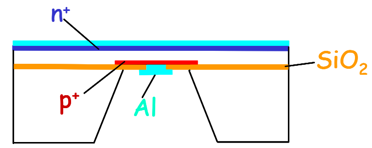


20 diodes → I_{rev}(50 V): <100pA/cm^2

The 3rd round - SOI Wafers in preparation…

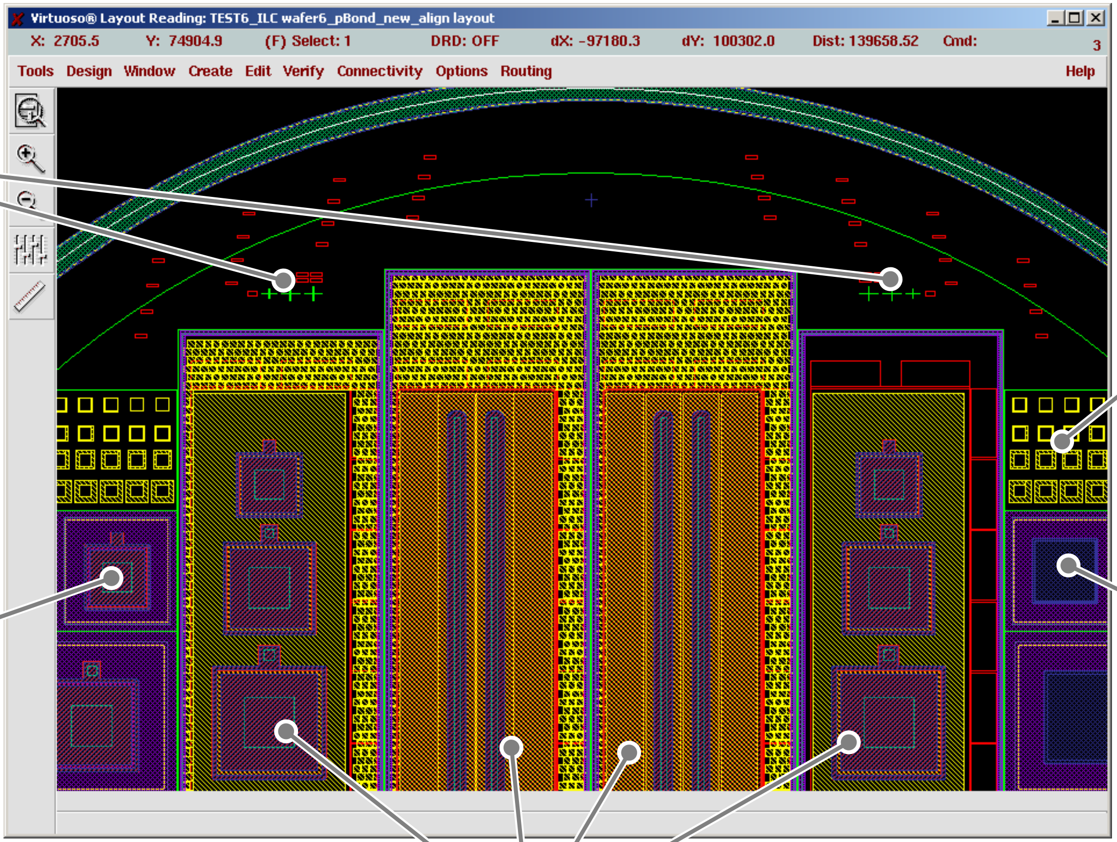
Alignment marks in BOX to find the partial p-implant after bonding

Implants like DEPFET config.



unstructured n+ on top
structured p+ in bond region

Diodes with various areas



Virtuoso® Layout Reading: TEST6_ILC wafer6_pBond_new_align layout

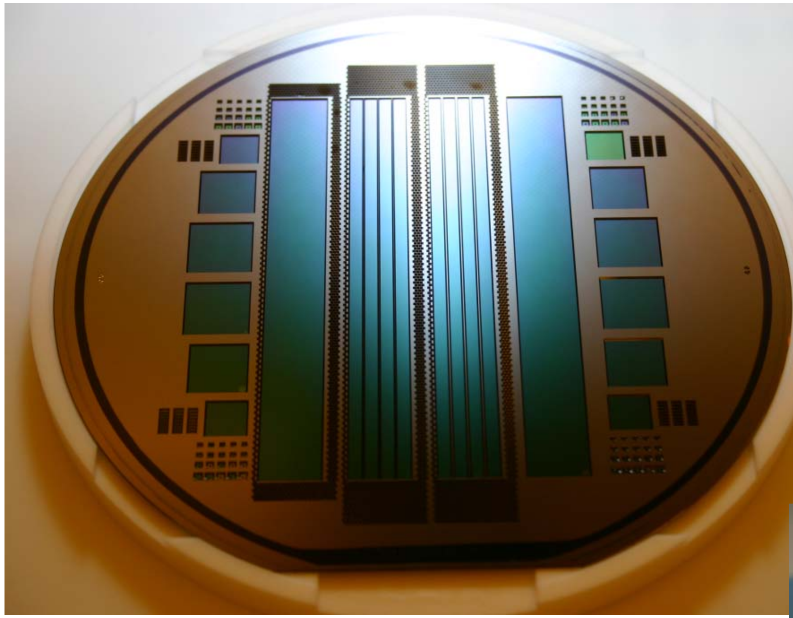
X: 2705.5 Y: 74904.9 (F) Select: 1 DRD: OFF dX: -97180.3 dY: 100302.0 Dist: 139658.52 Cmd: 3

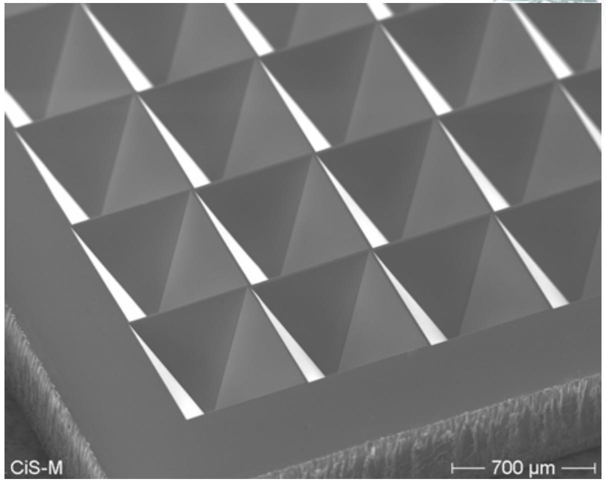
Some test structures

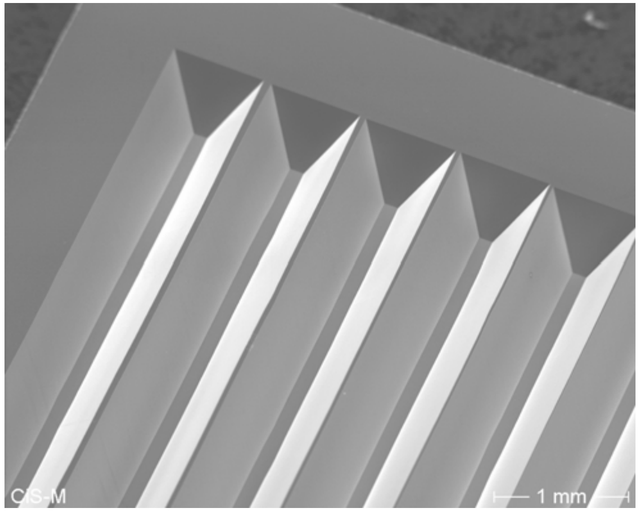
MOS-C with various areas

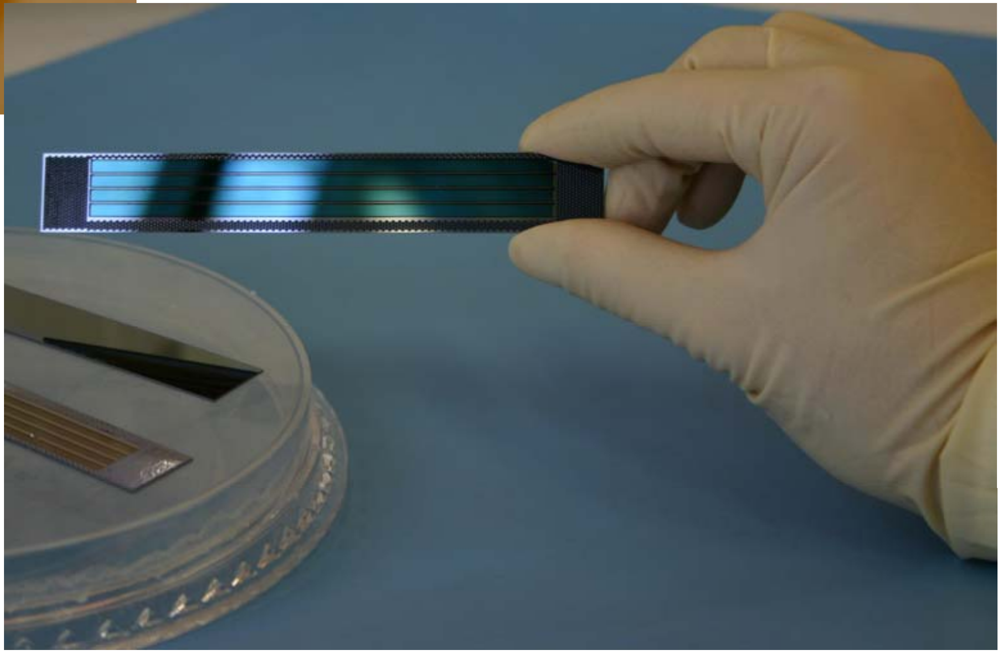
4 "full size" 1st layer ladders 100x13 mm², 1 and 3 mm frame along the long side

Thinning : mechanical samples

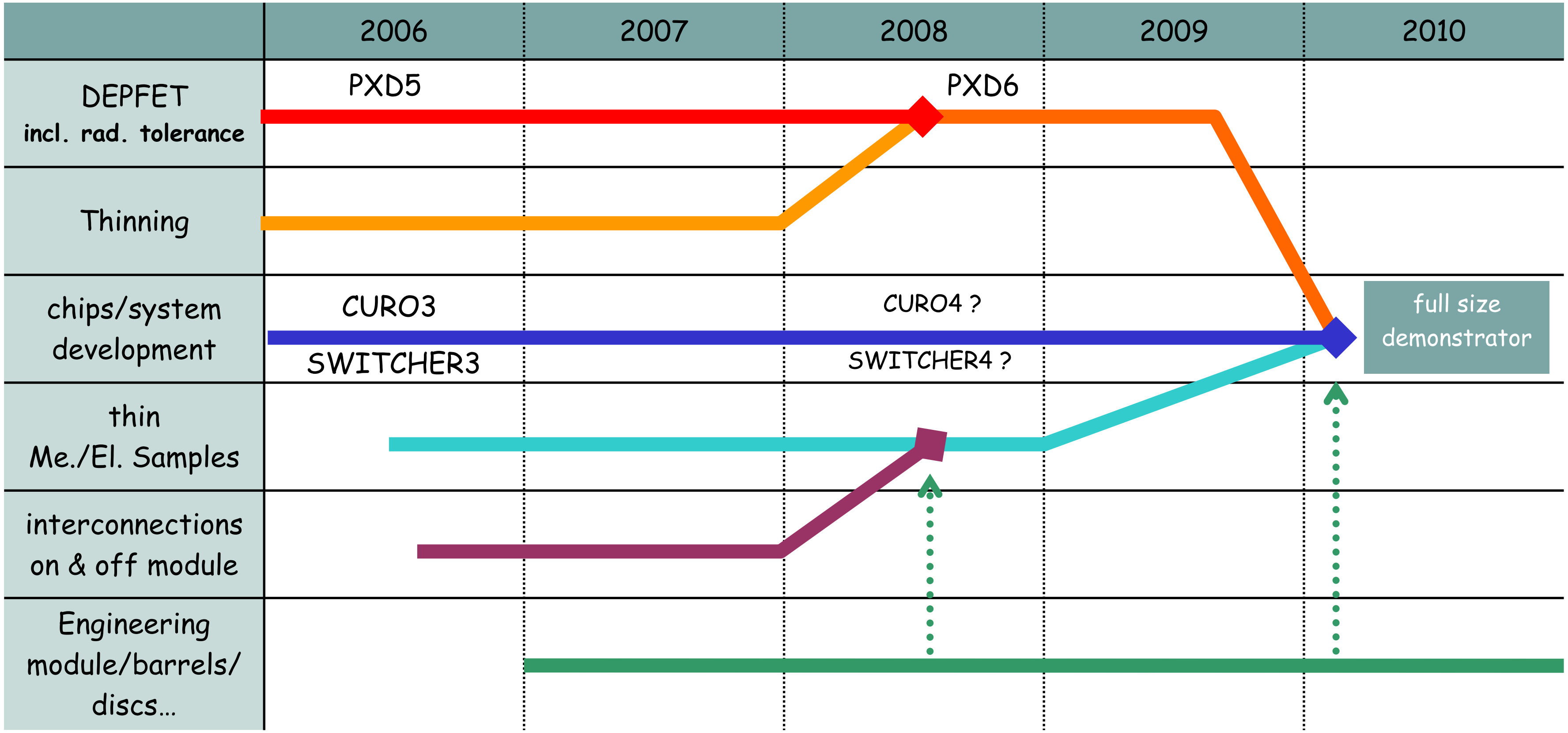








~~Roadmap~~ Subway map towards a thin demonstrator



2006 2007 2008 2009 2010

DEPFET incl. rad. tolerance: PXD5, PXD6

Thinning

chips/system development: CURO3, SWITCHER3, CURO4 ?, SWITCHER4 ?

thin Me./El. Samples

interconnections on & off module

Engineering module/barrels/ discs...

full size demonstrator

Summary

- ✓ Matrices operated ‘routinely’ in test beams at DESY and CERN including a 5 layer DEPFET **telescope.**
- ✓ New **Switcher** submitted (rad. hard, ready for bump bonding, fast: 9V in 10ns @ 20pF).
- ✓ New sensor production with ‘**full size devices**’ has started. Expect it back middle 2007.
- ✓ **Thinning** technology migrated to main HLL lab with excellent results using commercial vendors. Full ILC size diode structures are under way.

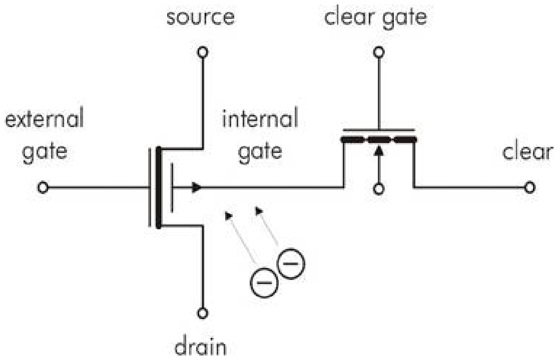
Unfortunately I had to skip the entire **work related to simulations**. The LDC VTX detector using "all-silicon" DEPFET ladders is now implemented in MOKKA and the results are extremely nice.

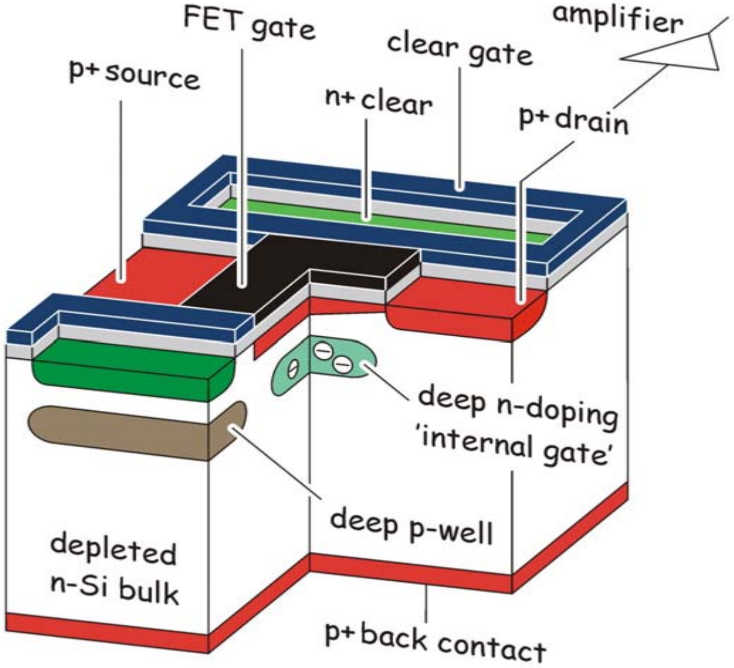
Also not mentioned is the **proton irradiation at LBNL**, which **confirmed the radiation tolerance** of the DEPFETs up to 1e12 p/cm^2 and 300 krad. These single pixel structures are now in Munich waiting for evaluation of their spectroscopic performance after irradiation.

The DEPFET is well under way towards a full size thin demonstrator by 2010!

DEPFET Principle of Operation

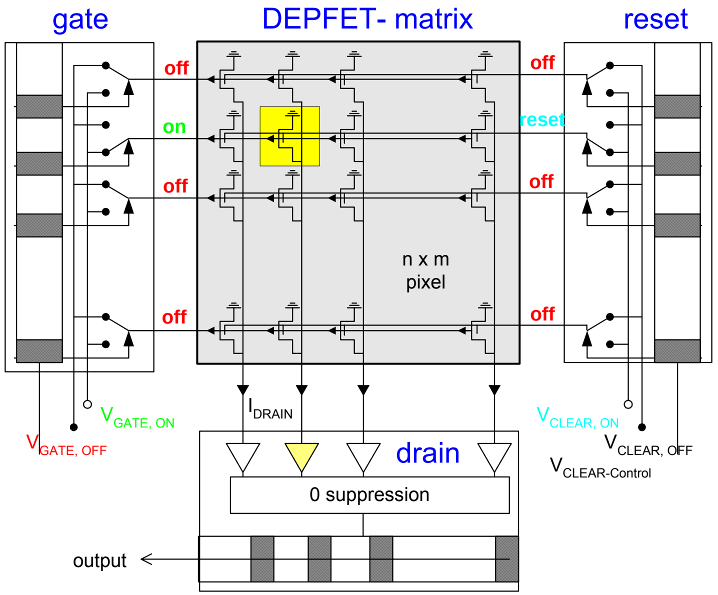
- A p-FET transistor is integrated in each pixel
- A potential minimum for electrons is created under the channel by sideward depletion
- Electrons are collected in the "internal gate" and modulate the transistor current
- Signal charge is removed via a clear contact



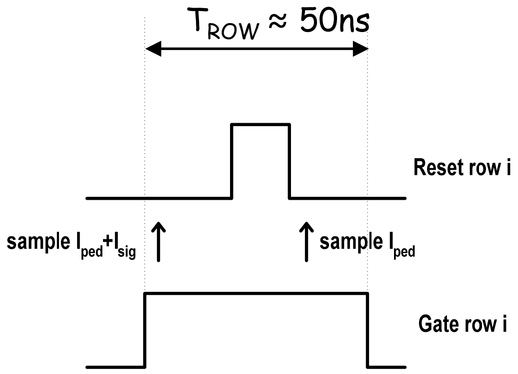


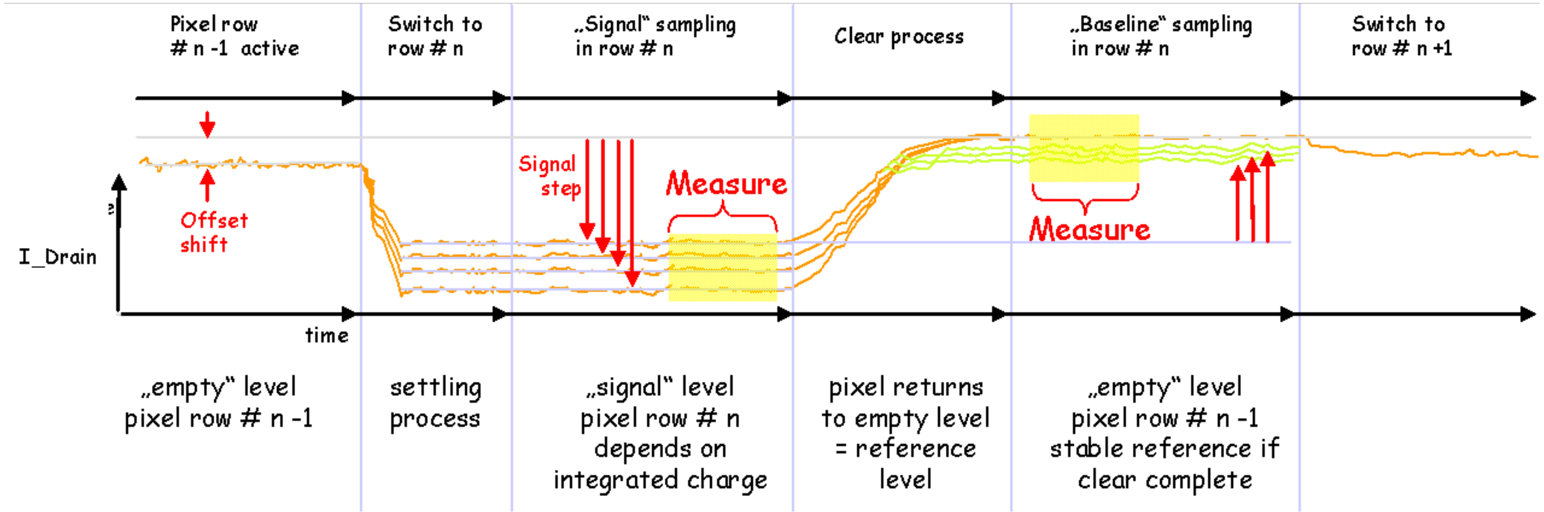
- Fast signal collection in fully depleted bulk
- Low noise due to small capacitance and internal amplification
- Transistor can be switched off by external gate – charge collection is then still active!

Matrix operation

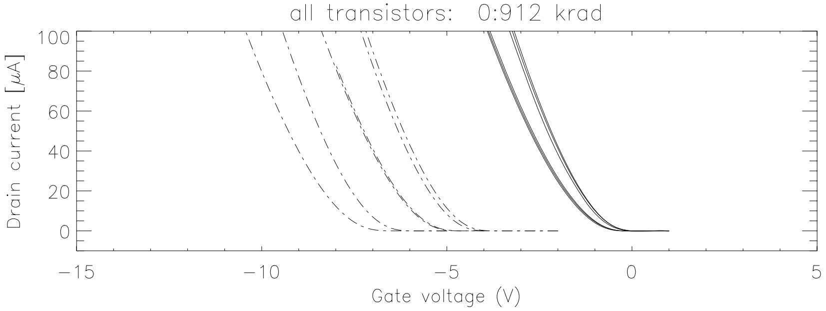


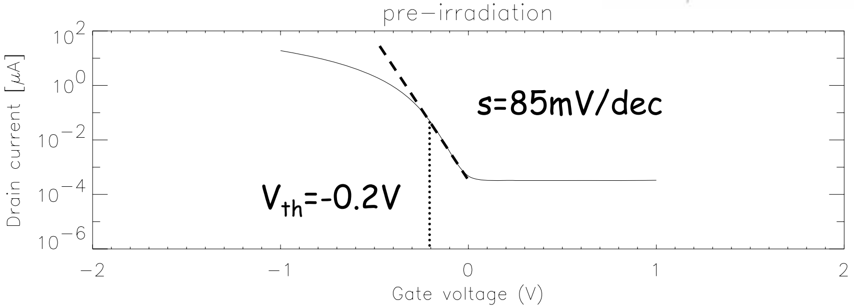
Row wise read out and
row wise CDS!
→ read 20 times/train

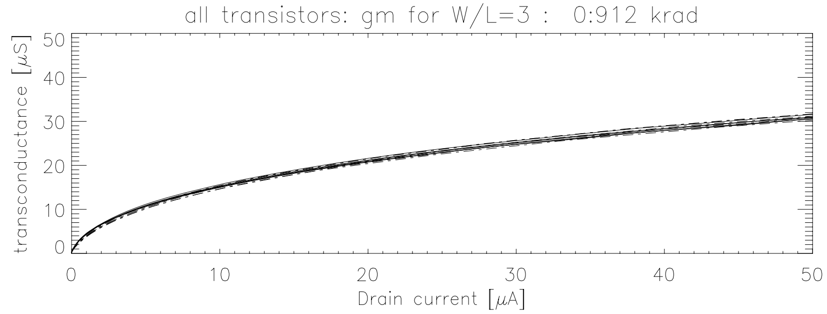


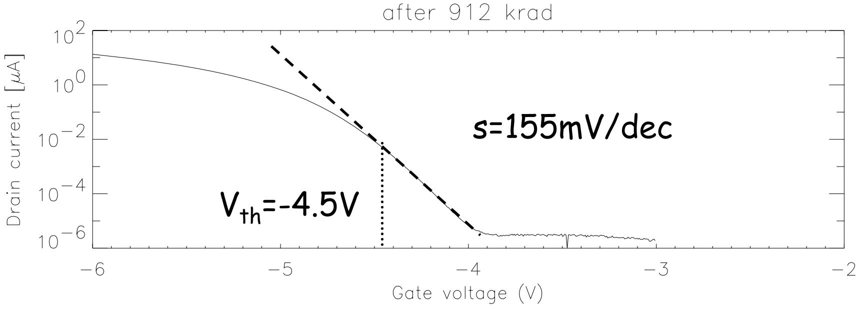


Transconductance and subtreshold slope









↓

No change of the transconductance g_m

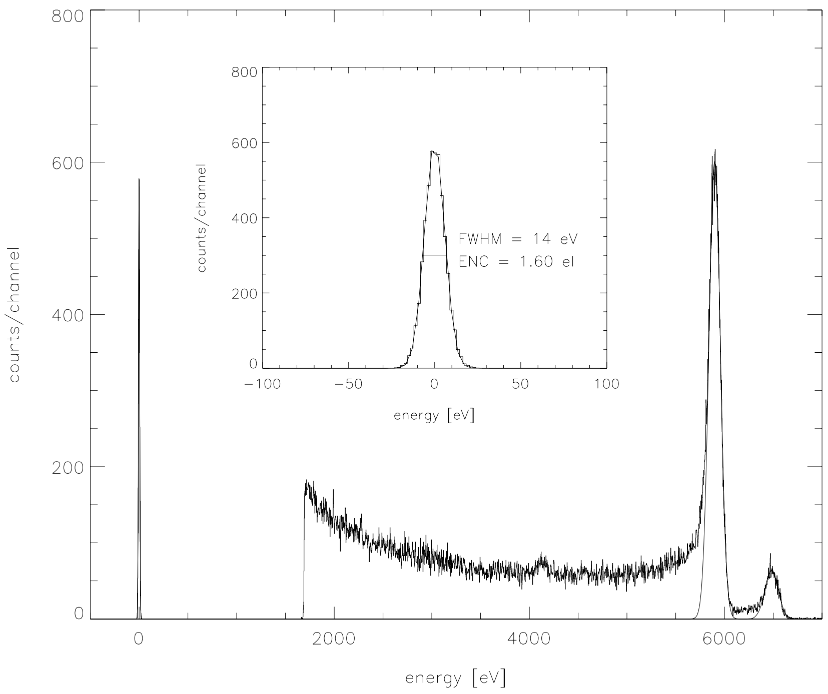
$$N_{it} = {C_{ox}}/{kT} \cdot \ln(10) \cdot (s_{D2} - s_{D1})$$

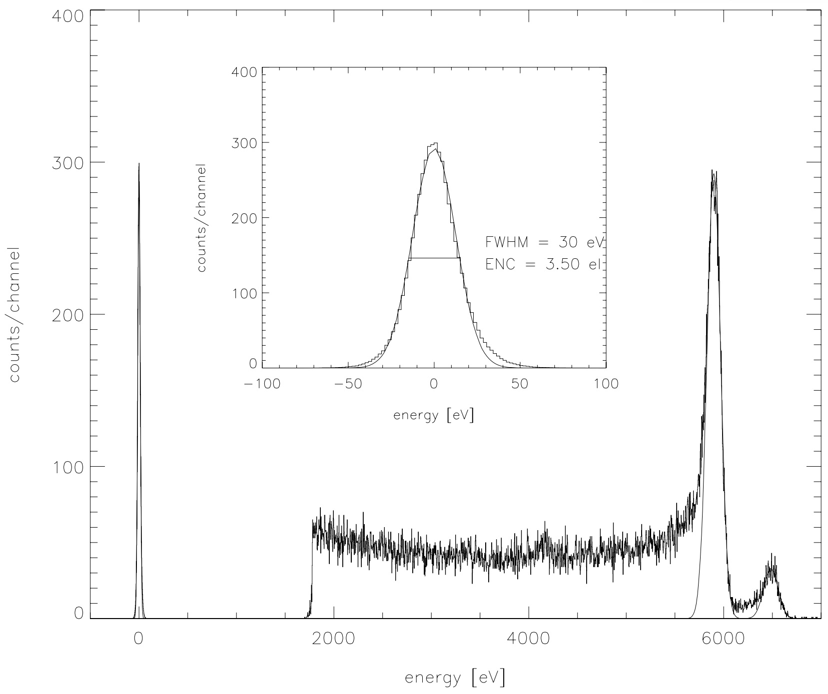
↓

300 krad → $N_{it} \approx 2 \cdot 10^{11}$ cm^{-2}
912 krad → $N_{it} \approx 7 \cdot 10^{11}$ cm^{-2}

Literature:
After 1Mrad 200 nm (SiO_2):
$N_{it} \approx 10^{13}$ cm^{-2}

^{55}Fe Spectrum (single pixel)





non-irradiated

$V_{thresh} \approx -0.2V$, $V_{gate}=-2V$

$I_{drain}=41\ \mu A$

time cont. shaping τ=10 µs

Noise ENC=1.6 e^- (rms)

at T>23 degC

912 krad ^{60}Co

$V_{thresh} \approx -4.0V$, $V_{gate}=-6.0V$

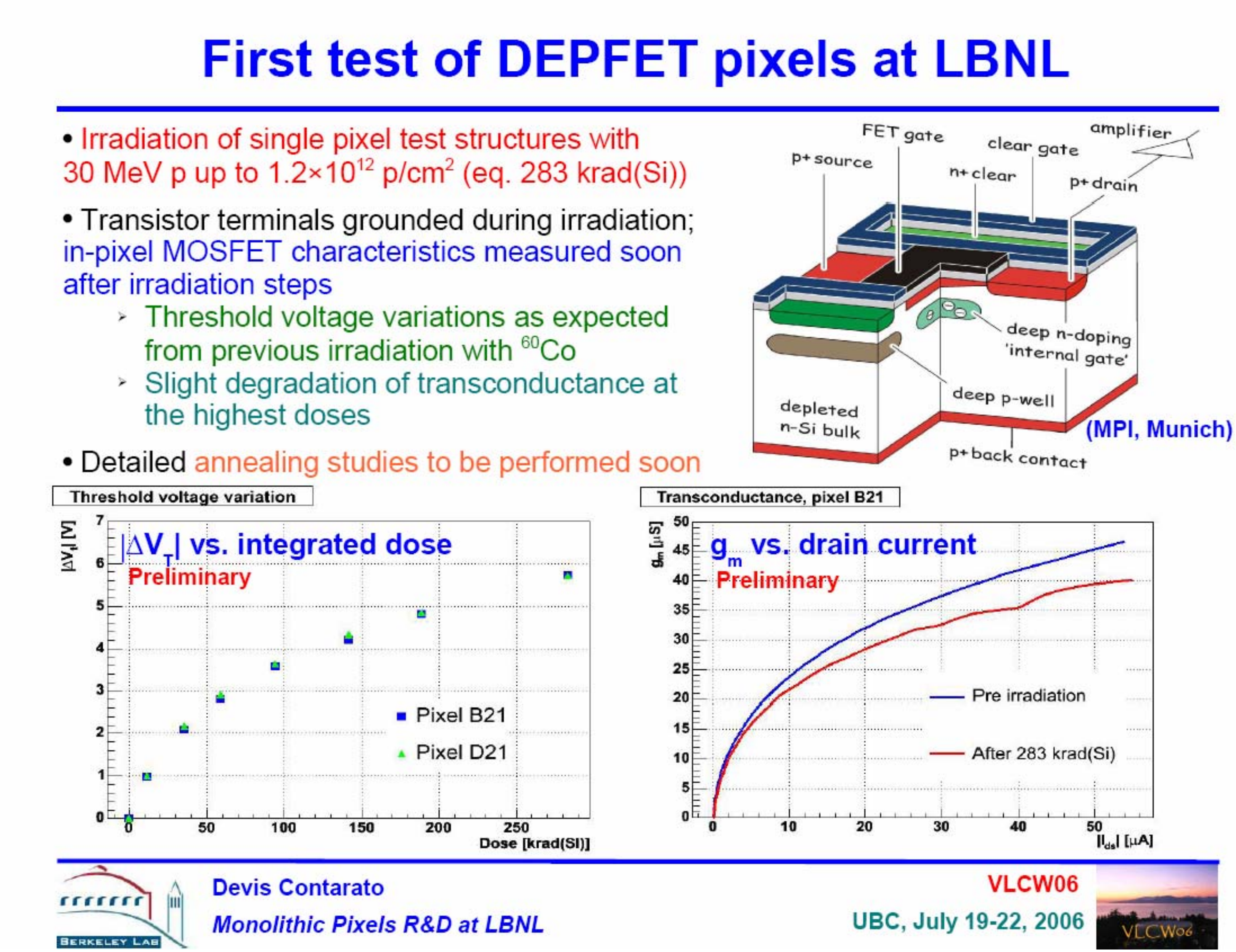
$I_{drain}=40\ \mu A$

time cont. shaping τ=10 µs

Noise ENC=3.5 e^- (rms)

at T>23 degC

Irradiations at LBNL - 88 inch Cyclotron, July 2006



First test of DEPFET pixels at LBNL

- Irradiation of single pixel test structures with 30 MeV p up to 1.2×10^{12} p/cm^2 (eq. 283 krad(Si))
- Transistor terminals grounded during irradiation; in-pixel MOSFET characteristics measured soon after irradiation steps
  - Threshold voltage variations as expected from previous irradiation with ^{60}Co
  - Slight degradation of transconductance at the highest doses
- Detailed annealing studies to be performed soon

(MPI, Munich)

Threshold voltage variation

Transconductance, pixel B21

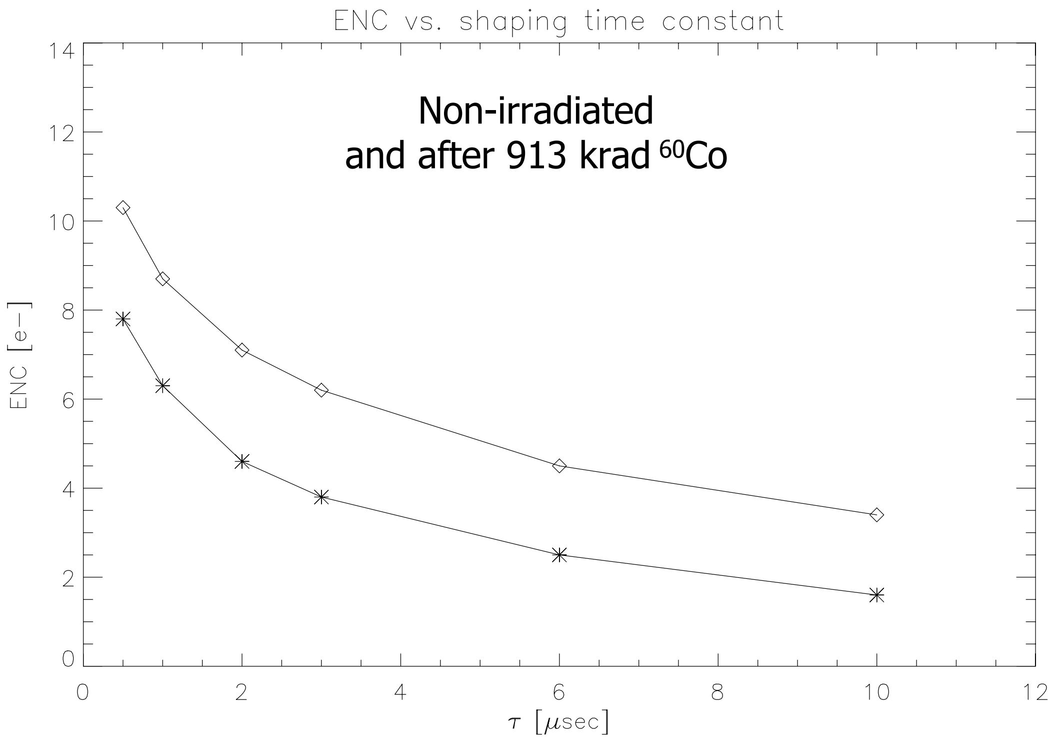
Devis Contarato

Monolithic Pixels R&D at LBNL

VLCW06

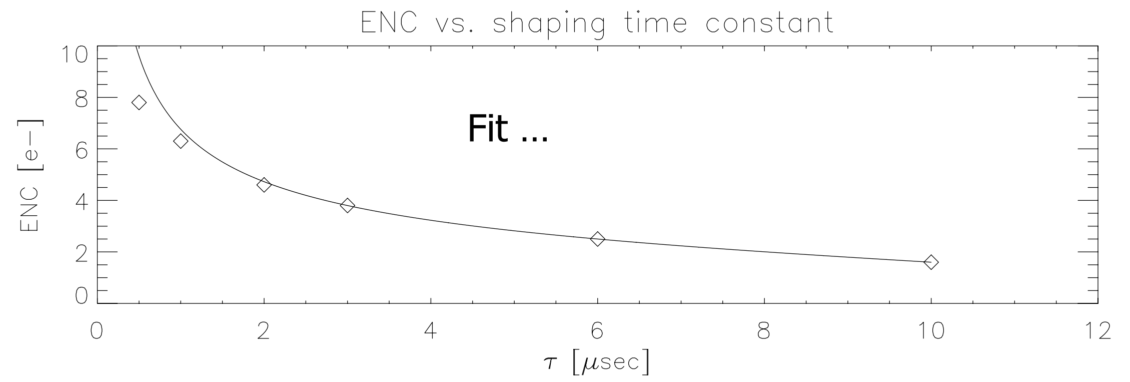
UBC, July 19-22, 2006

Noise vs. shaping time τ

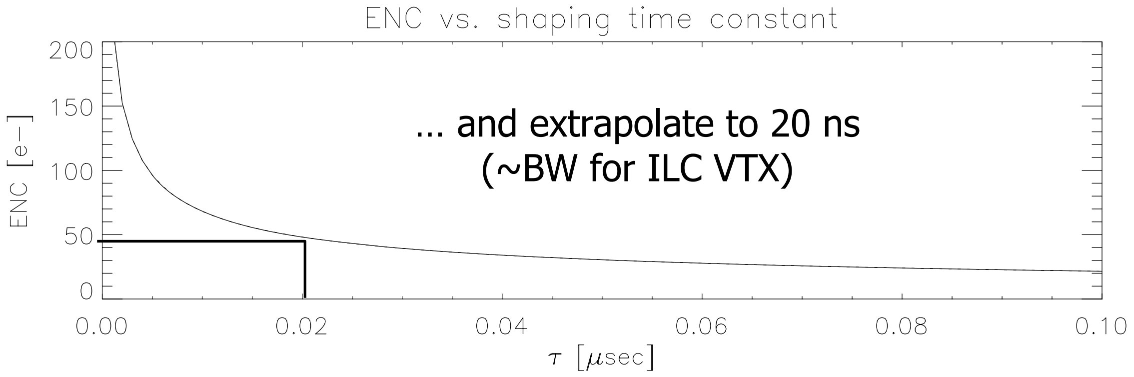


$$ENC = \sqrt{\underbrace{\alpha \frac{2kT}{g_m} C_{tot}^2 A_1 \frac{1}{\tau}}_{\text{Therm. noise}} + \underbrace{2\pi a_f C_{tot}^2 A_2}_{1/f} + \underbrace{q I_L A_3 \tau}_{I_L}}$$

Noise vs. shaping time τ



Fit …

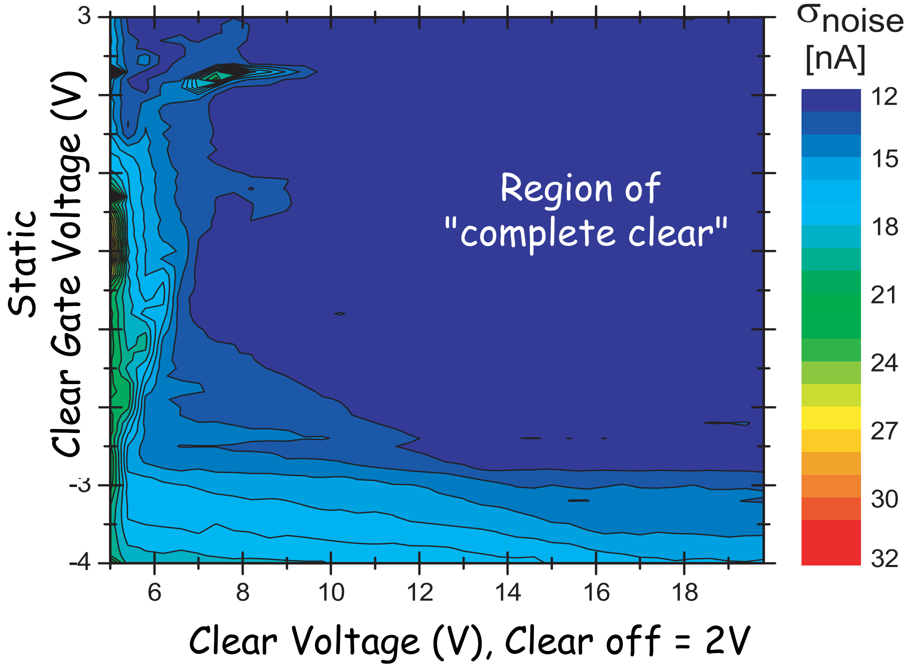


… and extrapolate to 20 ns
(~BW for ILC VTX)

$$ENC = \sqrt{\underbrace{\alpha \frac{2kT}{g_m} C_{tot}^2 A_1 \frac{1}{\tau}}_{\text{Therm. noise}} + \underbrace{2\pi a_f C_{tot}^2 A_2}_{1/f} + \underbrace{q I_L A_3 \tau}_{I_L}}$$

Clear Efficiency

- Study mini matrix devices in laser setup
- Scan wide parameter space of Clear Gate and Clear Voltage
- Study various designs, geometries (length of clear gate) and operating conditions (static or clocked clear gate)

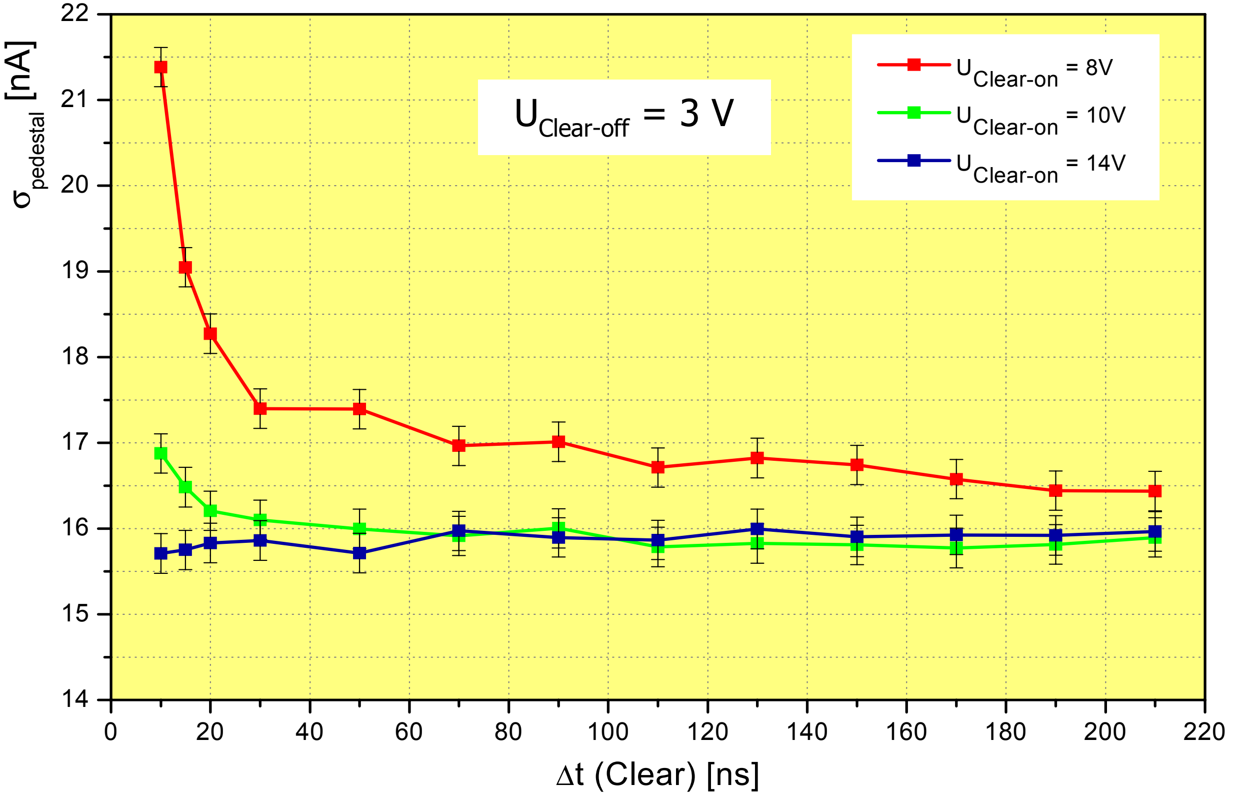


Complete clear achieved with static clear gate !
Required voltages are small (5-7V) – very important for future SWITCHER!

Fast Clearing

o Study clear efficiency for short clear pulses

Device with common clear gate



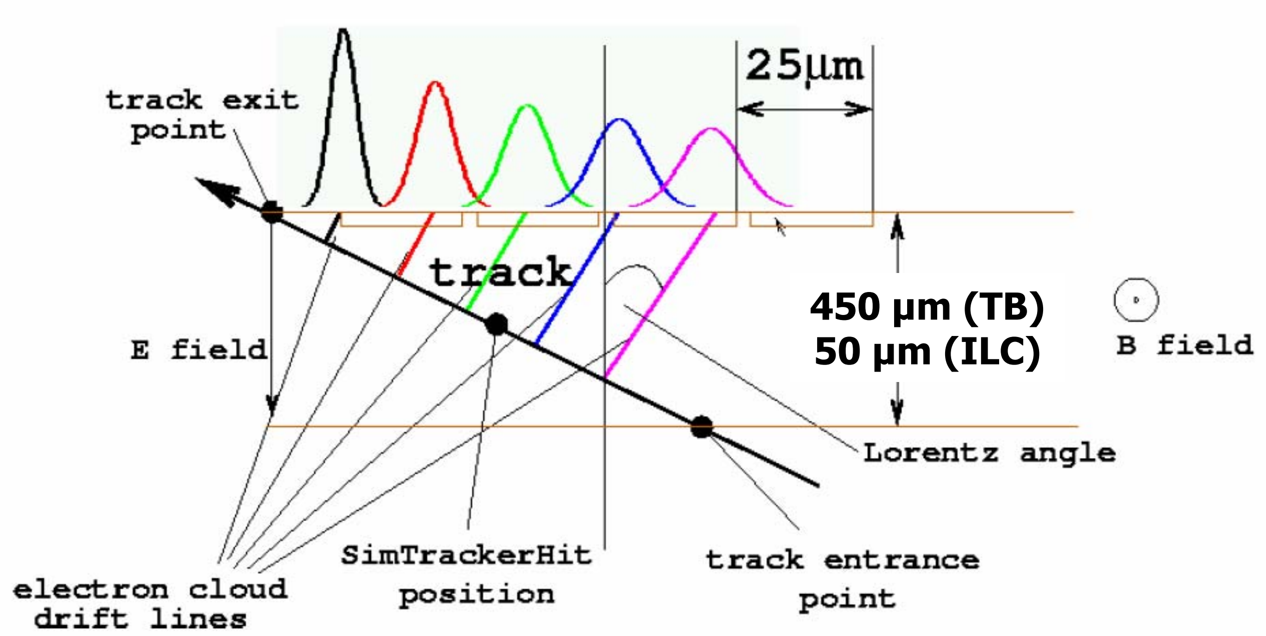
Complete clear in only 10-20 ns @ ΔV_{clear} = 11-7 V

Simulation: Parameters

DEPFET ladders (and TB modules) implemented in MOKKA

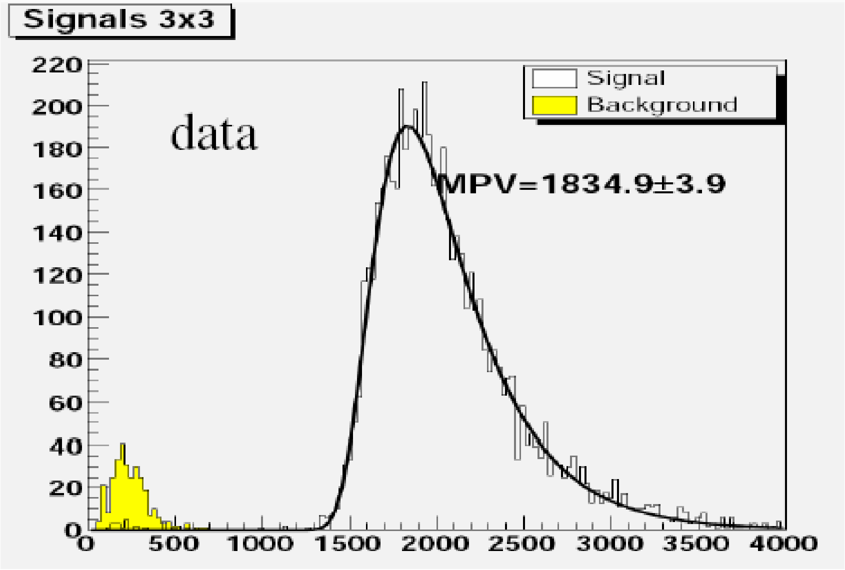
including:

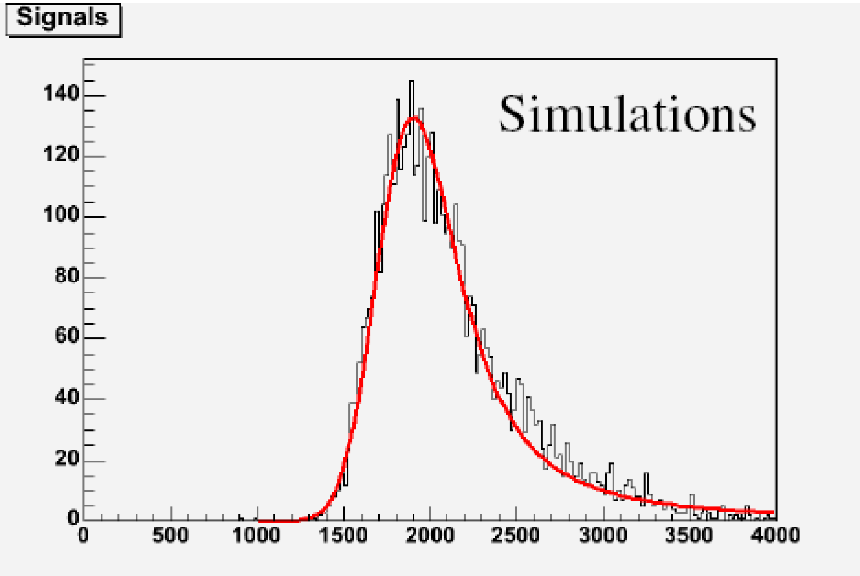
- E_{loss} fluctuations in thin layers
- Charge transport, sharing & diffusion
- Lorentz angle (33° @ 4T)
- Electronic noise 100 e- (goal for ILC), resp. 230e- (test beam)



Compare test beam results <-> Simulation

Here results with 450µm thick detector and 230e- noise:
normal incidence



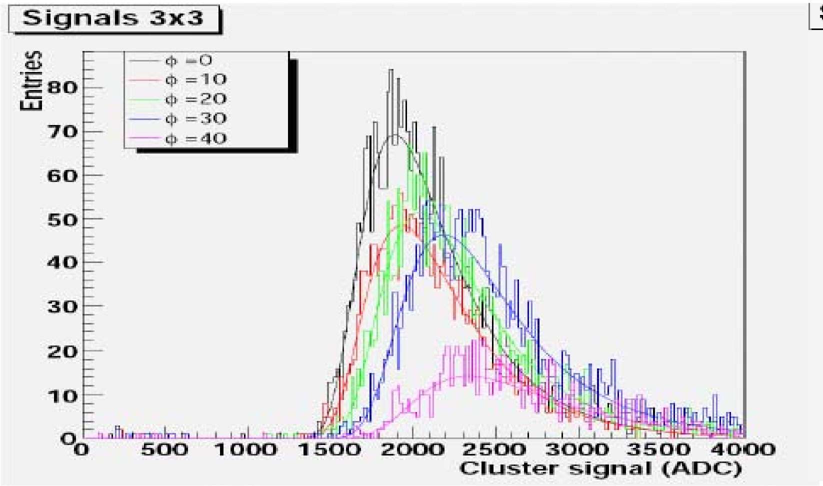


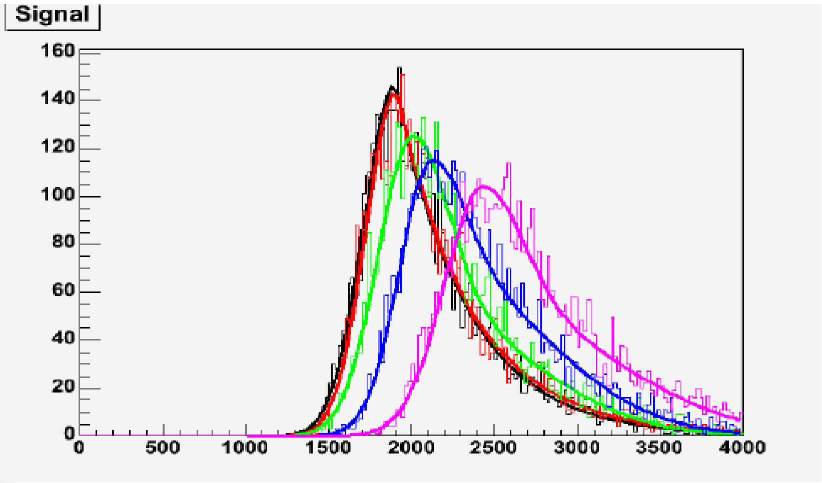
(Alexei Raspereza)

Data collected at normal track incidence is used to derive coefficient converting E_{Loss} into ADC counts

Compare test beam results <-> Simulation

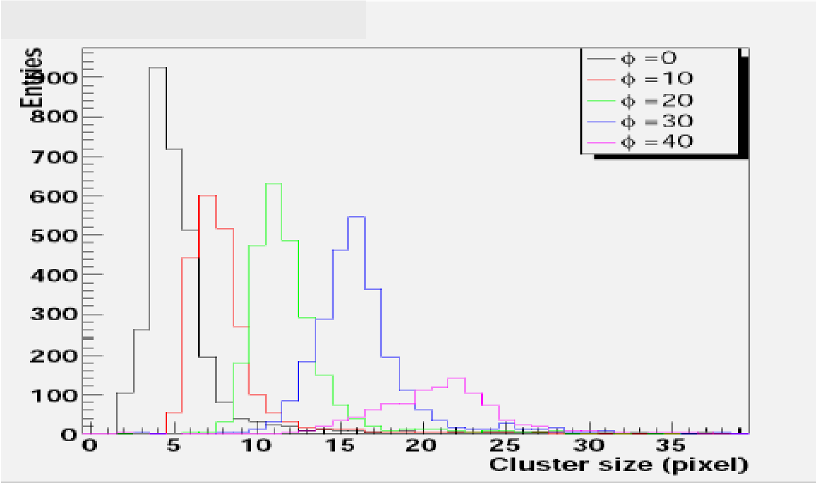
inclined tracks

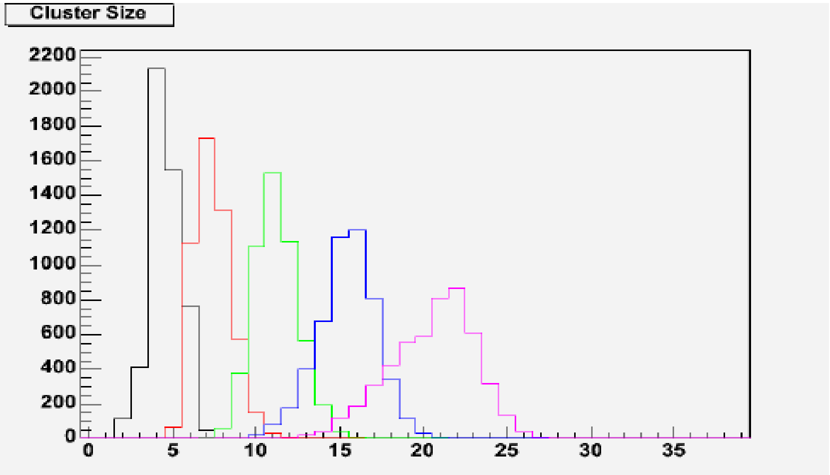




Data

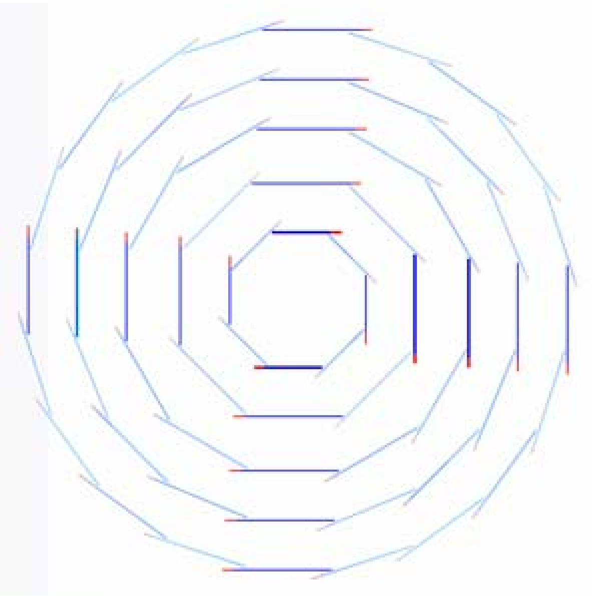
Simulation





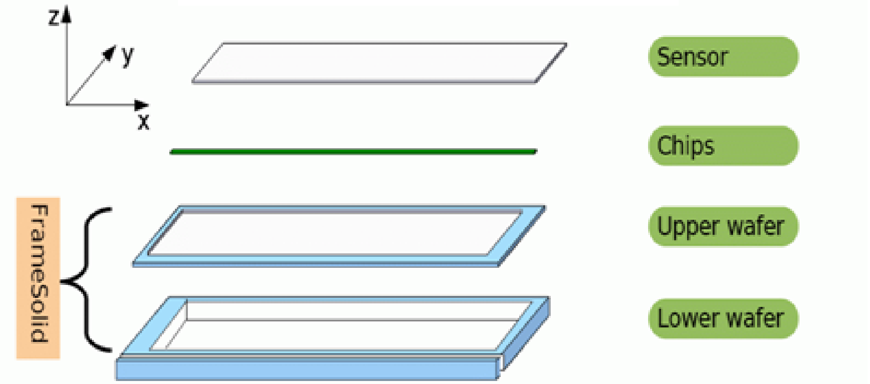
(Alexei Raspereza)

Simulation: LDC Geometry description

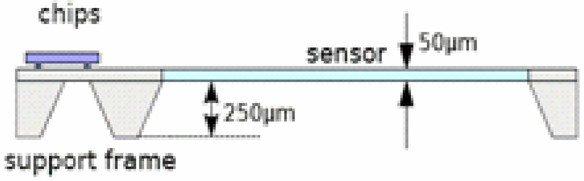


Sensitive layer thickness = 50 µm
Pixel size = 25×25 µm^2

	Radius (cm)	Ladders	Length (cm)
1	1.5	8	10.0
2	2.6	8	2 × 12.5
3	3.8	12	2 × 12.5
4	4.9	16	2 × 12.5
5	6.0	20	2 × 12.5

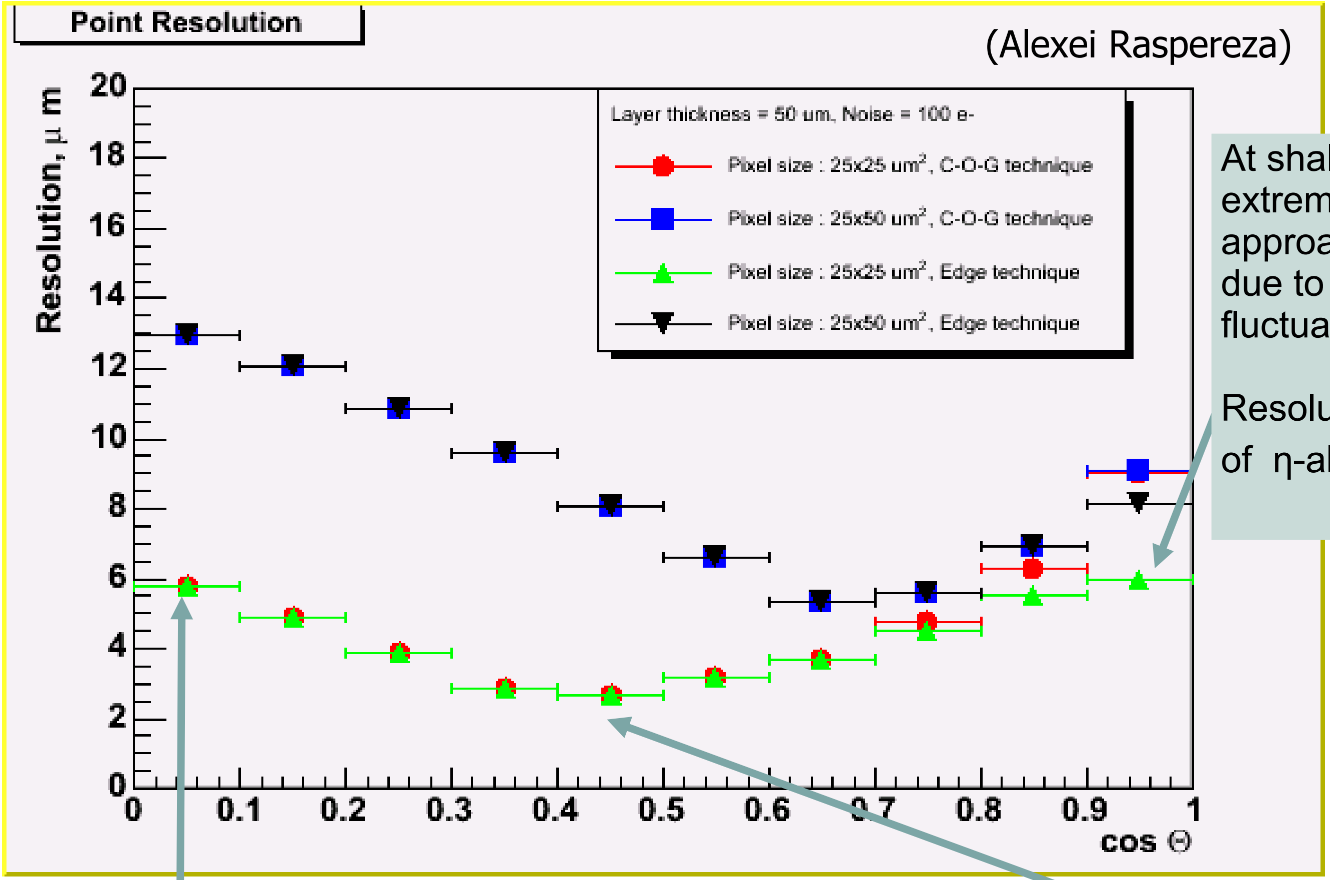


→ LDC laddders with support frames



Material up to first layer : beam pipe (500 µm beryllium)

Simulation: single point resolution



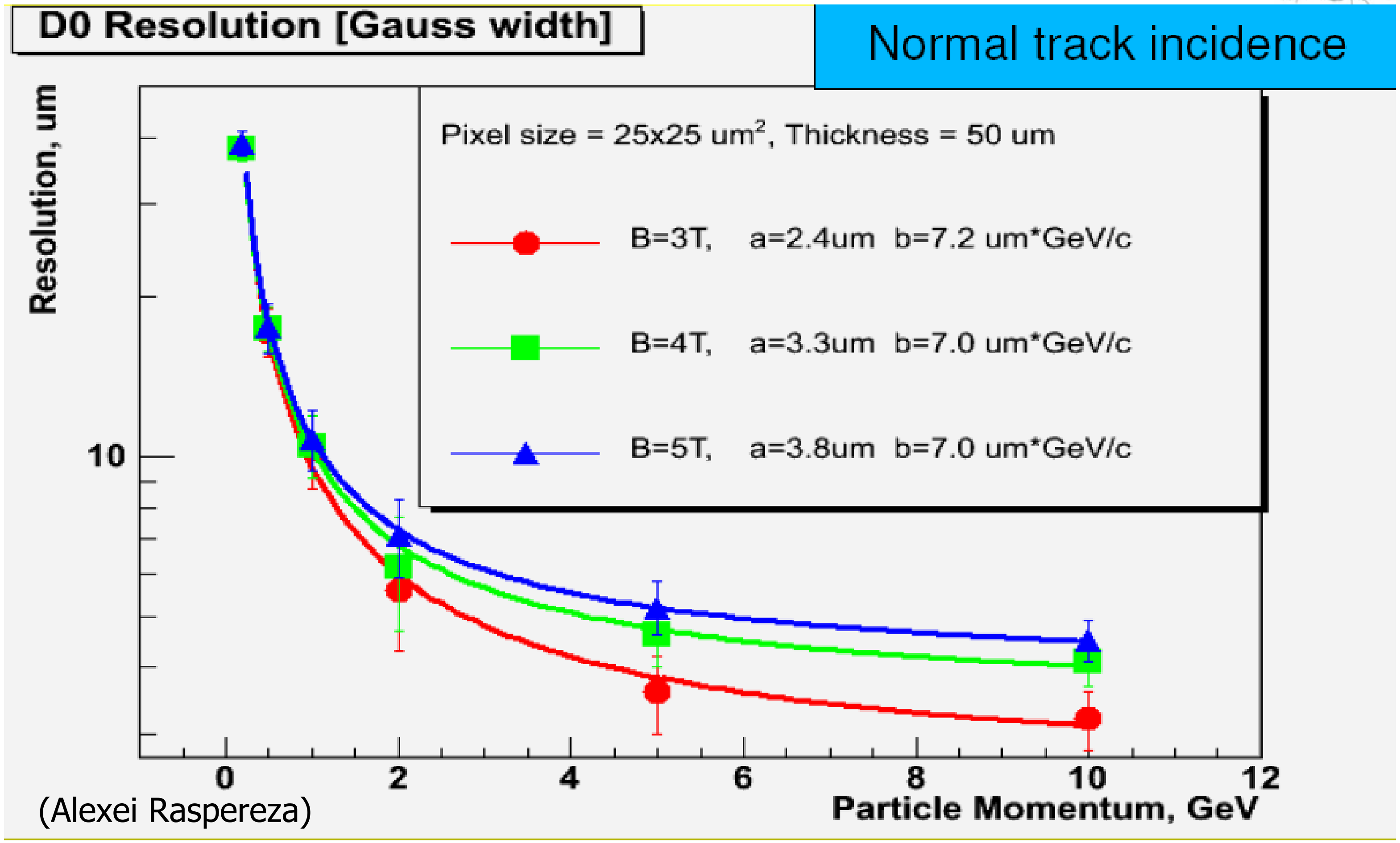
At shallow angles cluster size gets extremely large and simple COG approach yields poor resolution due to inter-pixel charge fluctuations.

Resolution is improved by means of η-algorithm (edge-technique)

In many cases at normal incidence only one row is fired : resolution is limited by pixel size

When track is inclined more than one row is fired -> resolution gets better

Simulation: IP resolution



Normal track incidence

(Alexei Raspereza)

$$\sigma = \sqrt{a^2 + \left(\frac{b}{p\sin^{\frac{3}{2}}\theta}\right)^2}$$

$a < 5\,\mu m$ (point precision)

$b < 10\,\mu m$ (multiple scattering)

→ IP resolution is OK!