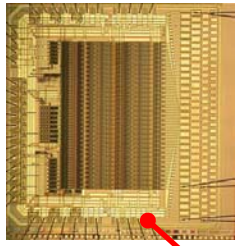
DEPFET Active Pixel Sensors for the ILC

Ladislav Andricek

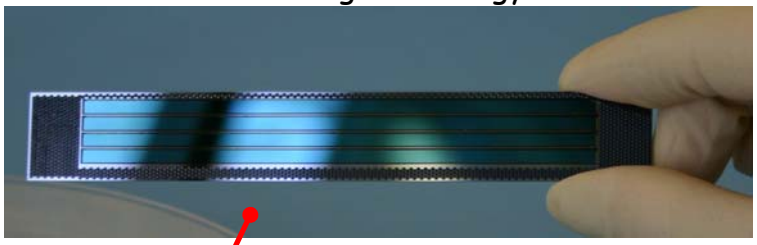
for the DEPFET Collaboration
(www.depfet.org)

The DEPFET ILC VTX Project

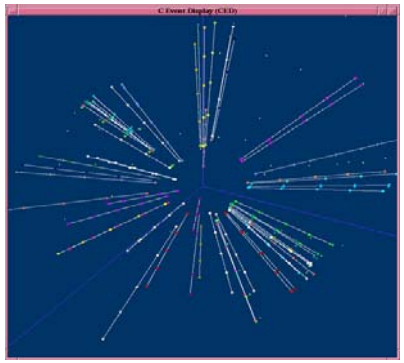
✓ steering chips Switcher



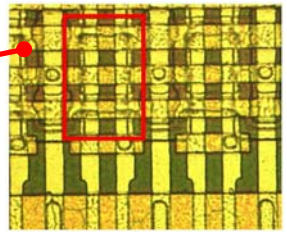
✓ thinning technology



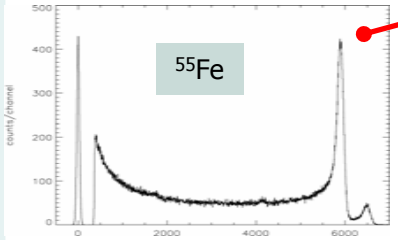
✓ Simulation



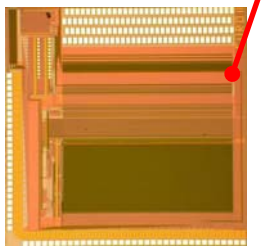
✓ sensor development



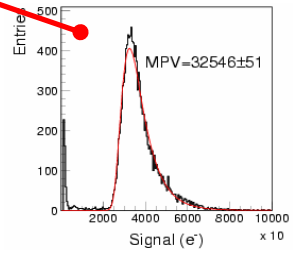
✓ tolerance against ion. radition



✓ r/o chips Curo

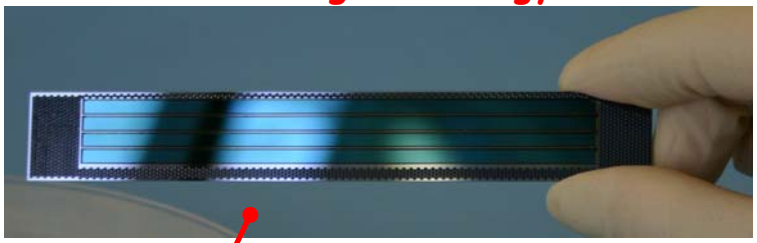


✓ beam test

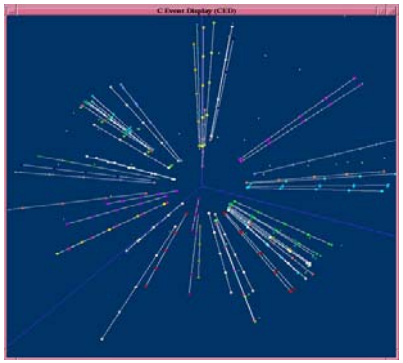


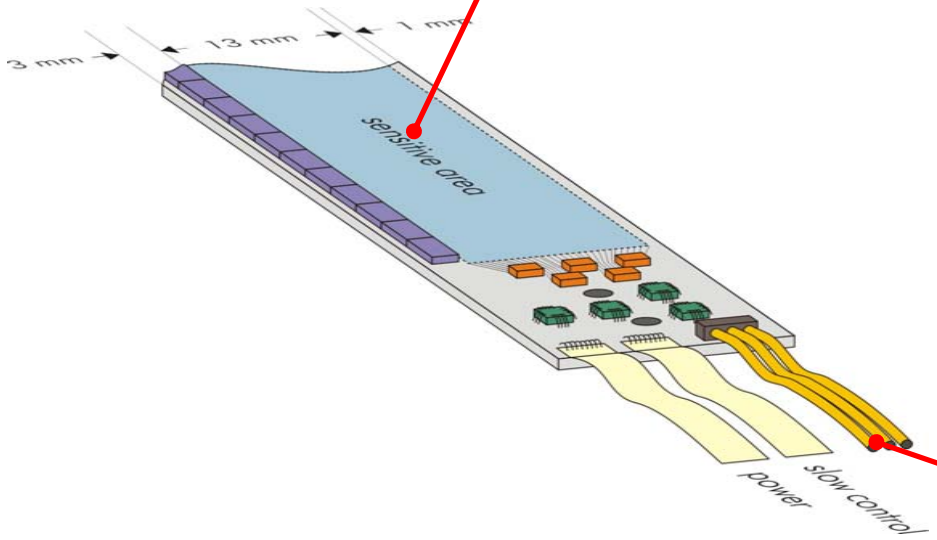
The DEPFET ILC VTX Project

✓ thinning technology

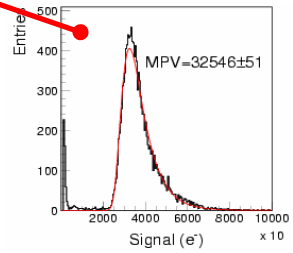


✓Simulation



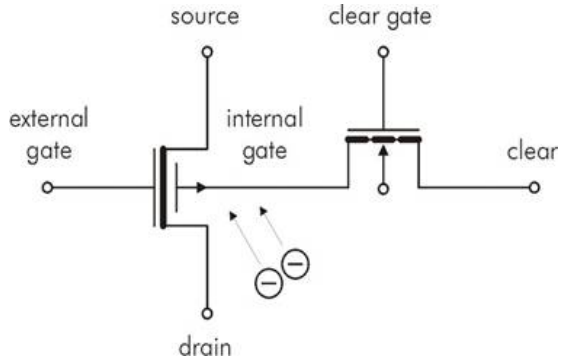


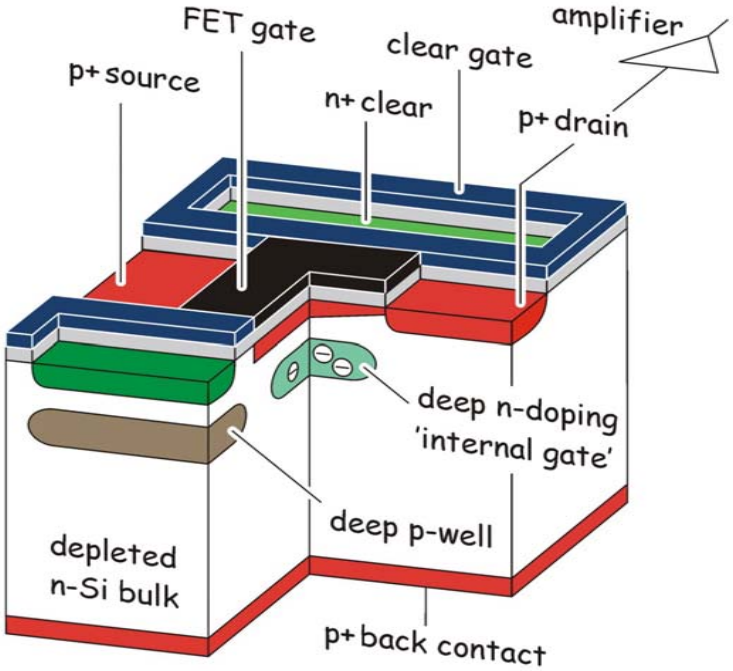
✓beam test



DEPFET Principle of Operation

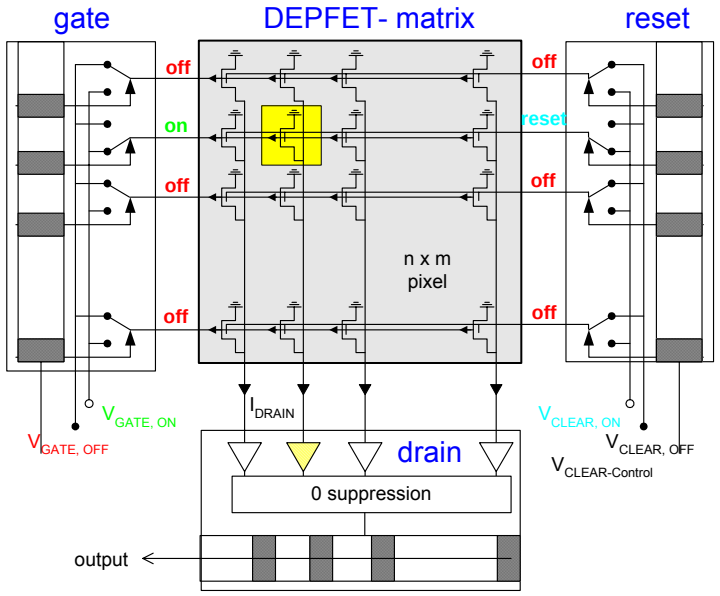
- A p-FET transistor is integrated in each pixel
- A potential minimum for electrons is created under the channel by sideward depletion
- Electrons are collected in the "internal gate" and modulate the transistor current
- Signal charge is removed via a clear contact



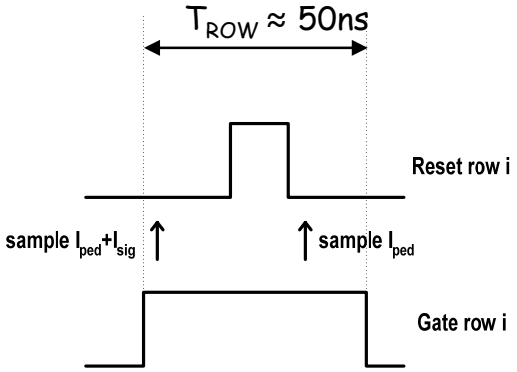


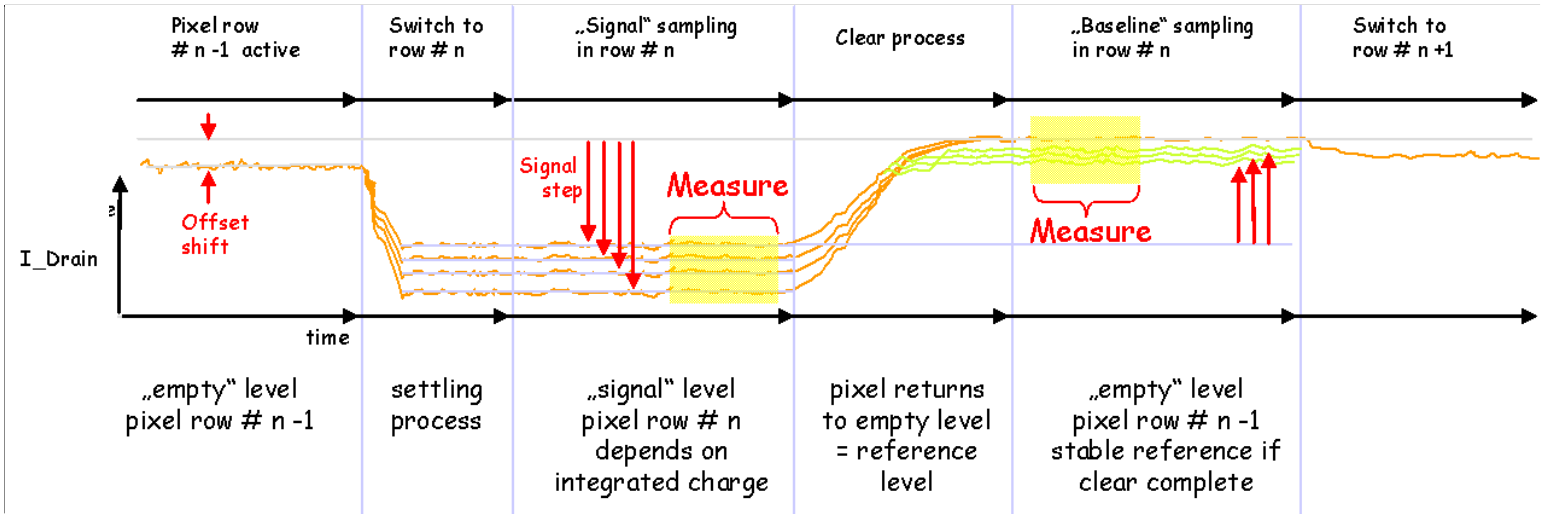
- Fast signal collection in fully depleted bulk
- Low noise due to small capacitance and internal amplification
- Transistor can be switched off by external gate – charge collection is then still active!

Matrix operation

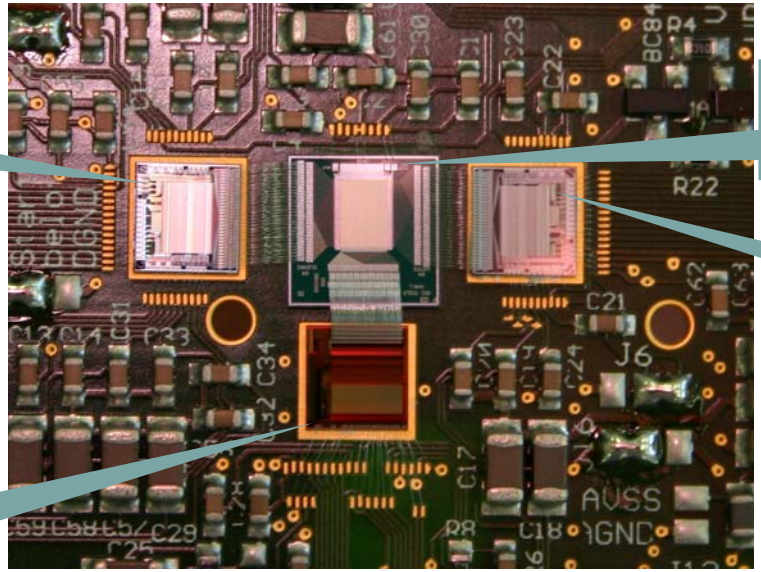


Row wise read out and
row wise CDS!
→ read 20 times/train





ILC Prototype System



Gate Switcher

DEPFET Matrix
64x128 pixels, 33 x 23.75µm²

Clear Switcher

- 2 analog MUX outputs with
- 64 channels each
- Can switch up to 25 V
- 0.8µm AMS HV technology

Current Readout CUROII

- current based 128 channel readout chip
- 50 MHz band width in the f/e
- On-chip pedestal subtraction by switched current technique (CDS)
- Real time hit finding and zero suppression
- 0.25µm CMOS technology (radhard design)

radhard version submitted
→ P.Fischer @ Vertex06

- 128 channels
- 0.35µm technology
- 10V swing (stacked transistors)
- 'zero' standby current

Test Beam(s)

:- 4 test beam periods have been done recently

3 x @ DESY (1-6GeV e^-) – spatial resolution limited by multiple scattering to ~6μm for us.

1 x @ CERN (120GeV p) – from 17th -30th August. Analysis in progress... Next run in October!

:- Reference system is the 4 layer Silicon strip telescope (Bonn)
(double sided strip detectors, 50 μm pitch)

:- Sensors are

450μm thick (mip = 27ke)

min. pixel size = **33x23.75μm²**

various DEPFET variations have been studied

:- Speed:

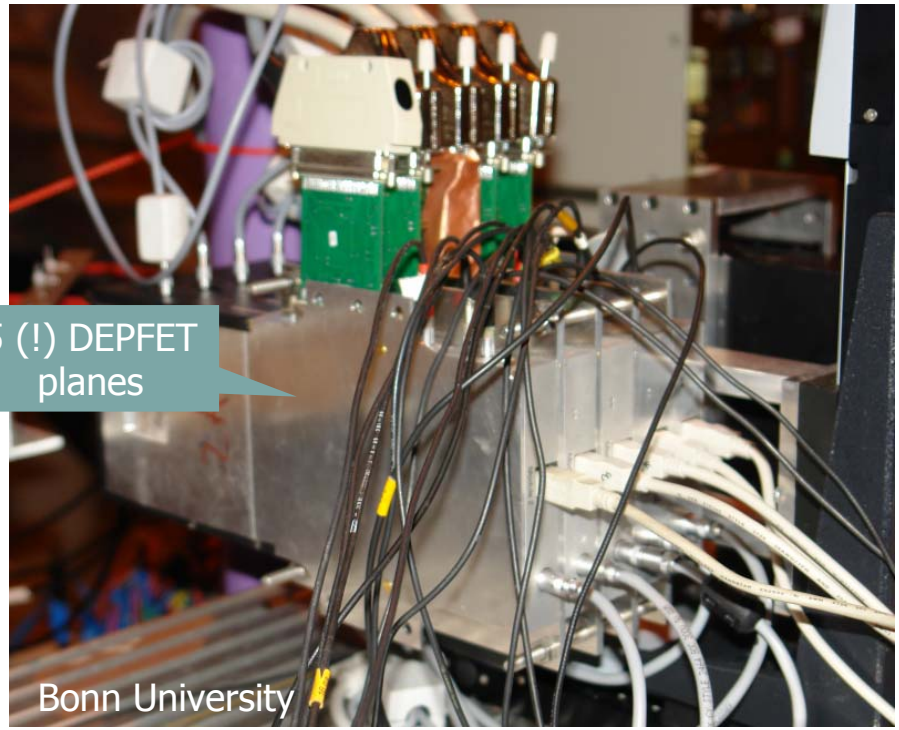
Clearing in 20ns

Sample-clear-sample in CURO: ~ 240 ns (This would give a 4 MHz row rate)

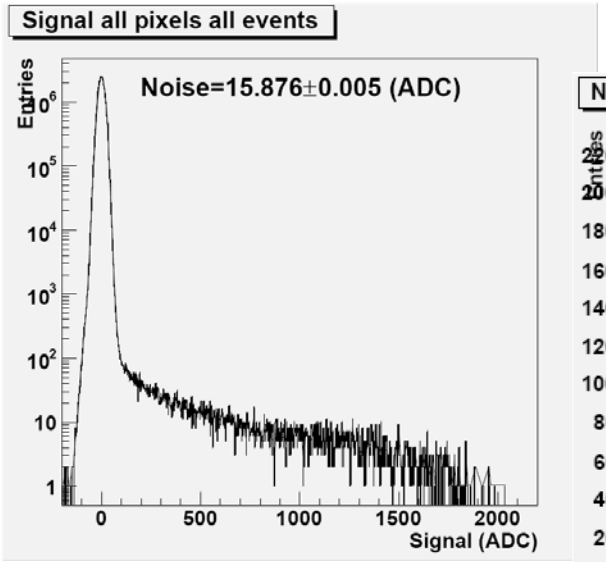
Non-zero suppressed readout (mostly) requires 12μs / row

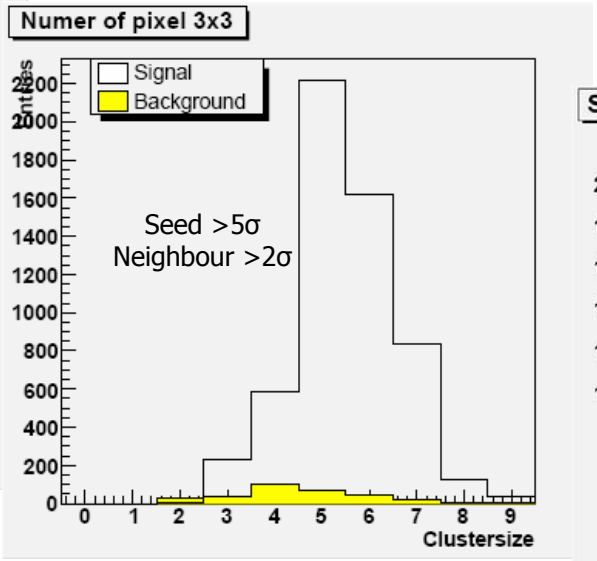
In the recent CERN test beam, a **beam telescope of 5 DEPFET planes** has been successfully operated!

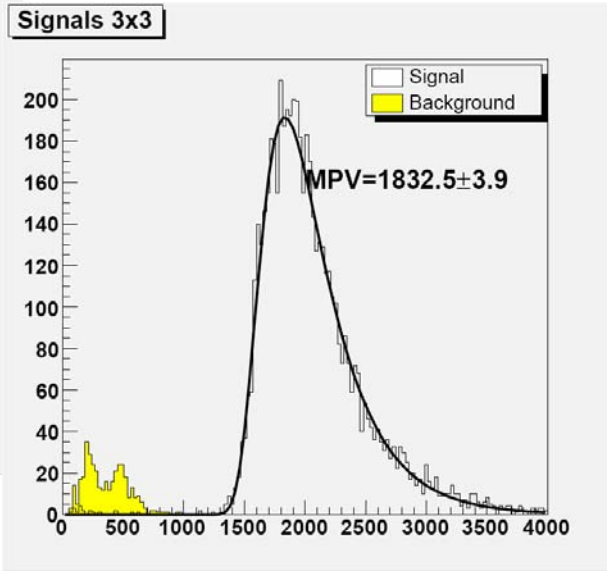
Test Beam Setup (at CERN)



Test Beam at DESY, Jan. '06







(Jaap Velthuis)

- Noise is determined from pedestal variations
- Seed pixel has signal >5 σ in central area
- Add neighbours if signal ≥2σ
- charge mostly confined in 3x3 cluster

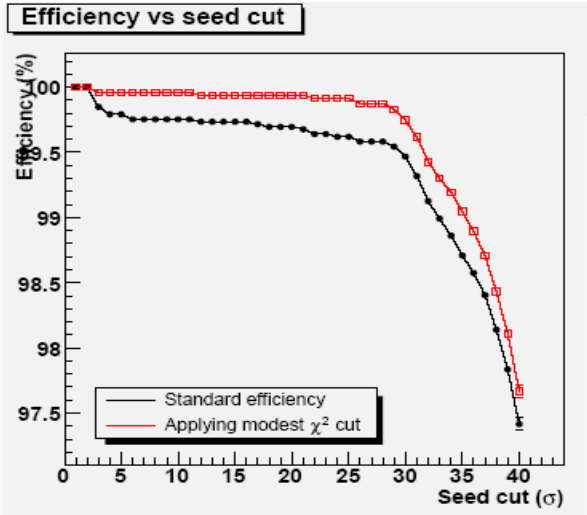
- S/N ≈ 110..115 (for 450 µm sensor!)
- Noise about 230 - 300 e- ENC

Usual suspects: system x-talk

CURO, external I2V converter…

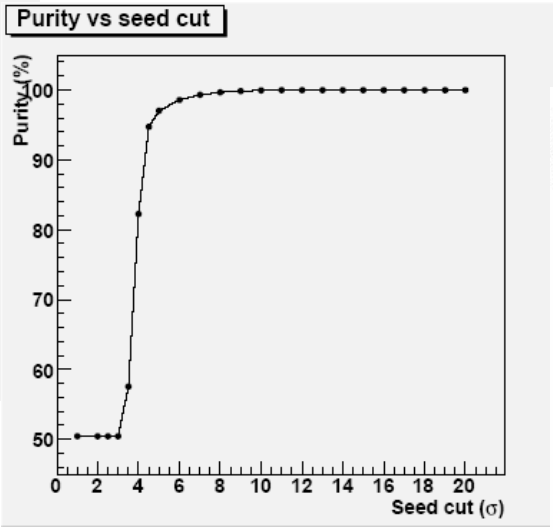
There is still room for improvement

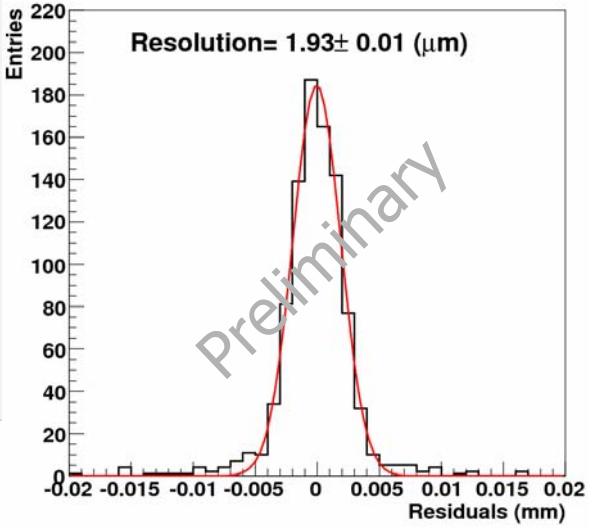
Efficiency & Position resolution



Efficiency = $\frac{\text{Number of tracks with cluster}}{\text{Total number of tracks}}$

Purity = $\frac{\text{Number of clusters with tracks}}{\text{Total number of clusters}}$





(Jaap Velthuis)

For 5 σ seed cut

- Efficiency ≈ 99.96%
- Purity ≈ 99.6 %

First preliminary result from CERN test beam,

120 GeV π, 33x23.75 μm² pixels

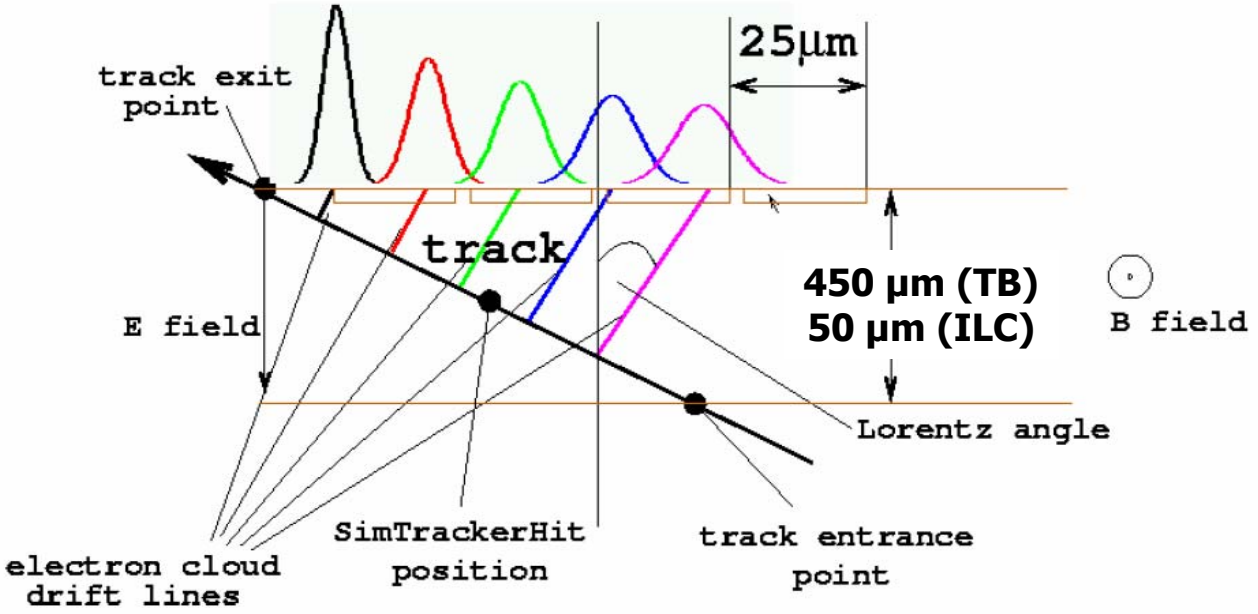
position resolution ≈ 2 μm

Simulation: Parameters

DEPFET ladders (and TB modules) implemented in MOKKA

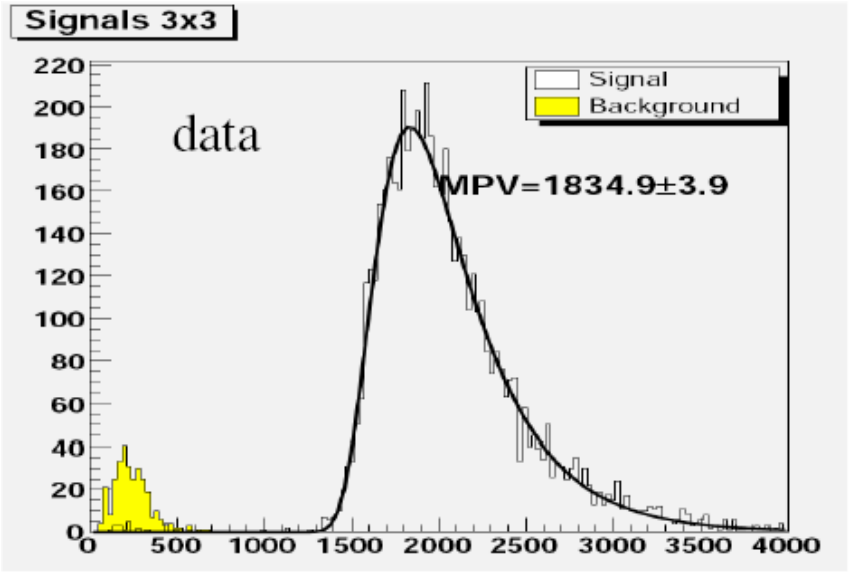
including:

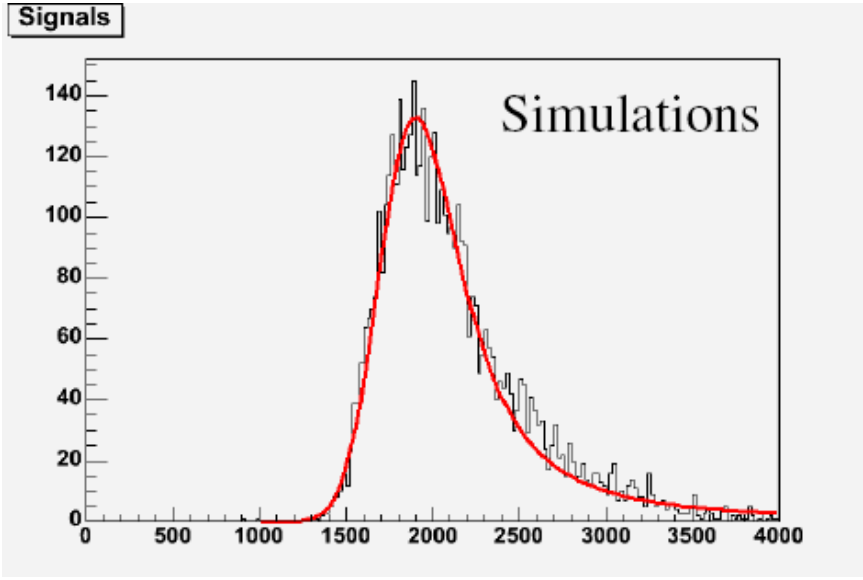
- E_{loss} fluctuations in thin layers
- Charge transport, sharing & diffusion
- Lorentz angle (33° @ 4T)
- Electronic noise 100 e- (goal for ILC), resp. 230e- (test beam)



Compare test beam results <-> Simulation

Here results with 450µm thick detector and 230e- noise:
normal incidence



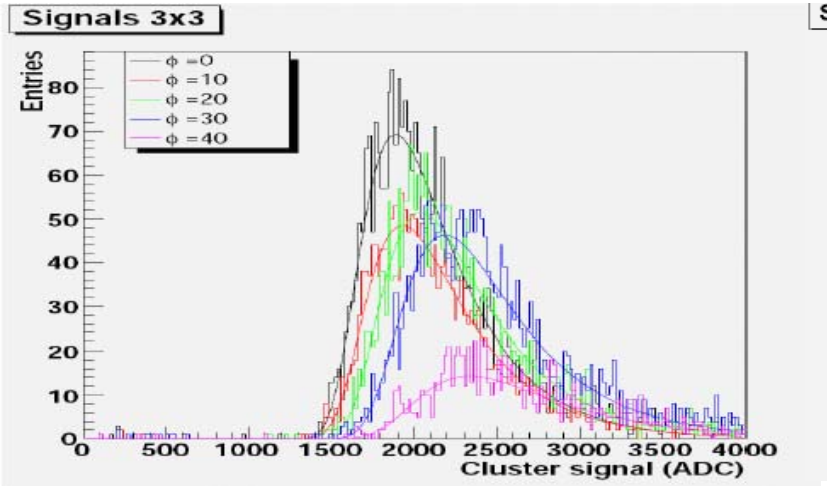


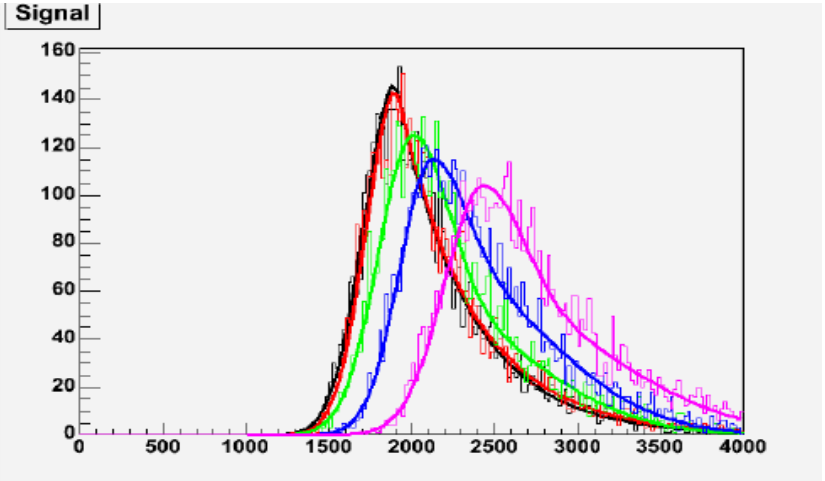
(Alexei Raspereza)

Data collected at normal track incidence is used to derive coefficient converting E_{Loss} into ADC counts

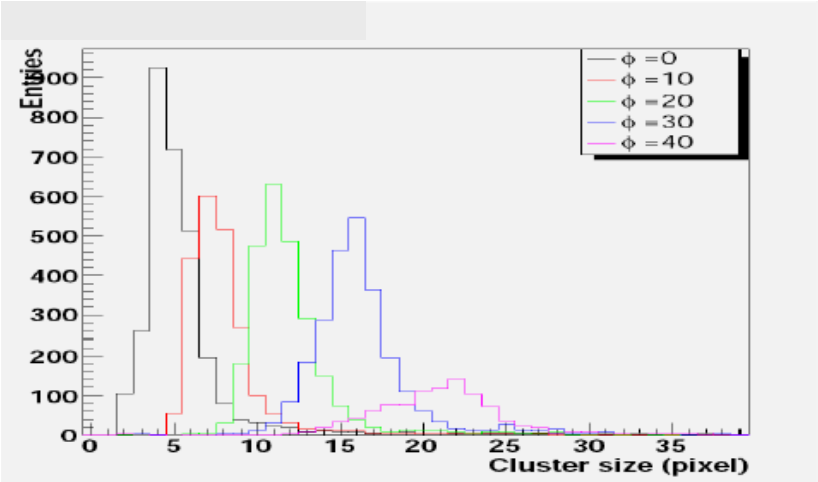
- Compare test beam results <-> Simulation

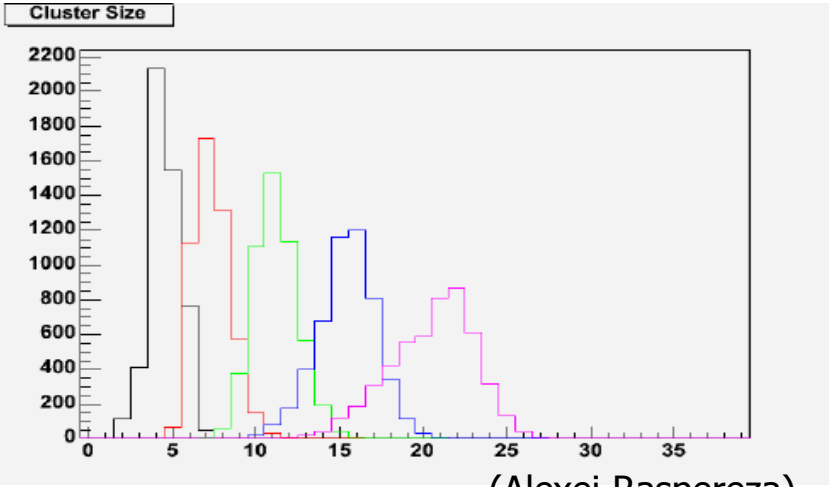
inclined tracks





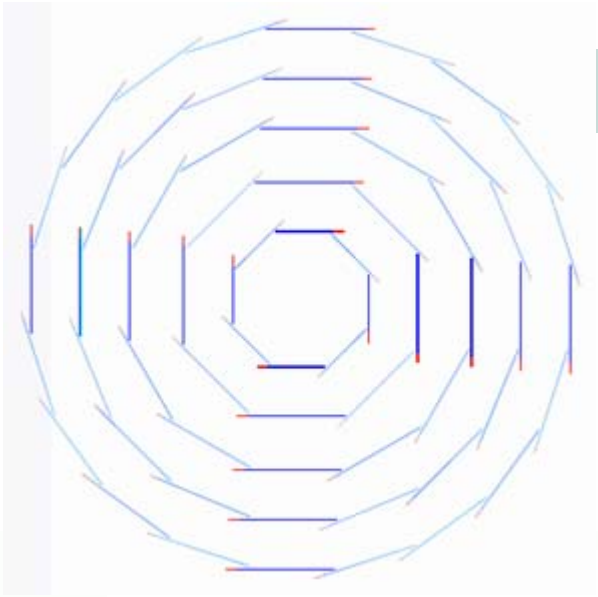
Data **Simulation**





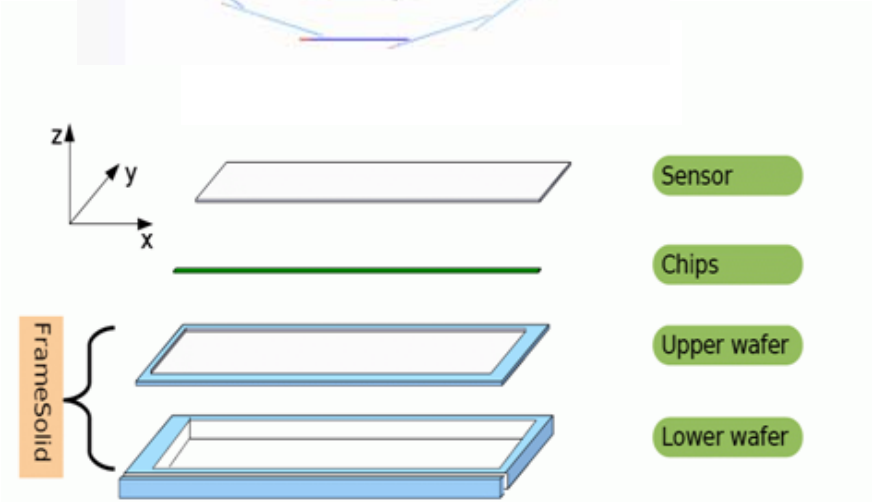
(Alexei Raspereza)

Simulation: LDC Geometry description

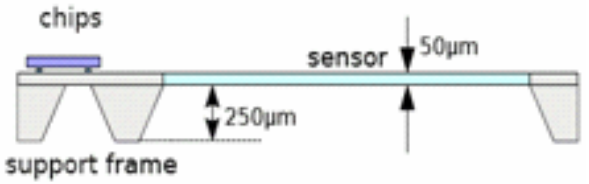


Sensitive layer thickness = 50 μm
Pixel size = 25×25 μm^2

	Radius (cm)	Ladders	Length (cm)
1	1.5	8	10.0
2	2.6	8	2×12.5
3	3.8	12	2×12.5
4	4.9	16	2×12.5
5	6.0	20	2×12.5

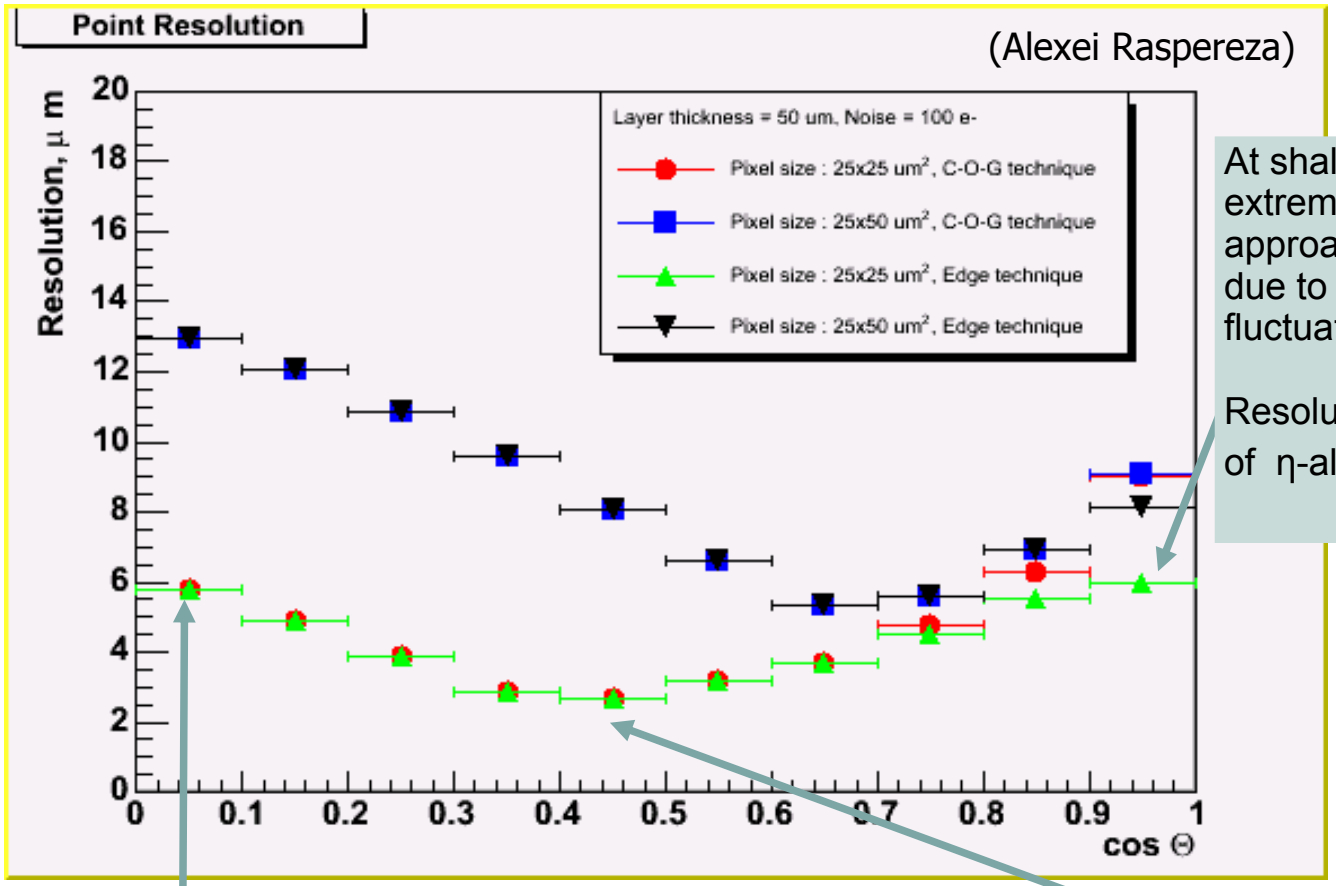


→ LDC ladders with support frames



Material up to first layer : beam pipe (500 μm beryllium)

Simulation: single point resolution



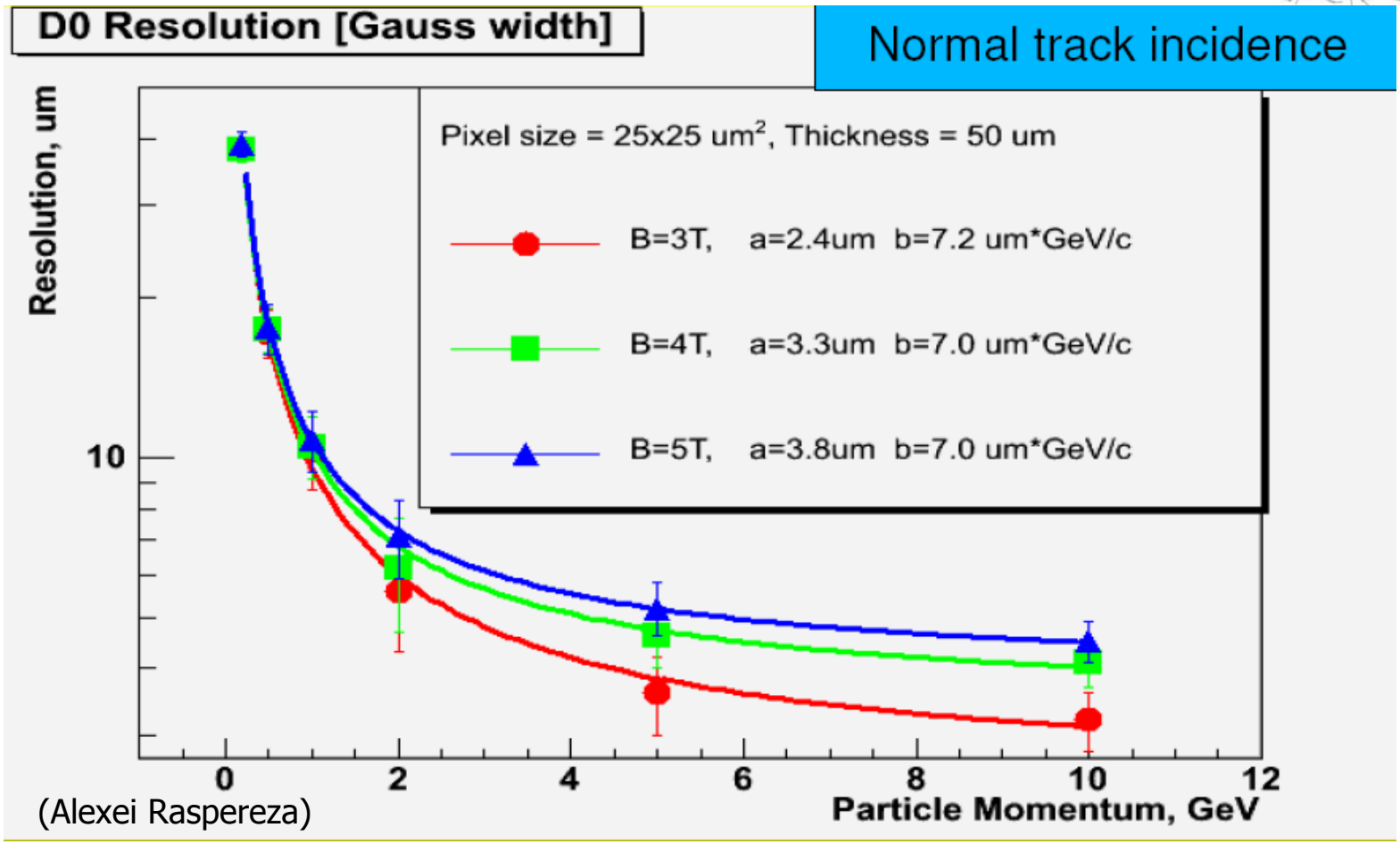
At shallow angles cluster size gets extremely large and simple COG approach yields poor resolution due to inter-pixel charge fluctuations.

Resolution is improved by means of η-algorithm (edge-technique)

In many cases at normal incidence only one row is fired : resolution is limited by pixel size

When track is inclined more than one row is fired -> resolution gets better

Simulation: IP resolution



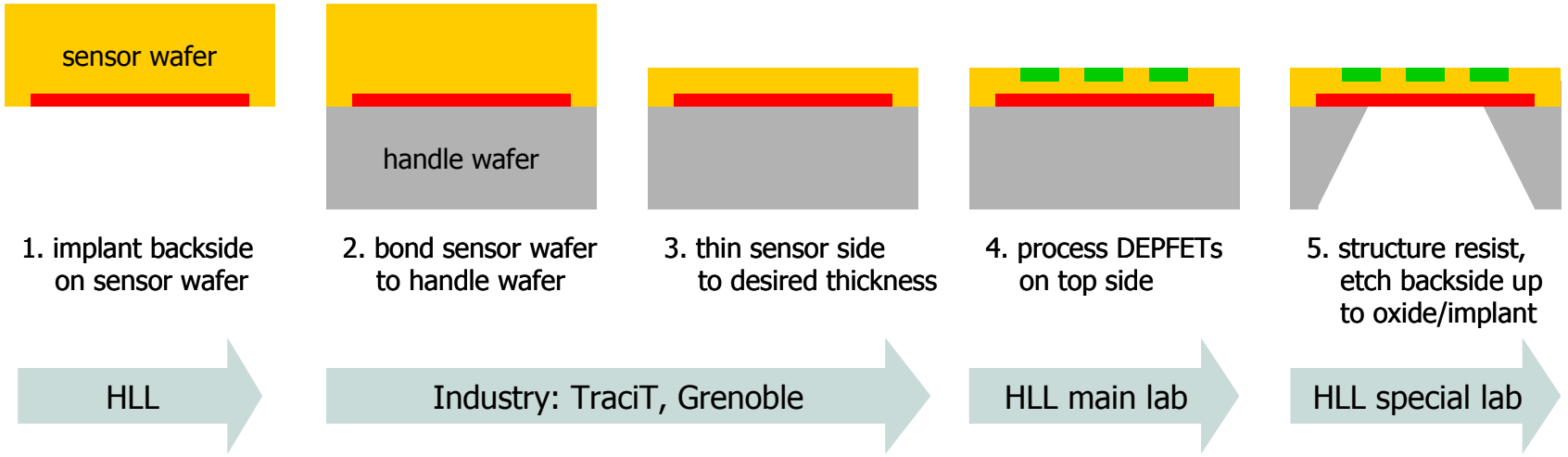
$$\sigma = \sqrt{a^2 + \left(\frac{b}{p\sin^{\frac{3}{2}}\theta}\right)^2}$$

$a < 5\,\mu m$ (point precision)

$b < 10\,\mu m$ (multiple scattering)

→ IP resolution is OK!

Thinning Technology



New: **150mm** Ø wafers!

New: Wafer bonding and thinning in **industry**

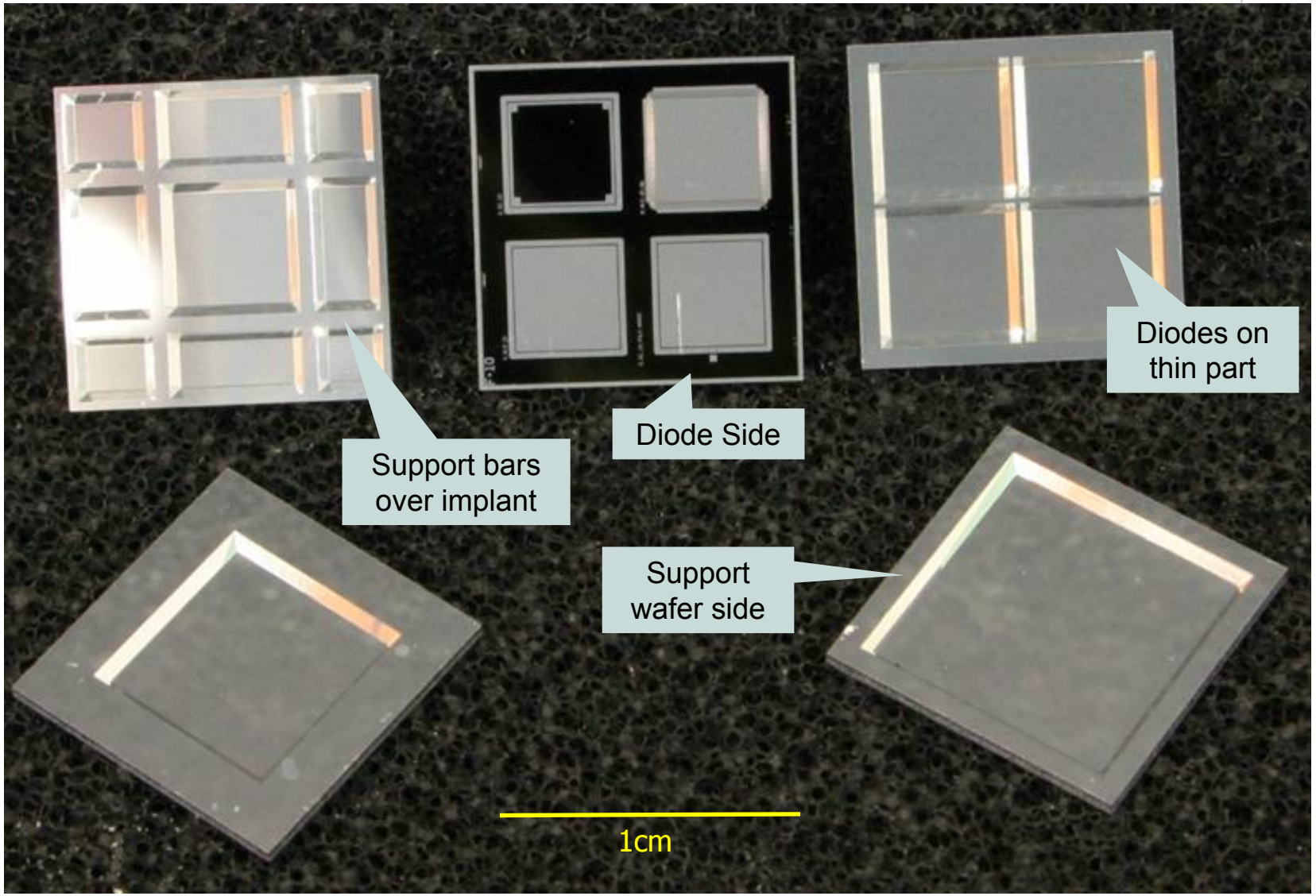
New: Processing in **HLL main lab**

Still in R&D phase:

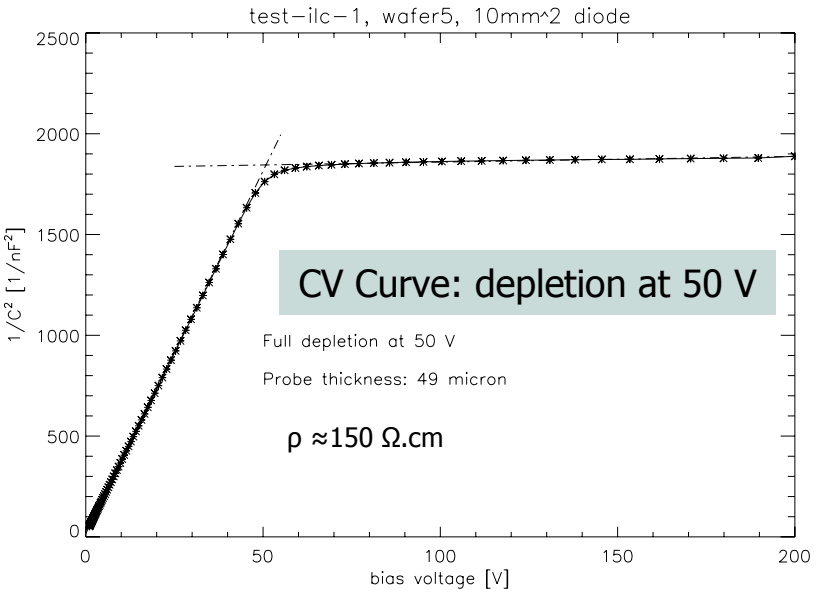
1: process test structures on SOI wafers

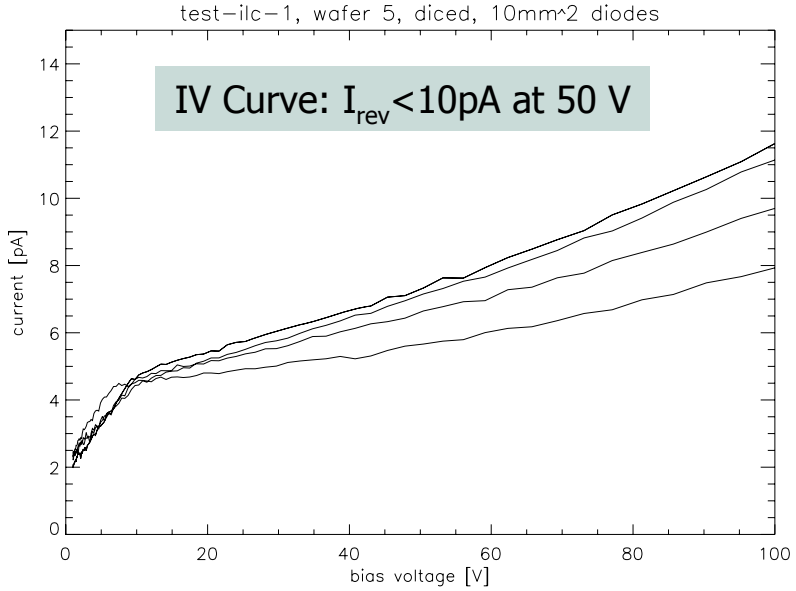
2: mechanical samples

PiN Diodes with Different Support Sides



PiN Diodes on thin Silicon

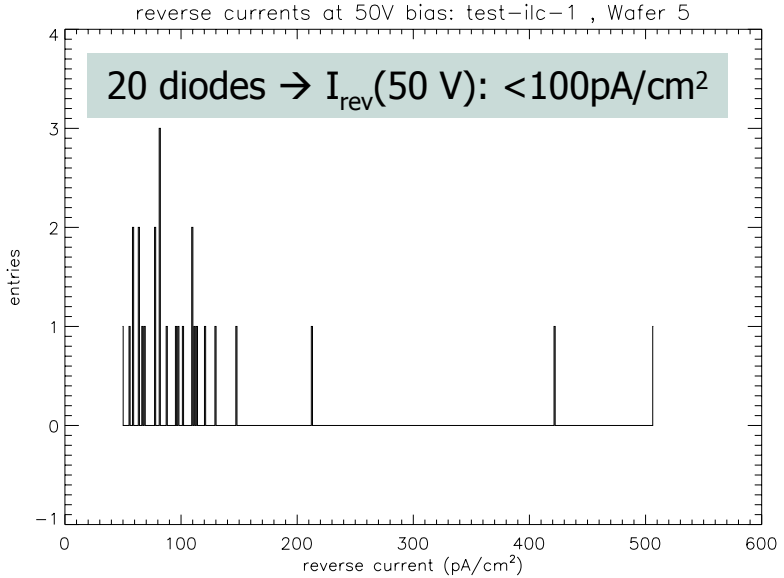




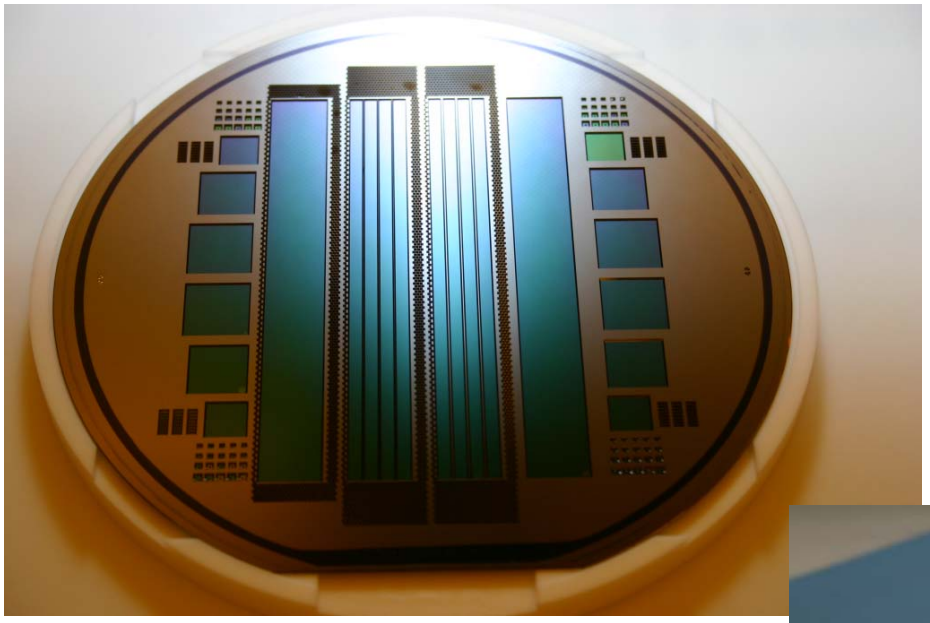
Thin diodes have **excellent** leakage currents (~100pA / cm²).

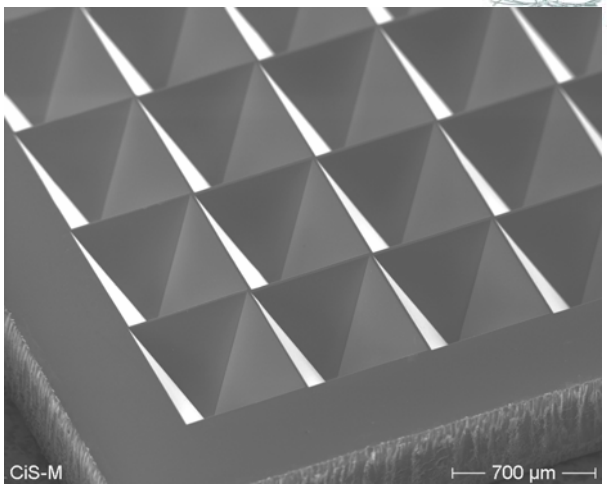
This shows:

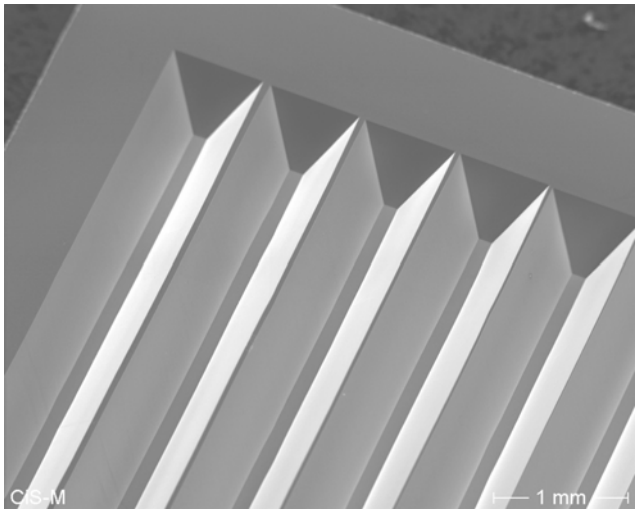
Processing of the SOI wafer and removal of handle wafer **does not degrade devices**!

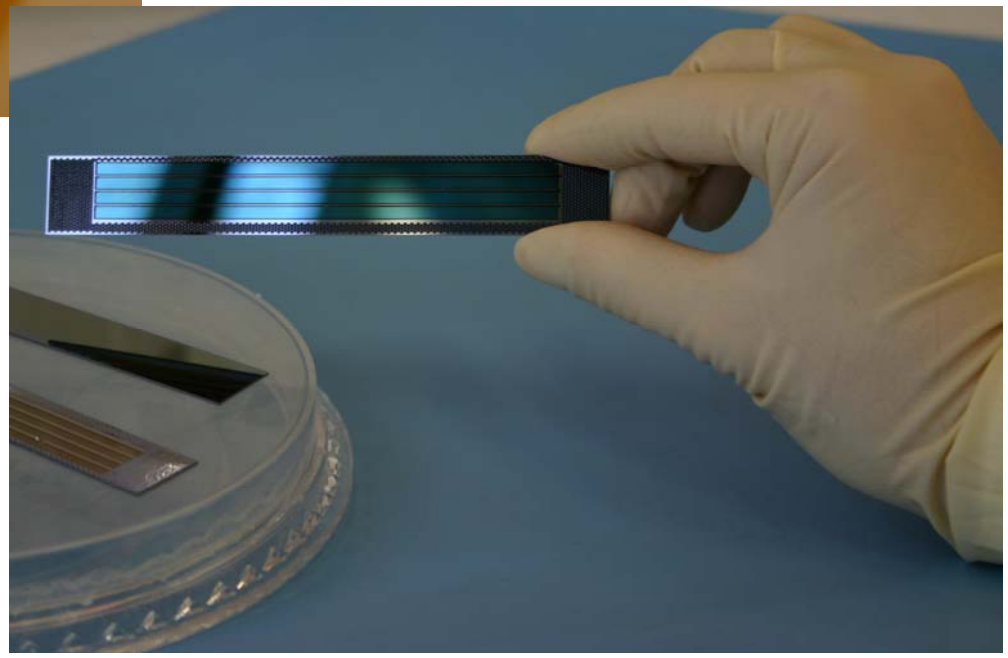


Thinning : mechanical samples









Summary

Hope I gave you at least an overview of this year's highlights.

In terms of speed and noise the DEPFET system is **not yet ready** for the ILC VTX. But the beamtest results with this **very first iteration of the system** are more than encouraging and the simulations show us that we are on the right track!

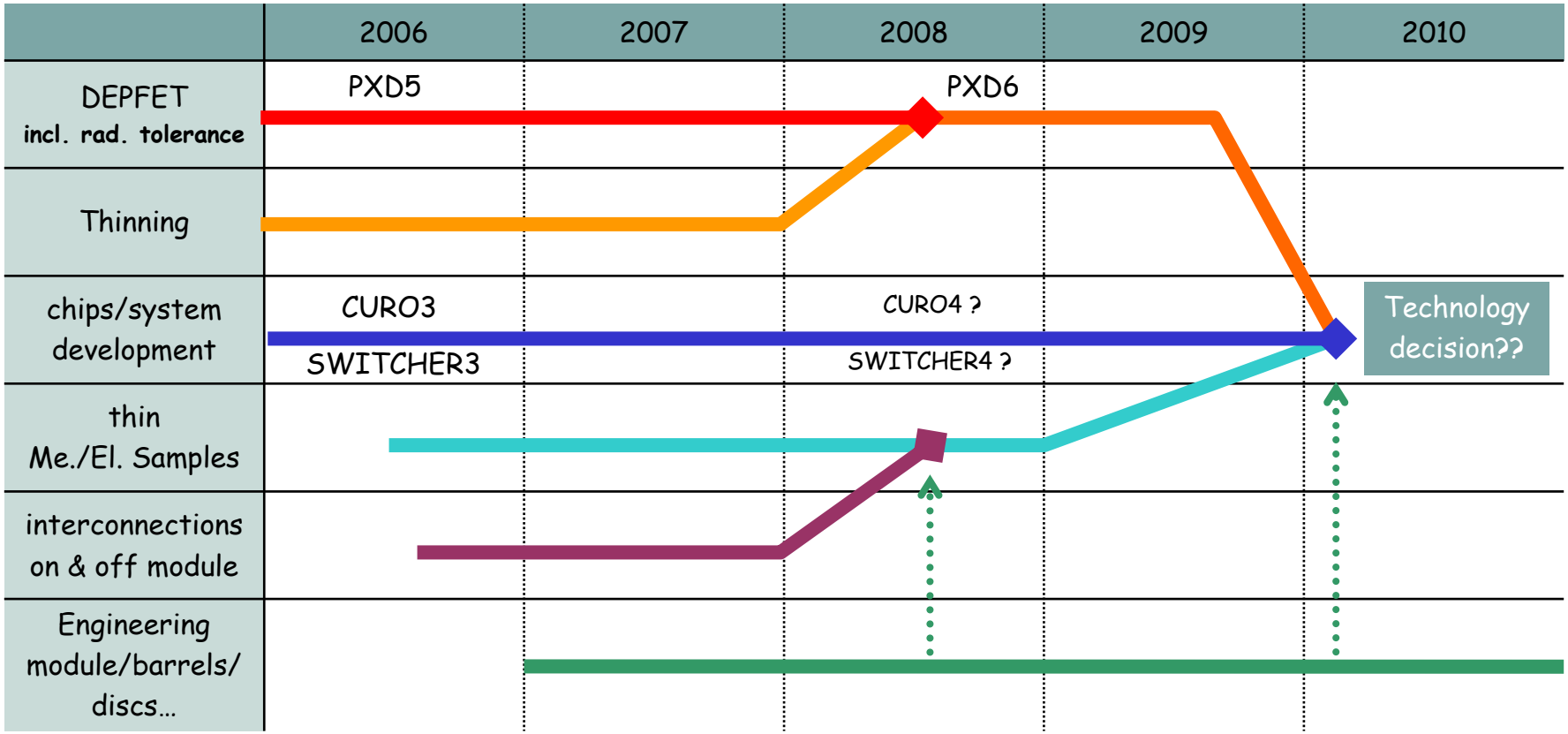
We are currently producing the next (of course better!!) generation of DEPFET sensors and are in the simulation phase for the new r/o chip.

I had to skip all the other important topics like:

:- sensor and technology development
:- single pixel characterisation
:- r/o ASIC
:- radiation tolerance

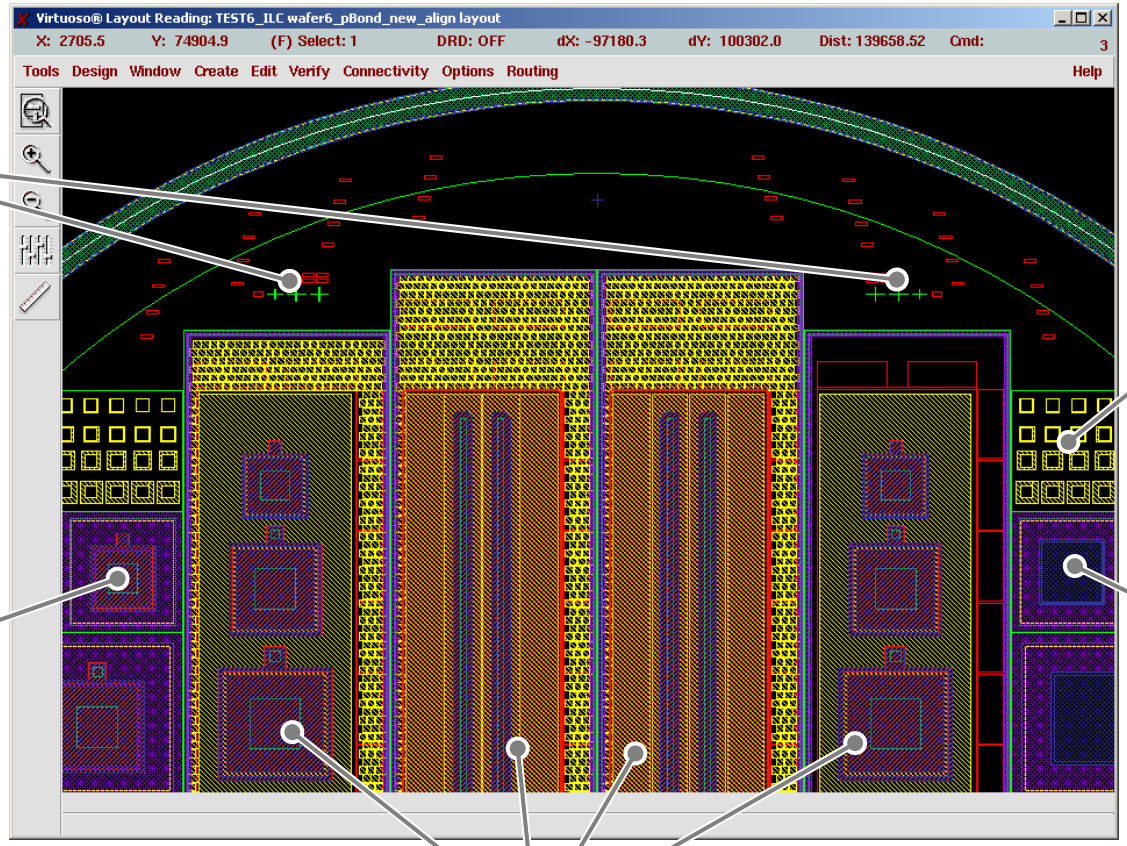
But I'm looking forward to your questions and the discussions during this workshop!

~~Roadmap~~ Subway map towards a thin demonstrator

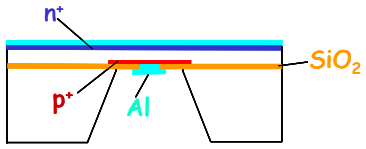


The 3rd round - masks just submitted…

Alignment marks in BOX to find the partial p-implant after bonding



Implants like DEPFET config.



unstructured n+ on top
structured p+ in bond region

Some test structures

Diodes with various areas

MOS-C with various areas

4 "full size" 1st layer ladders 100x13 mm², 1 and 3 mm frame along the long side

Module Concept/Power Consumption

Total power consumption of the vtx-d in the active region (TDR design, 25 μm pixel)

DEPFET matrix only:

1st layer : 2 rows active, 30 μA · 5V · 650 · 2 · 8 = 1.6 W

2nd .. 5th layer: 1 row active, 30 μA · 5V · 1100 · 1 · 112 = 18.5 W

Steering chips: assuming 0.15 mW for an inactive, 300 mW for an active channel

1st layer : [(4998 · 0.15 mW)+(2 · 300mW)] · 8 = 10.8 W

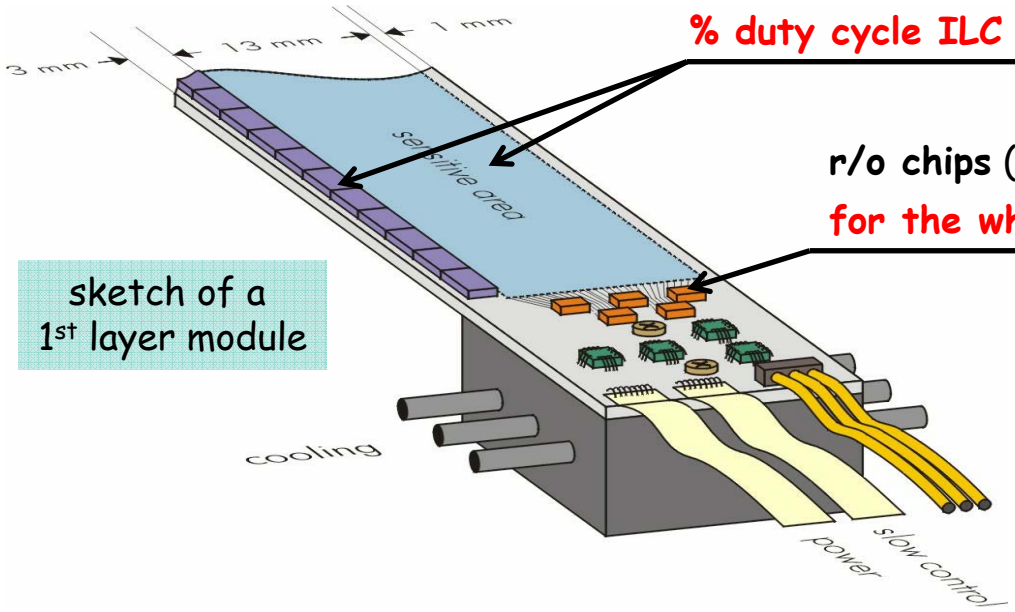
2nd ..5th layer: [(6249 · 0.15 mW)+(1 · 300mW)] · 112 = 138.6 W

Σ active region ≈ 170 W

% duty cycle ILC 1/200 → ≈ 0.9 W

r/o chips (current version):2.8 mW/chn.

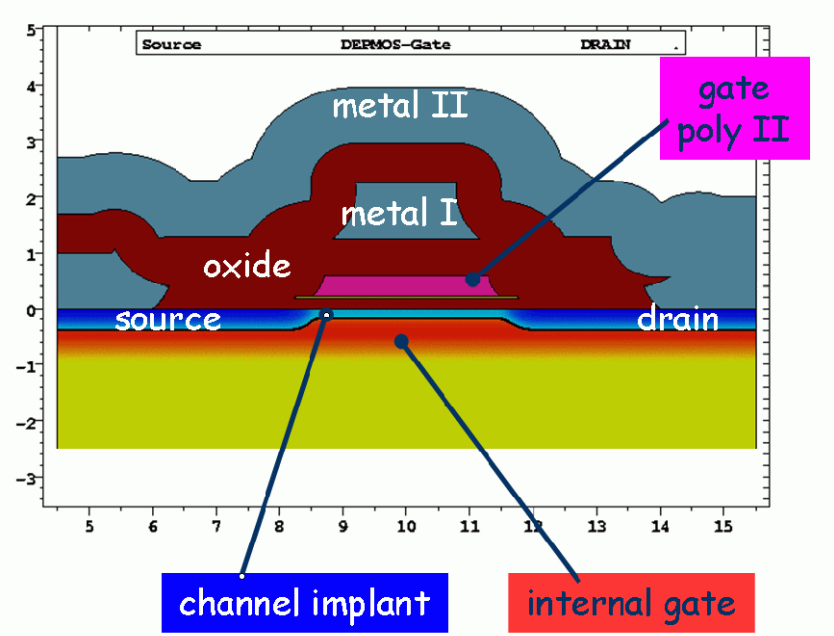
for the whole vtx-d: ≈ 2W

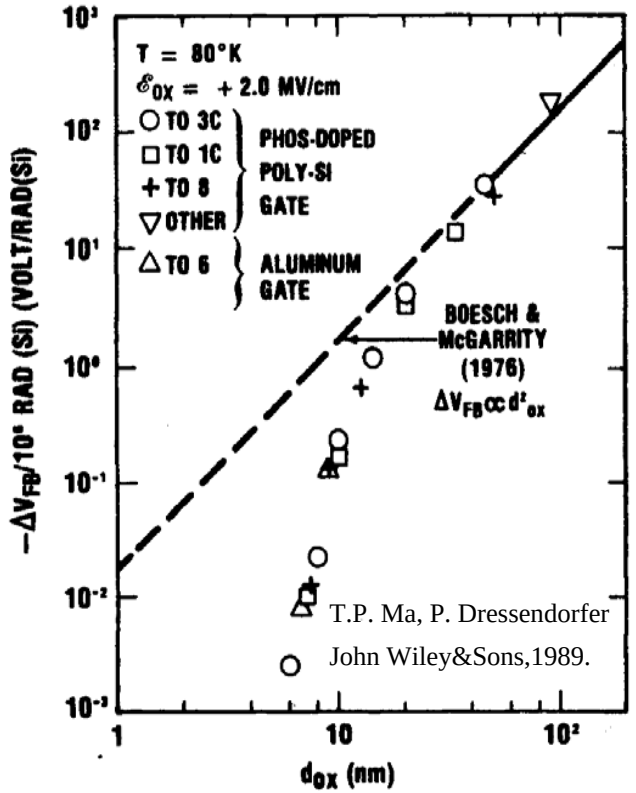


sketch of a 1st layer module

Radiation Effects

Gate Dielectrics t>200nm





1. positive oxide charge and positively charged oxide traps have to be compensated by a more negative gate voltage: negative shift of the threshold voltage

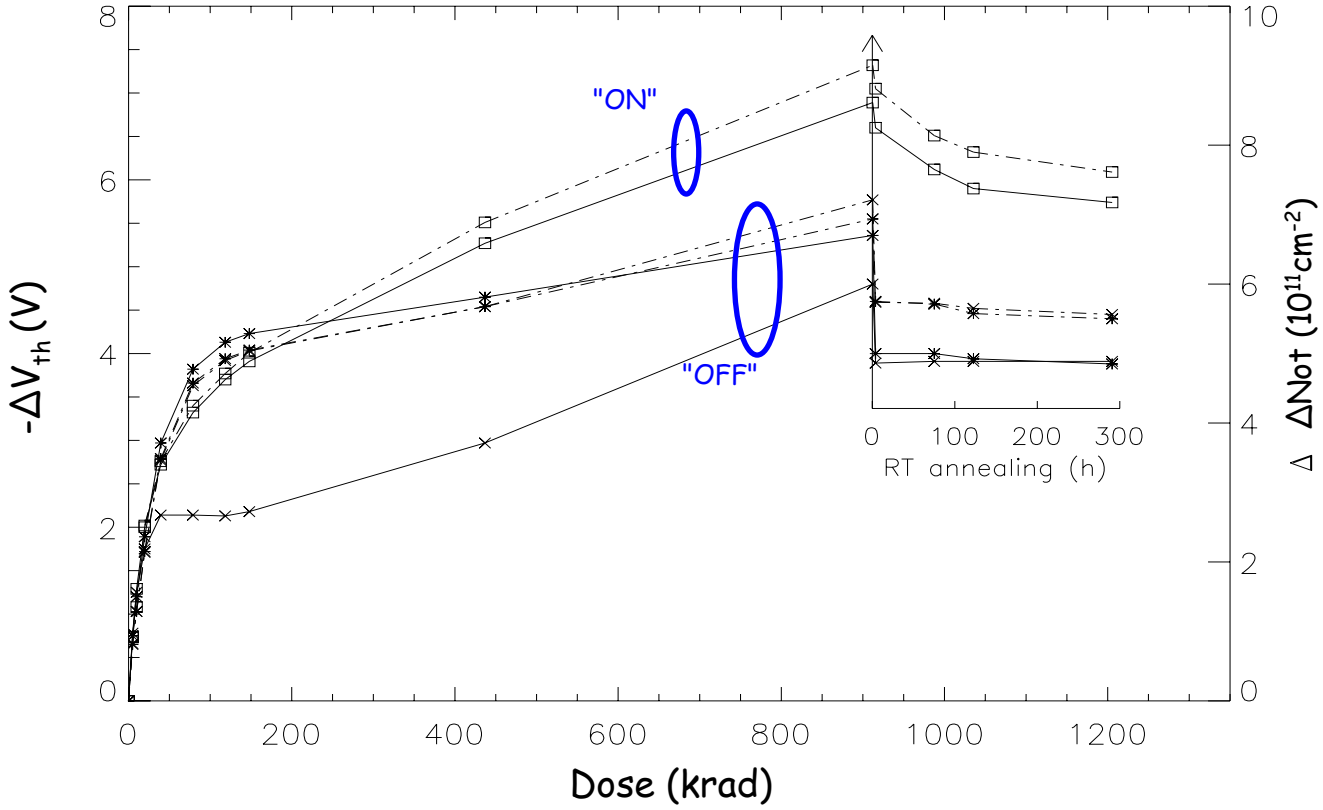
2. increased density of interface traps: higher 1/f noise and reduced mobility (g_m)

Threshold voltage shift

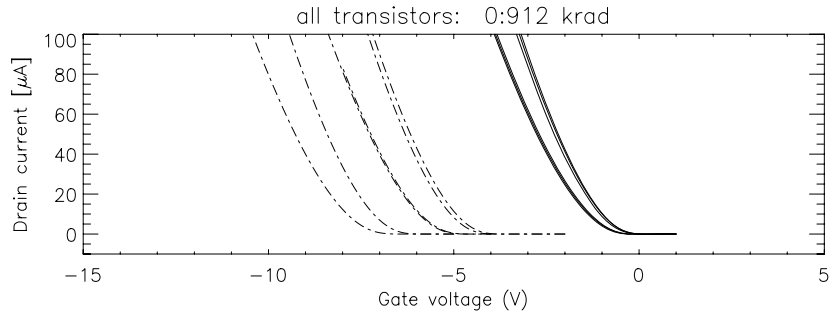
GSF – National Research Center for Environment and Health, Munich

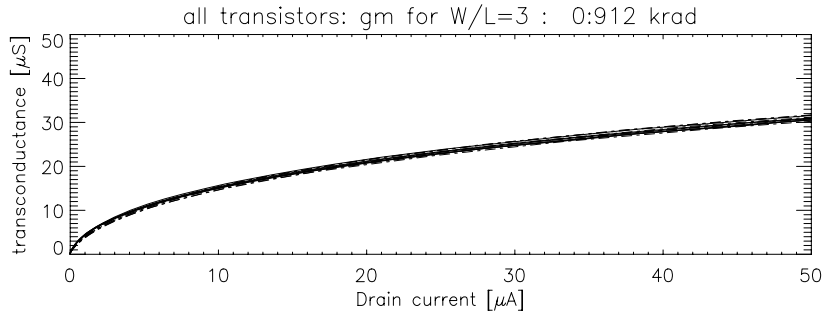
^{60}Co (1.17 MeV and 1.33 MeV)

No annealing during irradiation
→ ~ 3 days irradiation
Dose rate: ≈ 20 krad(SiO_2)/h

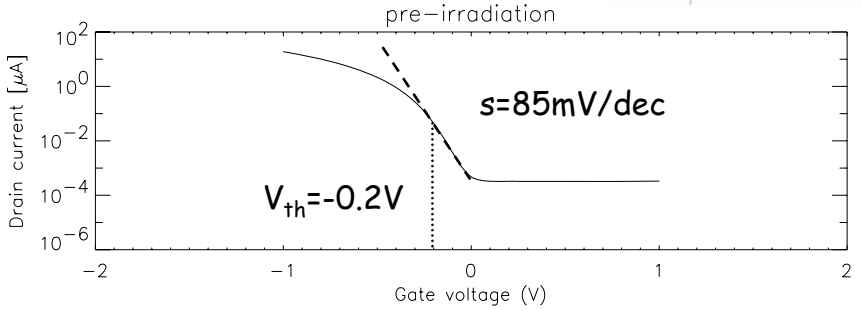


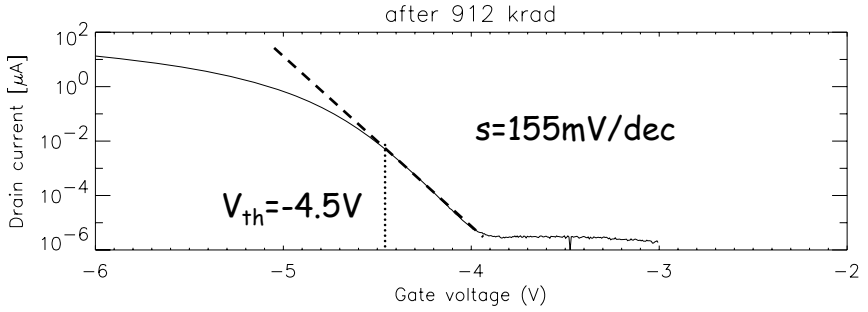
Transconductance and subtreshold slope





No change of the transconductance g_m



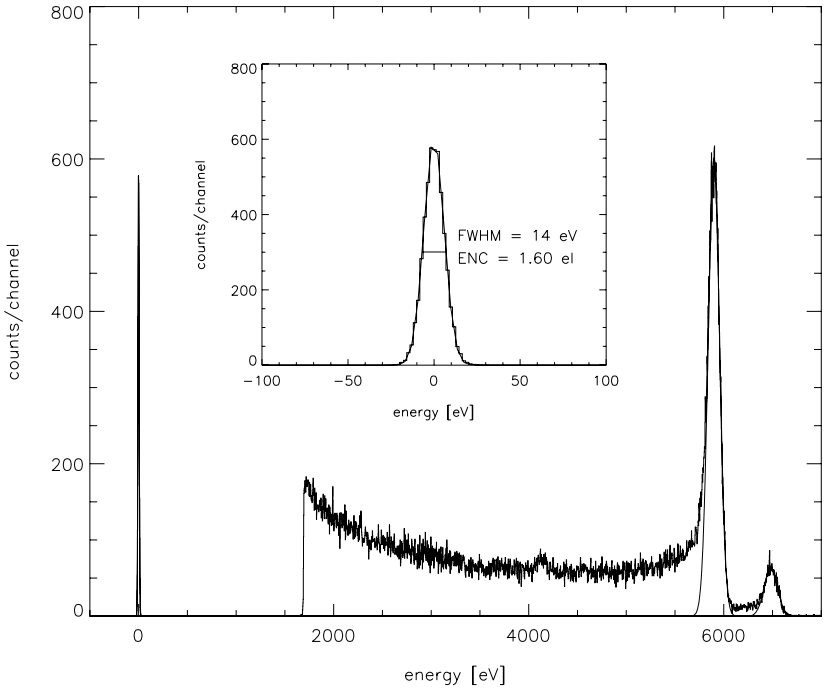


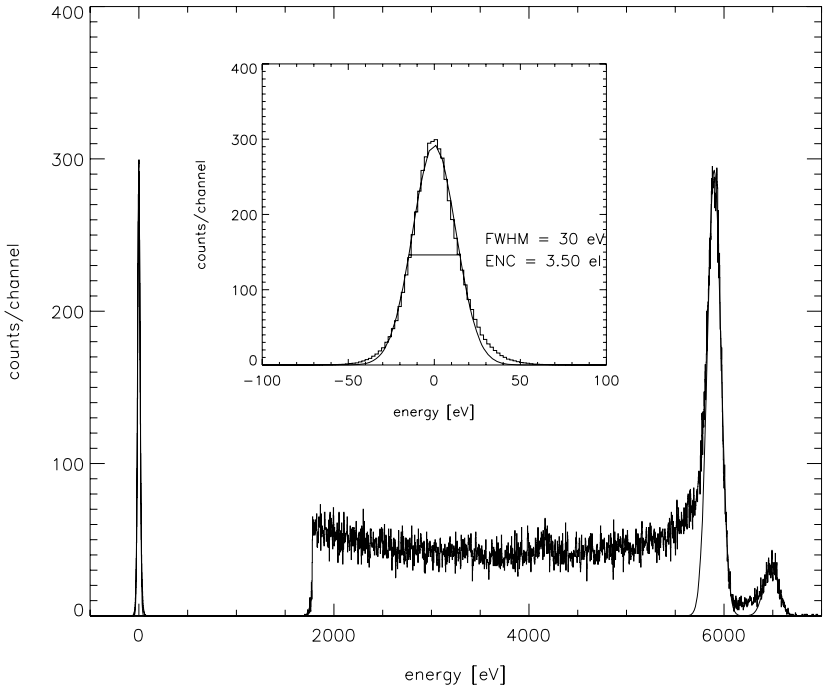
$$N_{it} = \frac{C_{ox}}{kT} \cdot \ln(10) \cdot (s_{D2} - s_{D1})$$

300 krad → $N_{it} \approx 2 \cdot 10^{11}$ cm^{-2}
912 krad → $N_{it} \approx 7 \cdot 10^{11}$ cm^{-2}

Literature:
After 1Mrad 200 nm (SiO_2):
$N_{it} \approx 10^{13}$ cm^{-2}

^{55}Fe Spectrum (single pixel)





non-irradiated

V_{thresh}≈-0.2V, V_{gate}=-2V

I_{drain}=41 μA

time cont. shaping τ=10 μs

Noise ENC=1.6 e^- (rms)

at T>23 degC

912 krad ^{60}Co

V_{thresh}≈-4.0V, V_{gate}=-6.0V

I_{drain}=40 μA

time cont. shaping τ=10 μs

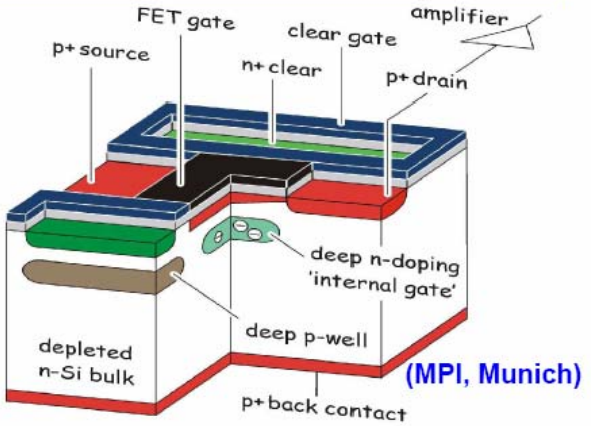
Noise ENC=3.5 e^- (rms)

at T>23 degC

Irradiations at LBNL - 88 inch Cyclotron, July 2006

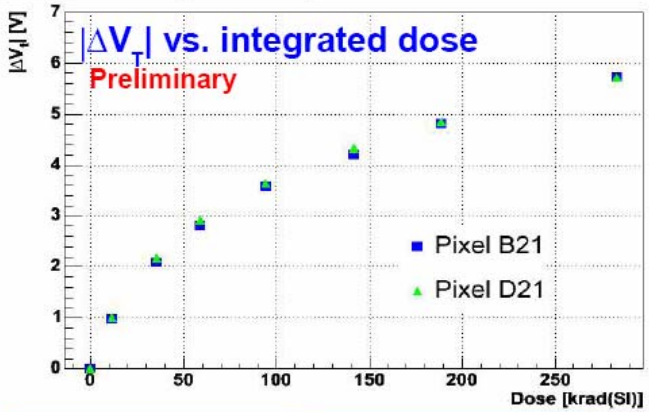
First test of DEPFET pixels at LBNL

- Irradiation of single pixel test structures with 30 MeV p up to 1.2×10^{12} p/cm^2 (eq. 283 krad(Si))
- Transistor terminals grounded during irradiation; in-pixel MOSFET characteristics measured soon after irradiation steps
  - Threshold voltage variations as expected from previous irradiation with ^{60}Co
  - Slight degradation of transconductance at the highest doses
- Detailed annealing studies to be performed soon

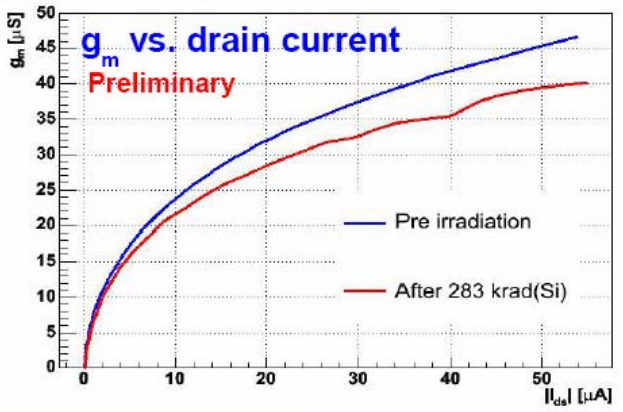


(MPI, Munich)

Threshold voltage variation



Transconductance, pixel B21



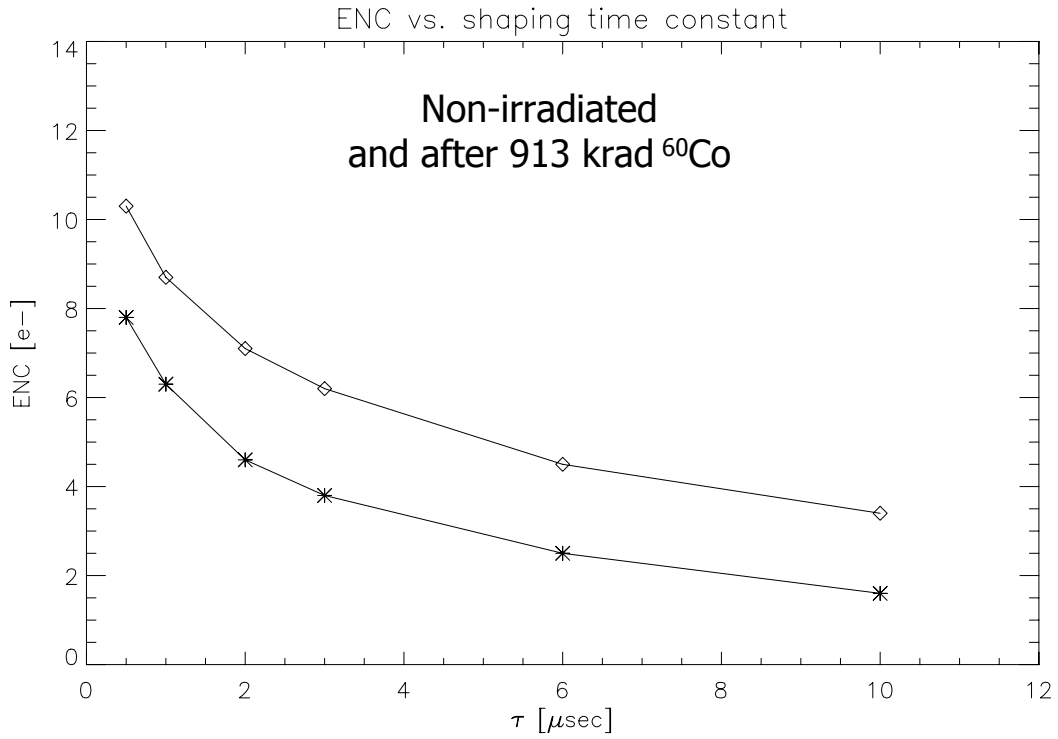
Devis Contarato

Monolithic Pixels R&D at LBNL

VLCW06

UBC, July 19-22, 2006

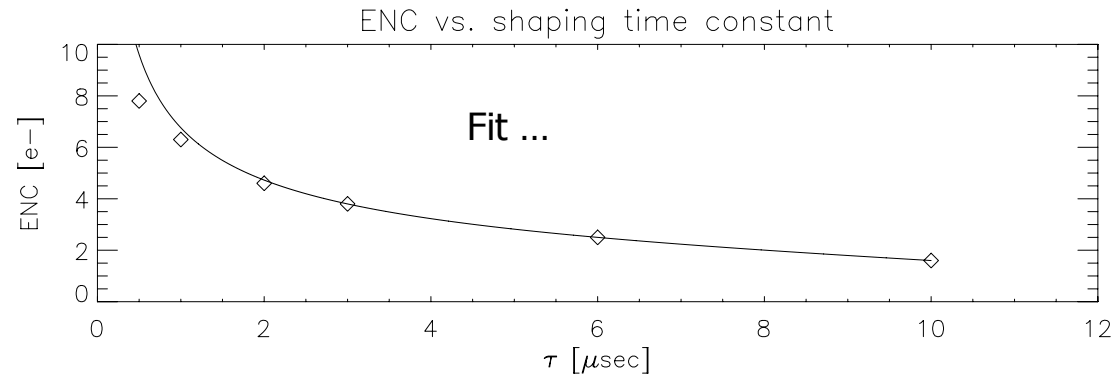
Noise vs. shaping time τ

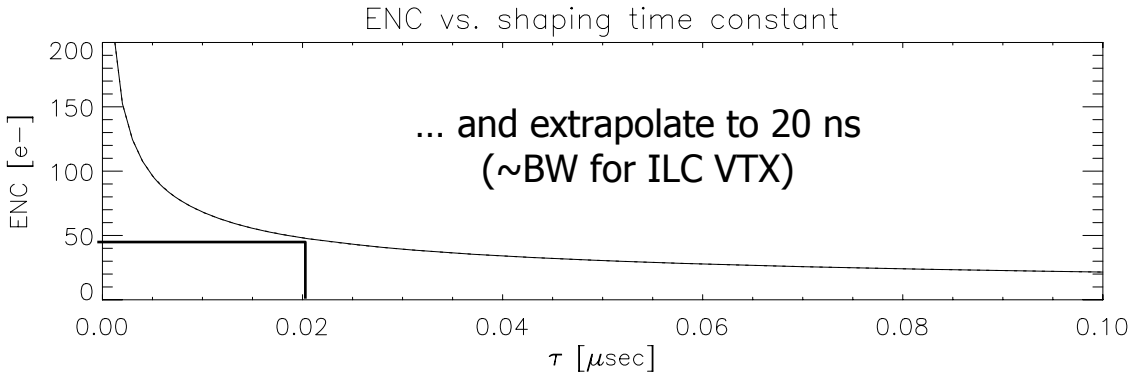


$$ENC = \sqrt{\alpha \frac{2kT}{g_m} C_{tot}^2 A_1 \frac{1}{\tau} + 2\pi a_f C_{tot}^2 A_2 + q I_L A_3 \tau}$$

Therm. noise | 1/f | I_L

Noise vs. shaping time τ

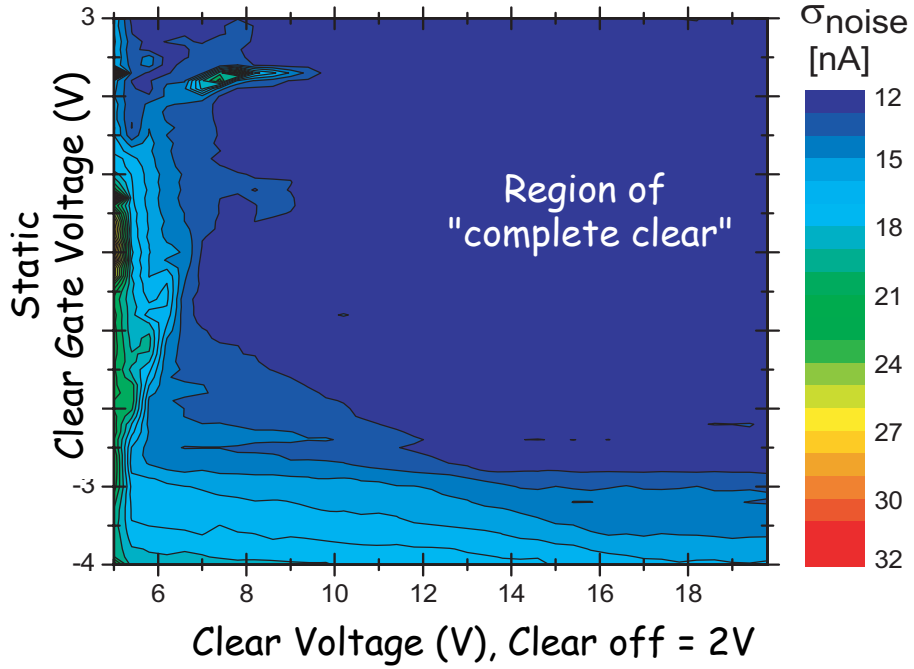




$$ENC = \sqrt{\underbrace{\alpha \frac{2kT}{g_m} C_{tot}^2 A_1 \frac{1}{\tau}}_{\text{Therm. noise}} + \underbrace{2\pi a_f C_{tot}^2 A_2}_{1/f} + \underbrace{q I_L A_3 \tau}_{I_L}}$$

Clear Efficiency

- Study mini matrix devices in laser setup
- Scan wide parameter space of Clear Gate and Clear Voltage
- Study various designs, geometries (length of clear gate) and operating conditions (static or clocked clear gate)

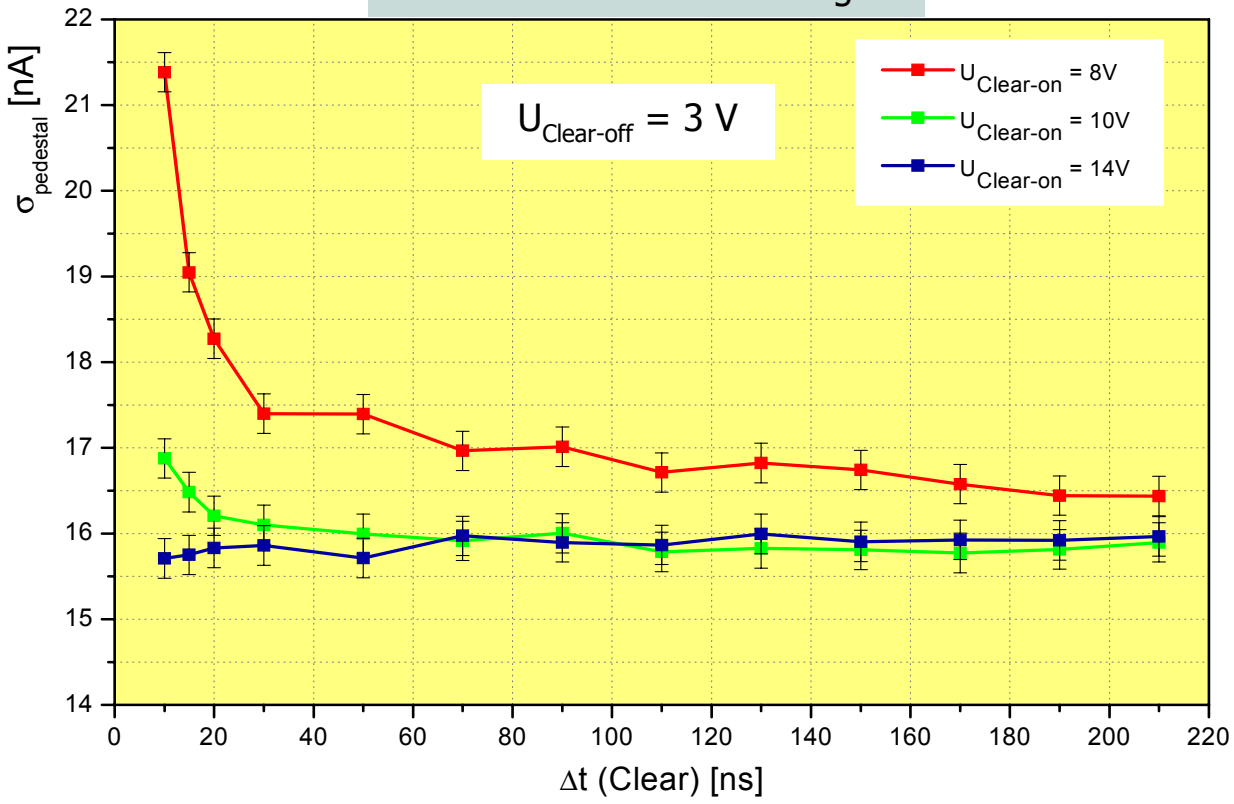


Complete clear achieved with static clear gate !
Required voltages are small (5-7V) – very important for future SWITCHER!

Fast Clearing

o Study clear efficiency for short clear pulses

Device with common clear gate



Complete clear in only 10-20 ns @ ΔV_{clear} = 11-7 V

Goals of new submission 'PXD5'

Mostly use 'baseline' DEPFET geometry

Build **larger matrices**

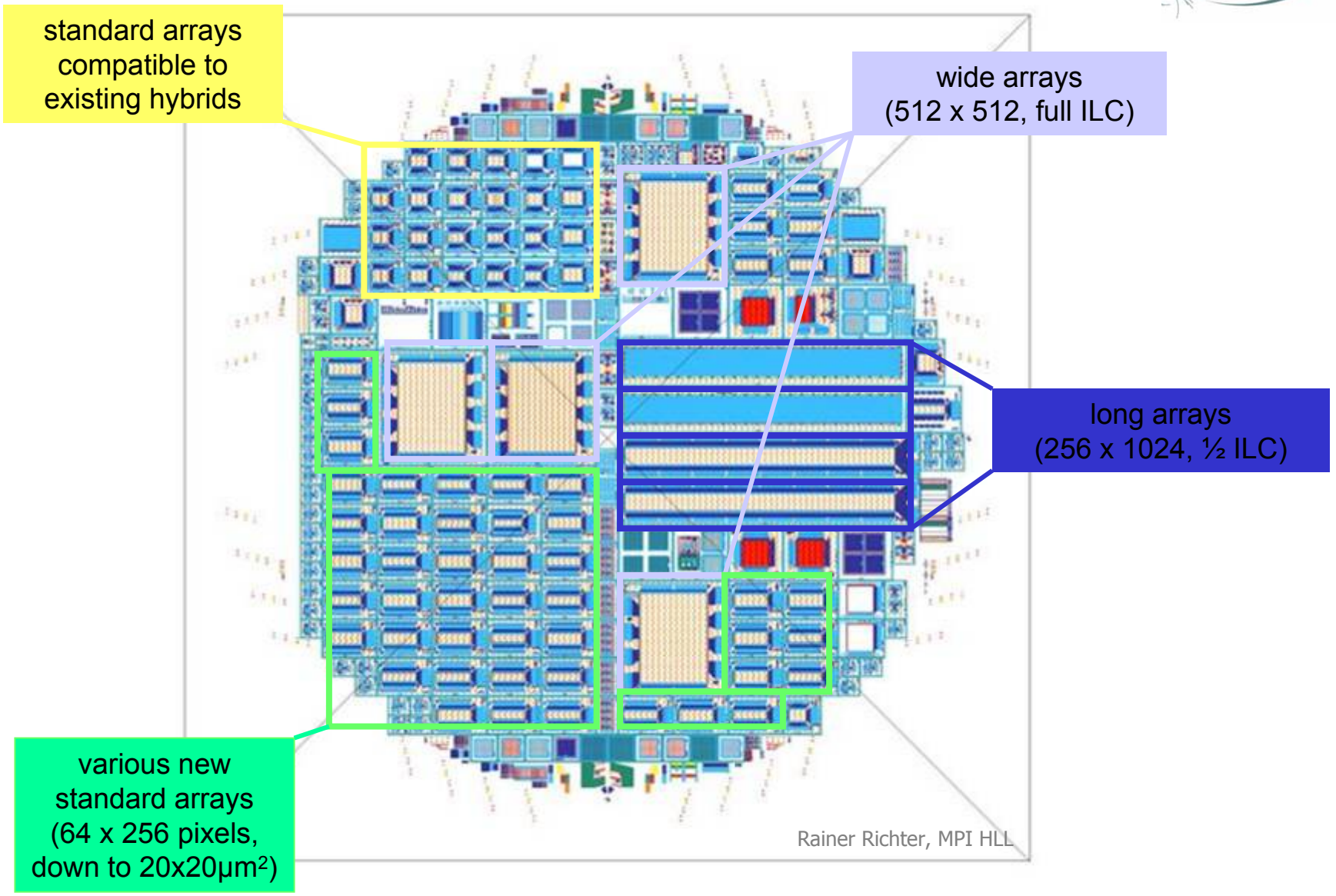
- Long matrices (full ILC drain length)
- Wide matrices (full Load for Switcher Gate / Clear chips)

Try new DEPFET variants:

- reduce **clear voltages** (capacitive coupling, modified implantations, modified geometry)
- Very **small** pixels (20μm x 20μm)
- Increase internal **amplification** (g_q)

Add some bump bonding test structures

Structures on PXD5 wafer

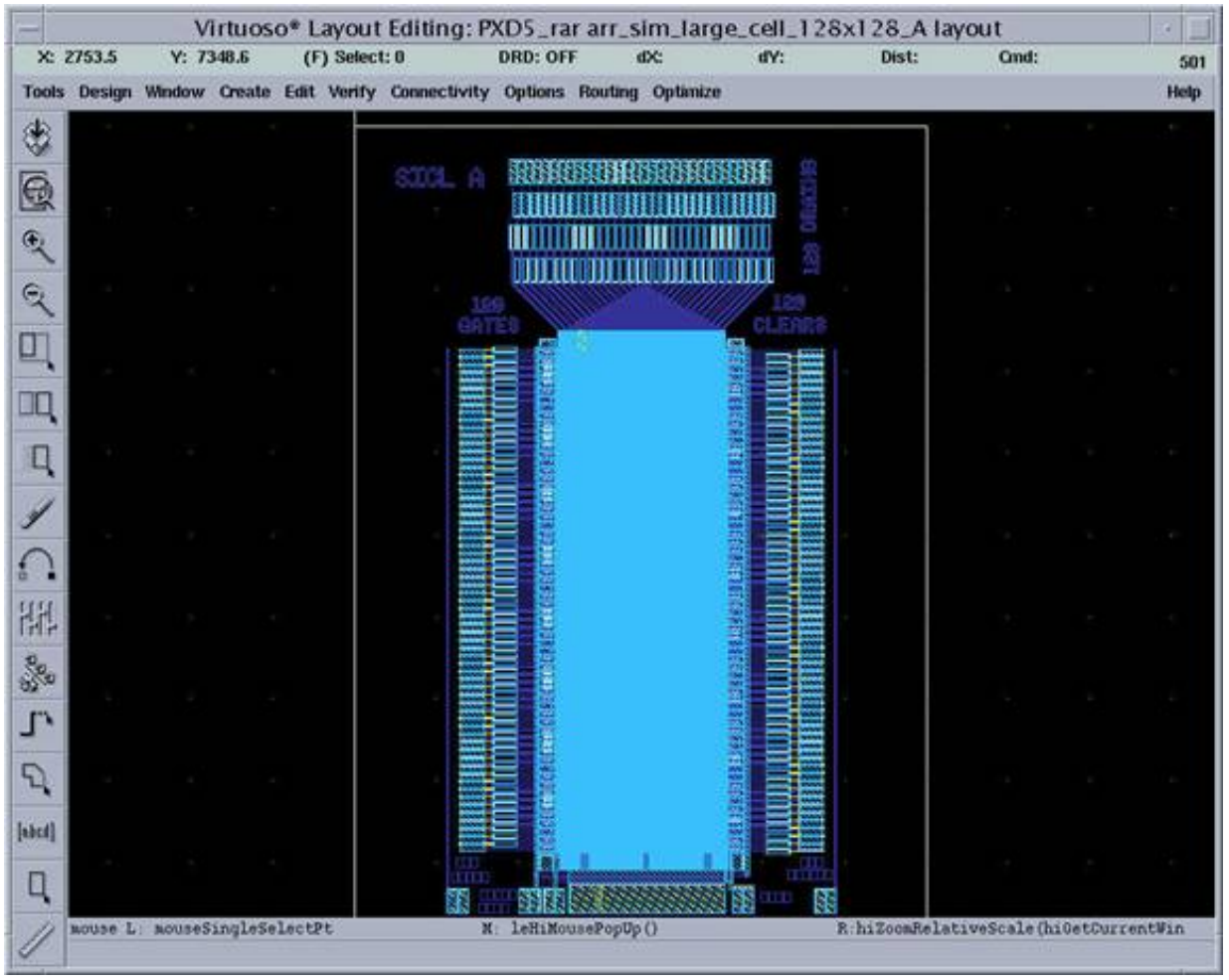


Standard Detector

64 (x) x 128 (y) double pixels = 64 x 256 pixels. Pixel size 24 (or 32) x 24 μm^2

2 x Switcher3, 1 x CURO

Provided in many design variations



Wide Detector

512 (x) x 256 (y) double pixels = 512 x 512 pixels (full ILC width). Pixel size 32 x 24 μm^2

2 x 2 x Switcher 3, 8 x CURO

Study full load on Switcher signals