Chronopixel development status

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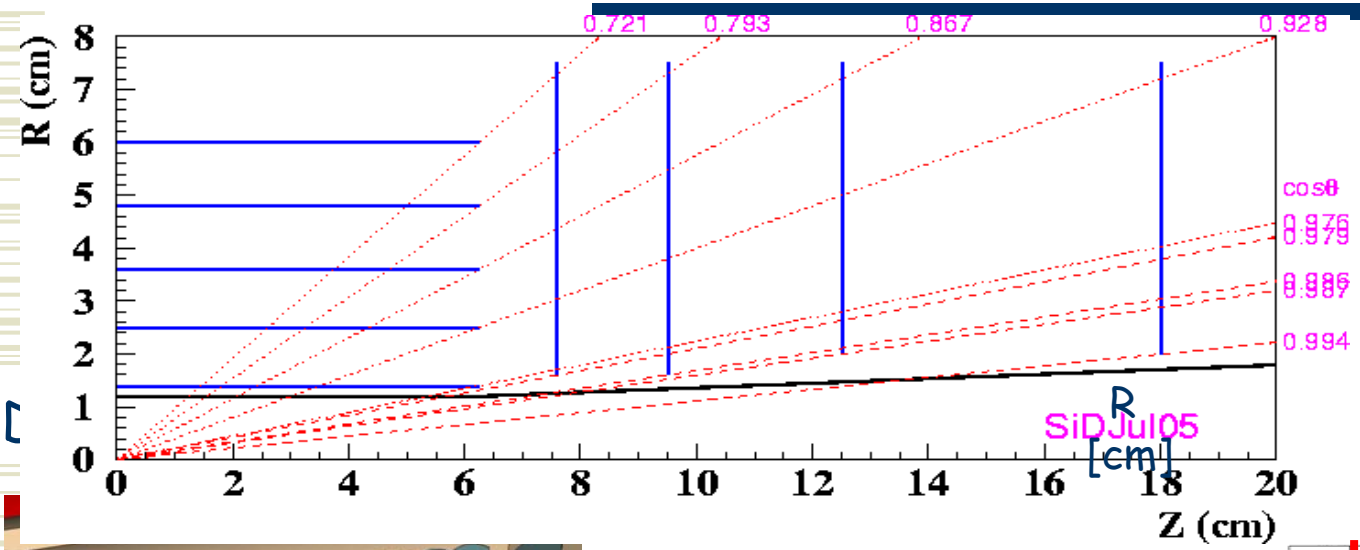
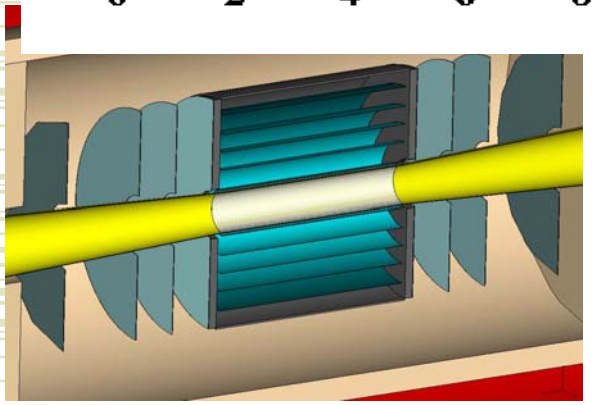
SiD Vertex Layout



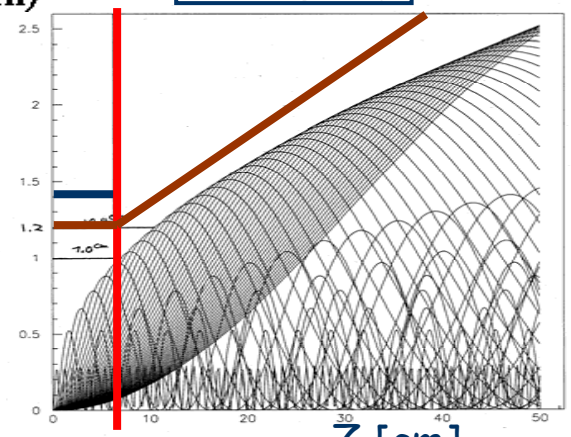
5 barrel layers
4 end disks

5 Tesla



Design drivers:

Smallest radius possible
Clear pair background



Role:

Seed tracks & vertexing
Improve forward region

SiD Vertex Detector

- BARREL
  - 100 sensors
  - 1750 cm^2
- FORWARD
  - 288 sensors
  - 2100 cm^2

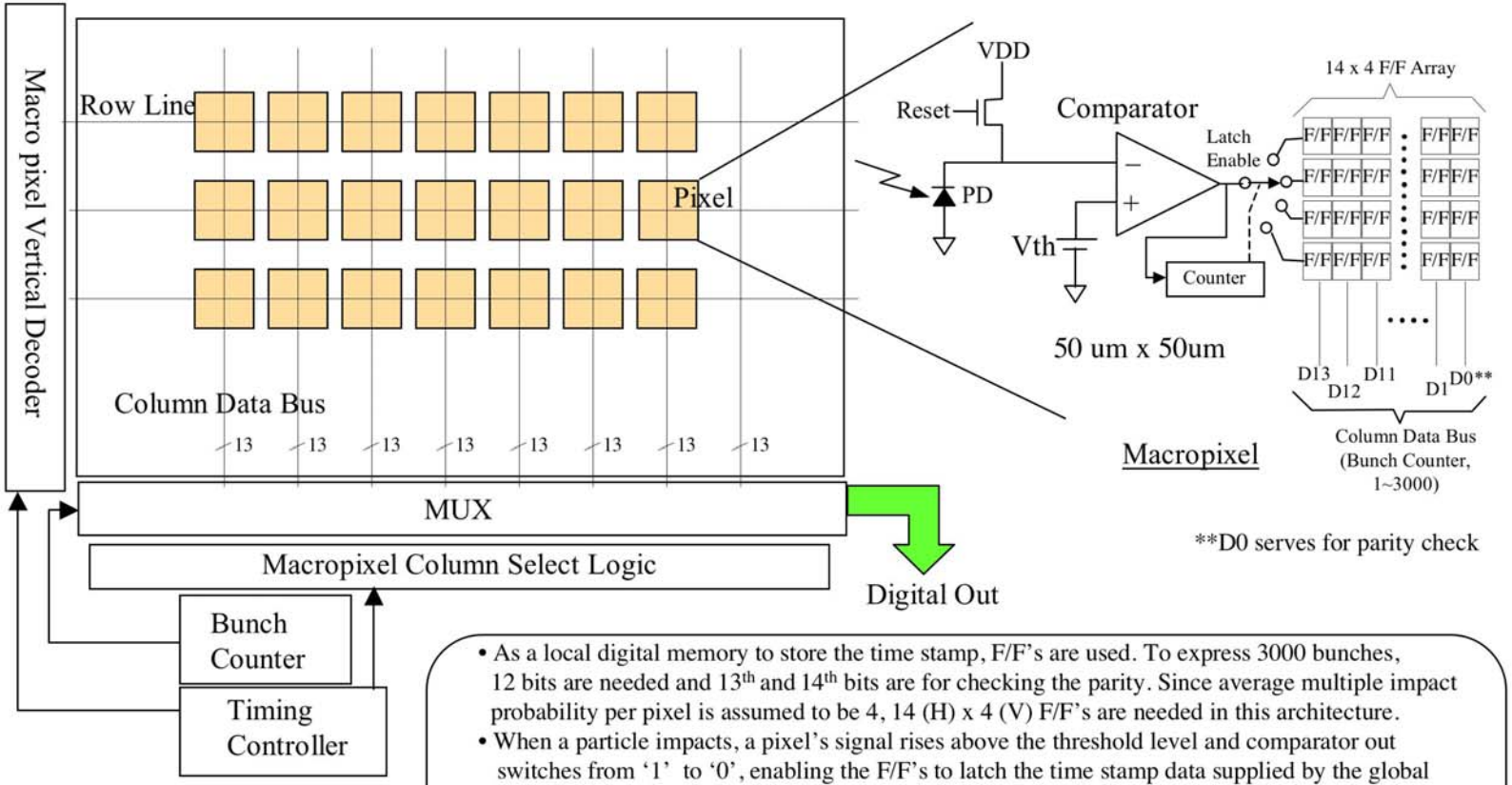
Table I: CMOS Detector Barrel Configuration

Layer	Radius (cm)	Total Length (cm)	No. of Chips	Chip Size (cm^2)
1	1.4	12.5	12	12.5×1.2
2	2.5	12.5	24	12.5×1.2
3	3.6	12.5	20	12.5×2.2
4	4.8	12.5	20	12.5×2.2
5	6.0	12.5	24	12.5×2.2

Table II: CMOS Detector Forward Disk Configuration

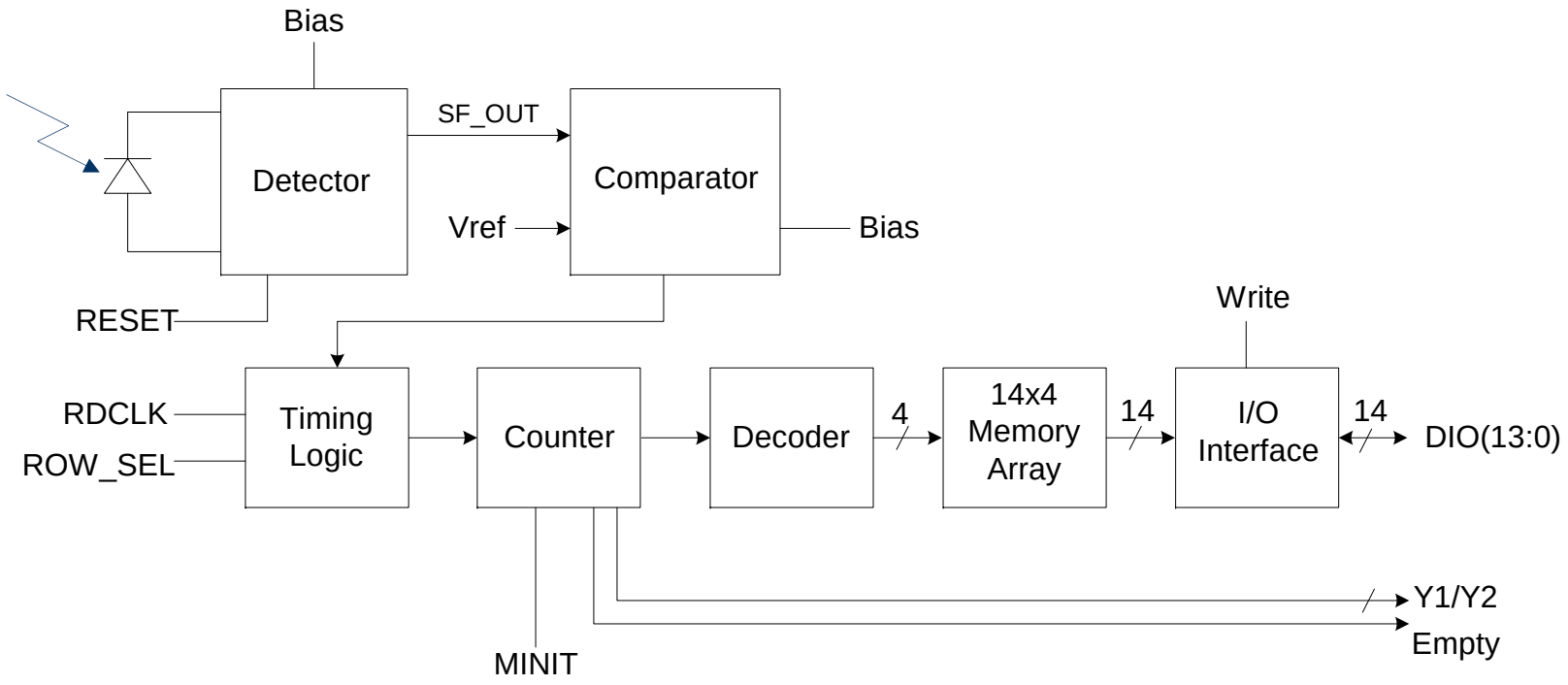
Annulus	Inner Radius (cm)	Z (cm)	No. of Chips	Chip Size (cm^2)
1	1.6	7.6	24	1.5×0.9
	3.1	7.6	24	4.4×2.2
2	1.6	9.5	24	1.5×0.9
	3.1	9.5	24	4.4×2.2
3	2.0	12.5	24	1.1×0.9
	3.1	125	24	4.4×2.2
4	2.0	18.0	24	1.1×0.9
	3.1	18.0	24	4.4×2.2

Macropixel Array Architecture



- As a local digital memory to store the time stamp, F/F's are used. To express 3000 bunches, 12 bits are needed and 13th and 14th bits are for checking the parity. Since average multiple impact probability per pixel is assumed to be 4, 14 (H) x 4 (V) F/F's are needed in this architecture.
- When a particle impacts, a pixel's signal rises above the threshold level and comparator out switches from '1' to '0', enabling the F/F's to latch the time stamp data supplied by the global bunch counter. When the data is latched, the pixel is reset.
- If next particle impacts the same location, comparator out enables next set of F/F's to preserve the previous time stamp data. This is implemented using a counter which increments the row address of the F/F array.
- Time stamp information is read out in the random access mode from the pixels of interest which stored nonzero time stamp data.

Macropixel Block Diagram



Read Noise

- Minimum ionizing particle leaves ~ 88e^- /micron in epitaxial layer
  - **15 um** thick epi layer 1% inefficiency threshold – 375 e^-, 50% hit sharing – 188 e^-, noise = ¼ x 188 = 47 e^-
- Readout noise scales with pixel capacitance: with 12 µm depletion depth it is 22 fF for 50x50 µm pixels and 3.5 fF for 20x20 µm pixels.
- Electronics noise estimation for 3.5 fF – 32 e^-

Power Consumption

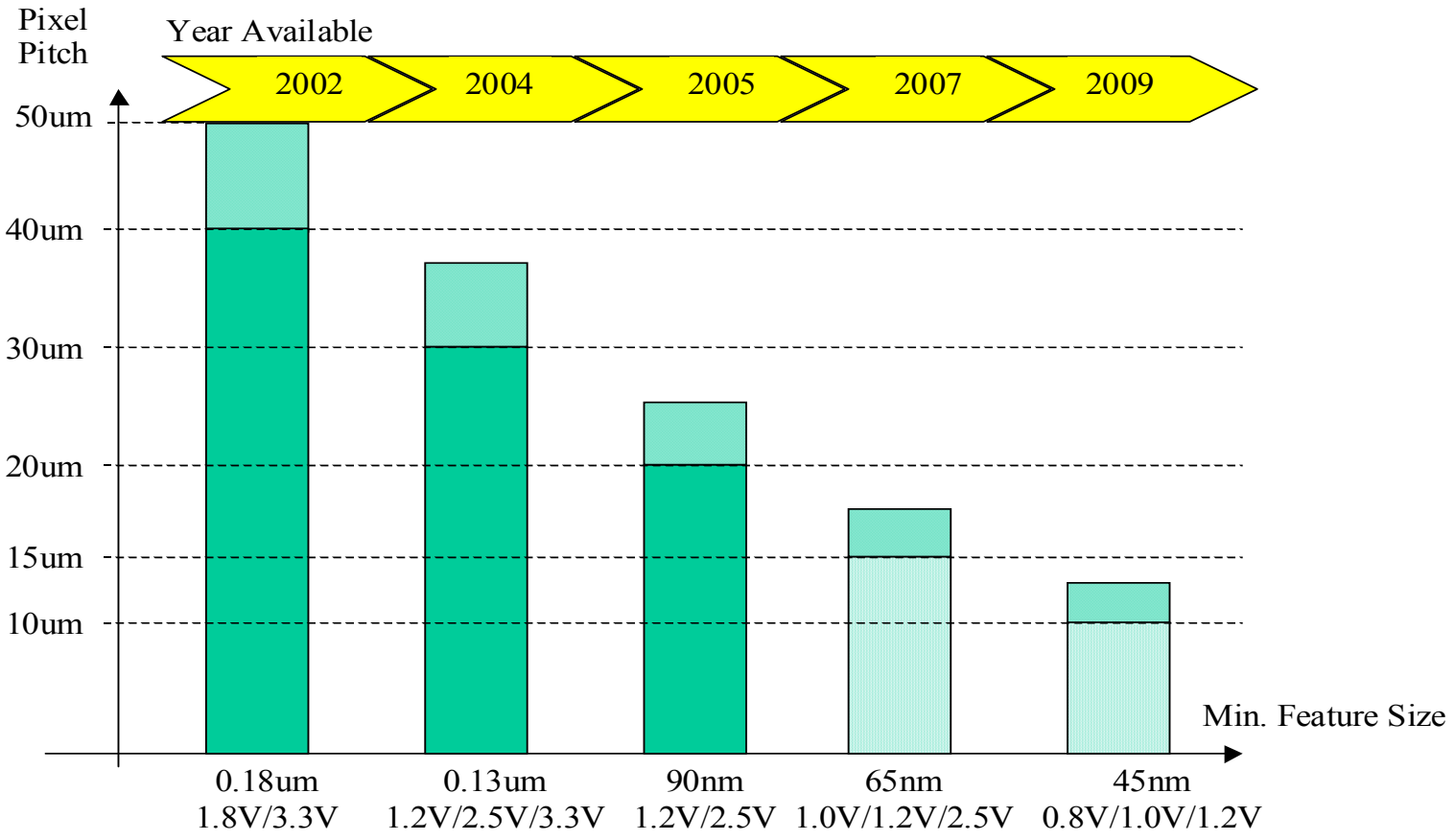
- Main power consumer is analog part (amplifier + comparator). However, we do not need to keep it all time on. Current estimation for 50x50 μm design (0.25 μm technology) 15mW/mm^2 (without taking into account duty cycle) for analog part and 0.05 mW/mm^2 for digital part. Assuming duty cycle for analog parts as 1/100 we get ~0.16 mW/mm^2.
- By conservative estimates power per unit of device area will not change by going to smaller pixel size with more advanced technology (goal – 0.045μm feature size by 2010). This is because reduction in capacitance allows smaller current in amplifier.
- So, we expect ~ 0.16mW/mm^2 x 2500 mm^2 chip = 0.4 W / chip.

Power Dissipation Analysis

	Component	Optimized Power Dissipation	Before Optimization
Analog	Detector	9.9uW	11.7uW
	Comparator	27.0uW	35.1uW
	Sub_total	36.9uW	46.8uW
Digital	Timing Logic	0.05uW	
	Counter/Decoder	0.07uW	
	Mem. Array	~ 0uW	
	IO Interface	0.01uW	
	Sub_total	0.13uW	
	Total	37.03uW	

SARNOFF Response to Question on Future

Technology Roadmap: Macropixel size estimation vs. Mixed-signal Process Technologies



CONCLUSION

- Completed chronopixel design
  - 645 transistors
  - Spice simulation verifies design
  - TSMC 0.18 um -> 40-50 um pixel
- Next phase under consideration
  - Complete design of macro pixel
  - Deliverable –tape out for foundry
- Future
  - Fab 50 um pixel chip
  - Then, 10-15 um pixel