Hadron Calorimeter Summary

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SiD Workshop, SLAC

October 2006

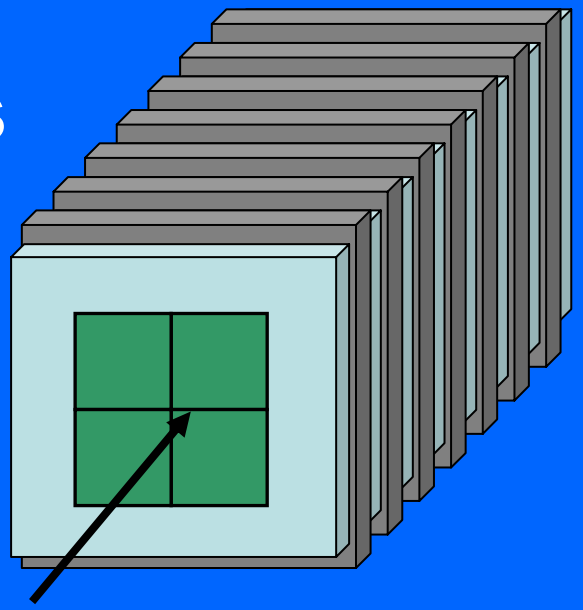
Overview

- Digital HCal (GEM, RPC) status, plans.

- Analog/Scintillator HCal/TCMT/SiPM status and plans.

[Note: Simulation studies to follow in PFA talk]

Slice test: RPCs and GEMs



Uses the 40 DCAL ASICs from the 2nd prototype run

Equip ~8 chambers with 4 DCAL chips each

256 channels/chamber
~2000 channels total

Order additional DCAL ASICs to equip GEM prototypes

Chambers interleaved with 20 mm copper - steel absorber plates

Electronic readout system (almost) identical to the one of the prototype section

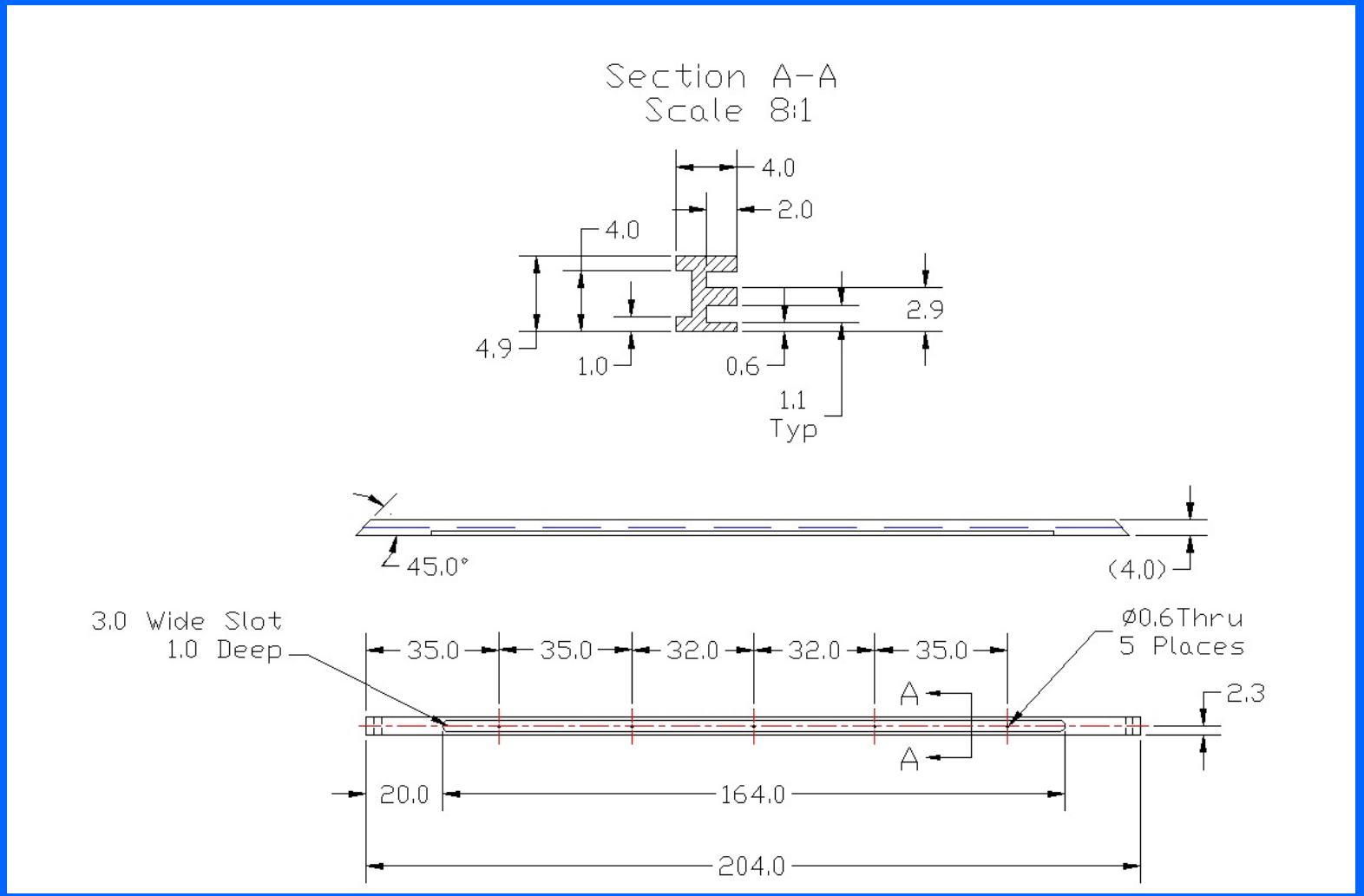
Tests in MTBF beam planned for March 2007

→ Measure efficiency, pad multiplicity, rate capability of individual chambers
→ Measure hadronic showers and compare to simulation

Validate RPC/GEM approach to calorimetry

Validate concept of electronic readout

Mechanical: RPC design

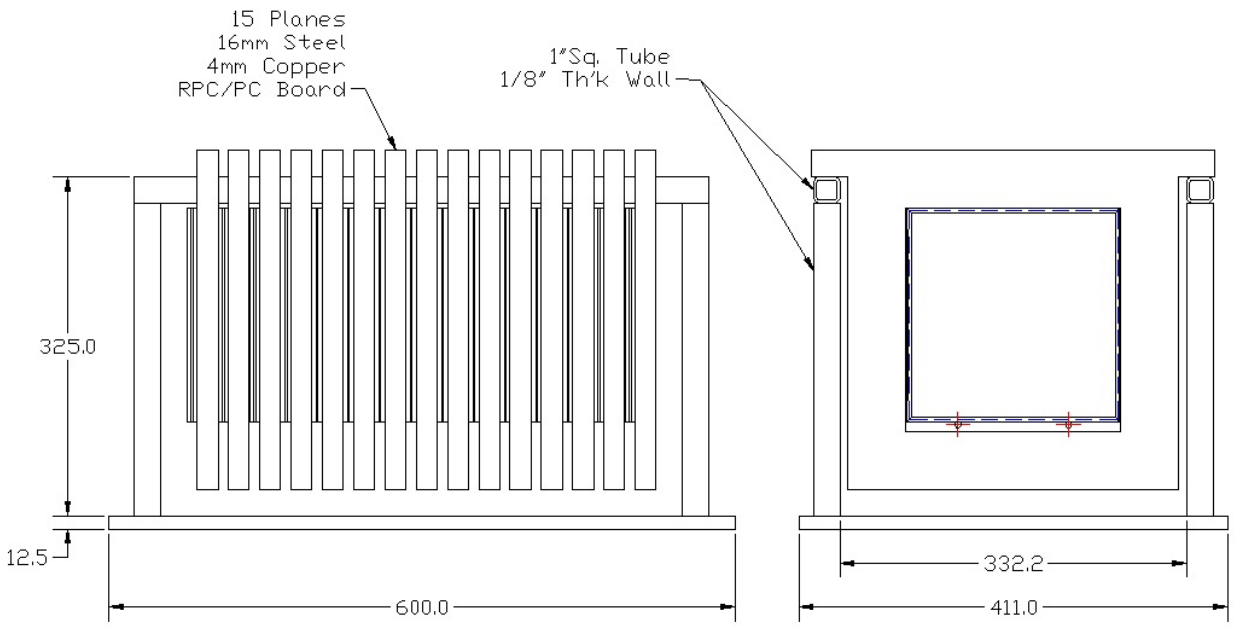


All chambers: channels, resistive paint, glass in hand

1st chamber → being assembled

V Guarino (ANL)

Mechanical: Stack



Design accommodates 20 x 20 cm^2 RPCs as well as 30 x 30 cm^2 GEMs
All parts in hand, stack will be assembled shortly

Electronic Readout System for Prototype Section

40 layers à 1 m² → 400,000 readout channels

More than all of DØ in Run I

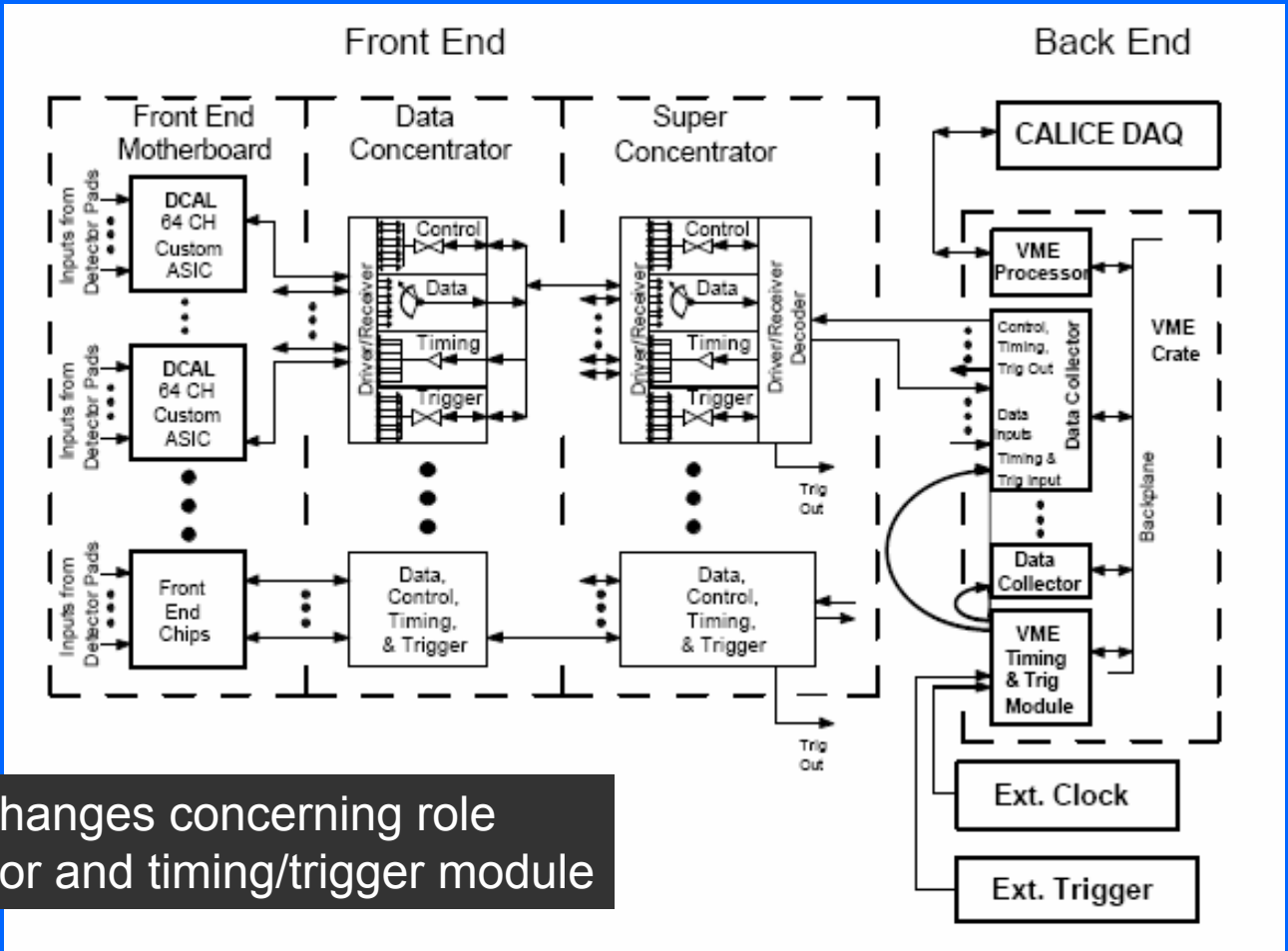
I Front-end ASIC and motherboard

II Data concentrator

III Super Concentrator

IV VME data collection

V Trigger and timing system

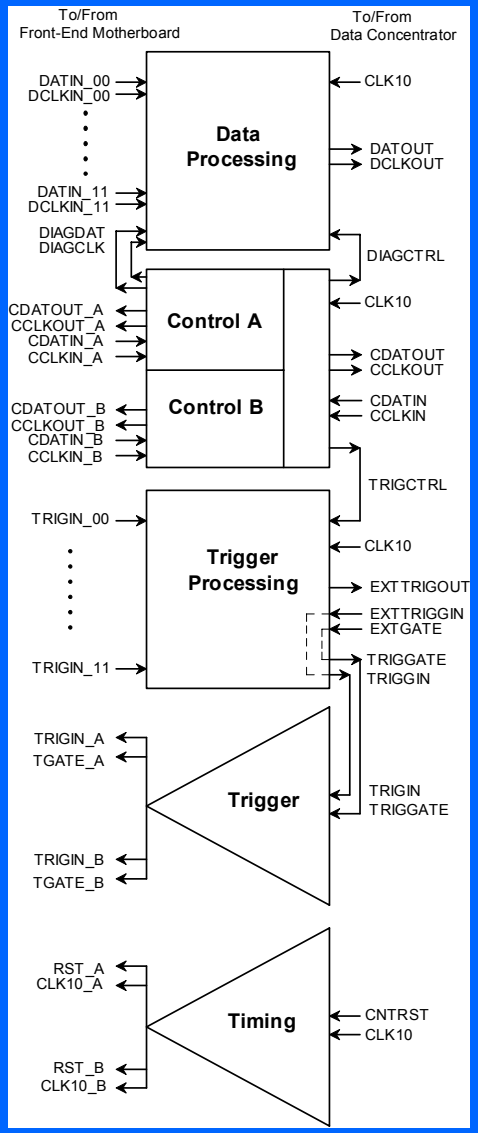


Some recent changes concerning role of data collector and timing/trigger module

G Drake (ANL)

Data concentrator boards

Functionality defined
Protocol to data collector defined
Being designed

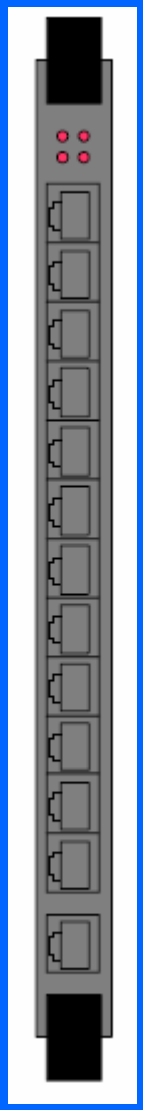


Timing and trigger module

Functionality defined
Possibly to be designed by Chicago

Data collector boards

E Hazen (Boston)



Three options considered

- **Re-use of CRC boards (CALICE)**

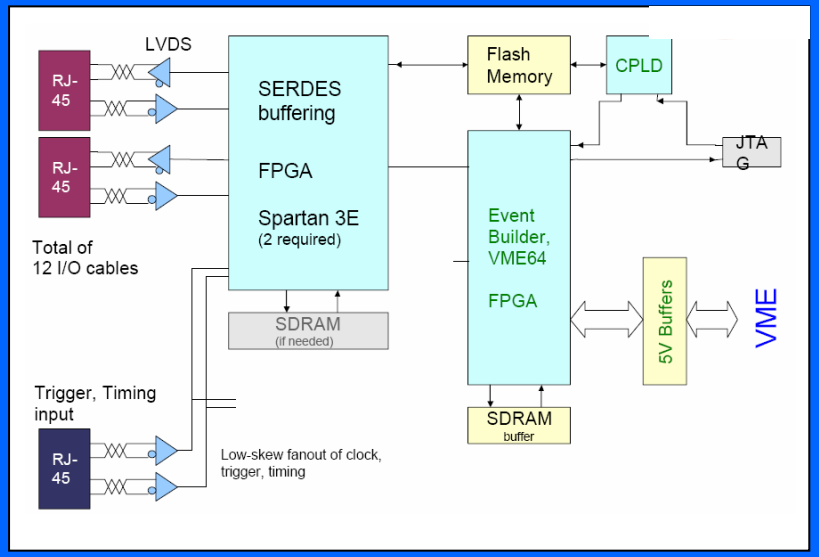
  Difficult to obtain
  Not matched to our application (trigger)
  Not considered anymore

- **Re-use of CMS boards (Boston)**

  Possible, but many drawbacks (availability)
  Costly (~ $70k for prototype section)
  Main advantage: could be ready in 3 months

- **New design**

  Not much more expensive (~$80k for prototype section)
  (~$60k for slice test)
  Will be exactly what we want
  Time needed ~ 6 months



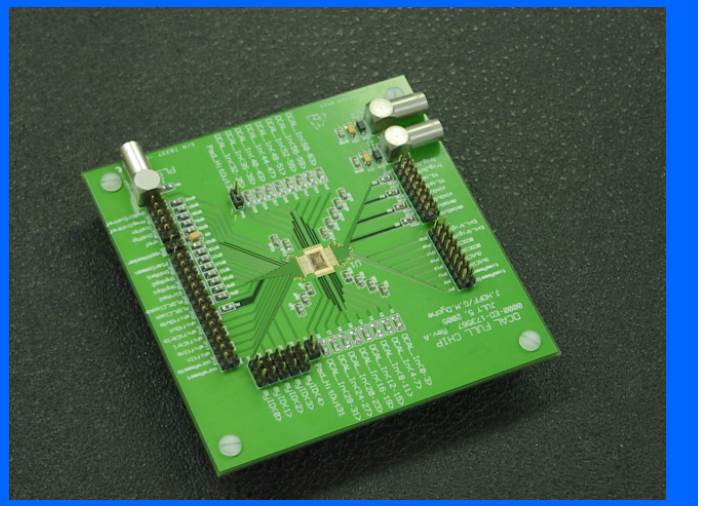
Decided to go for new design
→ contribution of Boston University
Interface meeting on September 22nd
Design work started

DCAL chip

G Drake (ANL)

1st version

→ extensively tested with computer controlled interface
→ all functions performed as expected



Redesign

→ decrease of gain by factor 20 (GEMs) or 100 (RPCs)
→ decoupling of clocks (readout and front-end)

2nd version

→ submitted on July 22nd
→ 40 chips (packaged) in hand

Test board

→ redesign of test board (changes in pin layout etc.) complete
→ boards fabricated
→ chip mounted on test board

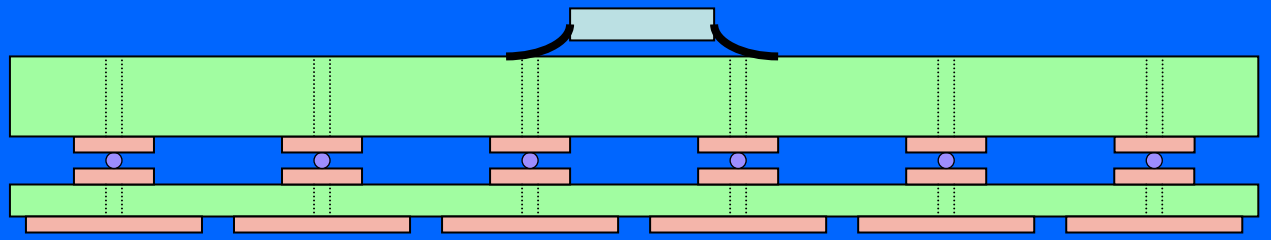
Testing (2/40)

→ all software written
→ unless serious problems: tests complete by mid-November

G Drake (ANL)

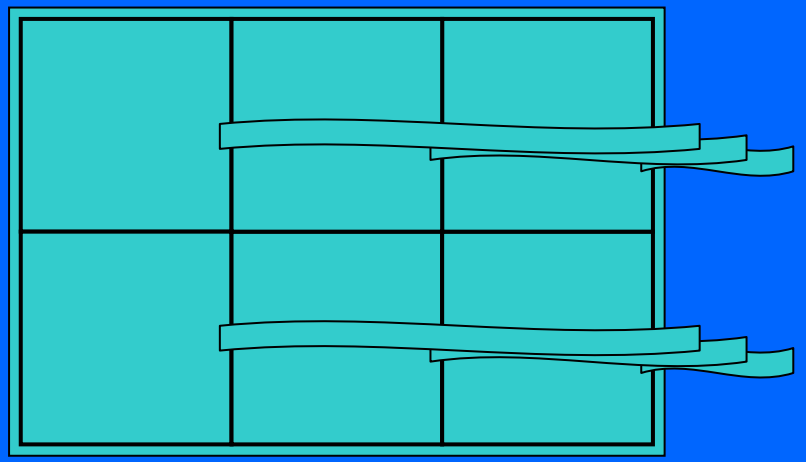
Pad and front-end boards

New concept



Pad boards

two-layer board containing pads
can be sized as big as necessary
cheap and simple
conductive epoxy to fill vias



Front-end boards

multi-layer board
16 x 16 cm^2
contain all transfer lines, houses DCAL chip
expensive (blind and buried vias) and tough to design

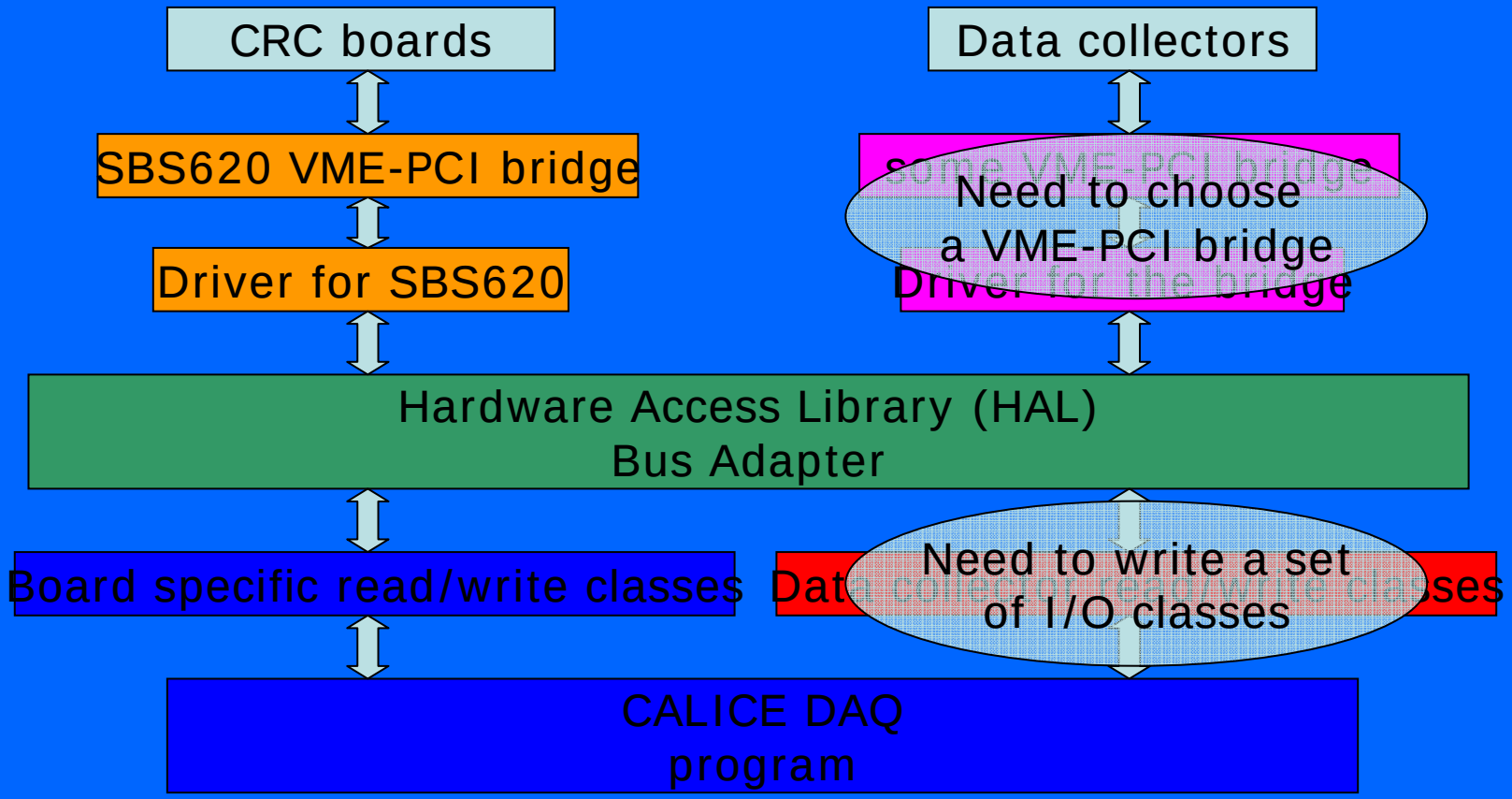
Connections

board to board with conductive glue on each pad (being tested)
cables for connection to data concentrators

Prototypes of pad boards expected by next week

DAQ software

Particular challenge to be compatible with CALICE software



CALICE **Slice test**

Will acquire SBS618 VME-PCI bridge next week

Beam telescope, HV, and gas

Beam telescope J Li, A White, J Yu (UTA)

6 counters (3 x (1 x 1 cm^2) + 1 x (4 x 4 cm^2) + 2 x (19 x 19 cm^2)
Mounted on rigid structure
In production

HV modules E Norbeck (Iowa)

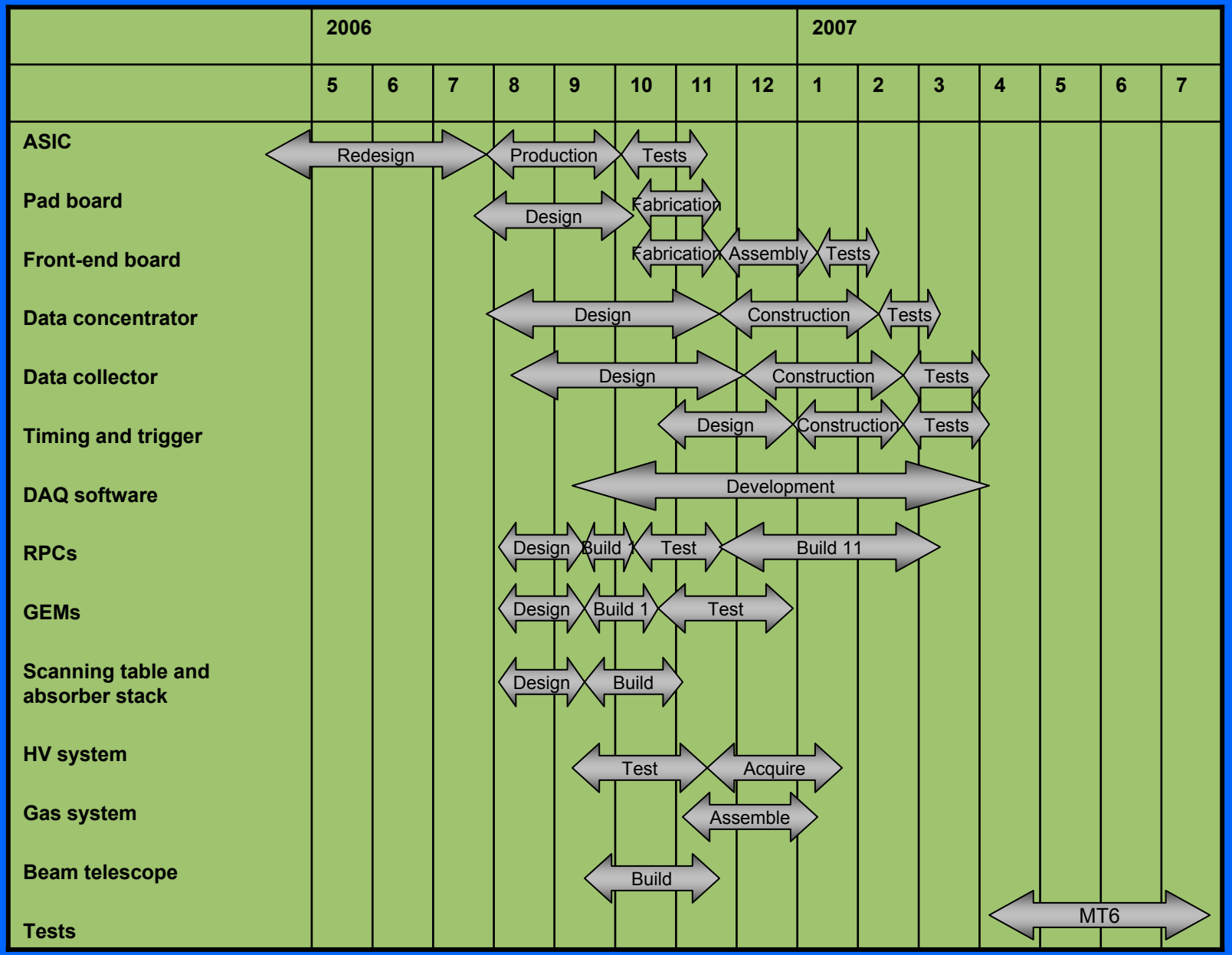
Need separate supplies for each chamber
Modules (from FNAL pool) being tested

With additional RC-filter perform similarly to our Bertran unit in analog tests (RABBIT system)
Still need to perform tests with digital readout

Gas system E Norbeck (Iowa)

Need manifold for 10 chambers (in hand! Thanks to D Northacker)
Need approval for gas tanks (safety issue)

Time scales


2006
2007
5
6
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11
12
1
2
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5
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ASIC
Redesign
Production
Tests
Pad board
Design
Fabrication
Front-end board
Fabrication
Assembly
Tests
Data concentrator
Design
Construction
Tests
Data collector
Design
Construction
Tests
Timing and trigger
Design
Construction
Tests
DAQ software
Development
RPCs
Design
Build 1
Test
Build 11
GEMs
Design
Build 1
Test
Scanning table and absorber stack
Design
Build
HV system
Test
Acquire
Gas system
Assemble
Beam telescope
Build
Tests
MT6

1 m^3 Prototype Section

Costs and Funding

A) Slice test is funded by LCDRD06, LDRD06 and ANL-HEP, and Fermilab funds

B) Prototype section not yet funded, but…

Stack	Item	Cost	Contingency	Total
RPC stack	**M&S**	607,200	194,600	801,800
	Labor	243,075	99,625	342,700
	Total	**850,275**	**294,225**	**1,144,500**
GEM stack*	**M&S**	400,000	165,000	565,000
* Reusing most of the RPC electronics	**Labor**	280,460	40,700	321,160
	Total	**680,460**	**205,700**	**886,160**
Both stacks	**M&S**	1007,200	359,600	1366,800
	Labor	523,535	140,325	663,860
	Total	**1,530,735**	**499,925**	**2,030,660**

Proposal for supplemental funds for $500k/year over two years submitted to DOE
Help from ANL (LDRD), ANL-HEP, FNAL expected…

Funding

LCRD funds for 2006

RPCs (ANL, Boston, Chicago, Iowa)	$98k
GEMs (UTA, Washington)	$60k

Supplemental LCRD funds for 2006/7

Available funds $1,200k/year?

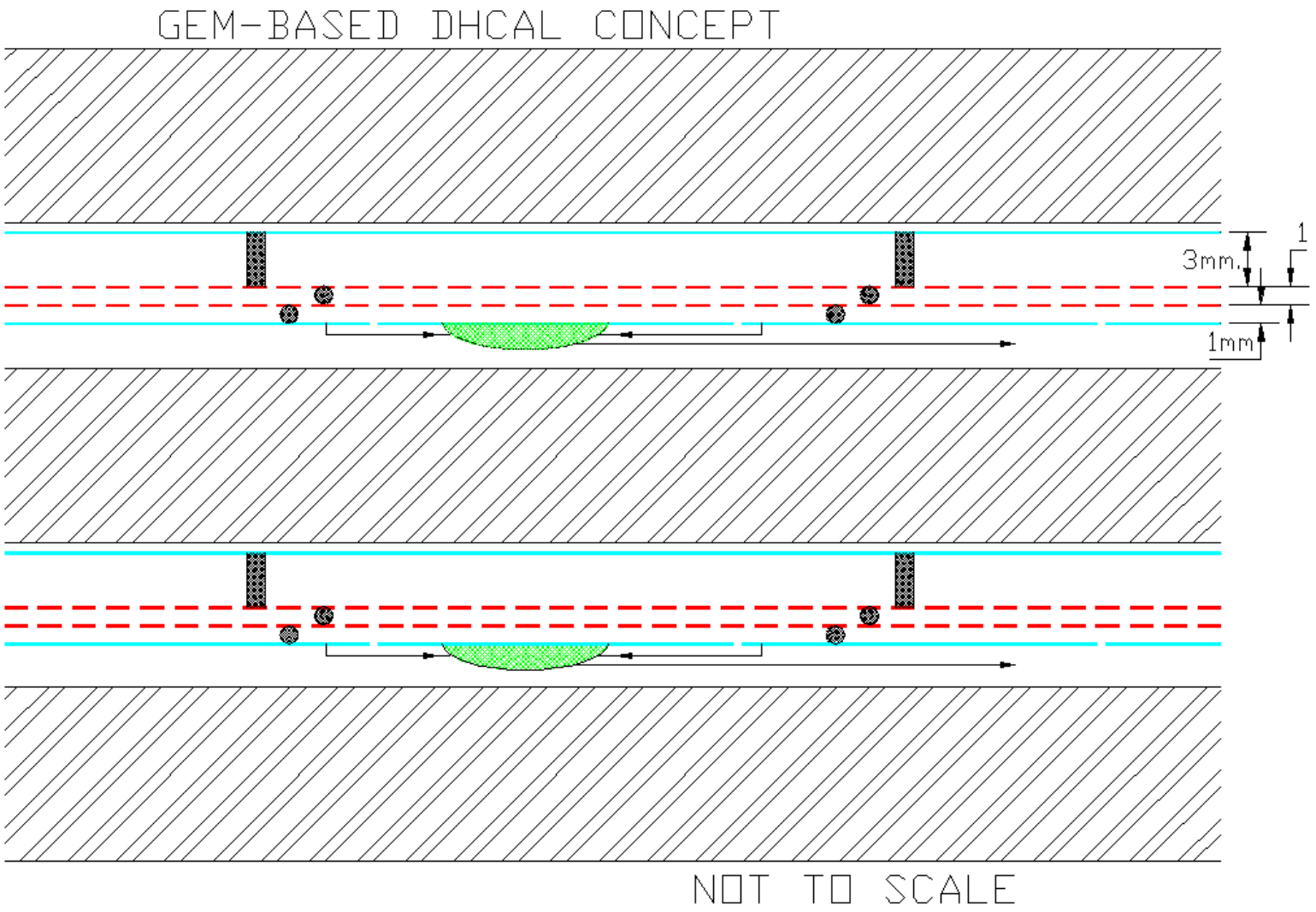
Submitted pre-proposal for RPC/GEM DHCAL

Requested $1,200k for 2006
~$800k for 2007

2006	build RPC-DHCAL continue R&D on GEMs
2007	test RPC-DHCAL at MTBF build GEM stack
2008	test GEM-stack

DOE asked us to submit proposal for $500k/year (done)

GEM-based Digital Calorimeter Concept



GEM Foils from 3M

- 30cm x 30cm foils made with three types of coating:

  a) bare copper

  b) "organic polymer" coating

  c) gold plating

- HV tests made on all three types -> conclusion is that we prefer to use the uncoated foils.

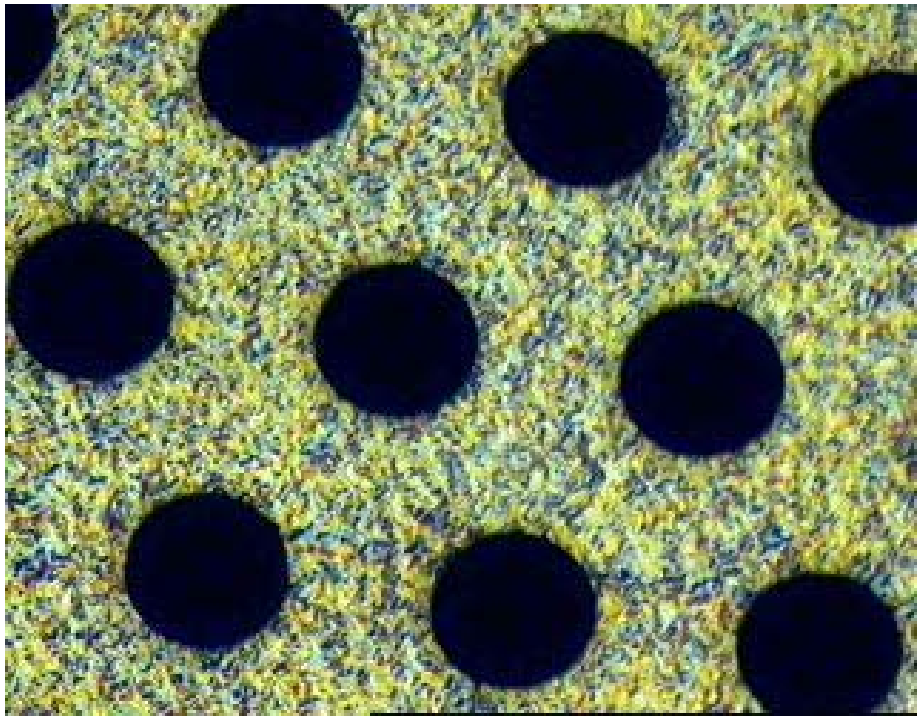
- We are using the uncoated foils in our current 30cm x 30cm chambers.

3M 30cm x 30cm GEM foils

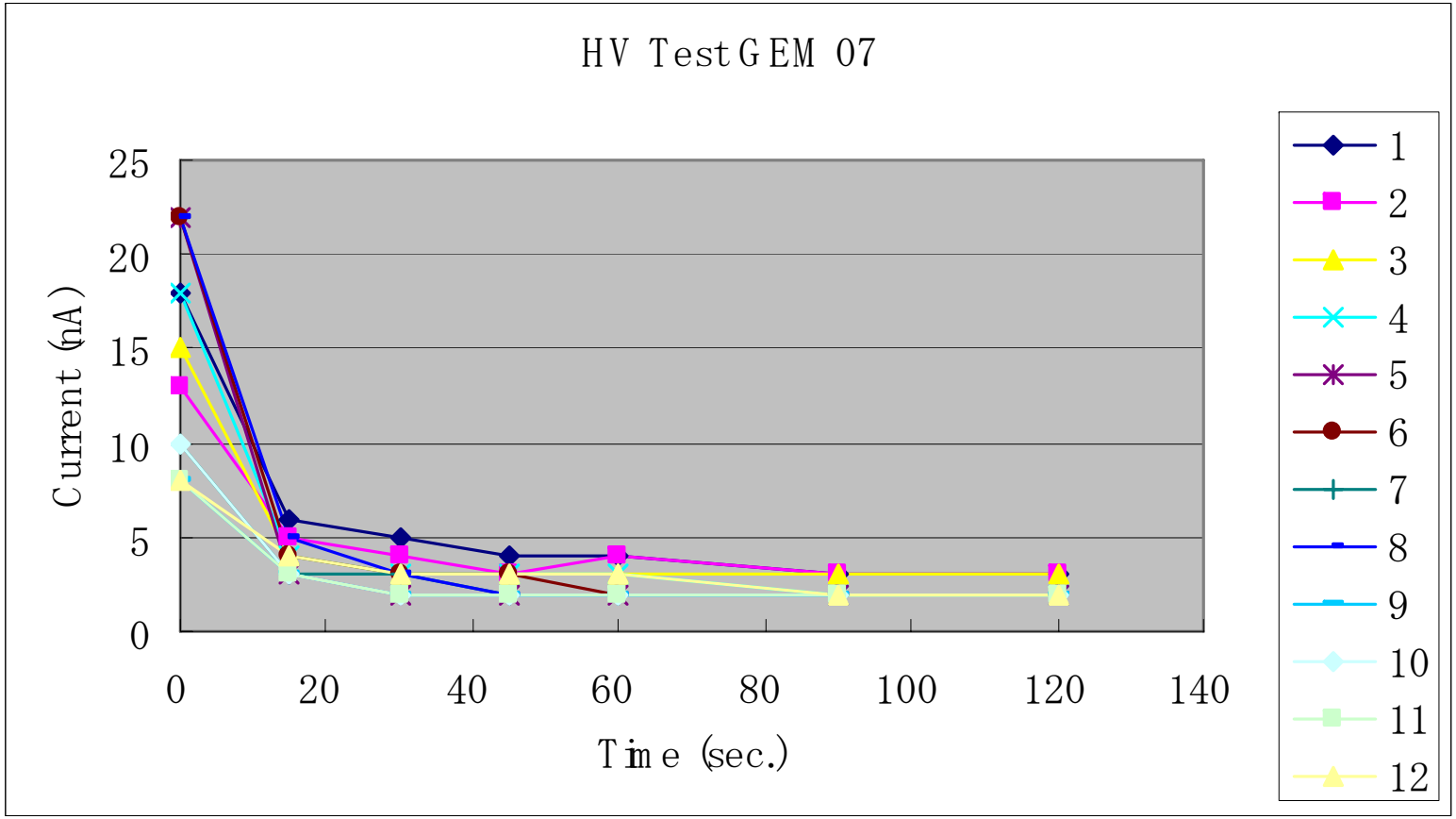
12 HV sectors on one side of each foil.

HV Sector Boundary

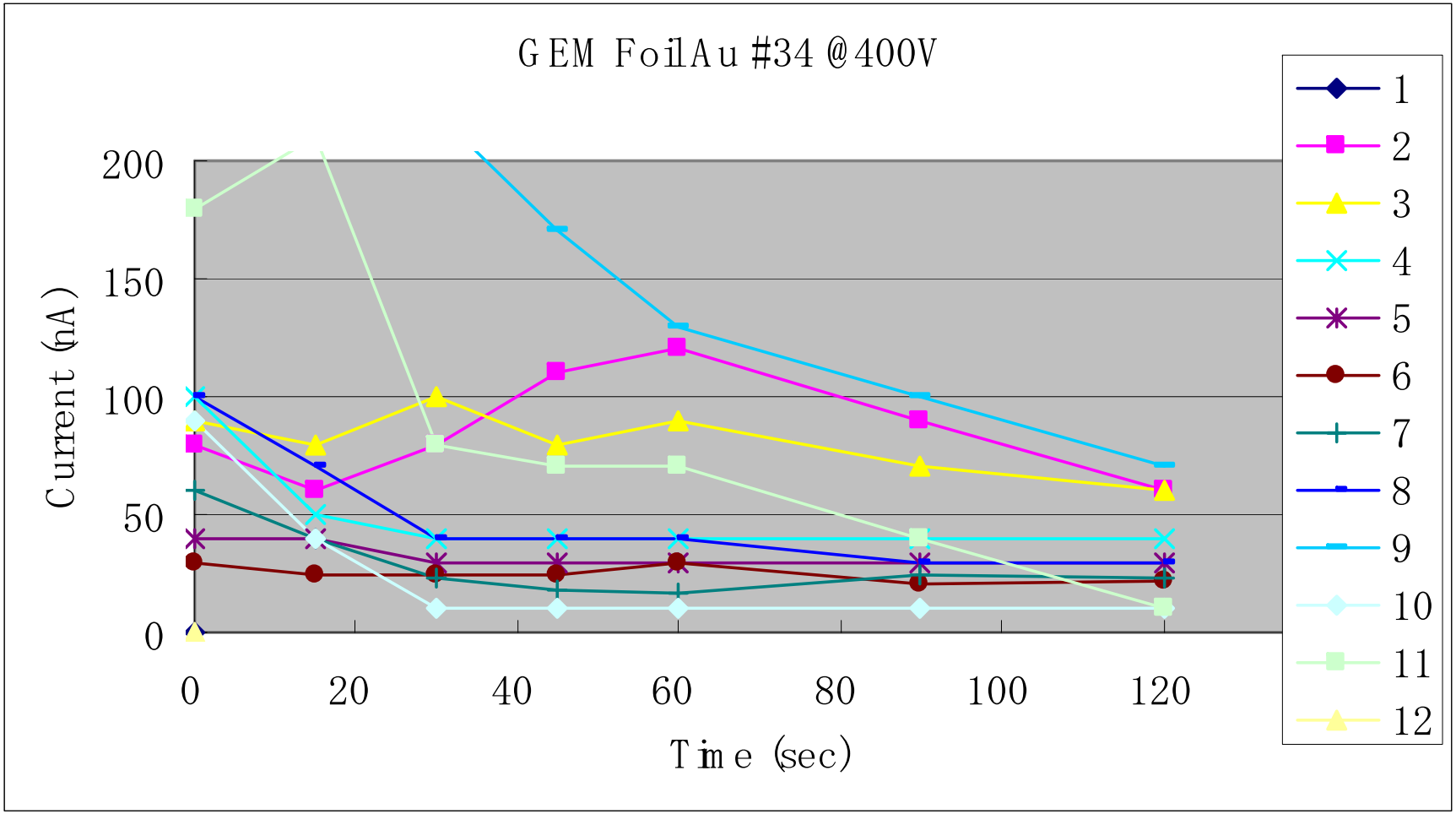
Magnified section of a 3M GEM foil.



HV tests on uncoated GEM foil



GEM Au #34


GEM FoilAu #34 @400V
Current (nA)
200
150
100
50
0
0
20
40
60
80
100
120
Time (sec)
1
2
3
4
5
6
7
8
9
10
11
12

3M Long (90cm) GEM Foil Design

-3M has setup a formal internal project to develop larger foils for the $1m^3$ prototype stack (the $30x30cm^2$ foil development did not require 3M process modification).

- Reusing the artwork (masks) from the 30cm x 30cm foil development.

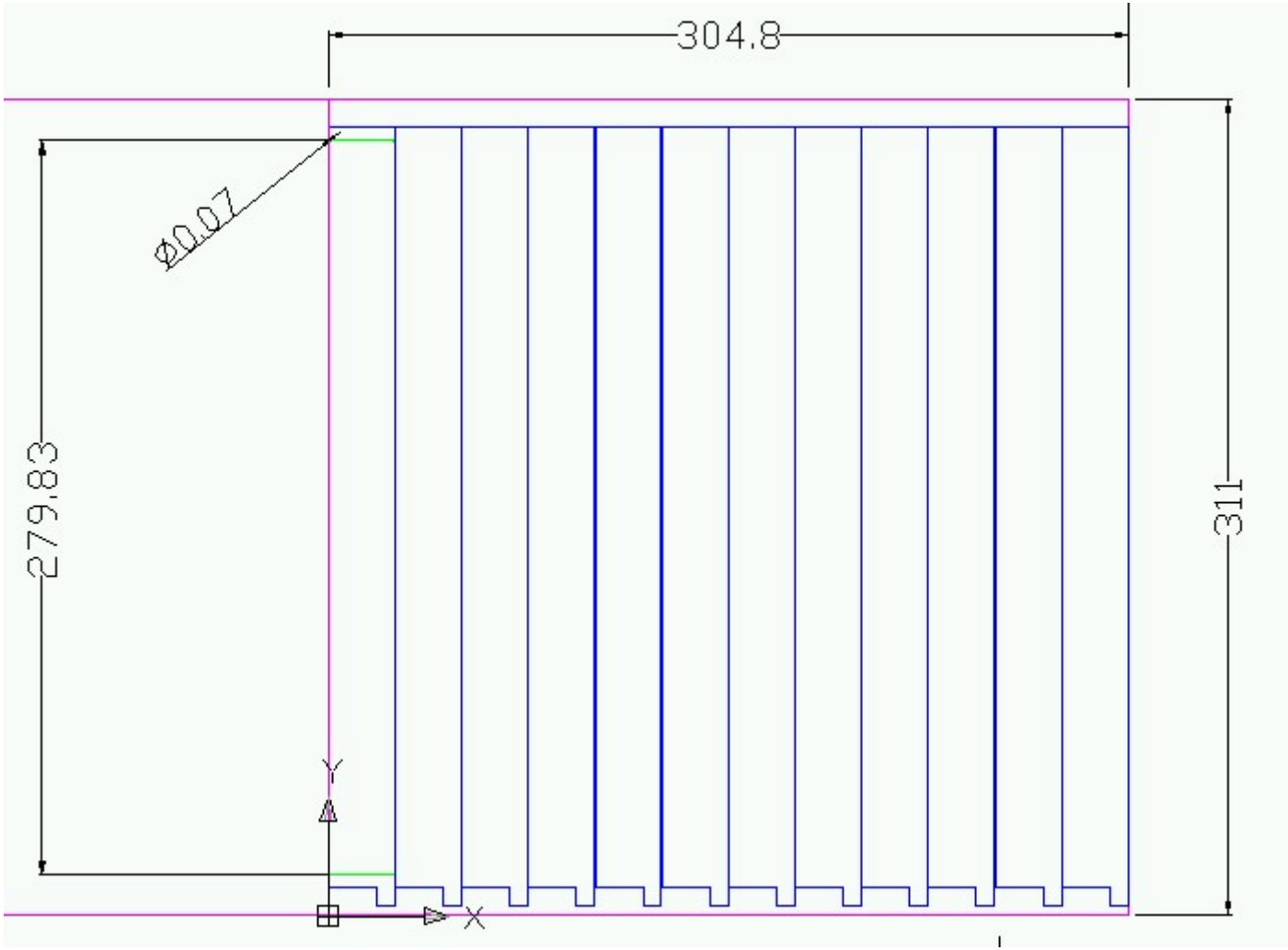
- Small area needed for re-registration foil moves through etching station.

- Anticipate first samples in November '06.

- First long chamber construction will follow 30cm x 30cm chamber construction for Slice Test.

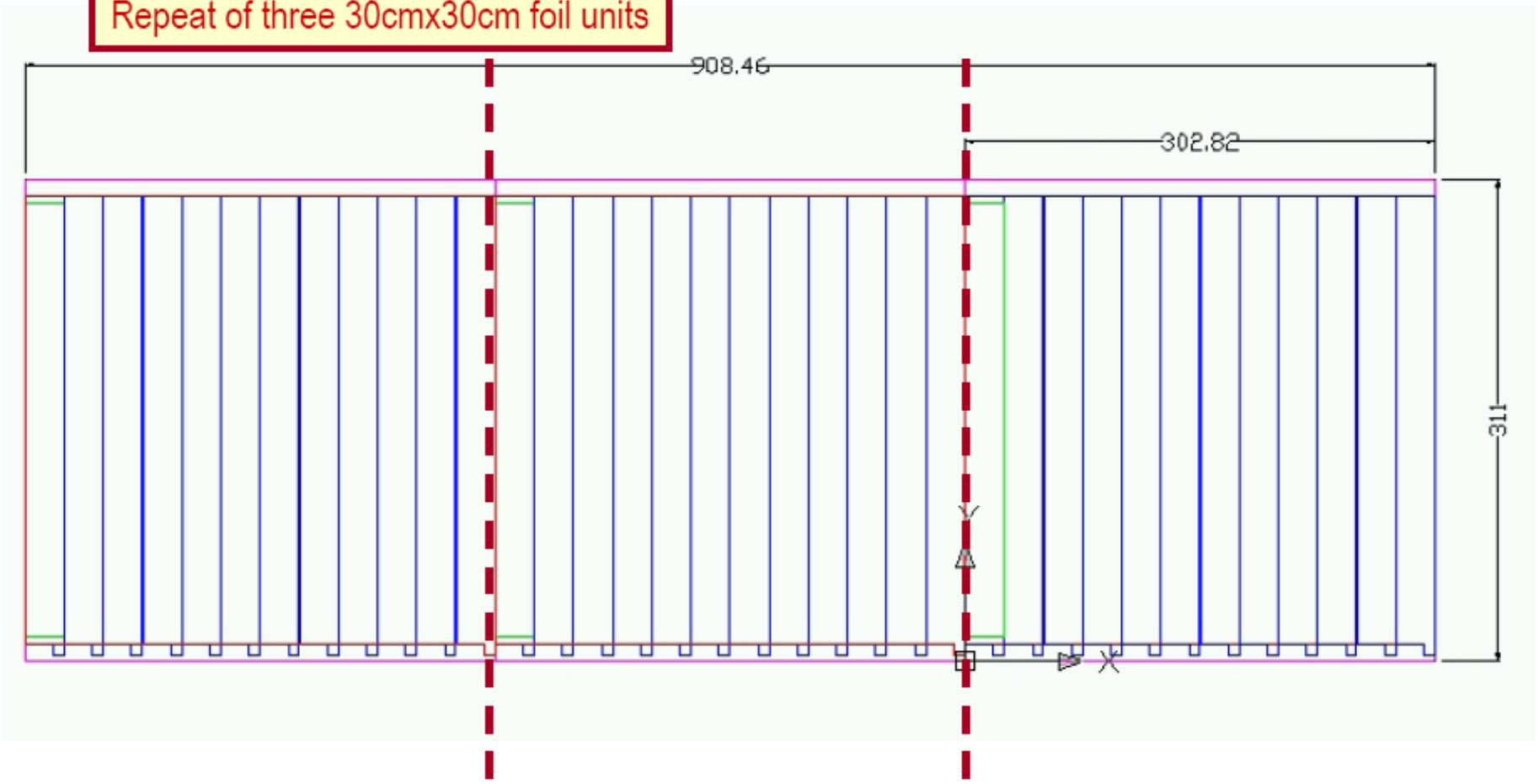
3M Long (90cm) GEM Foil Design

X3 Repeat for 90cm foil



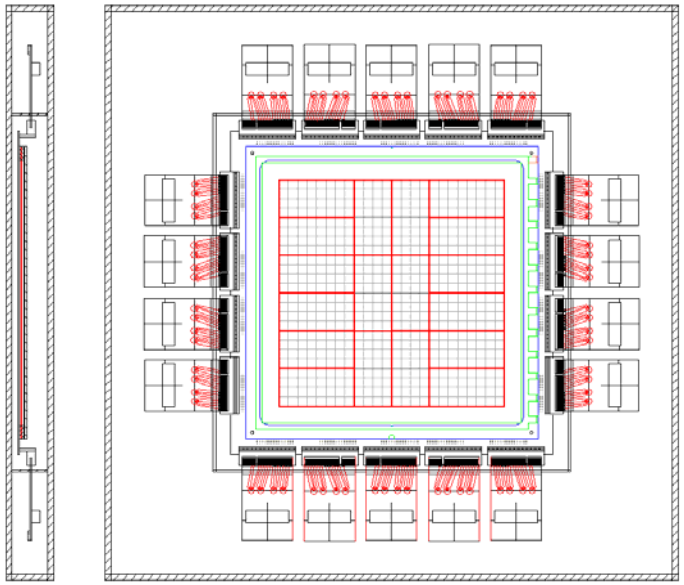
Proposed Initial 3M 30cmx100cm Foil Design

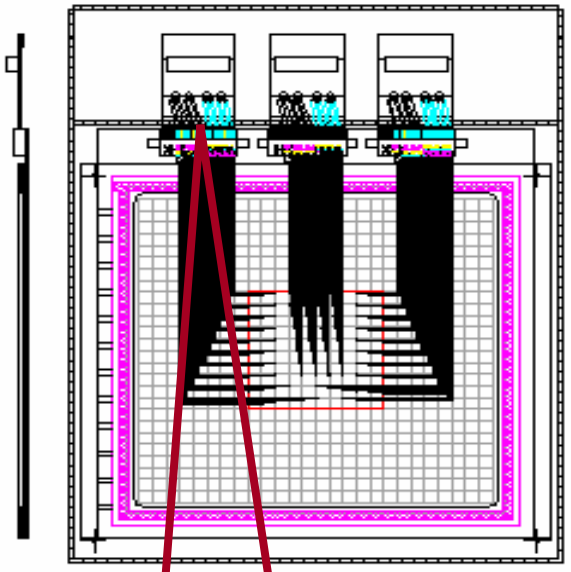
Repeat of three 30cmx30cm foil units



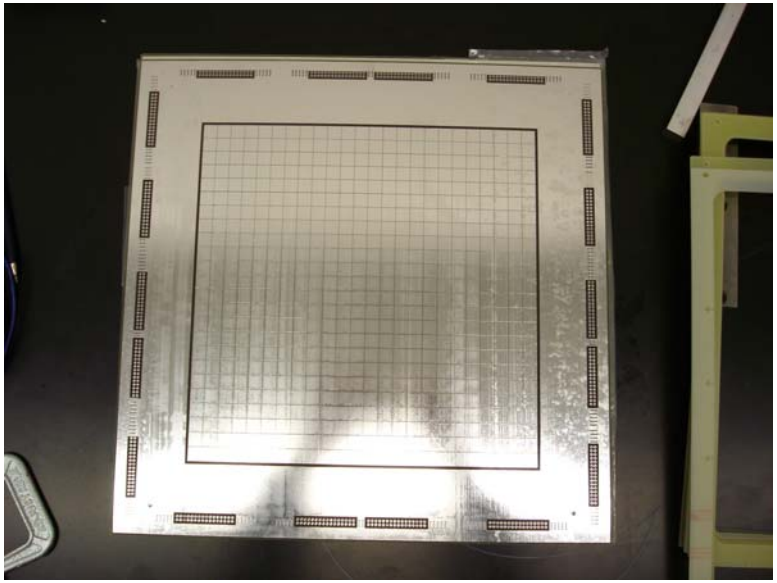
Can be produced in 6 weeks after the final specification

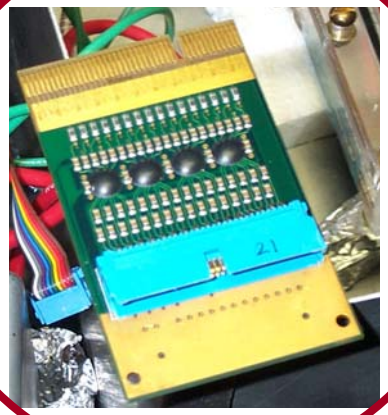
30cm x 30cm GEM chamber(s)





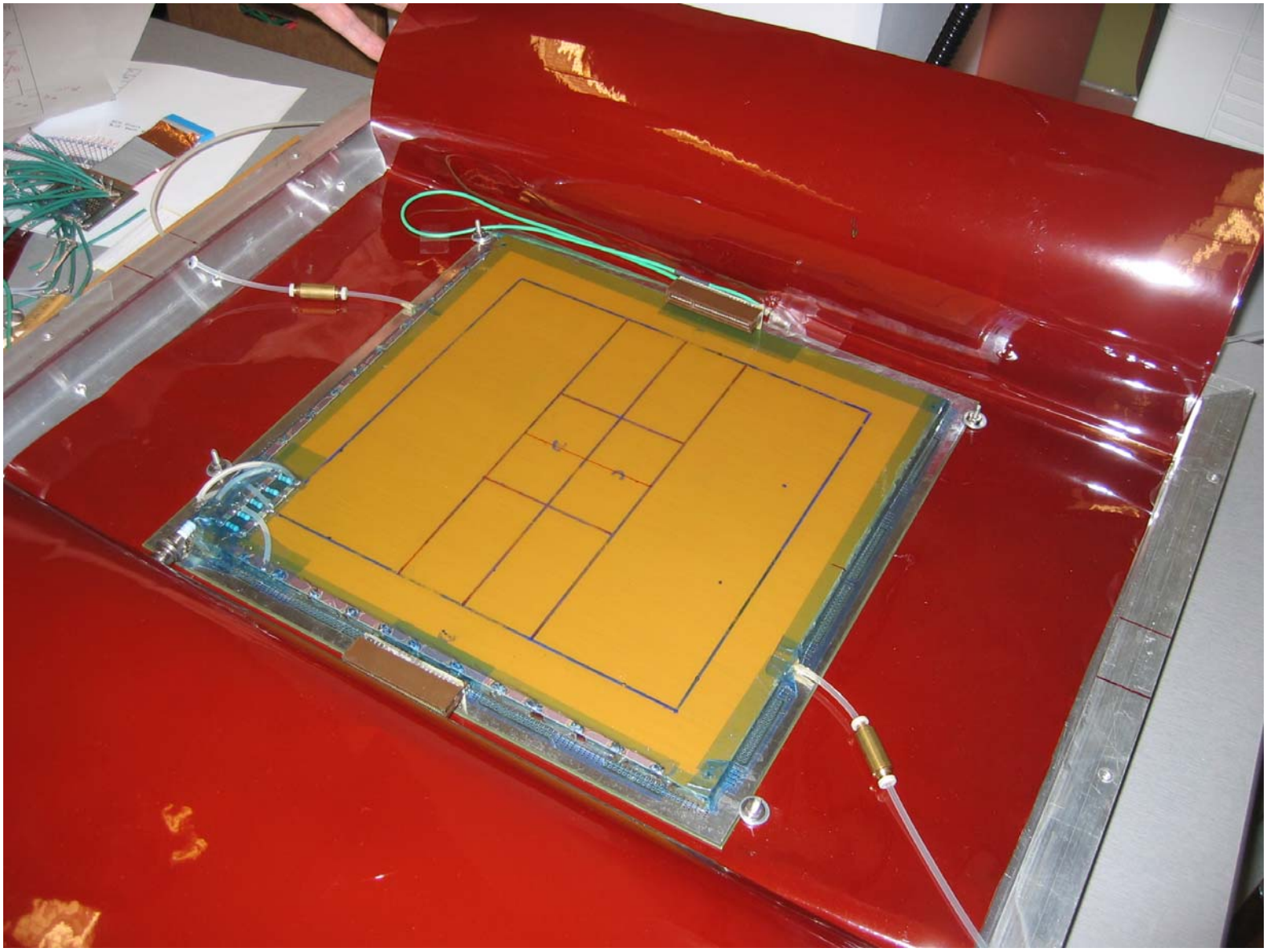
Anode boards designed to read 96 pads in the center





Use 32 channel FNAL preamps

30cm x 30cm GEM chamber



UTA GEM-DHCAL exposure

- 4-pad GEM area (2 x 2 pads) exposed to full beam

- Beam scans ~800mm x 50mm area every 2 sec, with 30ps pulse of 10^{10} e^-/pulse over a 5 cm^2 area, or ~10^9 e^-/sec on an anode pad.

- Total exposure ~2000sec

-> Estimate ~2 x 10^{12} e^-/pad (~ 1.6 x 10^{-2} mC/mm^2) and GEM chamber continued normal operation.

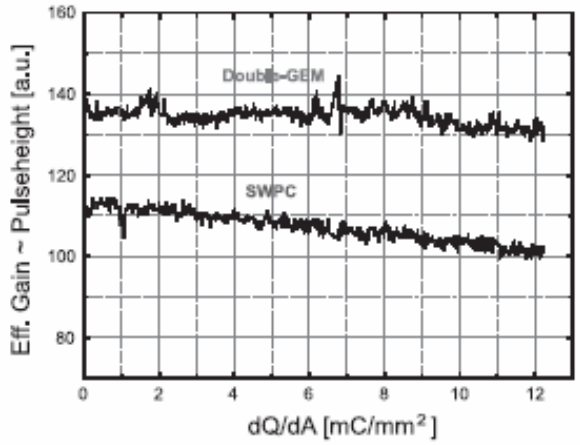


Fig. 3. Previous aging measurement of a double-GEM detector with Ar–CO_2 (70:30): effective gain versus accumulated charge dQ/dA.

- Much above total hits/10y/pad at ILC

- Much below any damage region for decrease in gain.

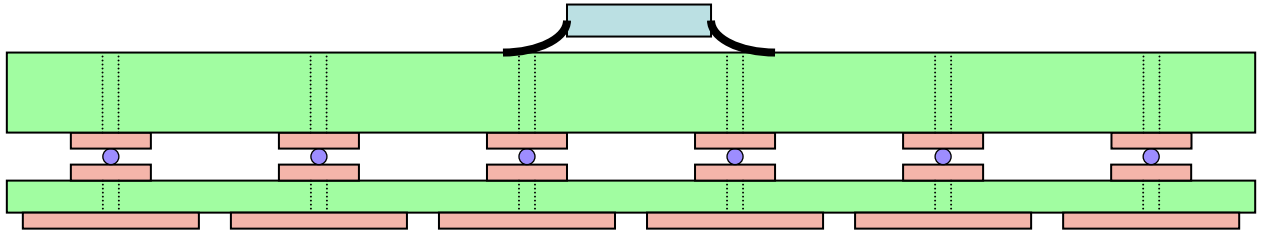
DCAL chip ANL/FNAL

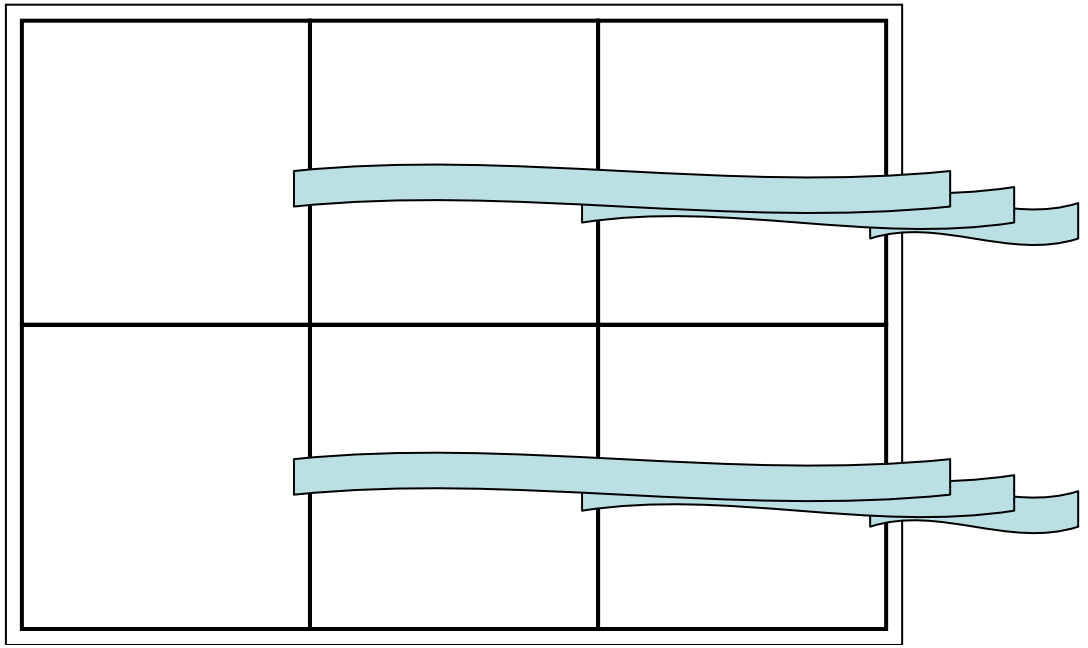
Digital hit output

RPC and GEM capabilities

GEM signals:

minimum signal ~10fC,
maximum signal ~few pC

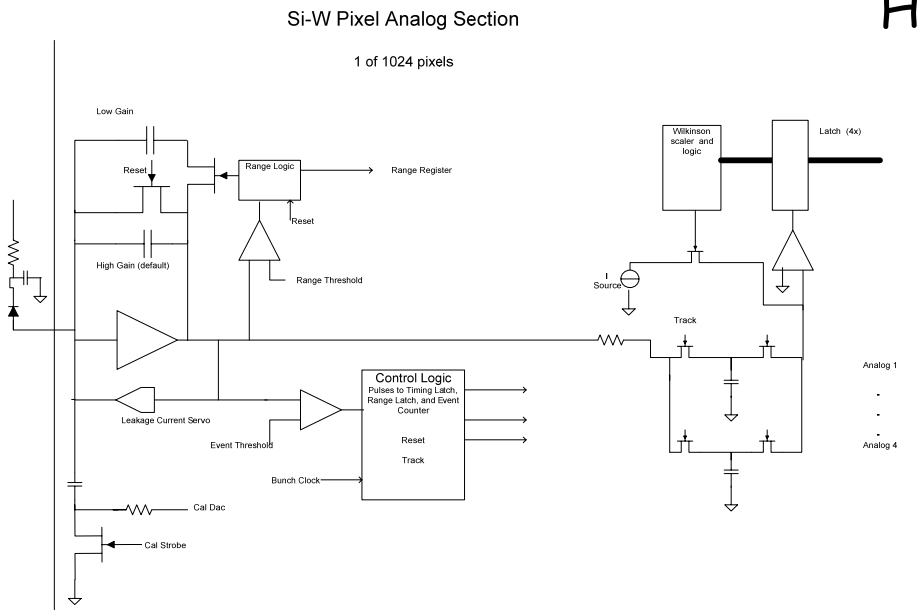


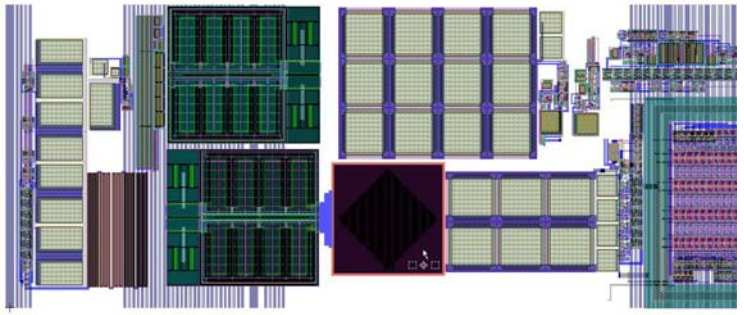


KPix Readout chip/SLAC

Analog output. Two gain ranges

High: 0 – 500fC, Low: 0 – 10pC



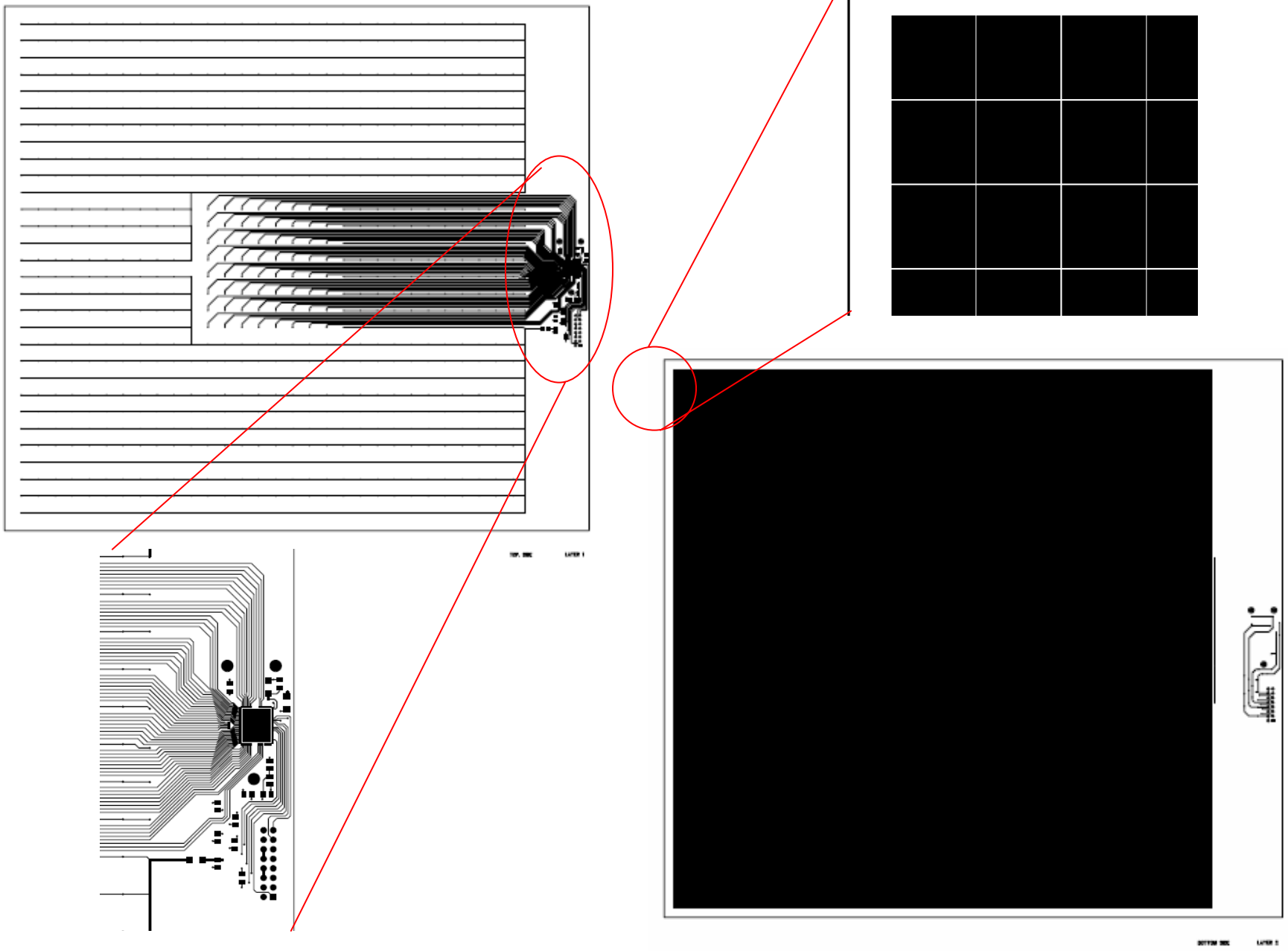


v3 – 64 channels – September 2006 (with GEM changes)

v4 – 64/128/1024 channels(??) end of 2006/early 2007?

KPix-GEM Pad+FEB with detail

M. Breidenbach/R. Herbst
SLAC



Schedule/budget for GEM-DHCAL

May 2006 – 30x30cm^2 chamber built, initial tests.

- low energy e^- beam tests in Korea.

Summer 2006 – built additional 30x30cm^2 chambers.

- work with ANL/SLAC on anode board designs.

Fall 2006 – Tests of GEM chambers with KPix, DCal chips as chips and boards become available.

- Build 2-3 chamber each for DCAL and KPix for Slice Test.

- build larger GEM chambers (~1m x 30cm) when 3M foils are available.

Early 2007 – Slice Test RPC and GEM chambers with DCAL and v3 KPix.

Scintillator/SiPM TCMT/HCal

Scintillator tiles read out via SiPM's is one of the technologies studied for the SiD HCal.

NIU has been working on this in the context of the CALICE Collaboration and applying the same technology to the proposed TCMT = Tail Catcher/Muon Tracker.

NOTE! All the CALICE HCAL/TCMT results here are preliminary!

The CALICE TCMT prototype

All 16 layers fully instrumented
(8 fine + 8 coarse)

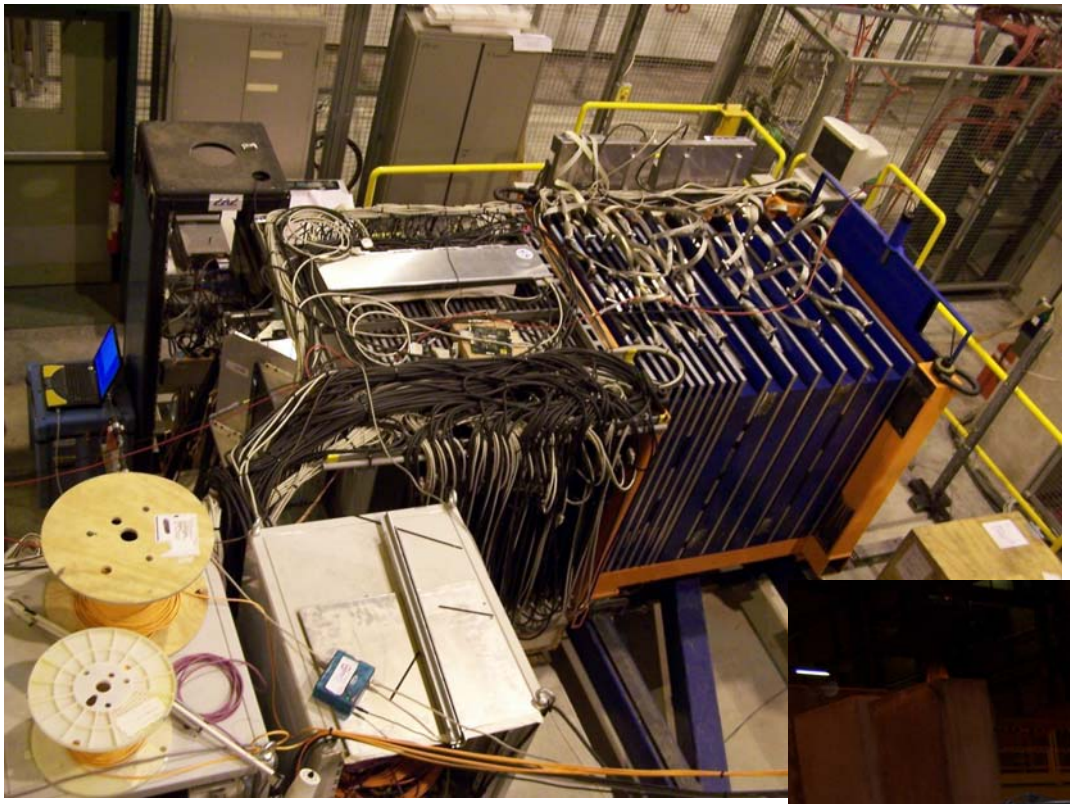
Alternate x,y orientations

Fine section (~ 2cm absorber)
Coarse section (~ 10cm absorber)

20 channels (strips) / cassette
Each strip is 100 x 5 x 0.5 cm^3,

beam

HCAL TCMT

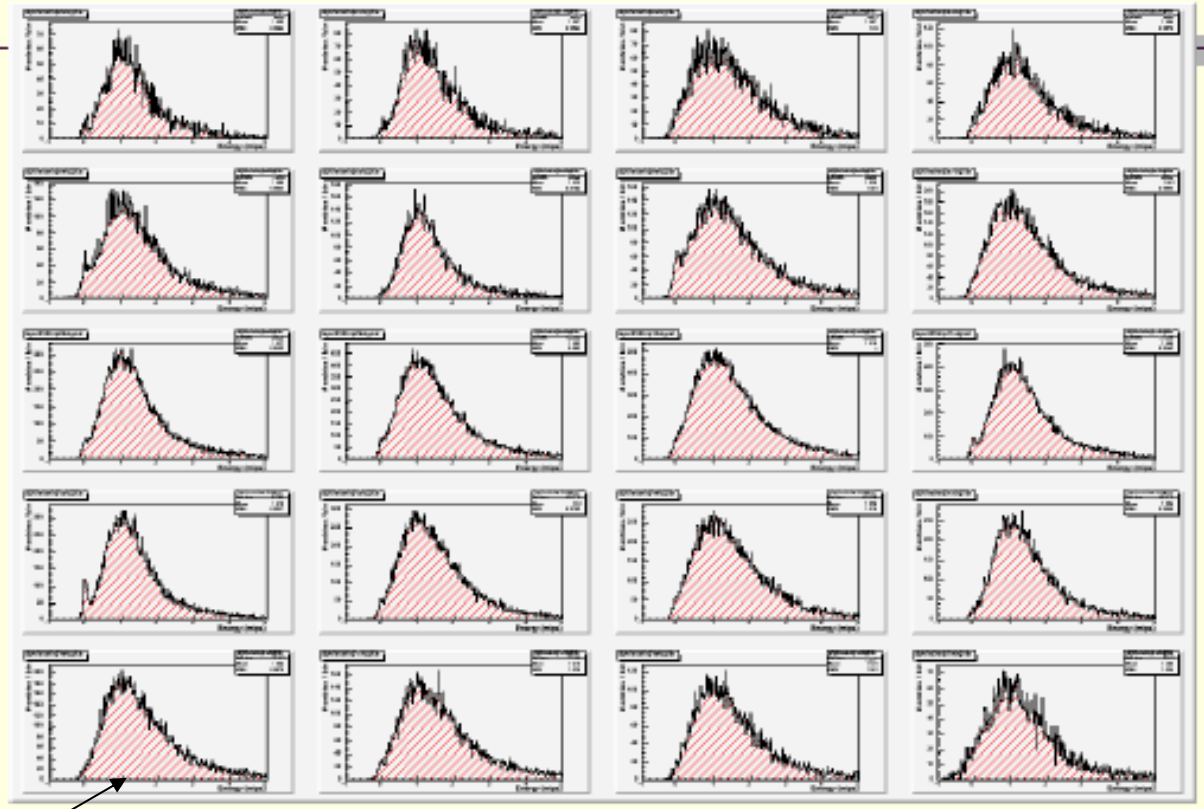


Scintillator/SiPM HCal

and

TCMT

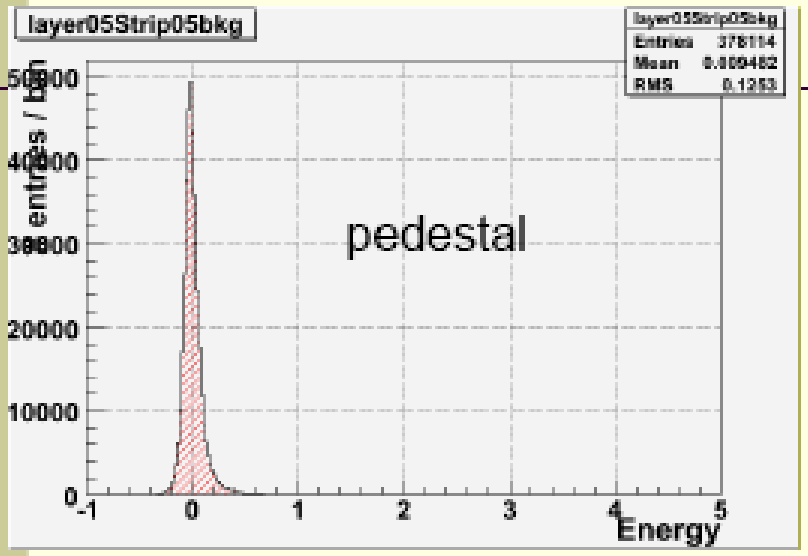
Layer 5: mips on each channel

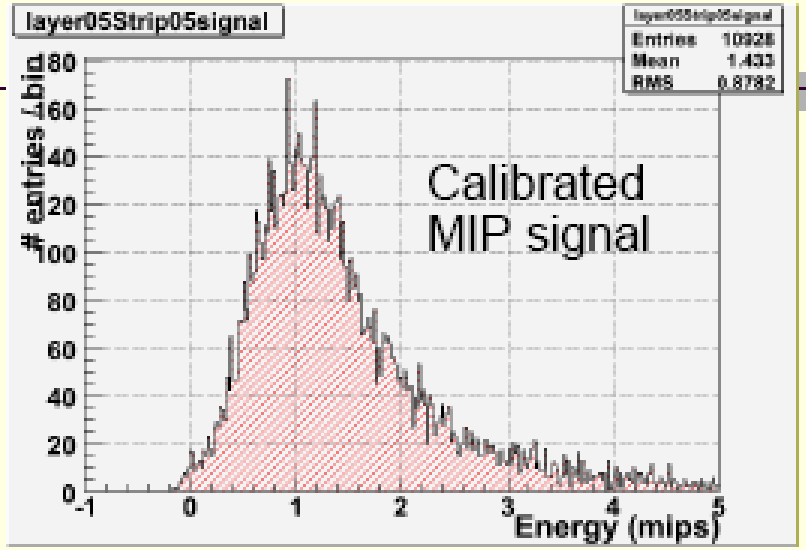


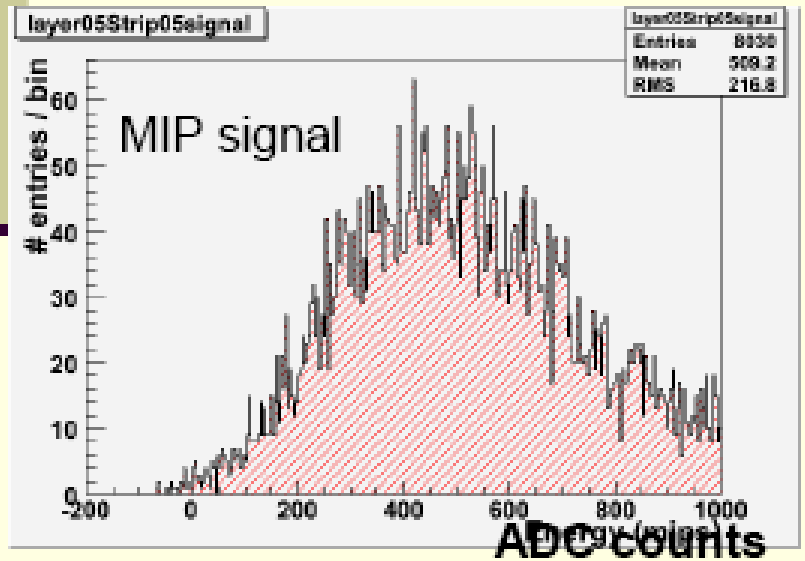
1 MIP

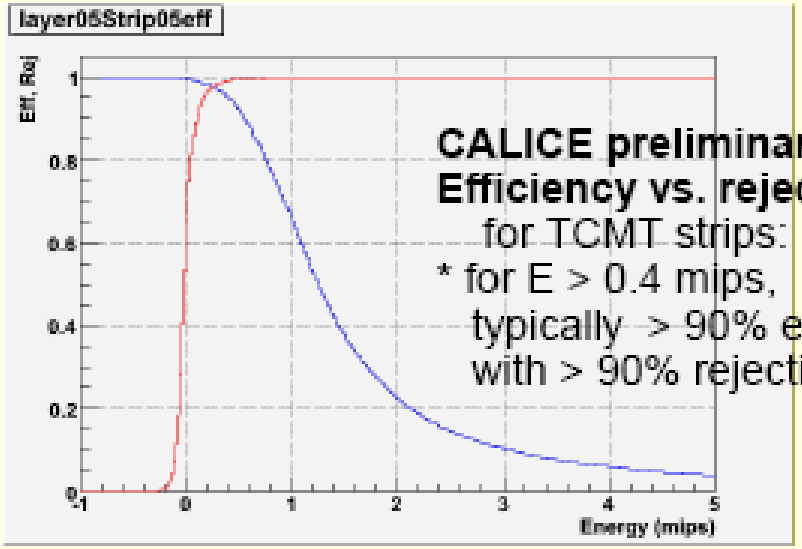
Calibrated hit energies in terms of E(MIP)

A closer look into a TCMT strip



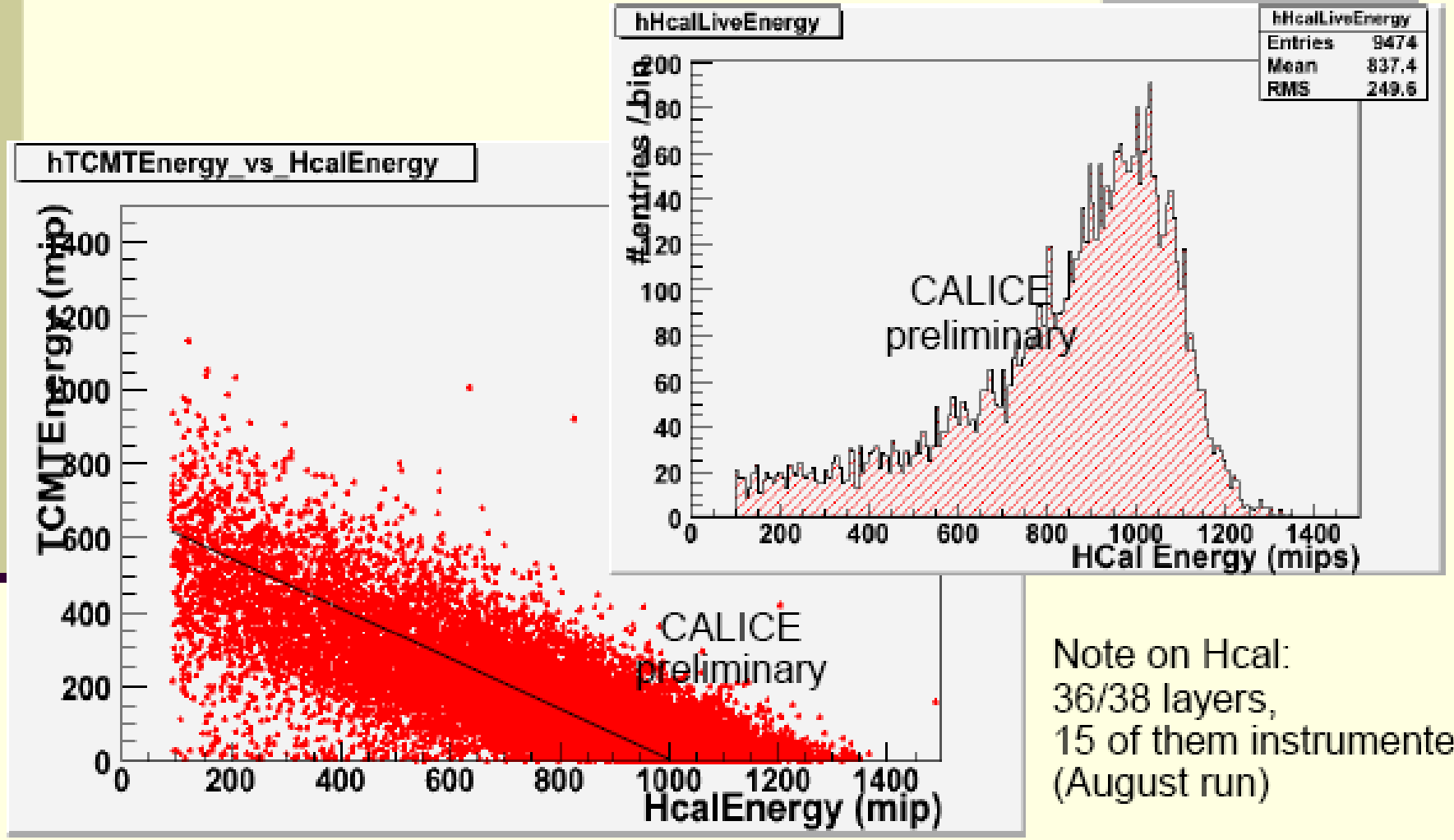






CALICE preliminary:
Efficiency vs. rejection
for TCMT strips:
* for E > 0.4 mips,
typically > 90% effic
with > 90% rejection

80 GeV pions: Hcal x TCMT correlation



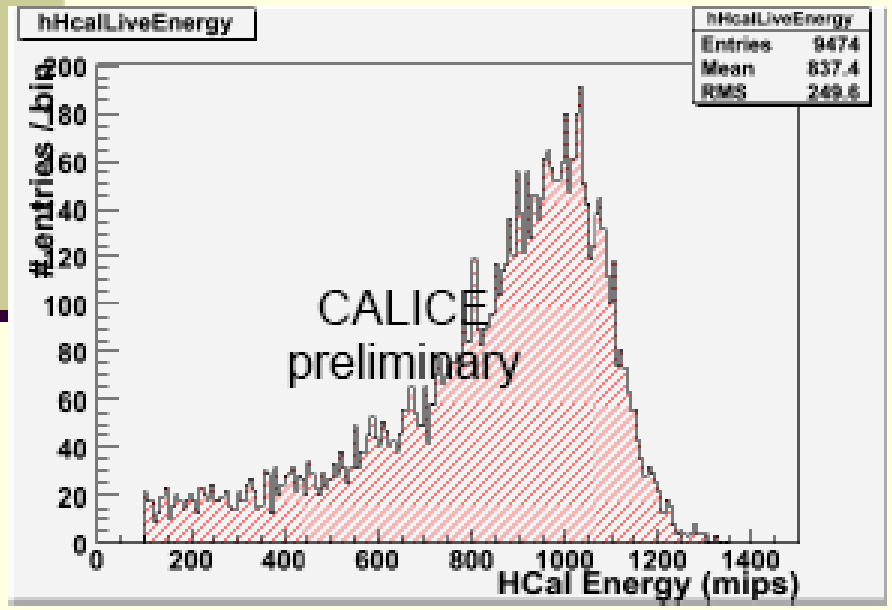
Note on Hcal:
36/38 layers,
15 of them instrumented
(August run)

80 GeV Pions – adding TCMT energy

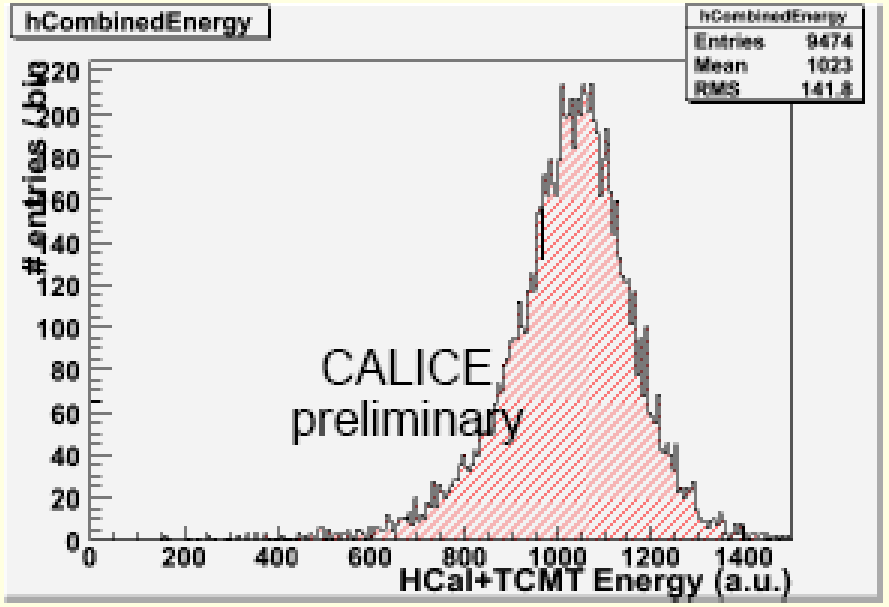
Combining the TCMT hits:
a factor of 1.4445 was applied to the TCMT hits

Much better, but Ecal hits not included yet... **Work in Progress !**

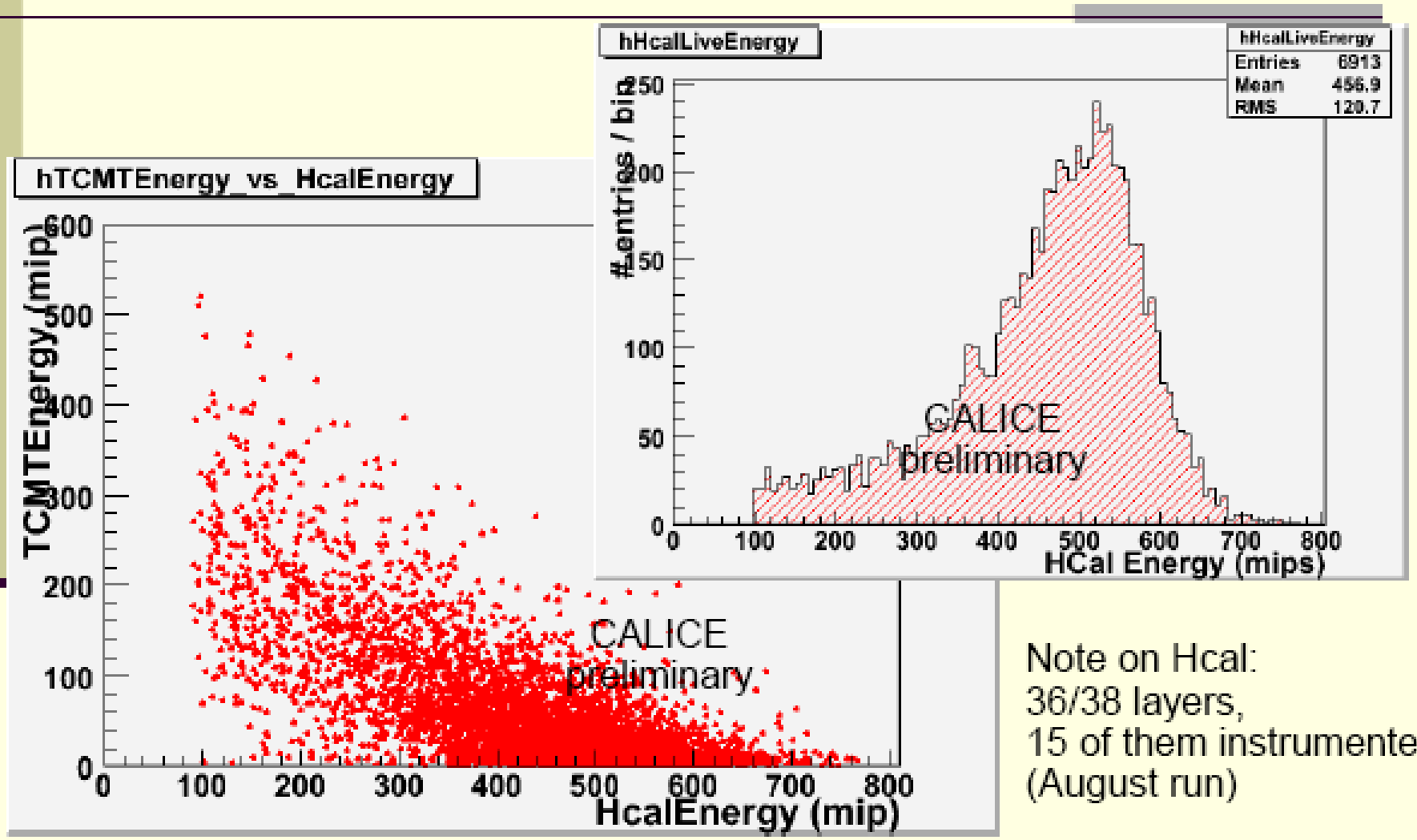
HCal only



HCal + TCMT



30 GeV pions: Hcal x TCMT correlation



Note on Hcal:
36/38 layers,
15 of them instrumented
(August run)

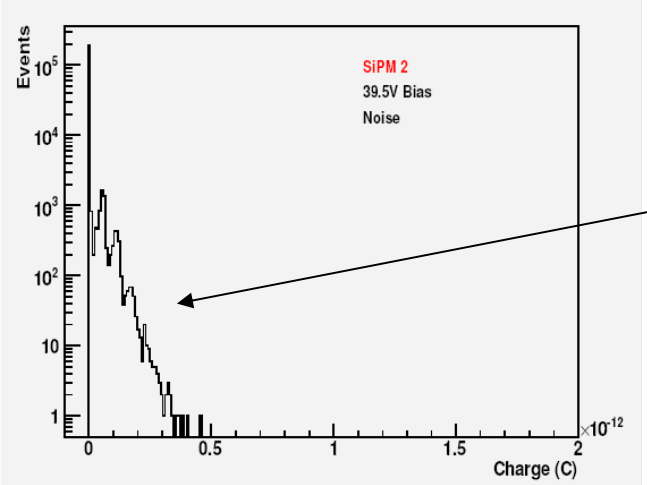
Scintillator/SiPM TCMT/HCal

- Present plans call for completion of the CALICE HCal and ECal in early 2007 and subsequent running at CERN

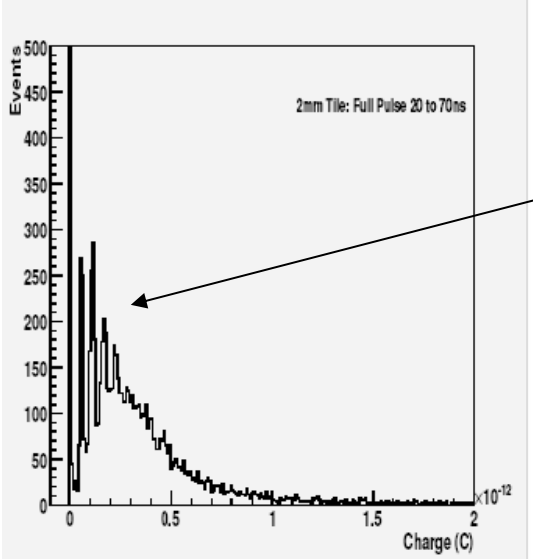
- Target for move of ECal/HCal/TCMT to Fermilab is September 2007 – more of this in Test Beam talk…

SiPM Development – U. Colorado

Pulsar/MEPI SiPM



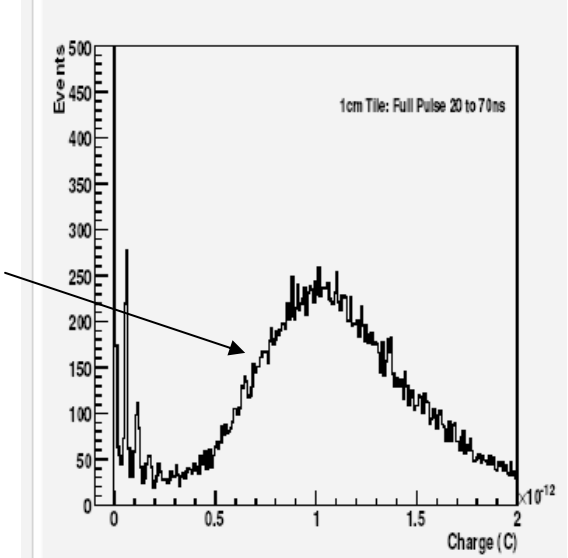
Very low noise device!



Blue LED -> Green WLS

2mm thick tile

1cm thick tile



U. Nauenberg

Scintillator/SiPM TCMT/HCal

From the R&D so far:

- Extruded Scintillator/SiPM's are living up to expectations and are a viable technology .

- focussing on detailed performance studies (e.g. uniformity).

- starting to consider cost/performance for HCAL.

Hadron Calorimeter - Conclusions

- High level of R&D activity for AHCAL/DHCAL/TCMT.

- RPC and GEM plan Slice Test at Fermilab in early 2007.

- Initial results on Scintillator AHCAL/TCMT from CERN.

- Latest versions of readout chips for RPC/GEM look close to acceptance.

- Plans for DHCAL stacks (RPC, GEM) to be tested at Fermilab 2007-8.

- Finally: planning for longer term R&D – developing a plan for a section of a calorimeter that could be part of a final SiD detector. This is a multi-year, expensive, exercise – in parallel with TDR…