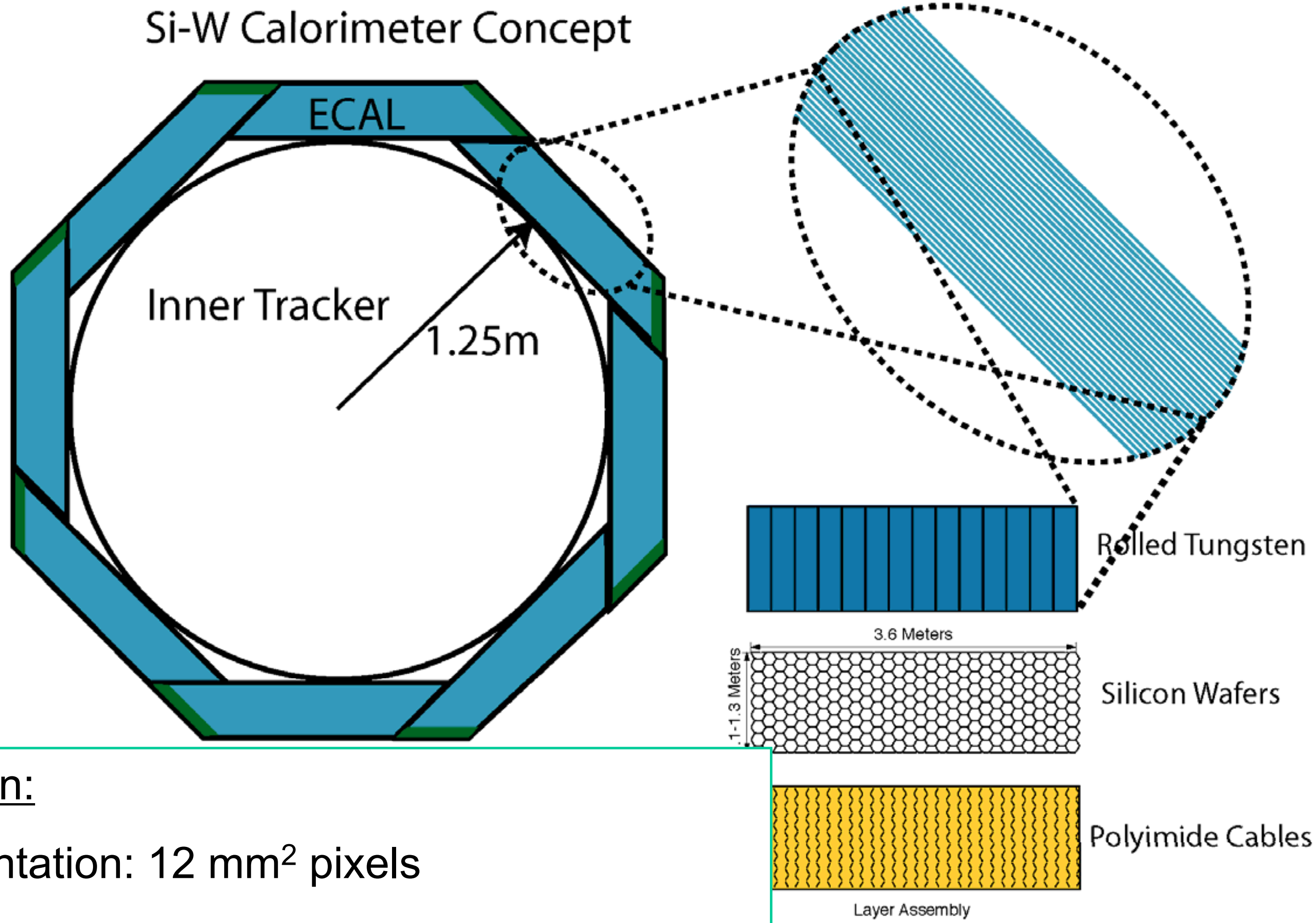
A Silicon-Tungsten ECal for the SiD Concept



Baseline configuration:

- transverse segmentation: 12 mm^2 pixels
- longitudinal: (20 x 5/7 X_0) + (10 x 10/7 X_0) $\Rightarrow$ 17%/sqrt(E)
- 1 mm readout gaps $\Rightarrow$ 13 mm effective Moliere radius

"U.S." Si-W ECal R&D Collaboration

M. Breidenbach, D. Freytag, N. Graf, G. Haller, R. Herbst, J. Jaros
Stanford Linear Accelerator Center

- KPiX readout chip
- downstream readout
- detector, cable development
- mechanical design and integration

J. Brau, R. Frey, D. Strom, M. Robinson, A.Tubman
U. Oregon

- detector development
- readout electronics

V. Radeka
Brookhaven National Lab

- readout electronics

B. Holbrook, R. Lander, M. Tripathi
UC Davis

- cable development
- bump bonding

Y. Karyotakis
LAPP Annecy

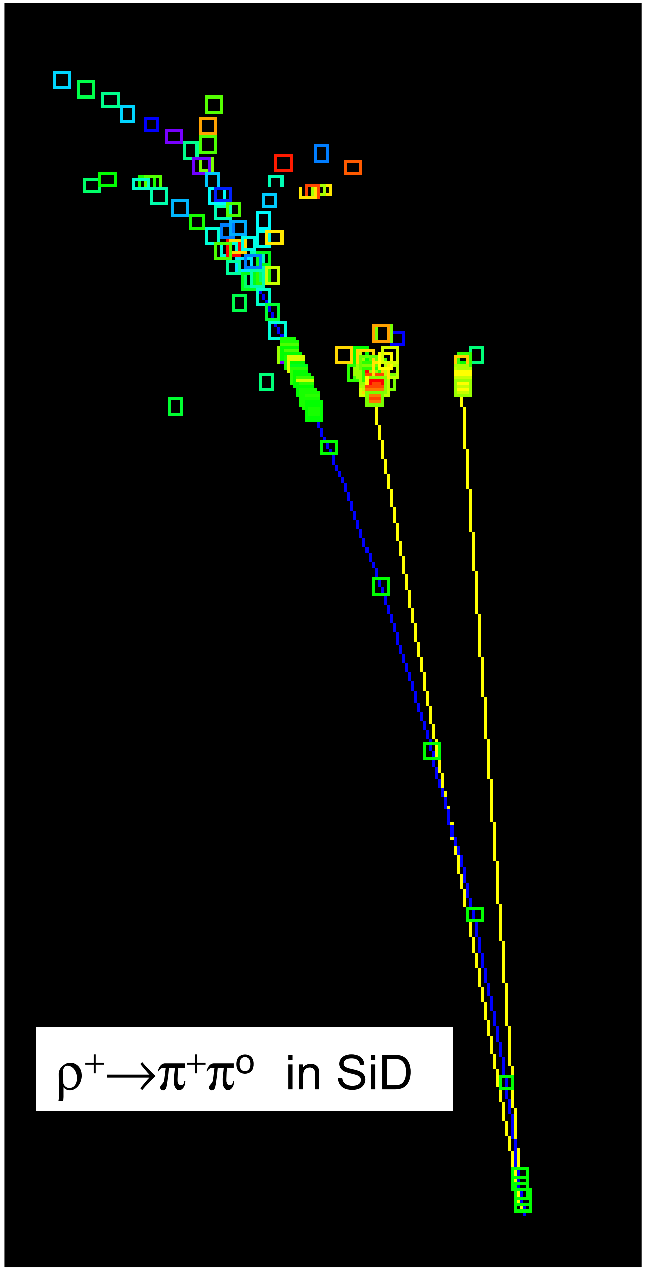
- mechanical design and integration

Goal of this R&D

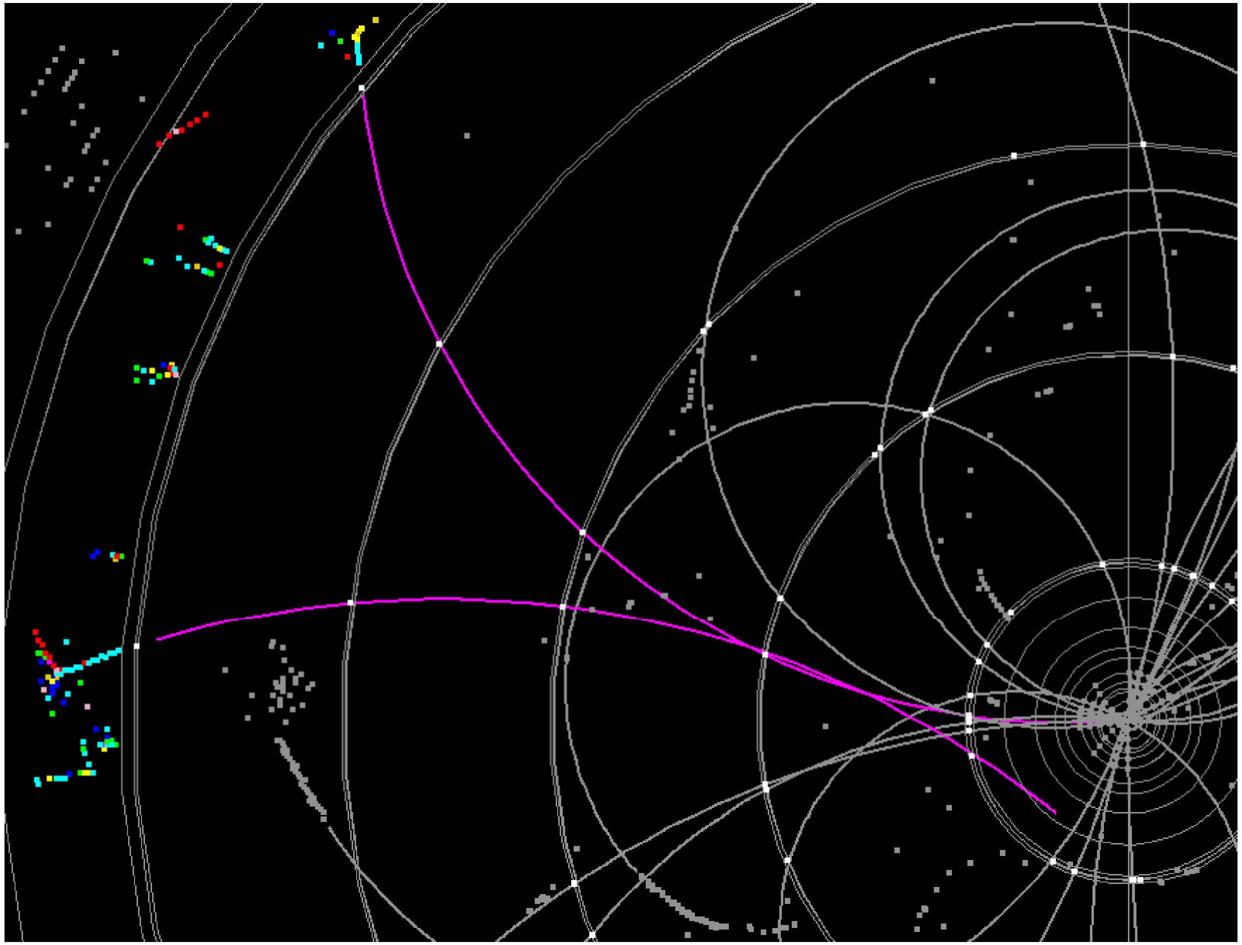
Design a practical ECal which (1) meets (or exceeds) the physics requirements (2) with a technology that would actually work at the ILC.

- The physics case implies a highly segmented "imaging calorimeter" with modest EM energy resolution $\Rightarrow$ Si-W
- The key to making this practical is a highly integrated electronic readout:
    - readout channel count = pixel count / ~1000
    - requires low power budget (passive cooling)
    - must handle the large dynamic range of energy depositions (few thousand) with excellent S/N
- This takes some time to develop (getting close).
- Testing in beams will be crucial (major test in 2008).

"Imaging Calorimeters"



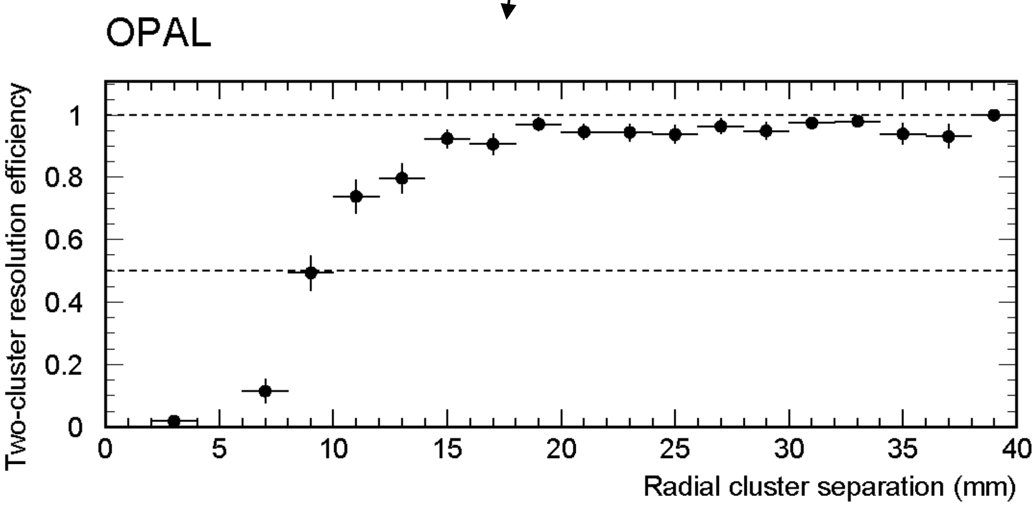
A highly segmented ECal is an integral part of the overall detector particle reconstruction and tracking (charged and neutrals)



Segmentation requirement

- In general, we wish to resolve individual photons in jets, tau decays, etc.
- The resolving power depends on Moliere radius and segmentation.
- We want segmentation significantly smaller than R_m

Two EM-shower separability in LEP data with the OPAL Si-W LumCal (David Strom)

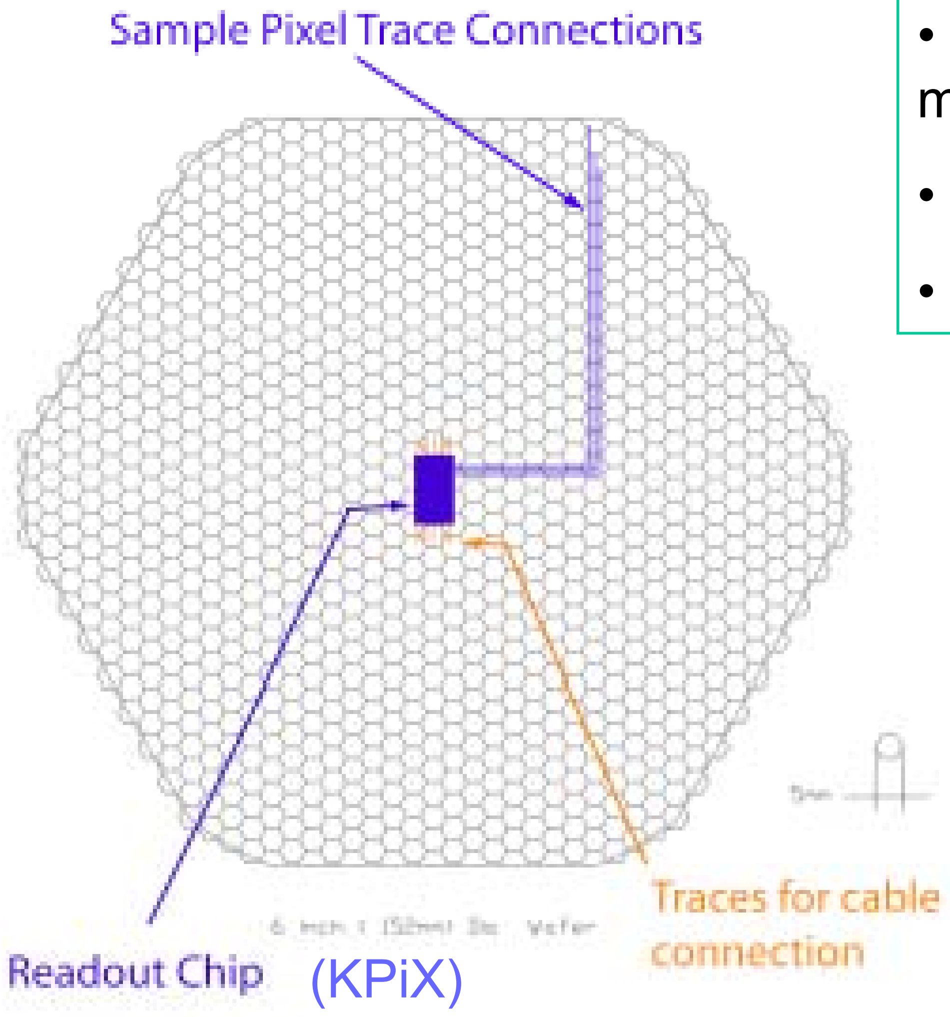


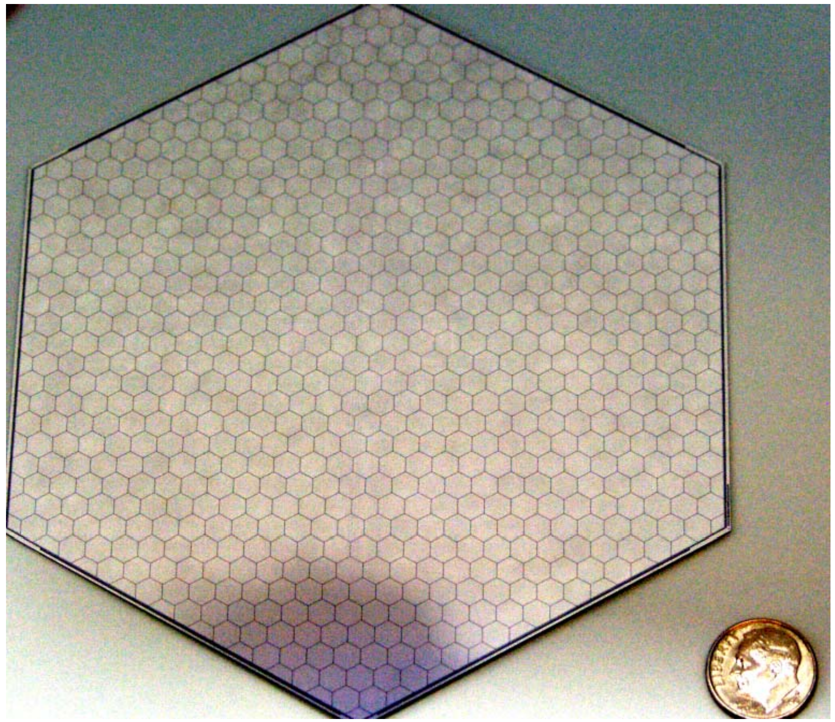
$$f_E \simeq \frac{R_{cal}}{\sqrt{R_M^2 + (4d_{pad})^2}}$$

$$d = 2.5\text{mm} \ , \ R_M \sim 17\text{mm}$$

Silicon detector layout and segmentation

- Silicon is easily segmented
- KPiX readout chip is designed for 12 mm^2 pixels (1024 pixels for 6 inch wafer)
- Cost nearly independent of seg.
- Limit on seg. from chip power ($\approx$2 mm^2)





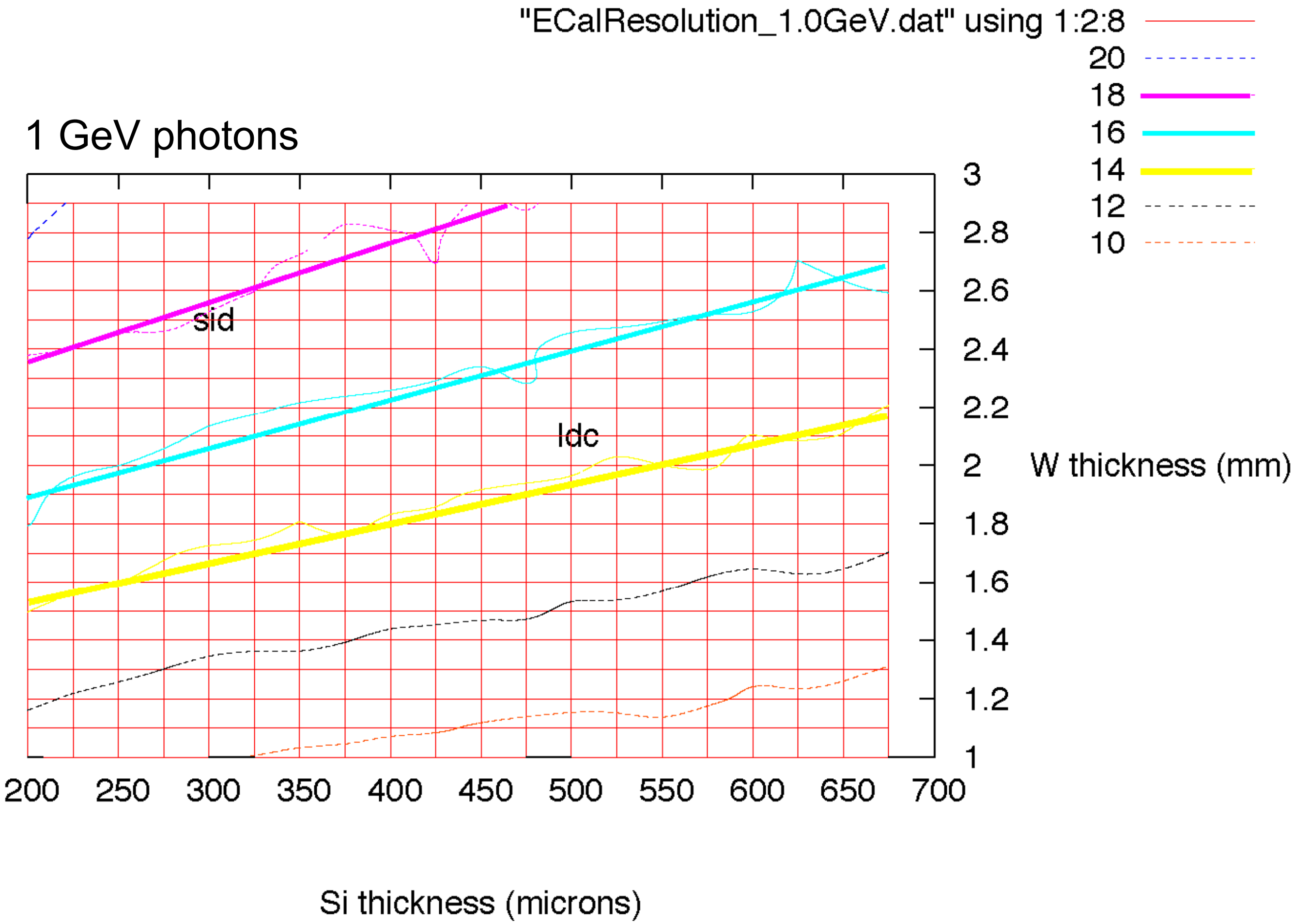
Fully functional prototype (Hamamatsu)

EM Energy Resolution

- Requirement for jet energy resolution in PFAs is modest for EM: $\lesssim$ 0.20/sqrt(E)
- There is no known strong physics argument for excellent EM energy resolution.

  $\Rightarrow$ Our current design provides moderate resolution: 0.17/sqrt(E)

However, it is useful to know how to “dial in” different resolutions, if needed.



Lines of constant resolution

Dependence on Si thickness due to straggling.

Simulation Results

- For a simple W-Si sampling calorimeter, the energy resolution is given by:

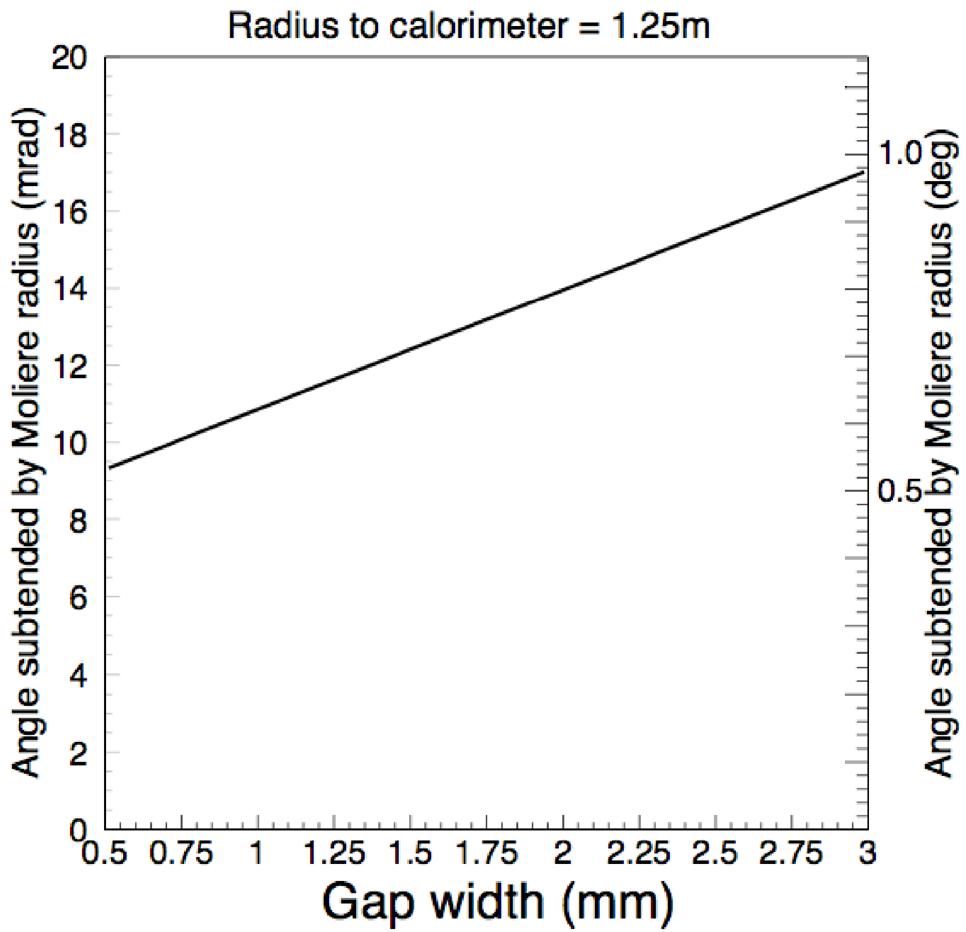
$$\frac{\sigma}{E} \approx \left[11.5\left(\frac{d_W}{2.5mm} \right) - 1.8\left(\frac{d_{Si}}{300\mu m} \right) + 8 \right]\%$$

  - Doubling silicon thickness to 600μm would reduce resolution by 1.8%
  - Decreasing tungsten thickness by 5% would reduce resolution by 1.4%
- Would like to see some of this space explored in testbeam:
  - Ideally with wafers of different thicknesses.
  - Could also use thick silicon and vary effective sensitive thickness (depletion depth) with bias voltage (cf. SICAPO).

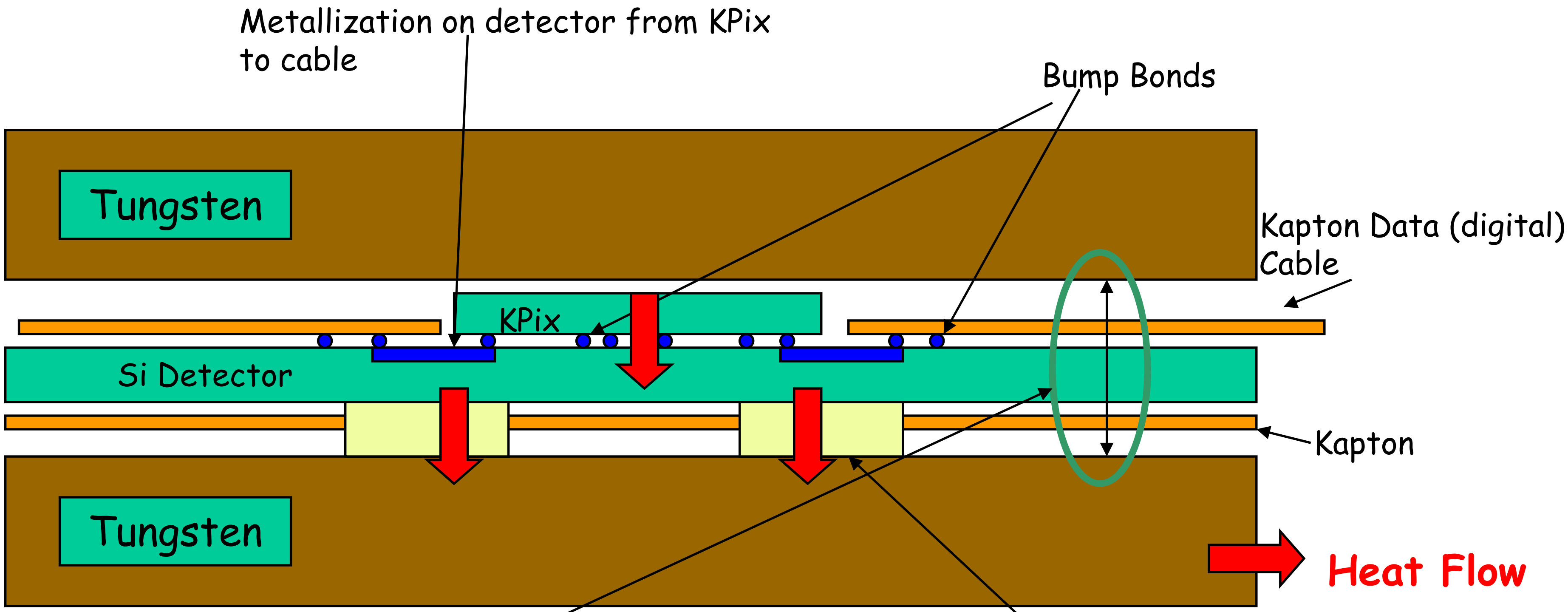
Critical parameter for R_M is the gap between layers

Config.	Radiation length	Molière Radius
100% W	3.5mm	9mm
92.5% W	3.9mm	10mm
+1mm gap	5.5mm	14mm
~~+1mmCu~~	~~6.4mm~~	~~17mm~~

Assumes 2.5mm thick tungsten absorber plates

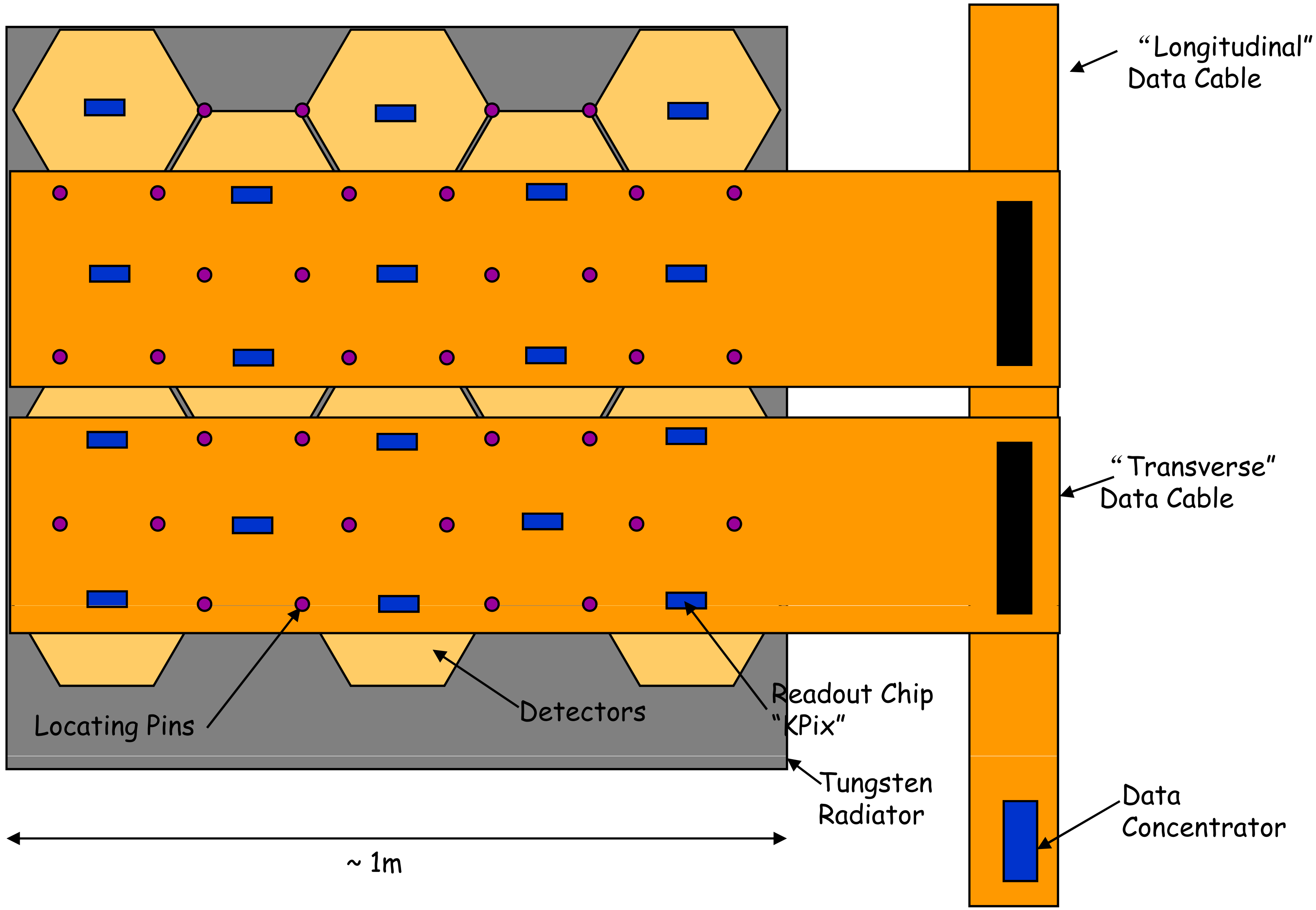


US Si-W readout gap schematic cross section



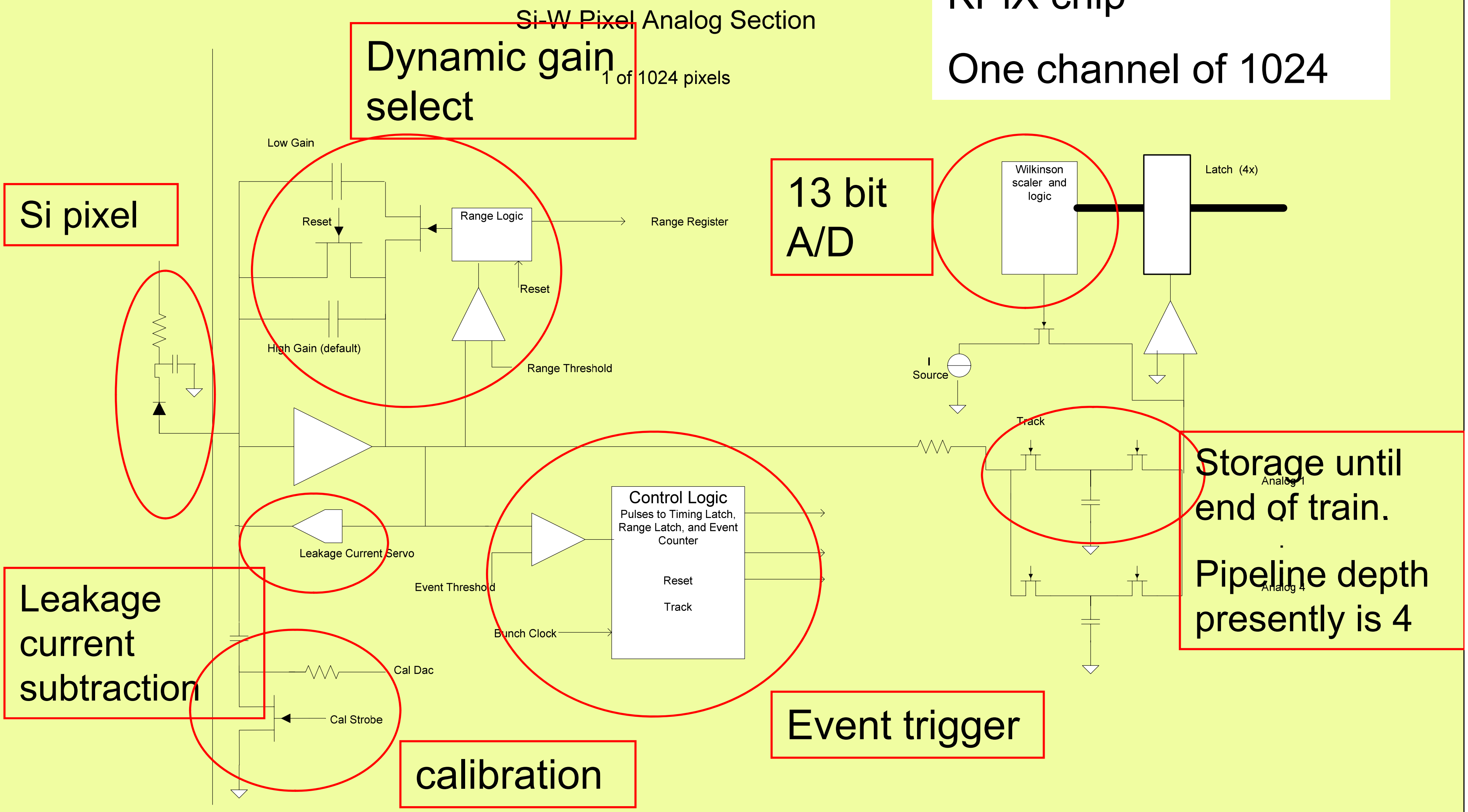
Gap ≤ 1 mm

Conceptual Schematic – Not to any scale!!!



KPiX chip

One channel of 1024

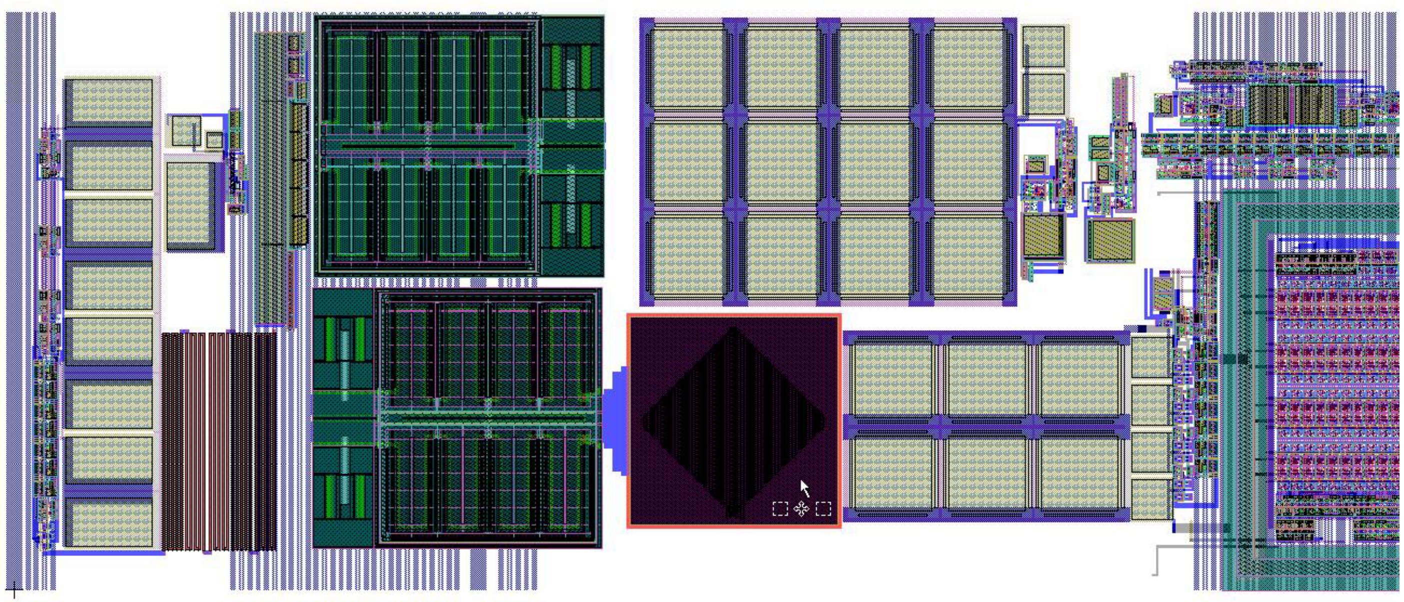


Simplified Timing:

There are ~ 3000 bunches separated by ~300 ns in a train, and trains are separated by ~200 ms.

Say a signal above event threshold happens at bunch n and time T0.
The Event discriminator triggers in ~100 ns and removes resets and strobes the Timing Latch (12 bit), range latch (1 bit) and Event Counter (5 bits).
The Range discriminator triggers in ~100 ns if the signal exceeds the Range Threshold.
When the glitch from the Range switch has had time to settle, Track connects the sample capacitor to the amplifier output. (~150 ns)
The Track signal opens the switch isolating the sample capacitor at T0 + 1 micro s. At this time, the amplitude of the signal at T0 is held on the Sample Capacitor .
Reset is asserted (synched to the bunch clock) . Note that the second capacitor is reset at startup and following an event, while the high gain (small) capacitor is reset each bunch crossing (except while processing an event)
The system is ready for another signal in ~1.2 microsec.
After the bunch train, the capacitor charge is measured by a Wilkinson converter.

KPiX Cell 1 of 1024



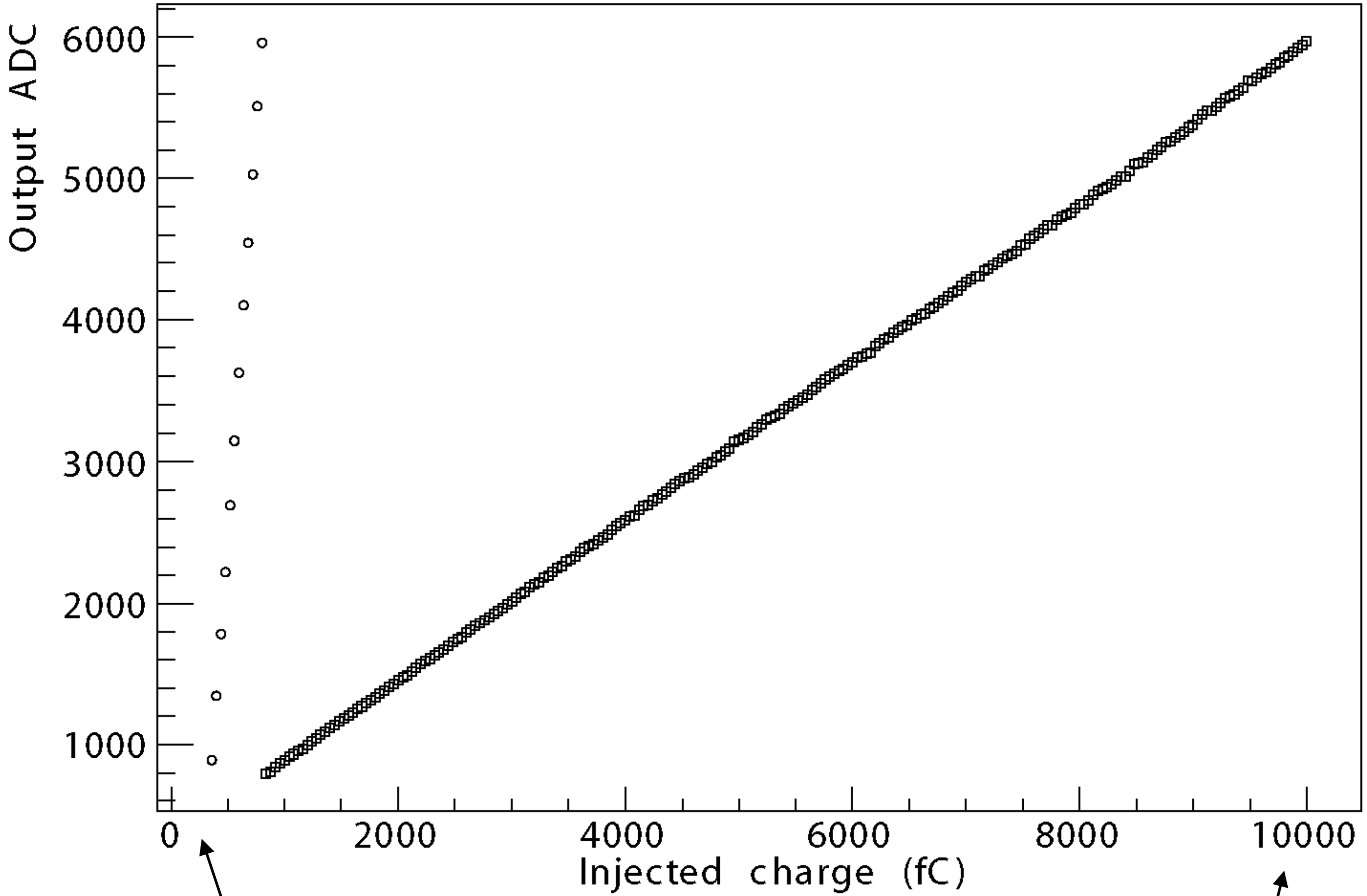
64-channel prototypes:

- v1 delivered March 2006
- v4 delivered Jan 16, 2007

It's a complicated beast – may need a v5 before going to the full 1024-channel chip ?

Dynamic Range

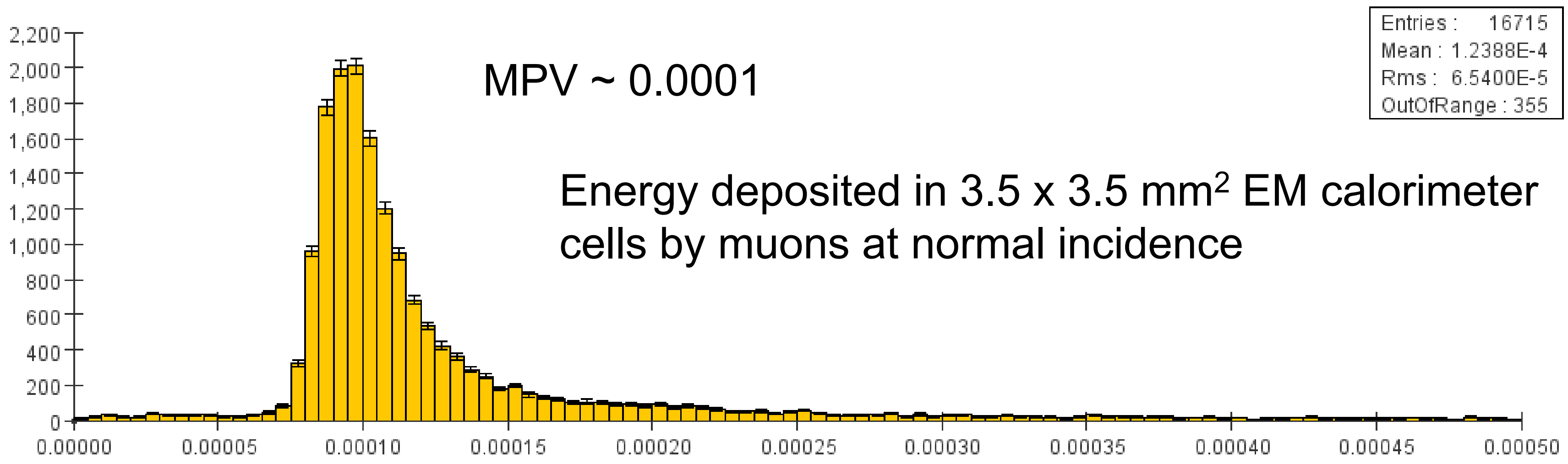
KPiX-2 prototype on the test bench

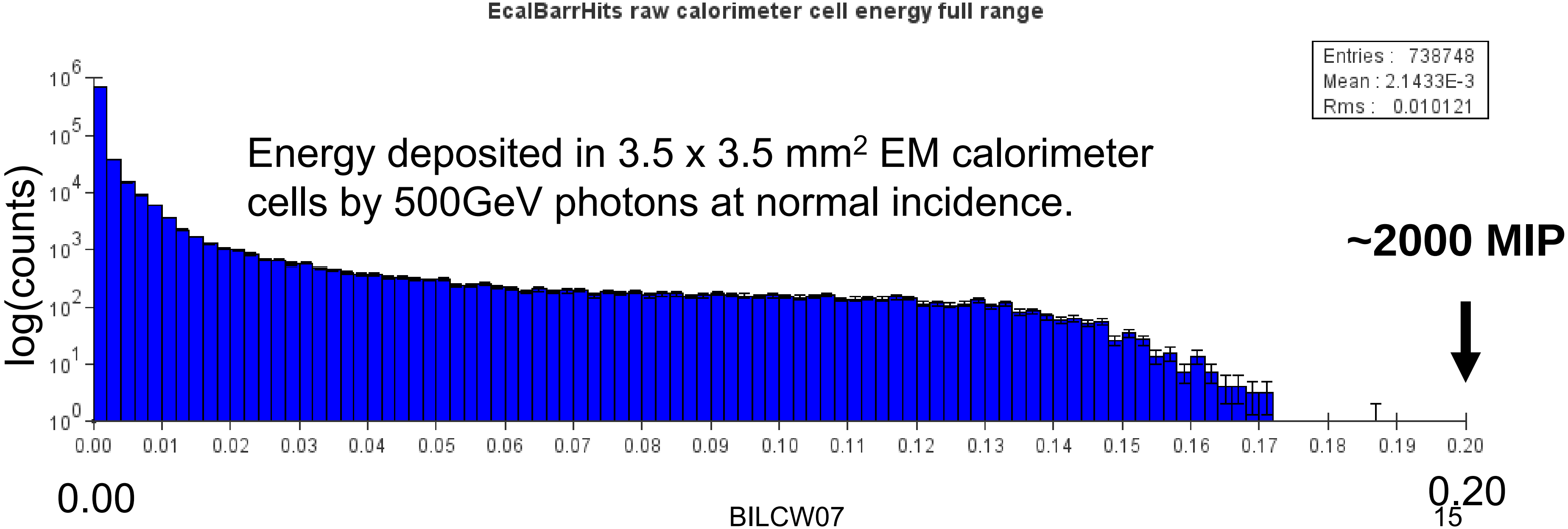


1 MIP (4 fC)

Max signal: 500 GeV electron

Saturation Simulation

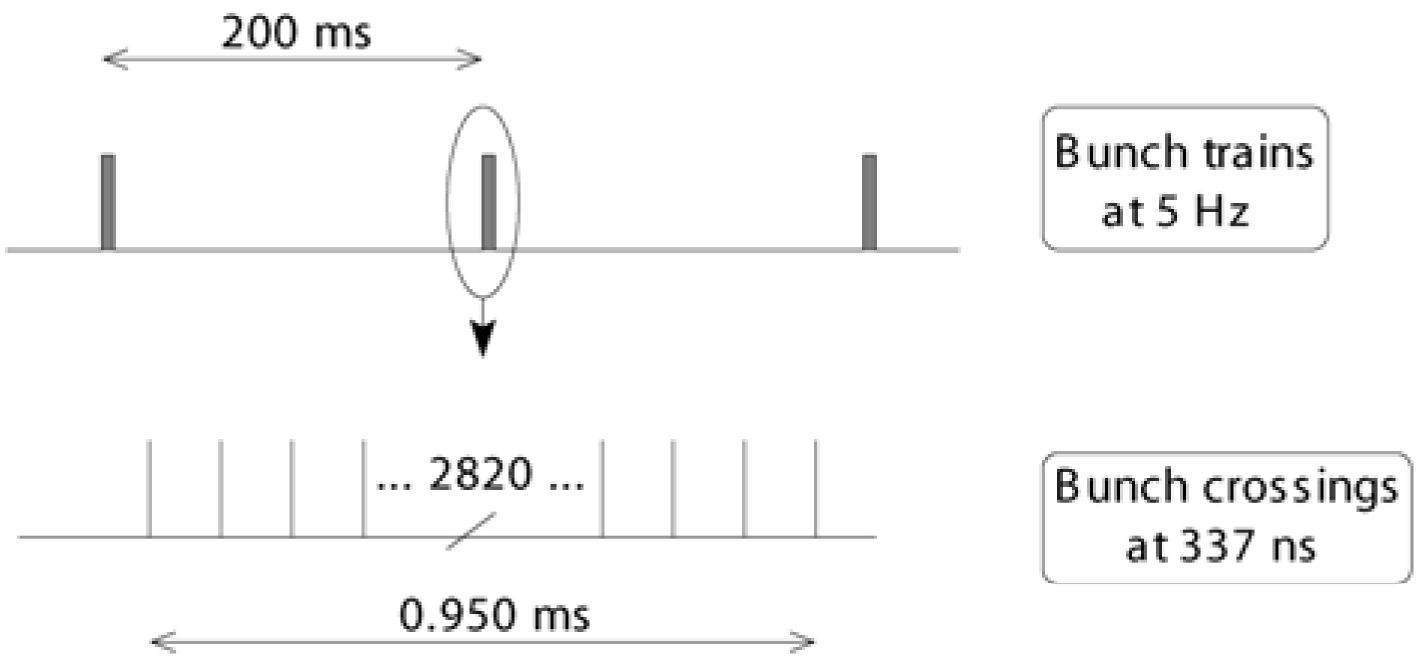




Simulation Results

- Saturation, even for highest energy electromagnetic showers (Bhabhas at a 1 TeV machine), is not a problem with the default design of 3.5 x 3.5 mm^2 cells read out using the KPiX chip.

Power Pulsing



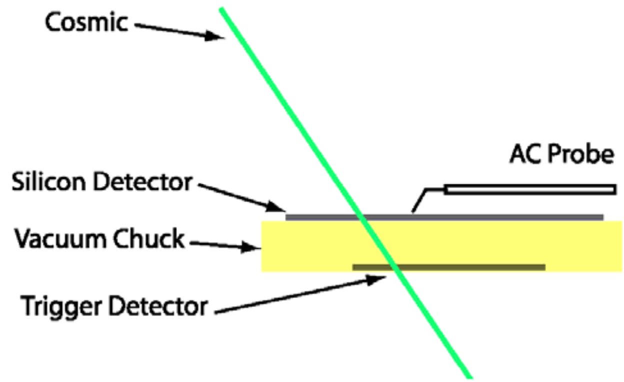
Switch off KPiX analog front-end power between bunch trains (1% duty cycle)

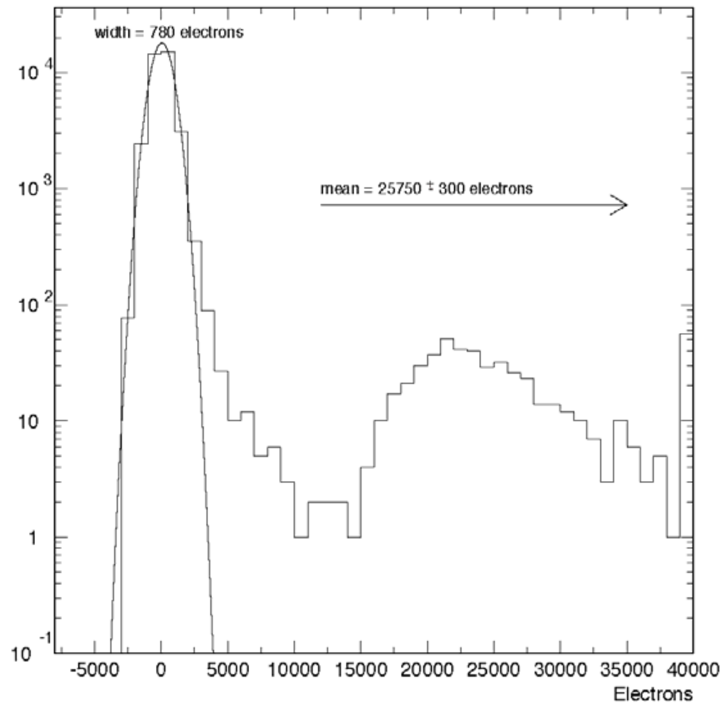
⇒ Average power of 18 mW per channel

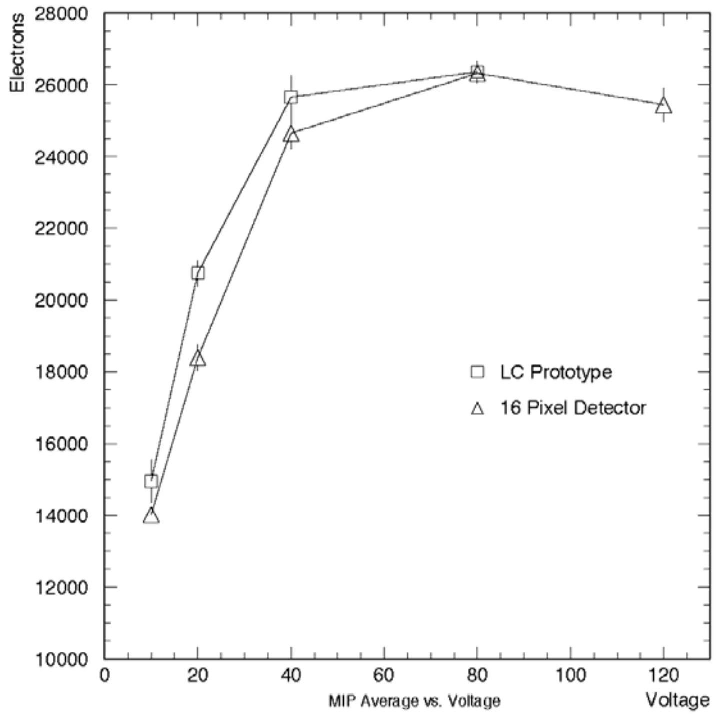
⇒ passive-only cooling should be OK

prototype Si detector studies

Response of detectors to Cosmics
(Single 5mm pixel)
Simulate LC electronics
(noise somewhat better)

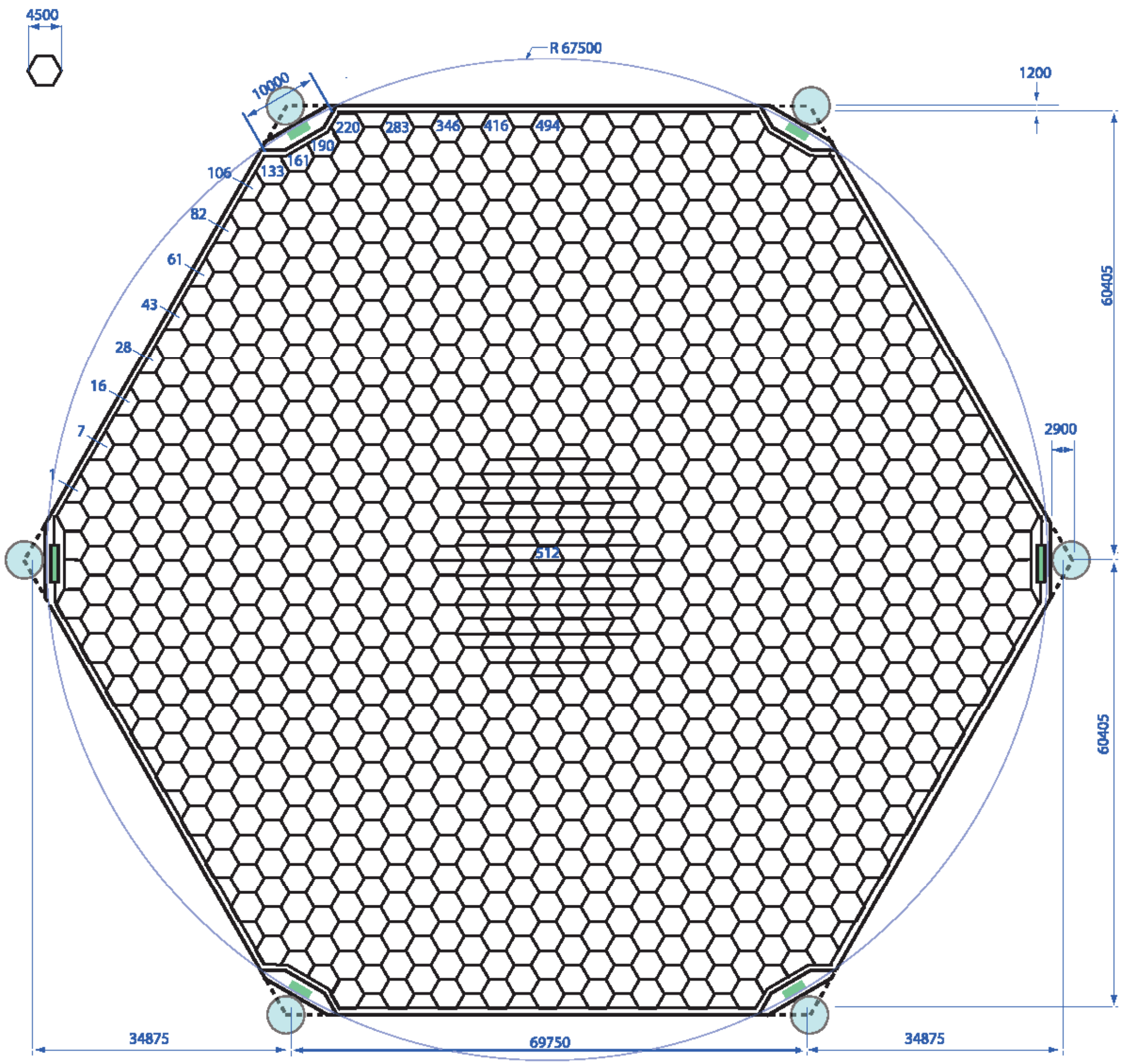






Errors do not include ~ 10% calibration uncertainty (no source calibration)

v2 Si detector – for full-depth test module



- 6 inch wafer
- 1024 12 mm^2 pixels

Allows for topside bias

Vertices removed for spacers

Trace layout minimizes C_{max}

Uses thinner traces near KPiX

Low resistance power and ground connections

ready to go except for funding

R&D Milestones

I. Connect (bump bond) prototype KPiX to prototype detector with associated readout cables, etc

- Would benefit from test beam (SLAC?) - 2007
- A "technical" test

II. Fabricate a full-depth ECal module with detectors and KPiX-1024 readout * – functionally ≈equivalent to the real detector

- Determine EM response in test beam – 2008
- Ideally a clean 1-30 GeV electron beam (SLAC?)

III. Test with an HCal module in hadron test beam (FNAL?) – 2008-?

- Test/calibrate the hadron shower simulations; measure response

IV. Pre-assembly tests of actual ECal modules in beam – >2010

* *pending funding*

Summary

- The R&D leading to an “ILC-ready” Si-W ECal technology is progressing well.
  - There are no show-stoppers for meeting the demanding physics and technical requirements.
- This effort depends crucially on highly integrated readout electronics (KPiX)

- This Si-W R&D should result in full-depth modules which will require test beam evaluation
  - Our Si-W module (30 layers x 16cm x 16cm) - 2008*

- These highly segmented, analog devices should provide an interesting test for simulation modeling of (early developing) hadron showers.