Summary of Vertex/Tracking

A. Sugiyama(Saga U.)

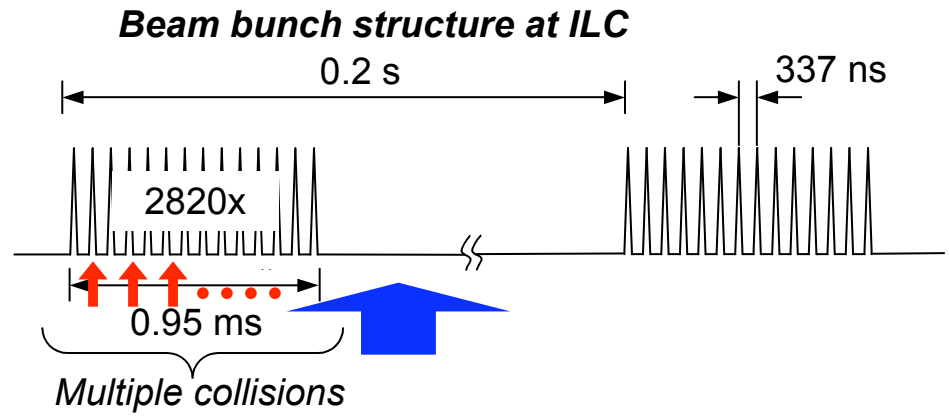
Talk list

Performance of the tracking system of the 4-th concept	C. Gatto(INFN)
Development of an ILC vertex detector sensor with single bunch crossing tagging	J. Brau(Oregon)
FPCCD Vertex detector for ILC	Y. Sugimoto(KEK)
Performance of FPCCD vertex detector	T.Nagmaine(Tohoku)
Simulation of the SiD Tracker	B.Schumm(UCSC)
Development of Microstrip Readout at SCIPP	B.Schumm(UCSC)
The trf Track Reconstruction package	N.Graf(SLAC)
Current status of the silicon strip sensor development in Korea	H.J.Kim(Kyungpook)
Study on GEM and TPC in Tsinghua University	Y.Li(Tsinghua)
The preliminary results of MPGD-based TPC performance at KEK	Y.Kato(Kinki)
Micromegas TPC studies in a 5 Tesla magnetic field with a resistive readout	P.Colas(Saclay)
Prototype test for LP TPC	A.Sugiyama(Saga)
A simulation study of GEM gating at ILC	A.Aoza(Saga)

VTX	3 talks
Si tracker	3 talks
Gas tracker	5 talks
simulation	2 talks

Brief Introduction of Vetex

required point resolution ~ a few um
low material < 0.5% X0
Occupancy < 1%



Key issue of R&D

Bkg. hits exceed "occupancy limit" (1%)
after ~3000BX(1 train) w/ standard 20um pixel

Solution: 1) read data before Occ. exceed limit (20 times/train)
can we read all data within 50usec? Column parallel CCD, CMOS, DEPFET
2) store data and reset sensor(20 depth in storage or 20 times finer pix.)
can we store data? read all data (within 199msec). ISIS, Macro/Micro
make pixel size small(20 times smaller in area; 5um pixel) can we make ? FPCCD
"Proof of Principle"

talks at this WS

with reasonably low power dissipation,
high S/N,
low material (thinning) ,
tough rad. hardness
away from RF pick-up

many more things
mechanical design, support, cooling
Optimization under physics benchmark
Software development

Development of an ILC vertex detector sensor with single bunch crossing tagging

Chronopixel[1] Sensors for the ILC

Macro / Micro
(50um pitch / 5um pitch)
high speed(timing) / precise position

→

Macro only
(50um pitch)
bunch tag (timing)
store 4 deep timing info.

occupancy/train ~23%

But prob. for getting 4 or more hits ~10^{-4}
as Poisson statisitics

563 Transistors (2 buffers +calibration)

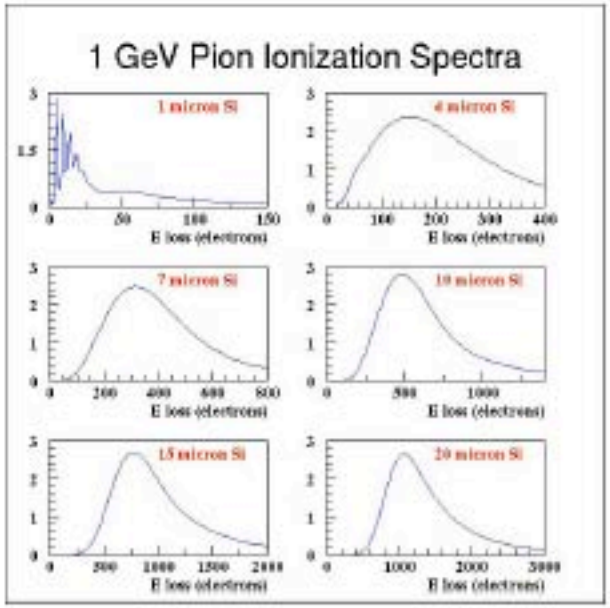
50 µm x 50 µm

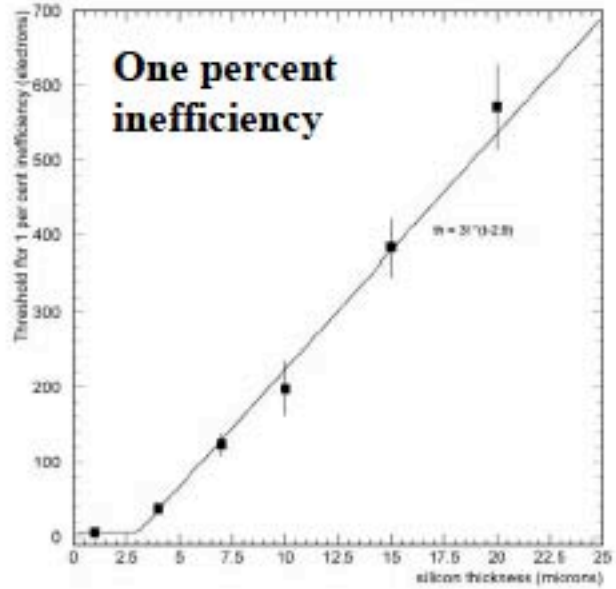
bunch timing seems to be quite useful for self tracking capability

current design(50um) use 180nm tech.

45nm tech. enable 20um or smaller pixel
@ near future

Expected Signal and Efficiency





epilayer thickness (μm)	1% ineff. threshold electrons	50% hit sharing electrons	noise electrons
5	65	32	4
7	127	63	16
10	220	110	28
15	**375**	**188**	**47**
20	530	265	66

Target: 15 μm fully depleted

Noise requirement for threshold = 4 * noise

Plans

Last summer-

- Analog design - completed
- Digital design of in-pixel circuit - completed
- Digital design of readout - completed

Near term plans as of last summer

- Explore alternative pixel designs - now completed
- Finish analog design and detailed pixel simulation - now completed
- Layout circuit - now completed

Medium term plan (2007-2008)

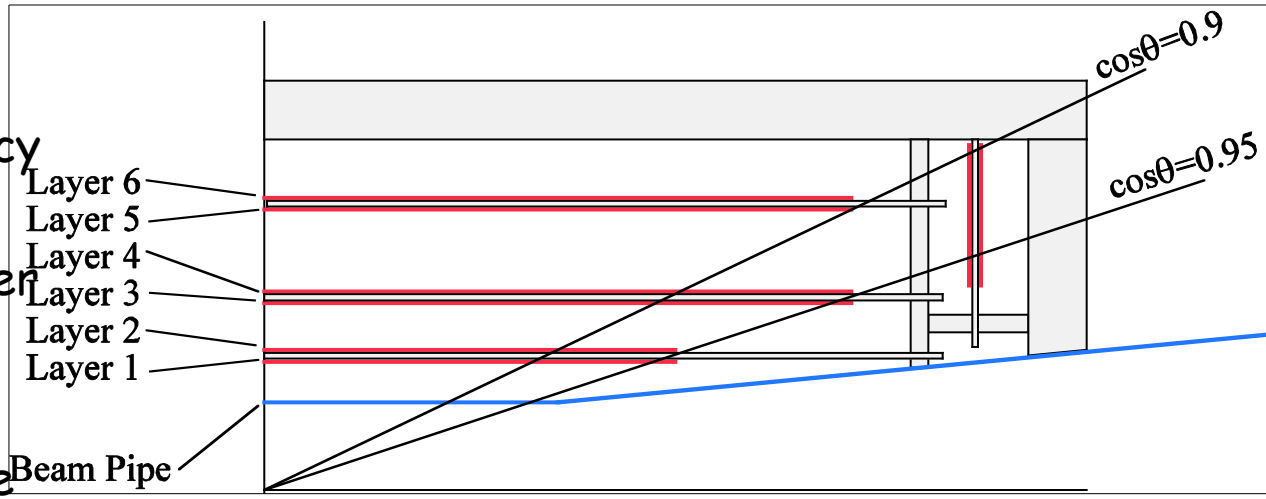
- Fabricate 5mm×5mm protoype with 50 μm × 50 μm pixels in 180nm CMOS (Requires supplemental funding)
- Fabricate readout board (SLAC)
- Test with laser in lab
- Test with sources in lab
- Simulated charge collection efficiency of TSMC prototype and ultimate device - in progress

FPCCD Vertex Detector for ILC

Y.Sugimoto (KEK)

Simple CCD with 5umx5um pixel
in order to reduce Occupancy
Fully depleted epitaxial layer
3 super-layers / 2 layers/super-layer
free from EMI

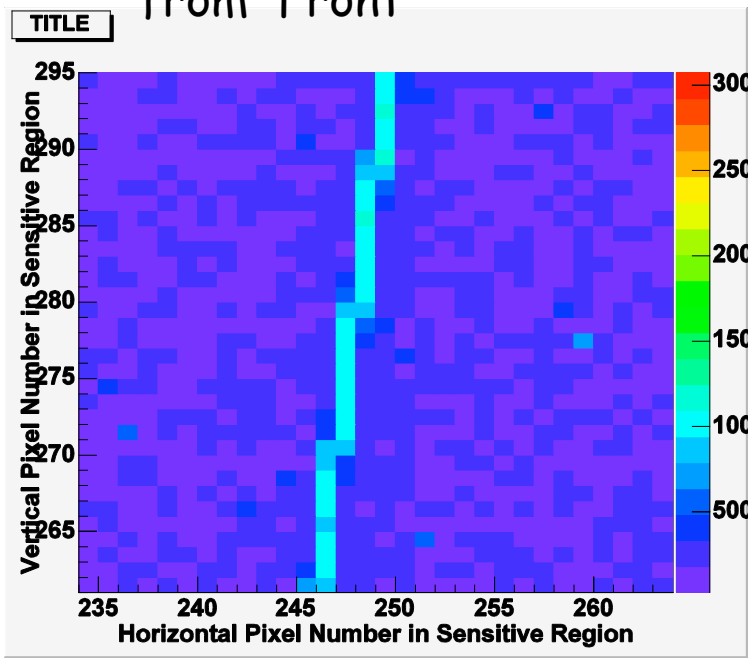
B.G. rejection from hit cluster shape



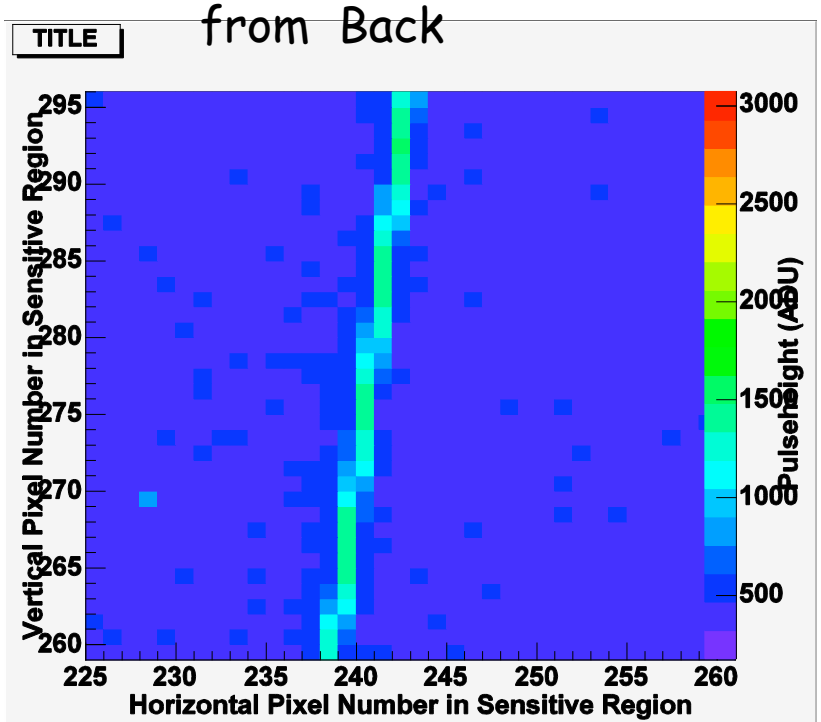
Charged spread

ilumination to thinned(30 um thick) CCD

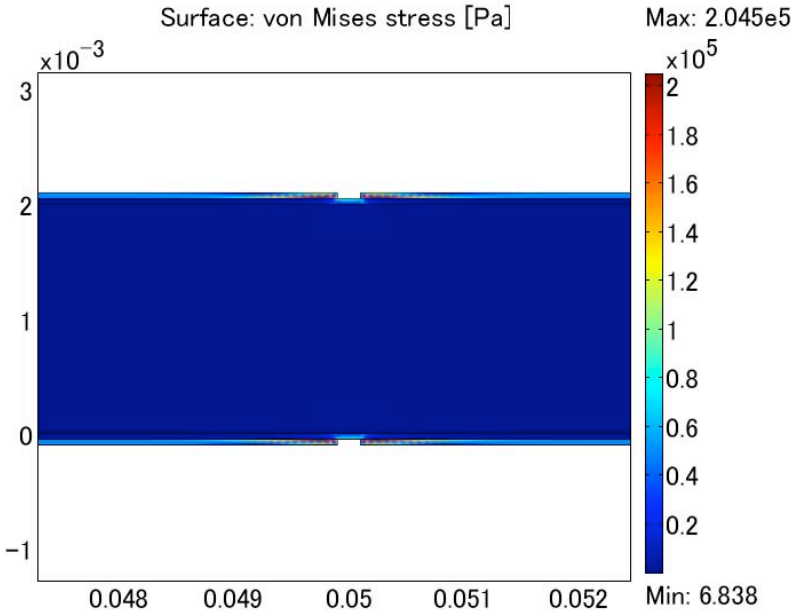
from Front

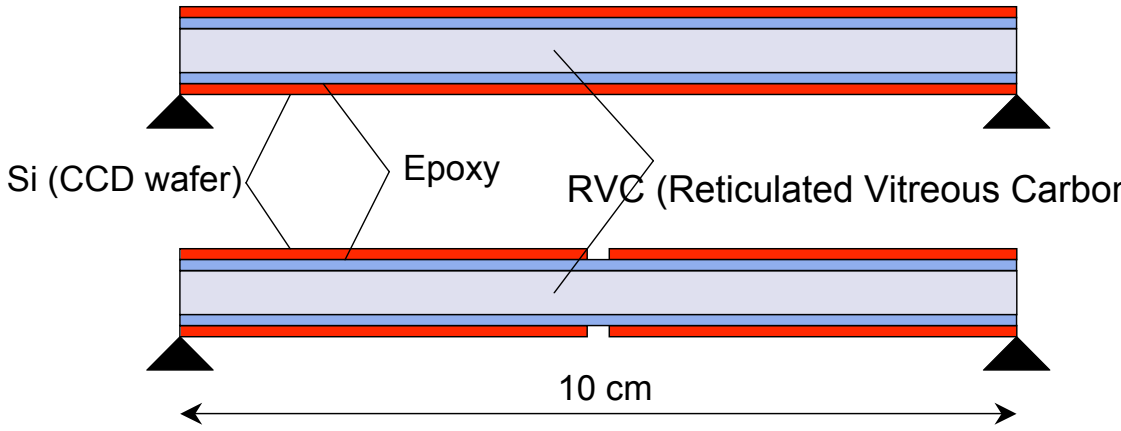


from Back



Mechanical design of Ladder





max. deformation is 0.54um w/o gap
0.72um w/ 0.2mmgap

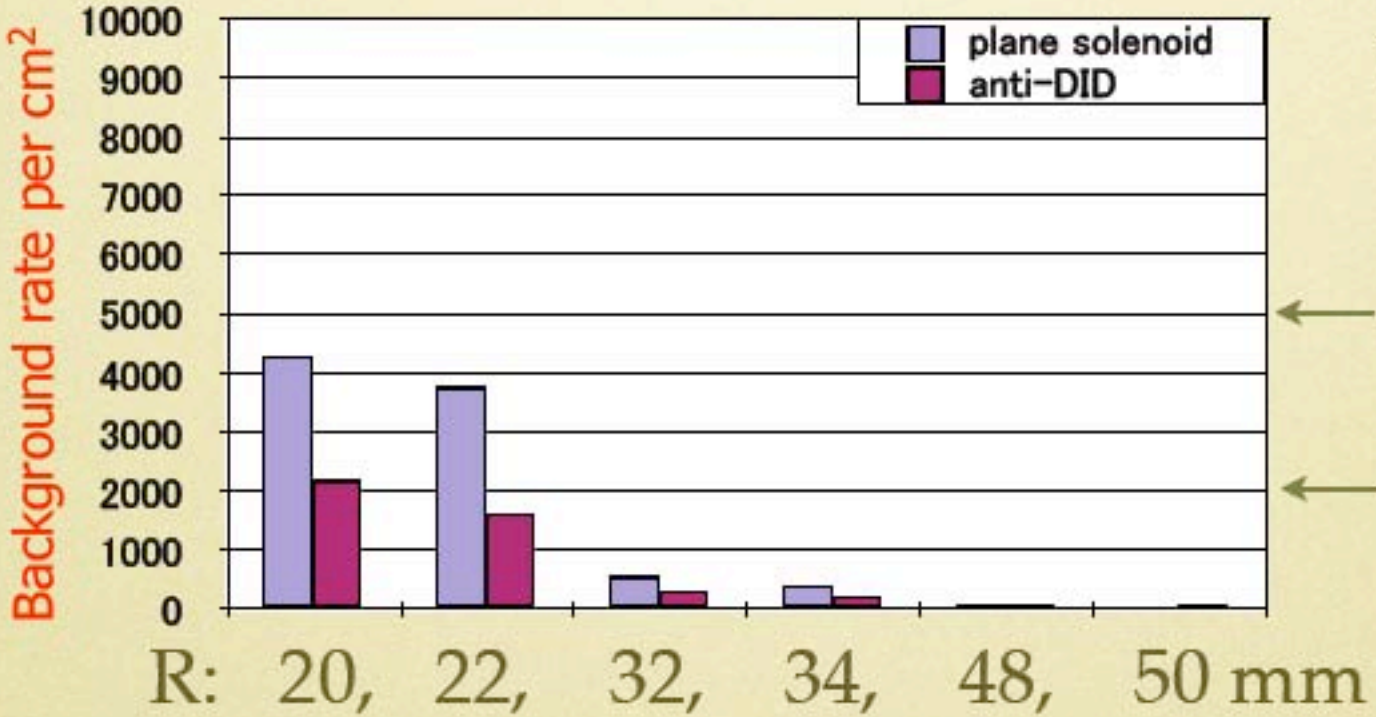
Deformation by self-weight is calculated by FEA program COMSOL

The most important progress is
HAMAMATSU agree to make FPCCD in FY2007

"Performance of FPCCD" T.Nagamine(tohoku)

Full simulation : impact parameter resolution, bkg,

Background rate Plain vs. anti-DID in VTX



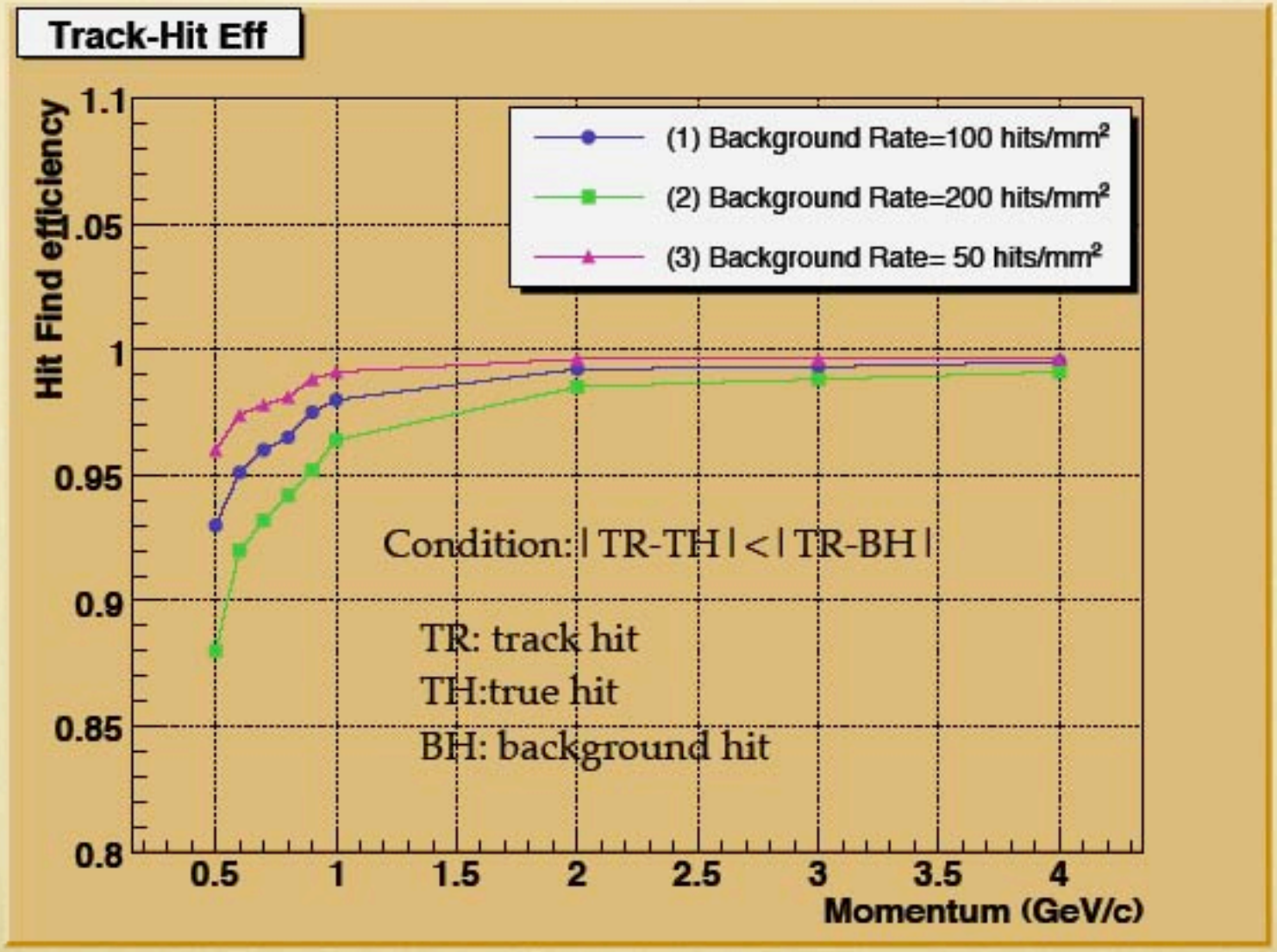
By Fujishima, Saga Univ.

← 50 hits/mm²

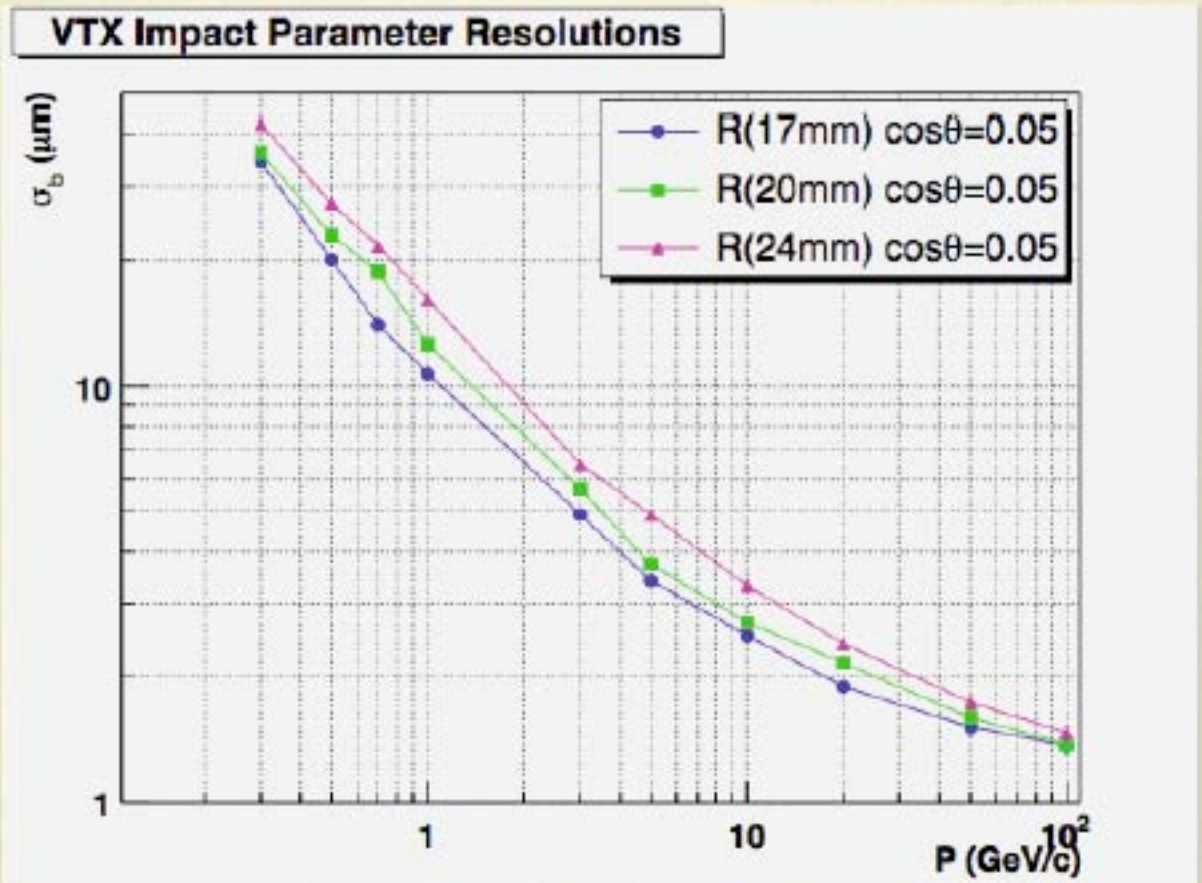
← 20 hits/mm²

- CAIN/Jupiter/Geant4 results
- Beam Parameter: nominal 500GeV, 14mrad
- Background rate is reduced to 1/2 with ANTI-DID Field

Efficiencies for different hit rates



Impact Parameter Resolution R dependence (OLD Geometry)



- Impact Parameter Resolution(R-phi plane) v.s. Momentum
- μ^- at cos(θ)=0.05
- Impact Parameter Resolution increases as radius increases

it can meet the goal if R<20mm

Si tracker

(IT + main) spent 1+2+3=6hrs @ review session

not many talks in the parallel session

FE electronics

how to read a lot of channel

how to suppress noise

Power recycling

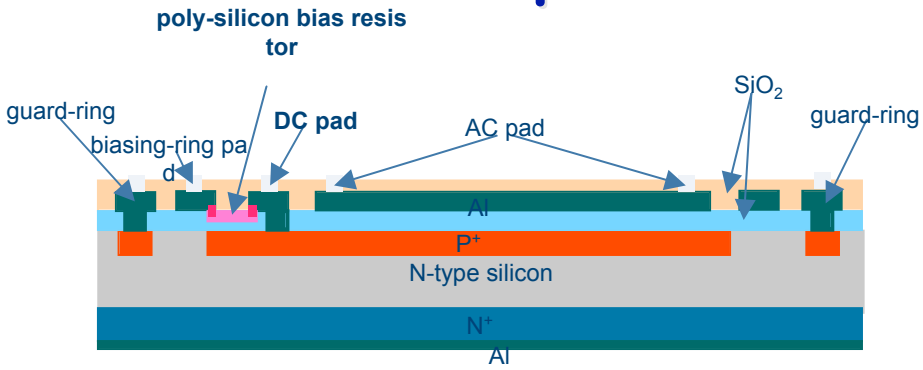
Mechanical issue

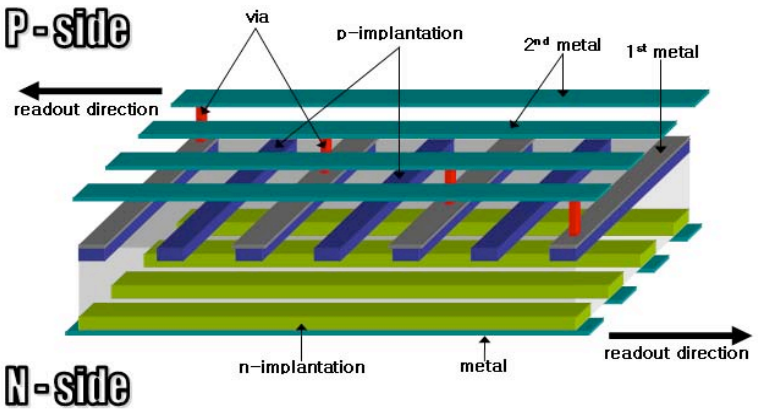
how to mount/align

Sensor

Current status of the silicon strip sensor development in Korea

H.J.Kim





AC-type single-sided strip sensor

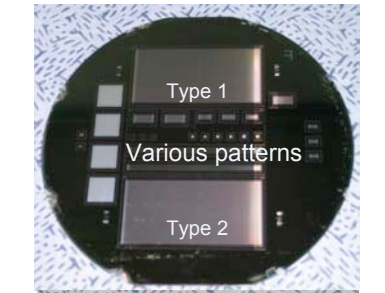
Silicon Strip Sensor Summary

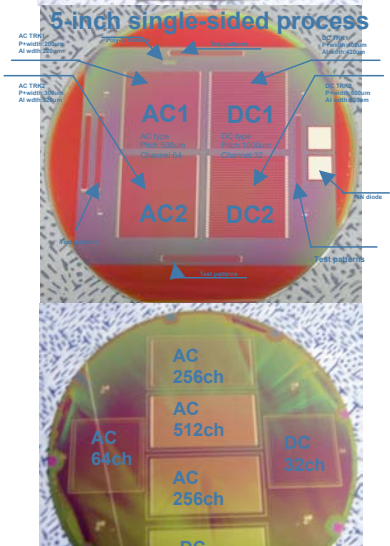
- **yields**

type	DC-type	AC-type
single-sided	90%	80%
double-sided	< 30%	N/A

- **fabrication line**

line	DC-type	AC-type
5 inch	double/single-sided	single-sided
6 inch	single-sided	single-sided (in progress)
8 inch	thickness (725 um, can be thinned ~500 um)	





- Double sided silicon sensor, DC-type single side d silicon sensor and AC-type single sided silicon sensor was successfully produced and tested.
- Beam test and radiation damage shows that de veloped sensor can be used for the ILC environ ment.
- Radioactive source test and beam test showed that S/N ratio is good enough for the ILC envi ronment.
- Electronics R&D is under progress.

SCIPP R&D on Time-Over-Threshold Electronics and Long-Ladder Readout

B.Schumm

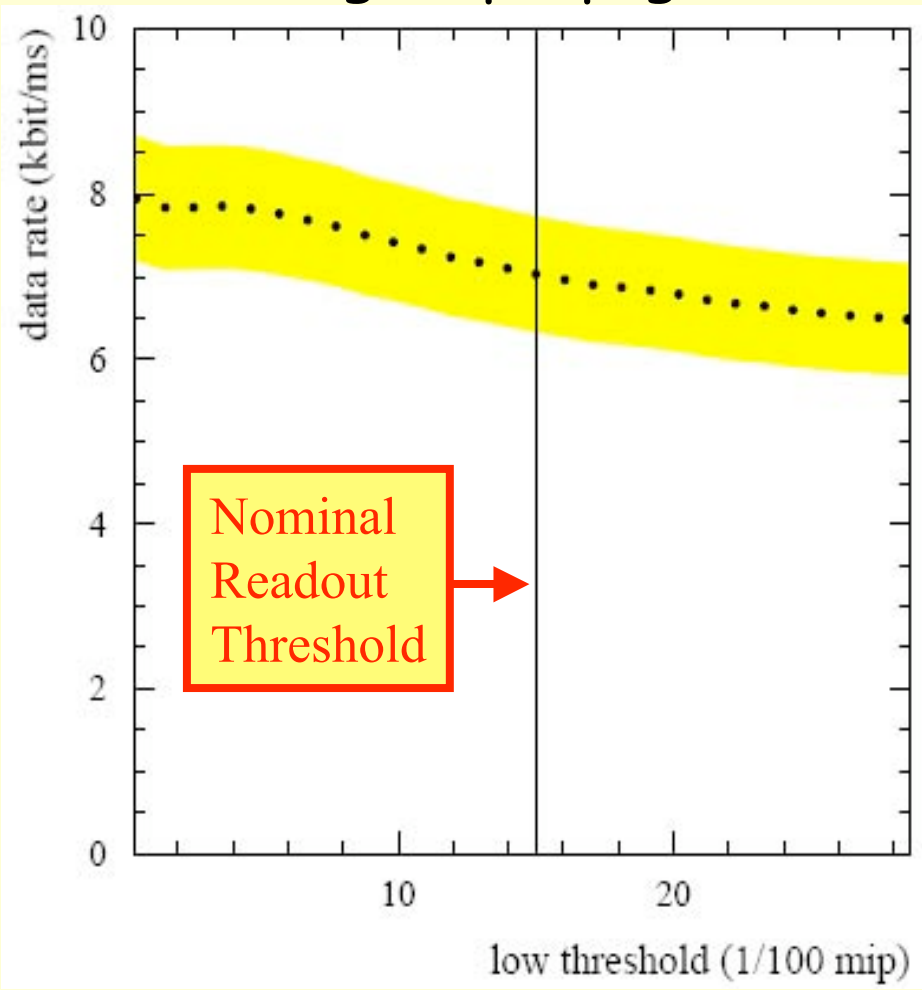
Use of time-over-threshold (vs. analog-to-digital conversion) permits real-time storage of pulse-height information.

➔ No concern about buffering

➔ LSTFE system can operate in arbitrarily high-rate environment; is ideal for (short ladder) forward tracking systems as well as long-ladder central tracking applications.

DIGITAL ARCHITECTURE SIMULATION

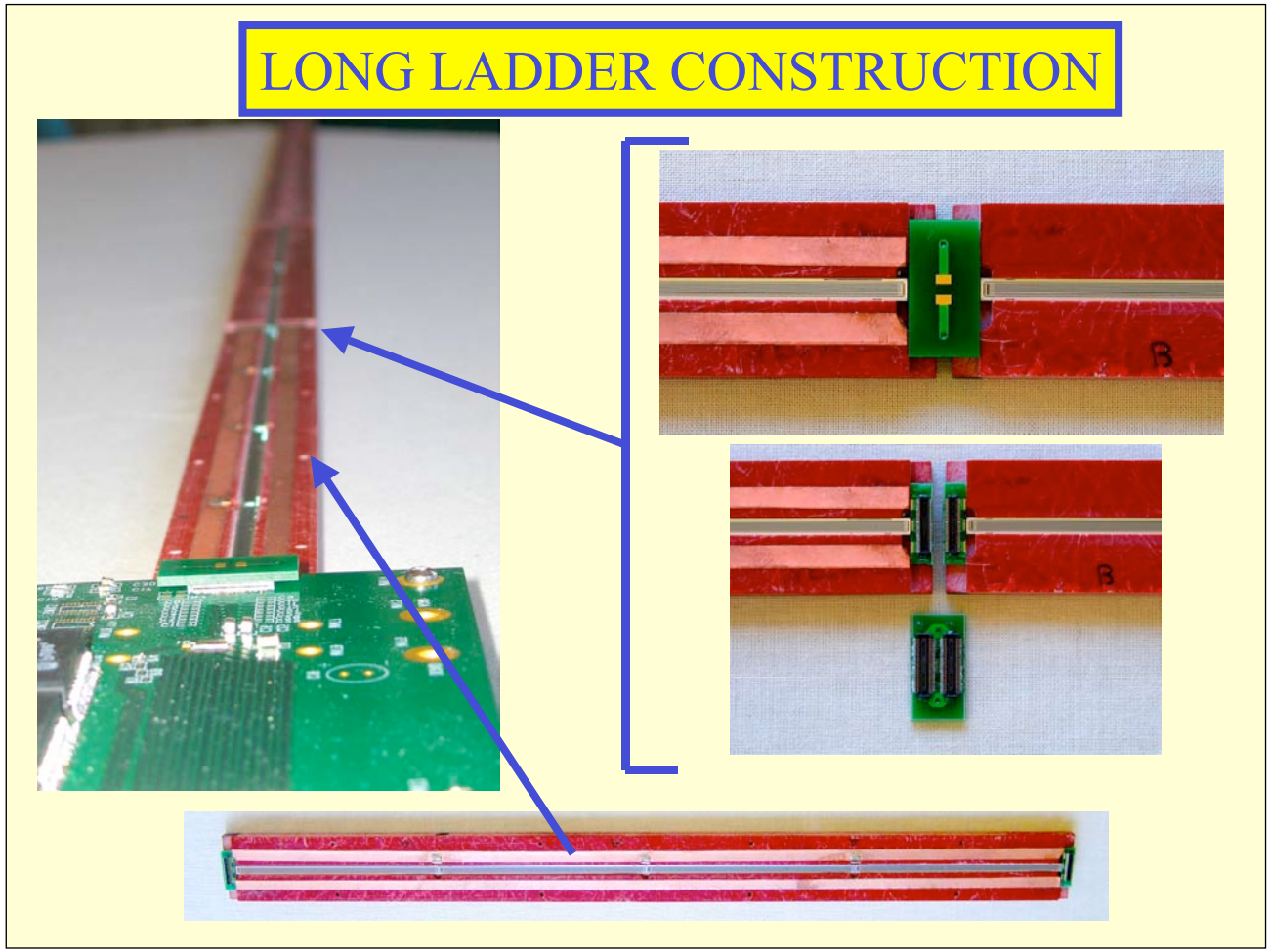
ModelSim package permits realistic simulation of FPGA code (signal propagation not yet simulated)



Simulate detector background (innermost SiD layer) and noise rates for 500 GeV running, as a function of read-out threshold.

Per 128 channel chip ~ 7 kbit per spill ➔ 35 kbit/second

For entire SiD tracker ~ 0.5-5 GHz data rate, depending on ladder length (x100 data rate suppression)



Using GLAST "cut-off" (8 channel) sensors; 237 um pitch with 65 um strip width

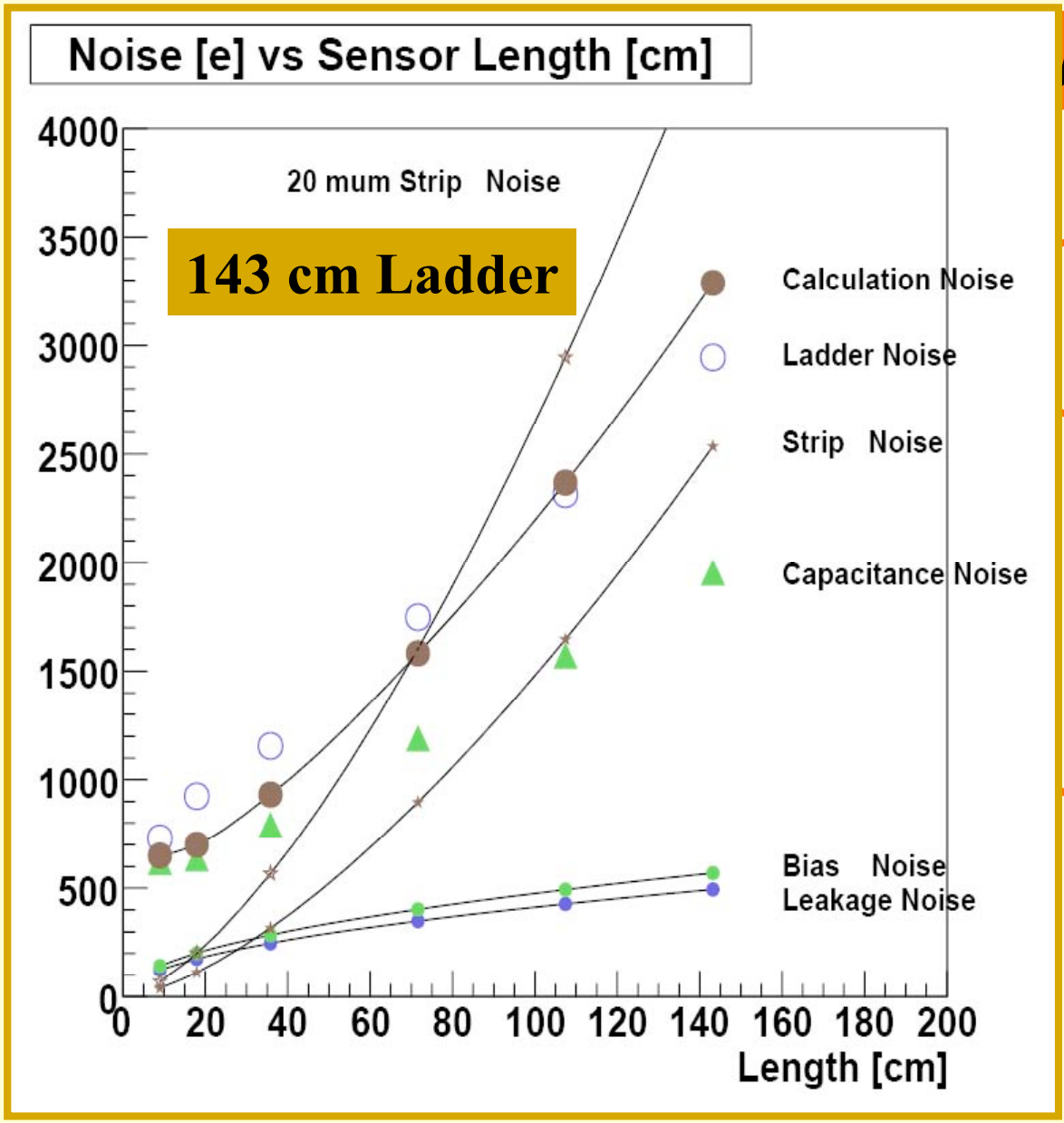
Have now studied modules of varying length, between 9cm and 72cm. [2/1/07: Now have up to 143 cm…]

Strip resistance for fine pitch could be an issue

are starting careful study and considering options

feedback to detector/module design.

Measured Noise vs. Sum of Estimated Contributions



Measured noise

Sum of estimates

Projected Johnson noise for 20 □m strip (not part of estimate)

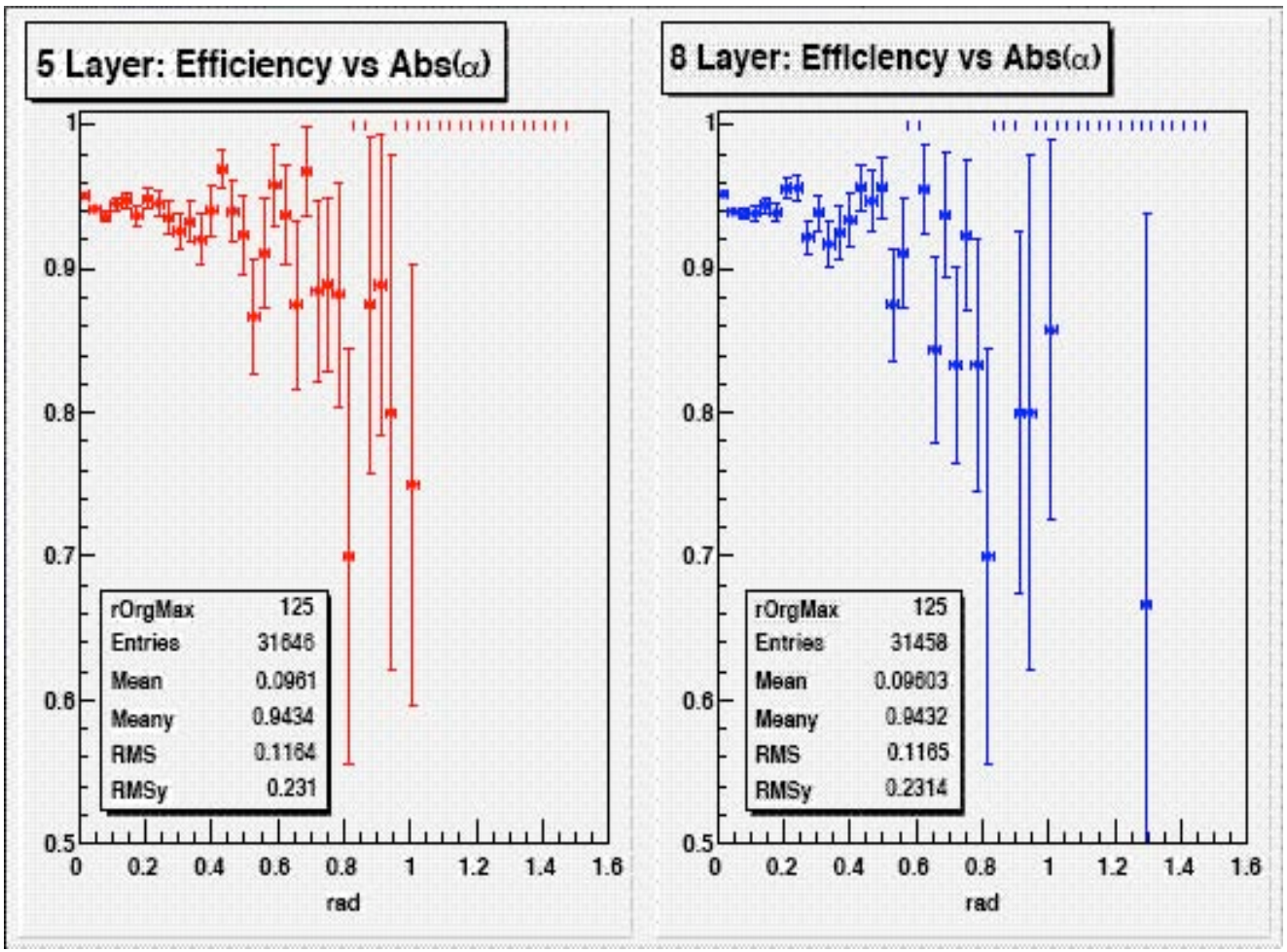
Estimated Johnson noise for actual 65 □m strip (part of estimate)

Simulation Results from the Santa Cruz Linear Collider Group

B.Schumm

Goals:

- Verify tracking efficiency for all-silicon tracking
- Verify track parameter resolution



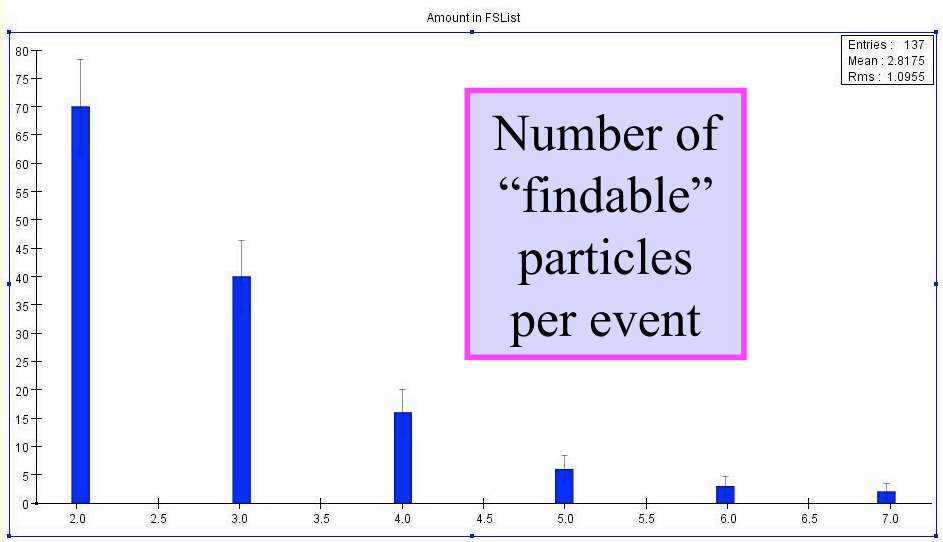
VXD based recon. loose 5% of tracks originate beyond r~3cm

track originate within beampipe has efficiency ~1

AxialBarrelTrackFinder Performance

Define “findable” particle as

- $P_t > 0.75$
- Radius of origin < 400 mm (require four layers)
- Path Length > 500 mm
- |cos□| < 0.8



Number of “findable” particles per event

~30% of findable track are found.

low!!

it may be improved w/ CAL and Z segment

Track Reconstruction: the trf toolkit

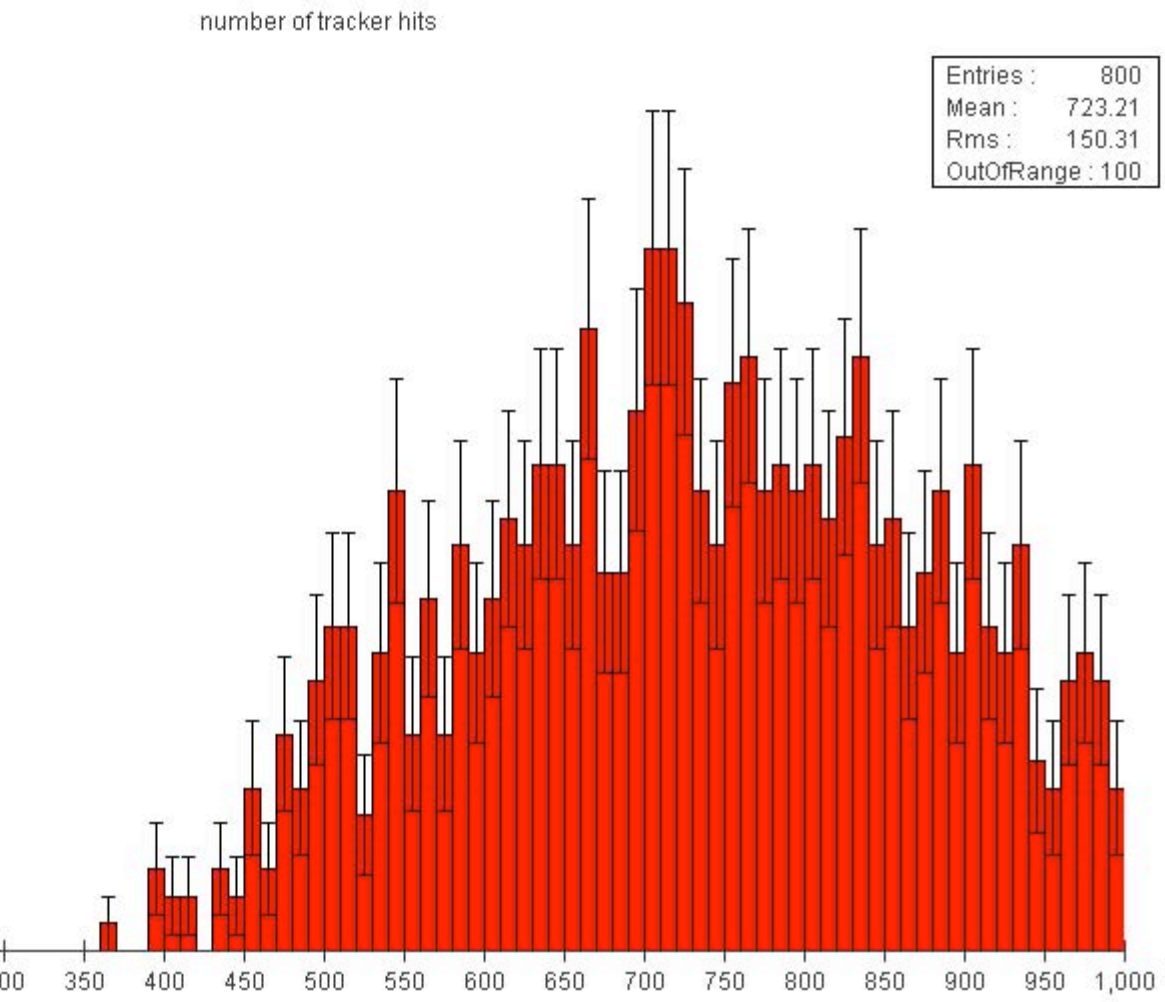
N.Graf

Develop track reconstruction package

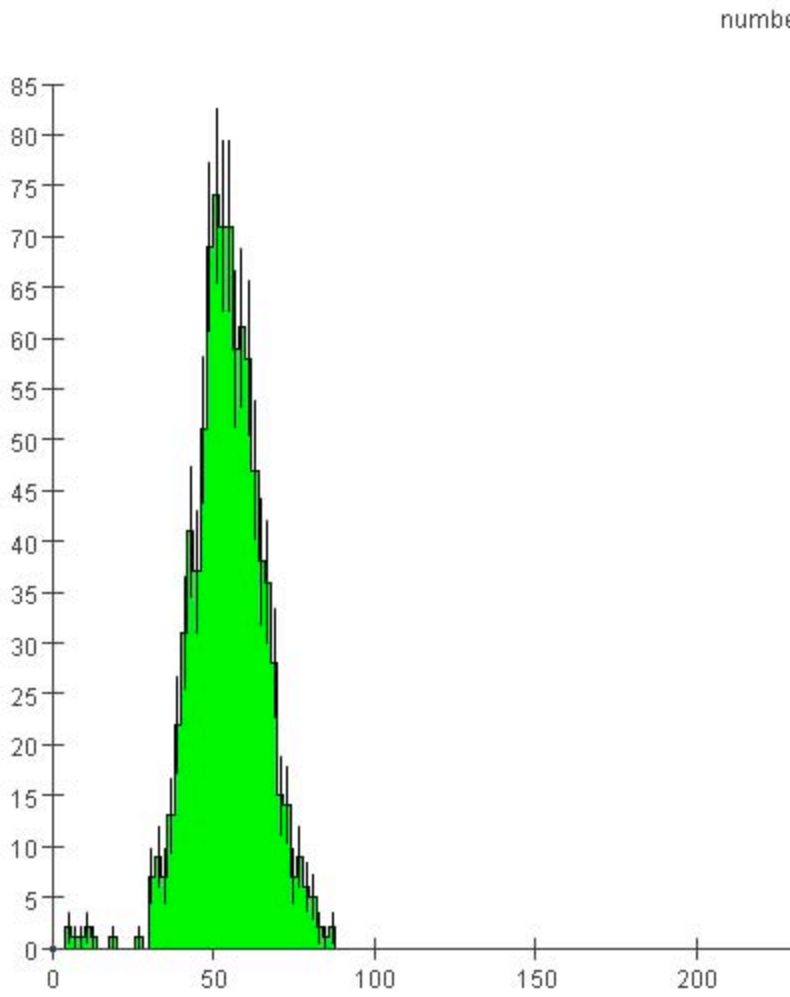
Definition: Digit -> Cluster -> Hit (finder)
trajectory space (fitter)

Track finder use a conformal mapping technique

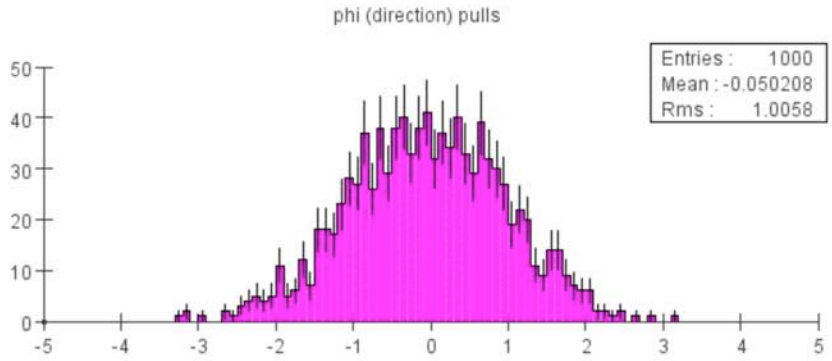
tt six jets # of Hits

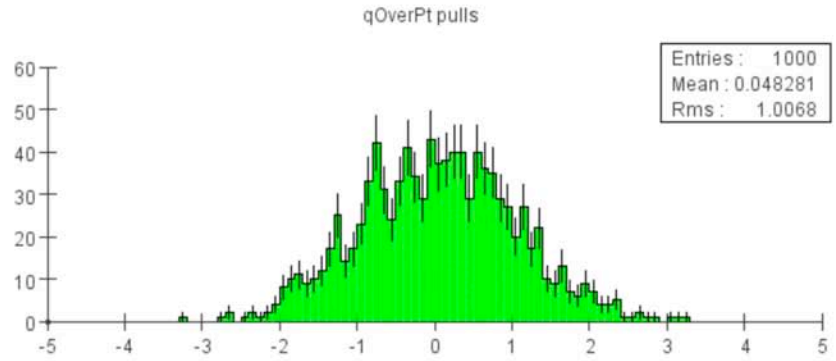


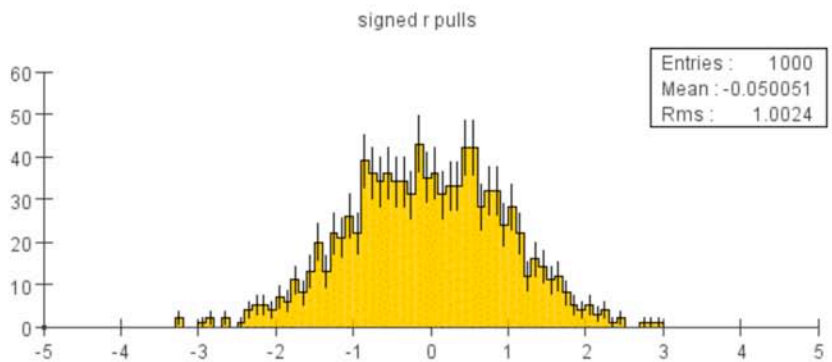
of tracks found

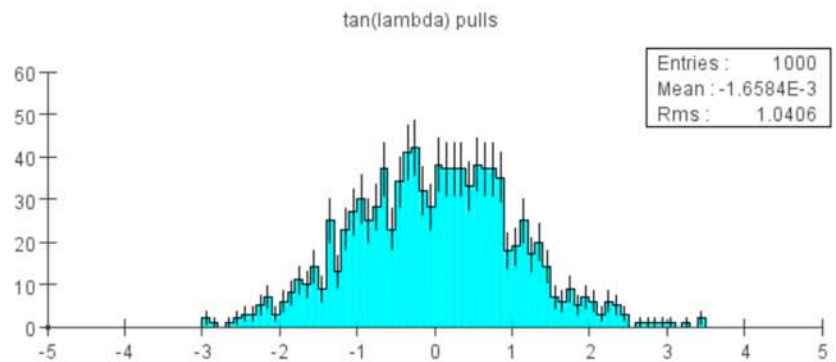


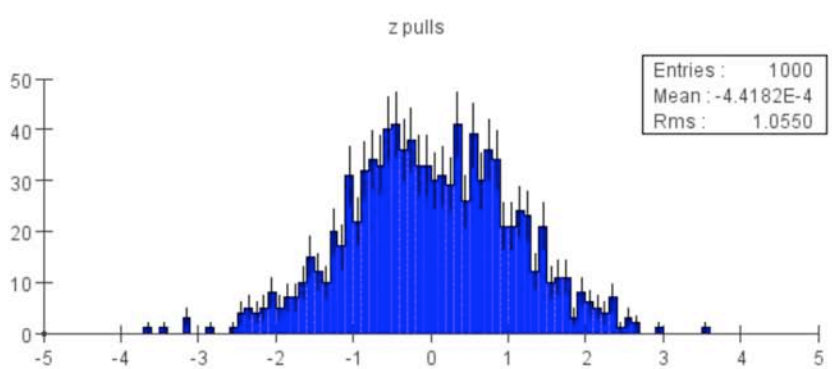
Full Kalman Fit pulls







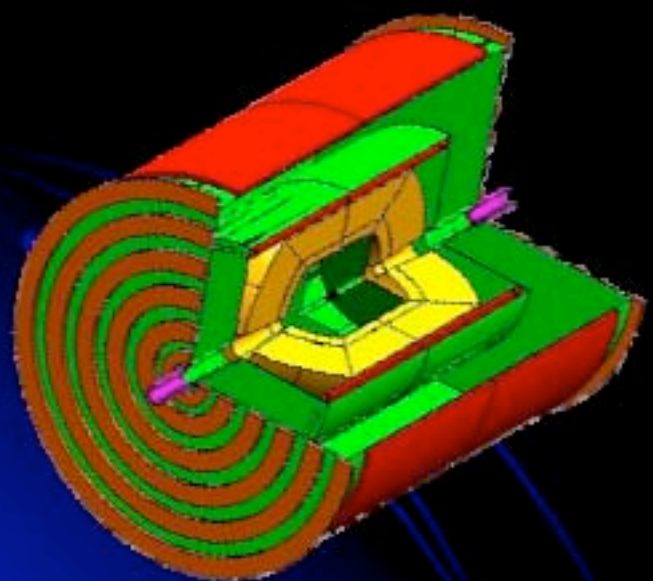




Single 10GeV muons in central region (5 2D + 5 1D pts).

Test Detector w/ELoss and MCS

Performance of the 4th Concept Tracking System

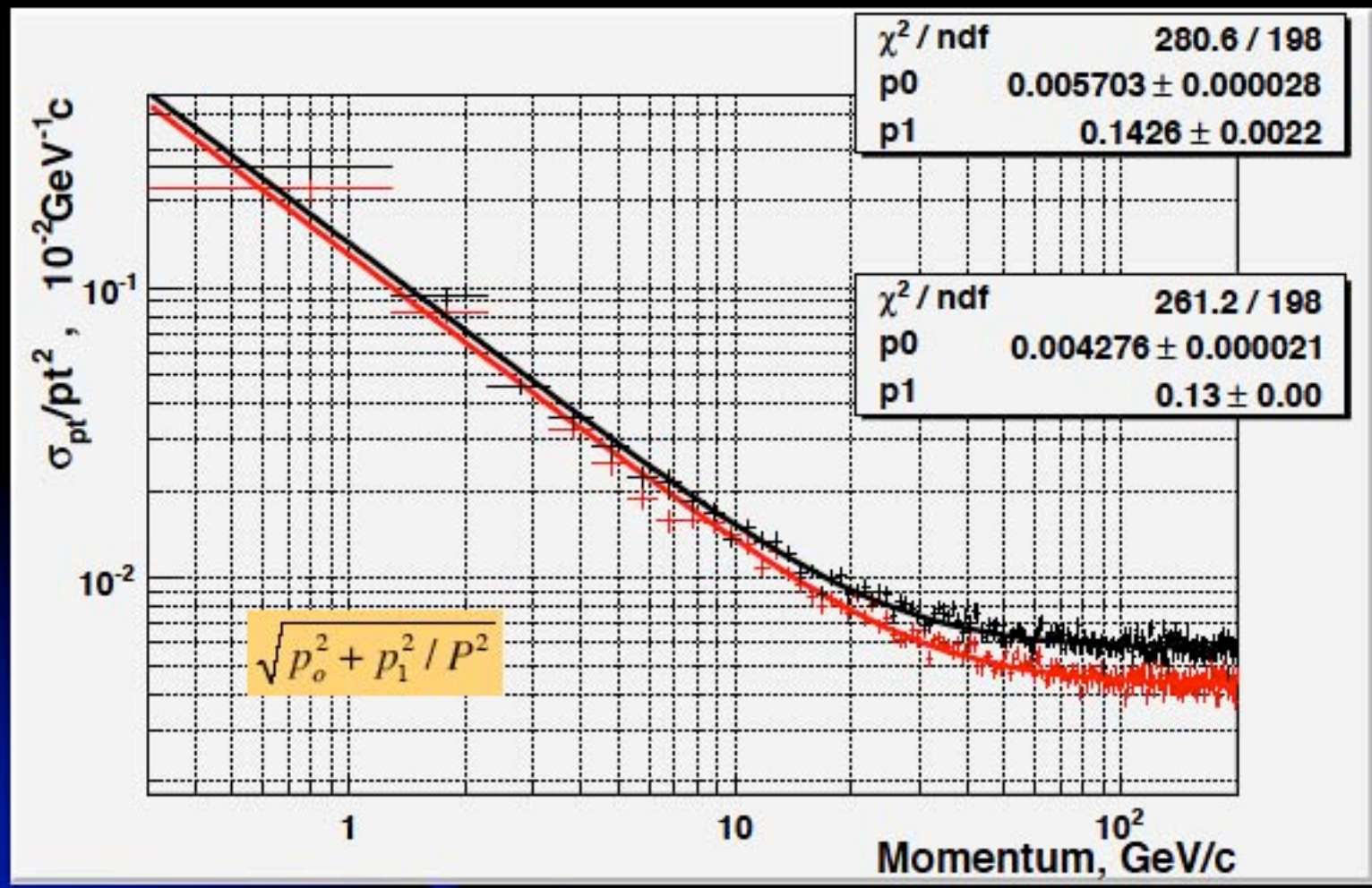


On behalf of 4th Concept Software Group

D. Barbareschi
V. Di Benedetto
E. Cavallo
F. Ignatov
A. Mazzacane
G. Terracciano

Progress in full simulation study

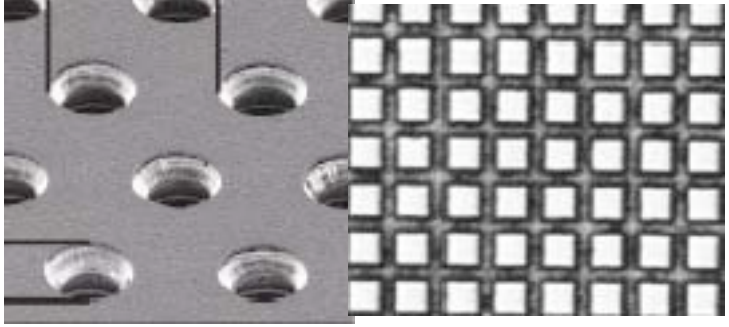
Momentum Resolution



- VXD + TPC
- 10 muons
- P = 0.5-200 GeV

- mMegas + Pads
- Pads only

Brief Introduction of TPC



Required position resolution ~ 100-120um $\Delta P/P \sim 10^{-4} P$

Good two track separation

Key Issue

Can we achieve this resolution @ 2.5m drift ?

High B field suppress transverse diffusion.

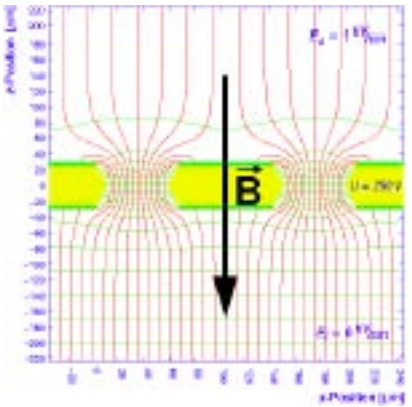
MPGD (GEM, Micromegas) -TPC is a candidate as it is free from ExB effect.

Many groups have been studied performances using small prototype.

R&D towards TDR

We are here

phase I	phase II(~3years)	phase III
"Demonstration"	"Consolidation"	"Design"
Small Prototype	Large Prototype	



besides the resolution

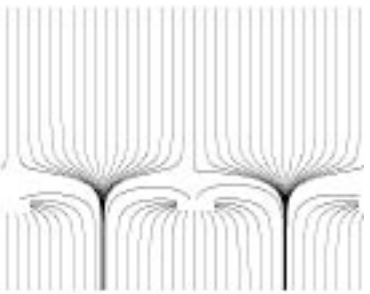
- gas study
- ion backdrift
- neutron background
- non-uniform B/E field
- software

Readout method

- standard pad readout
- std+charge dispersion
- advanced pixel readout

electronics

material budget at endplate



Tsinghua U. group has joined LC-TPC collab.

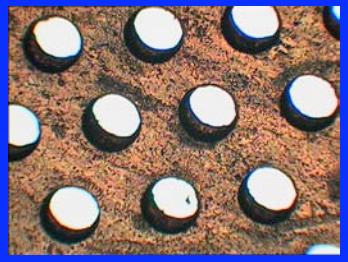
though Y.Gao has been a member already

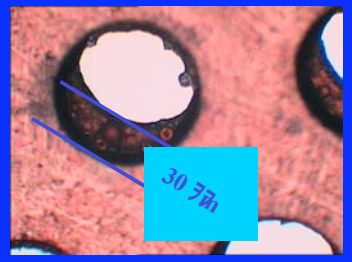
"Study of GEM and TPC in Tsinghua Univ." Yulan Li

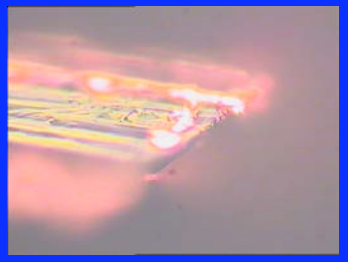
- **Projects under study:**
  - ✓ Experimental study of GEM detectors
  - ✓ GEM foil etching
  - ✓ Electronic Readout
    - ➢ FET array readout for X-ray imaging
    - ➢ ASIC
  - ✓ TPC based on GEM readout

□100□m GEM foil etching

- Based on FPCB Technology



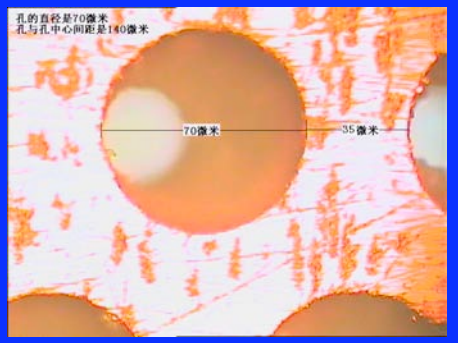


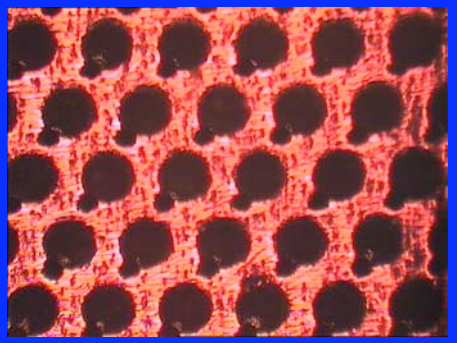


- Based on general FPCB manufacturer, failed in the alignment of mask (30 □m/100□m)

□70□m GEM foil etching

- Based on laser Technology (Drilling)
- etching copper, then laser drilling





- Low efficiency, also failed in alignment

They decided to setup a whole system !

Cu etching

Kapton etching

Effective area up to 30cm x 30cm

will be ready in 2~3 months

They have own small prototype TPC

Future working plan

- Continue study on SP@ Tsinghua
  - ✓ Optimal working gas
  - ✓ Gating: simulation, different GEM foil conf.
  - ✓ Continue study on GEM foil manufacture
  - ✓ Test under magnet
- Join the CDC/Philippine LP work on GEM panels
- Join the design team of LCTPC electronics

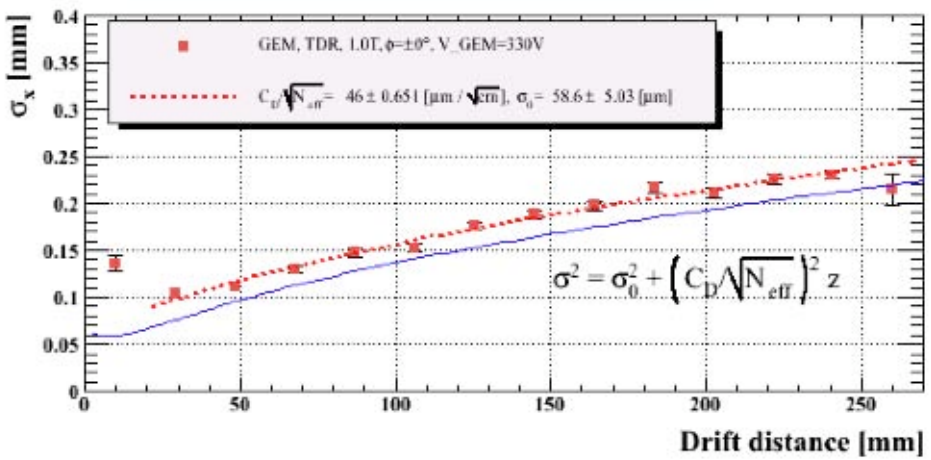
The preliminary results of MPGD-based TPC performance at KEK beam test

Y.Kato

pi beam at KEK-PS
w/ PCMAG (1T)

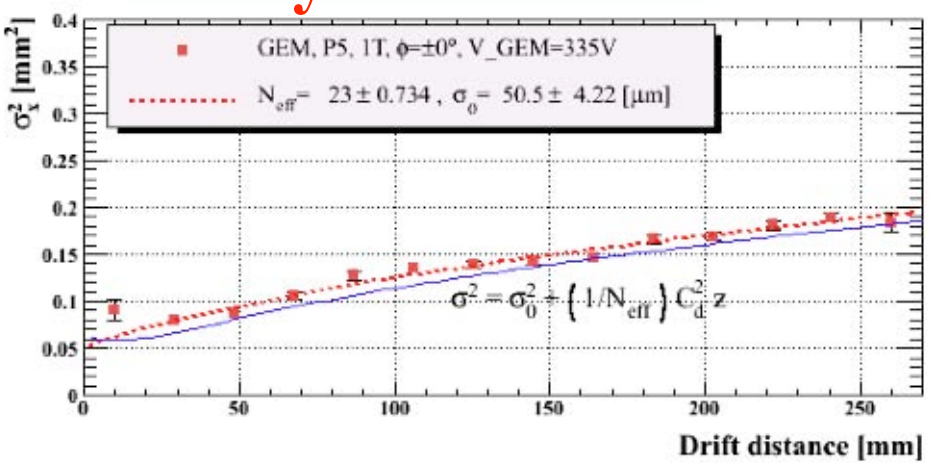
Spatial resolution

GEM



TDR
$N_{\mathrm{eff}} = 21.4 \pm 0.3$

preliminary result

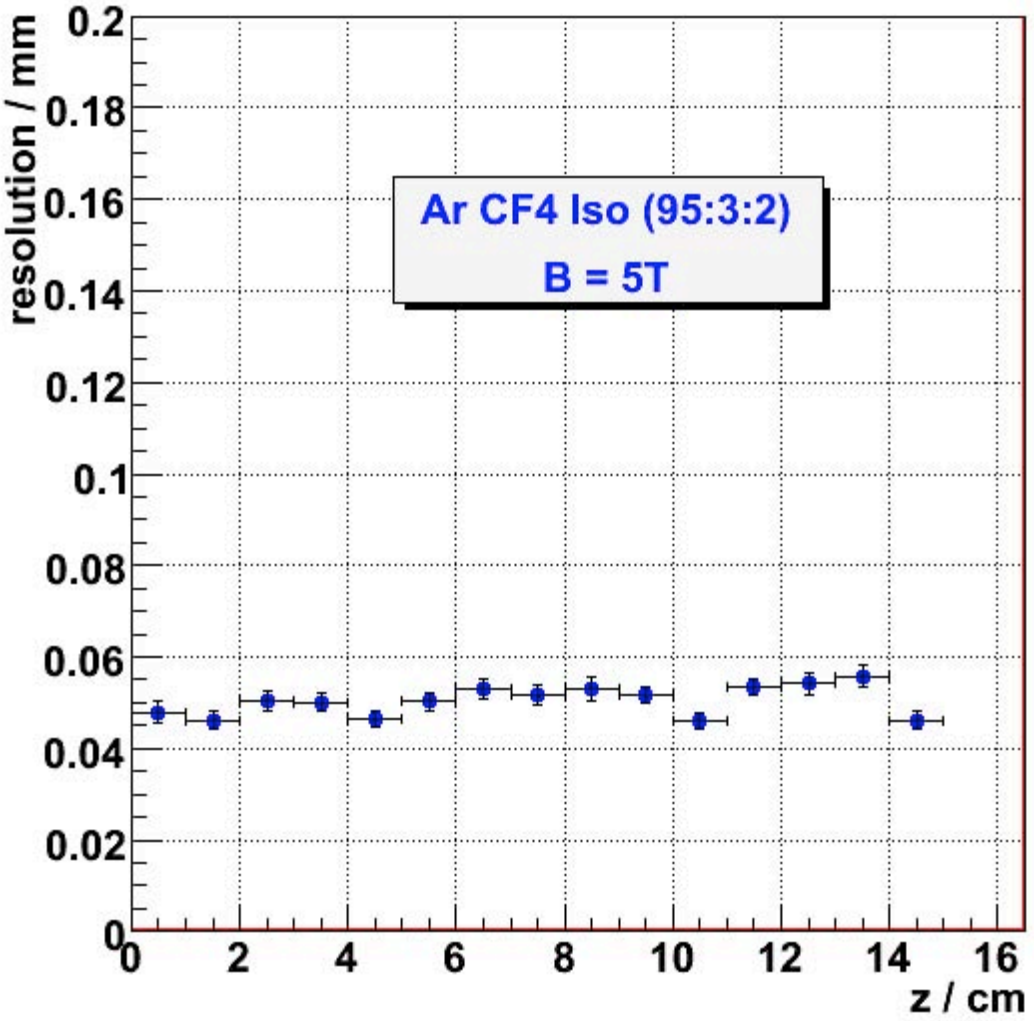


P5
$N_{\mathrm{eff}} = 23.0 \pm 0.7$

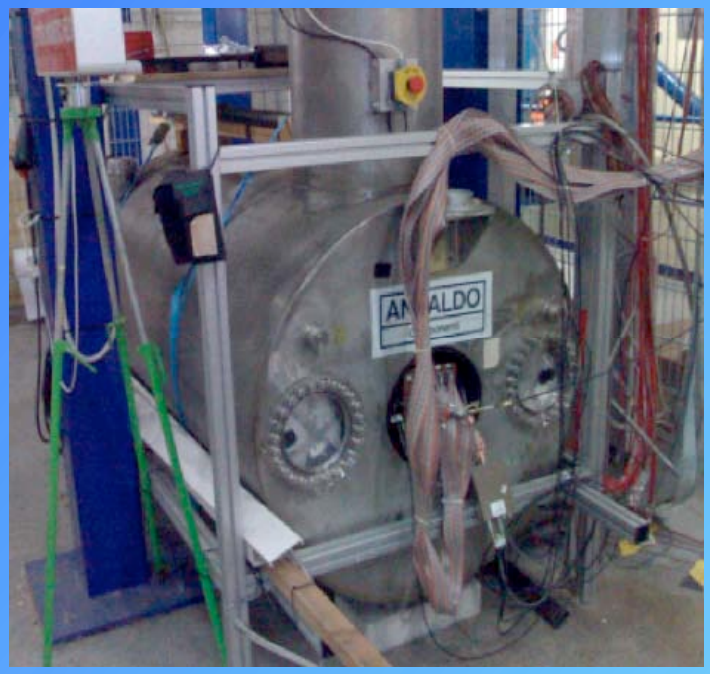
Micromegas TPC studies in a 5 Tesla magnetic field with a resistive readout

P.Colas

Resolution = 50 μ independent of the drift distance



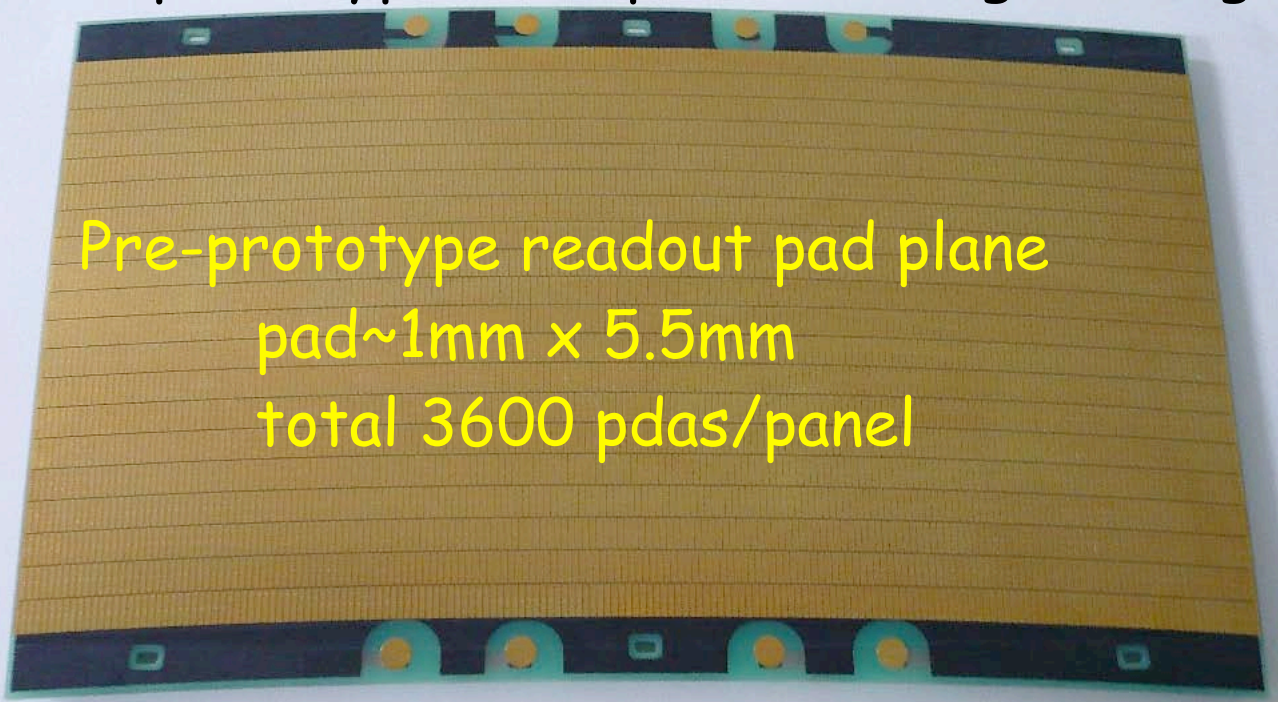
using 5T mag.@DESY



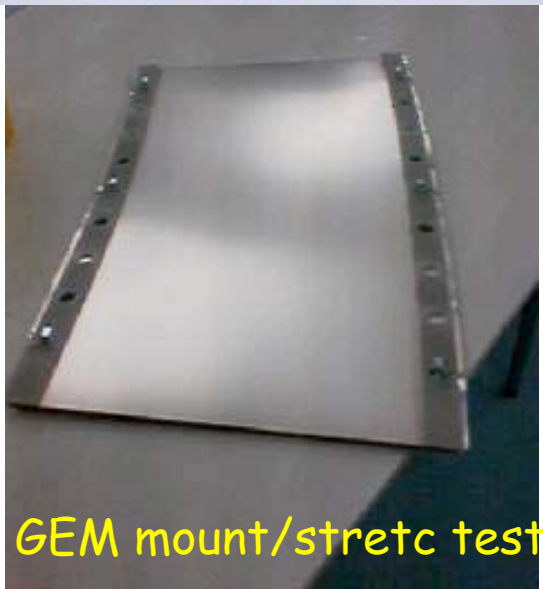
Prototype test for LCTPC

A.Sugiyama

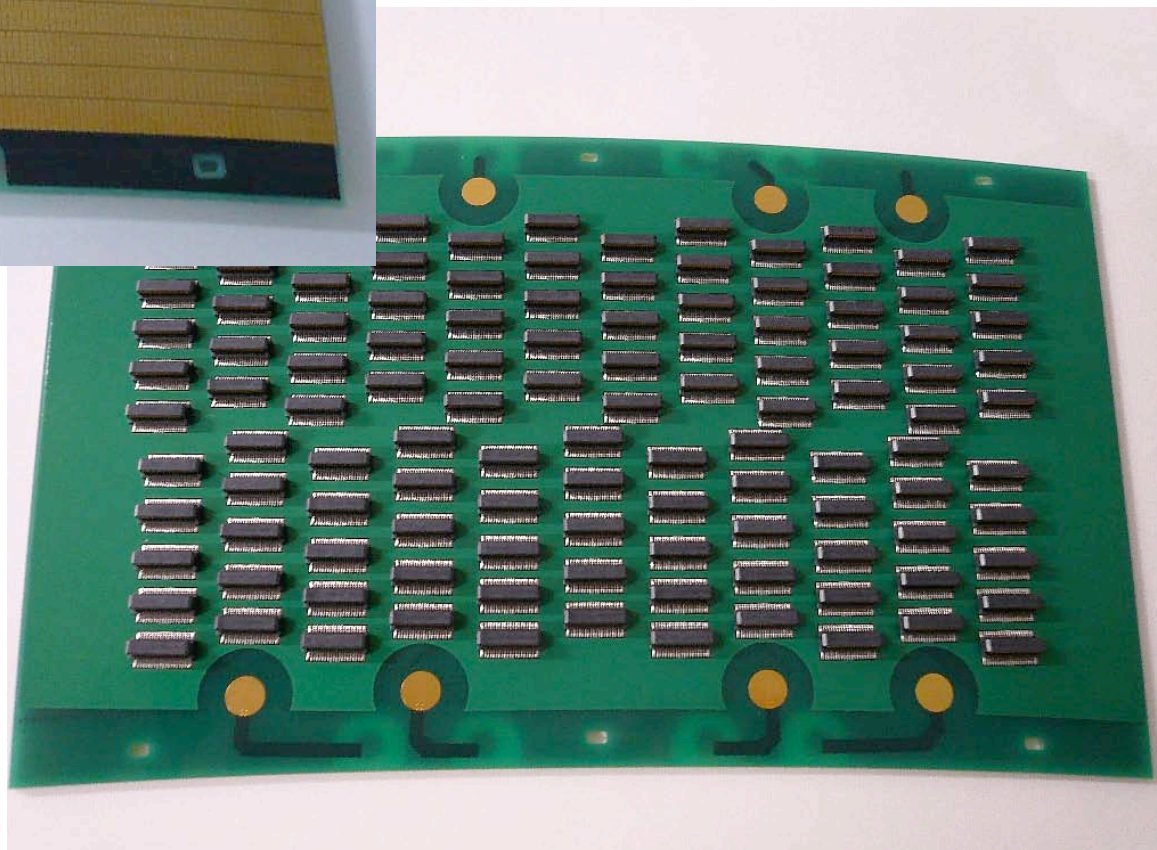
Pre-prototype GEM panel for engineering R&D of LP1



Pre-prototype readout pad plane
pad~1mm x 5.5mm
total 3600 pdas/panel



GEM mount/stretc test



A Simulation Study of GEM gating at ILC-TPC

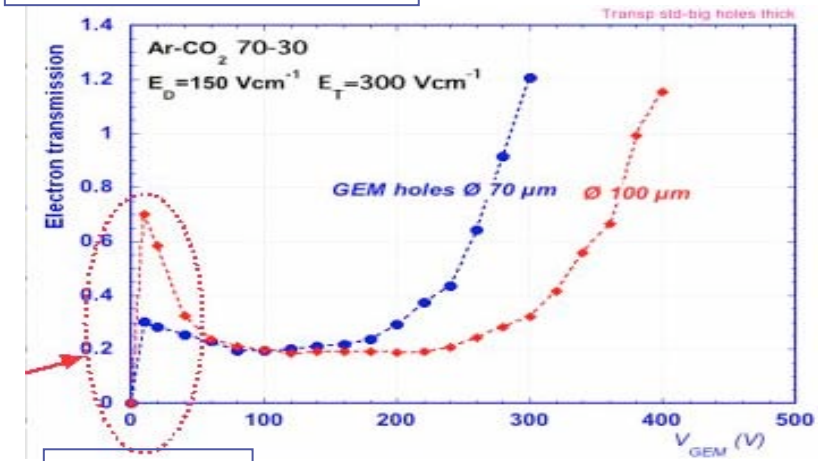
A.Aoza

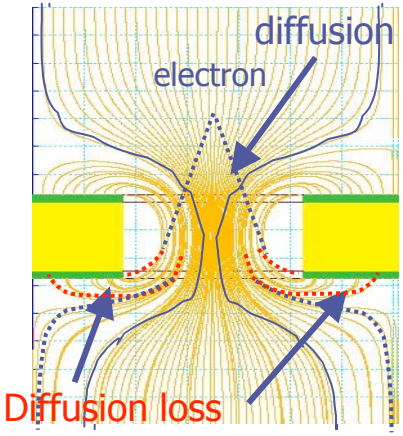
Electron transmission is important

•HOLE DIAMETER EFFECT

transmission = collection x extraction

Measurement by Sauli



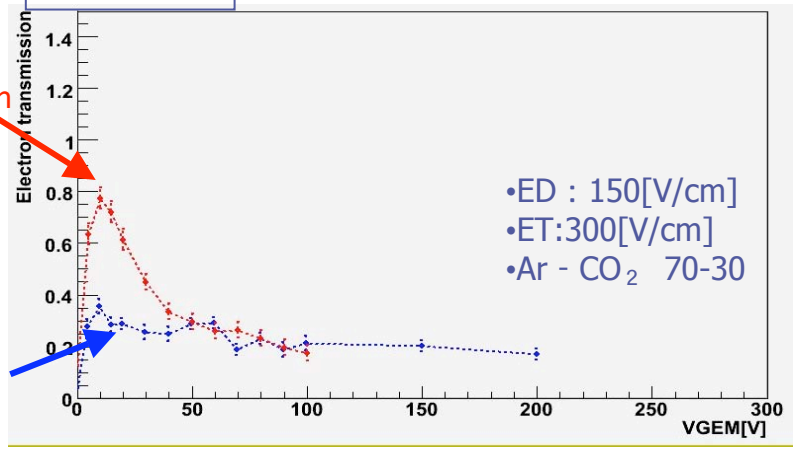


collection : ratio of Ed:Eh
hole size

extraction : Ed:Eh:Et
diffusion@highE

simulation

Φ100μm



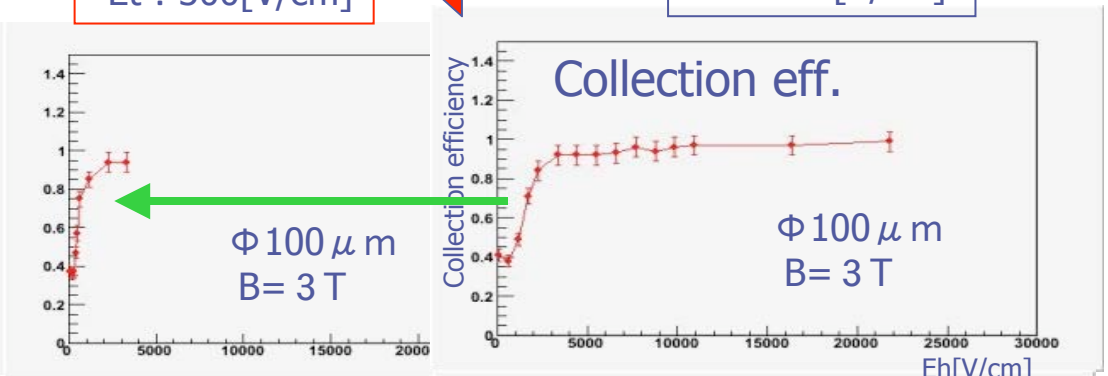
ϕ70μm

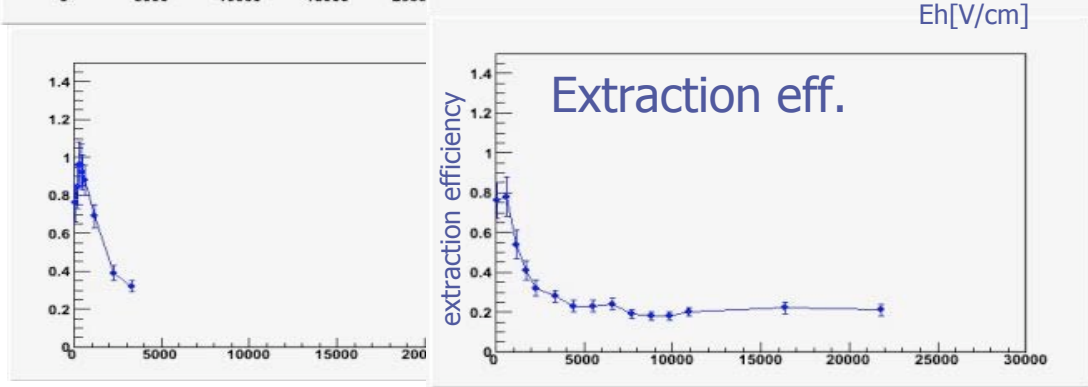
Proper "Step size" in "Garfield" must be chosen !!

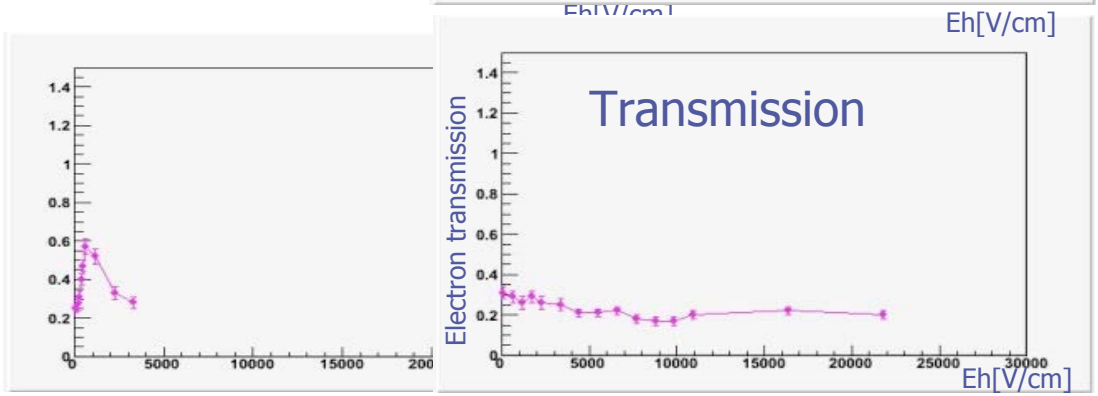
ArCF4 in magnetic field

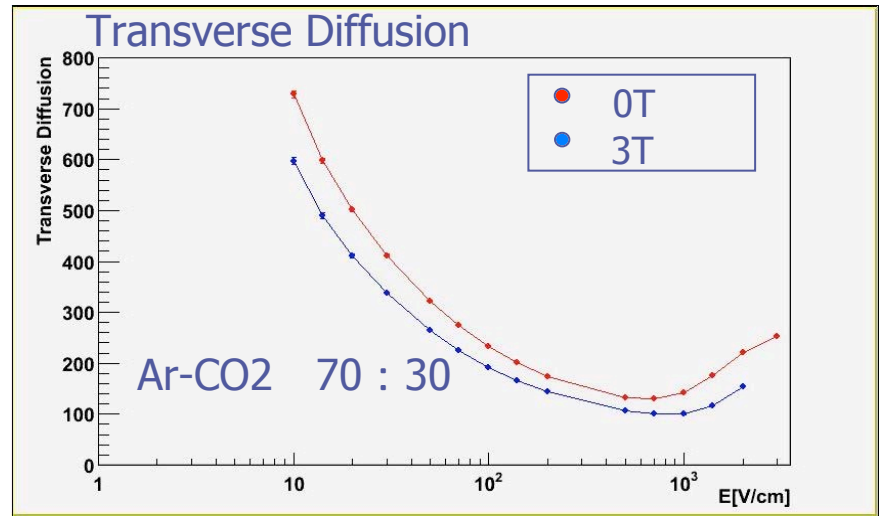
•Ed : 50[V/cm]
•Et : 300[V/cm]

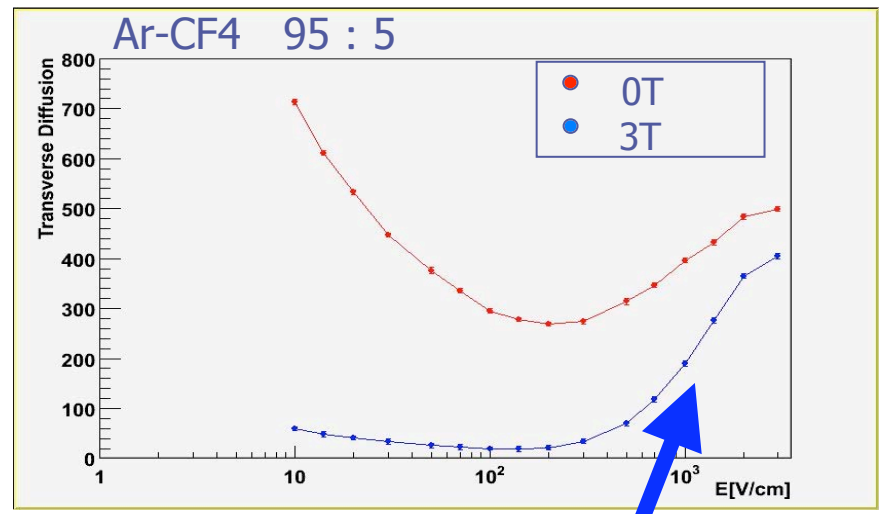
•Ed : 150[V/cm]
•Et : 300[V/cm]











Gas which has
low diffusion even at high E region
is necessary
to obtain high transmission w/ GEM gating

We will try to find a better operation condition
or better structure of GEM