# RPC-DHCAL Progress & Status

*H.Weerts*

Argonne NATIONAL LABORATORY


Research done as part of program of CALICE collaboration with main efforts from:

- Argonne National Lab
- Boston Univ.
- Univ. of Chicago
- Fermilab
- Univ of Iowa
- Univ. of Texas, Arlington

BILCW07, Beijing, February 4 – 7, 2007

# Outline

## Introduction

## Vertical Slice Test

Test of ~8 chambers with complete electronics
At MTBF in Spring 2007

- Mechanical
- DCAL2 chip
- Pad and Front-end boards
- Data concentrators
- Data collectors
- DAQ software
- Beam telescope, HV, gas

## Prototype Section plans

Measurements with complete 1m$^3$ section
Hopefully starting in 2008

- Funding

# Introduction I

Big Picture: There are several technologies being pursued as options for HCAL for ILC detectors.

Precision required/aimed for jet energy demands new and novel approaches $\sigma = 30\%\sqrt{E_{jet}}$

Either use PFA, which requires very fine longitudinal and transverse segmentation OR compensating calorimetry ( for all components ( EM, charged & Neutral).

Options: Vary from scintillator (tiles or fibers) with analog readout to gas based calorimeters with digital/multibit readout.

All these options are either new technologies or have aspects that need to be verified before they can be used for an ILC HCAL

Lot of efforts by many

In this talk present progress on HCAL for a PFA application:

Gas calorimeter using RPC's and a digital readout system ( not coupled)

Transverse sampling is 1x1 cmxcm ➔ high channel count

# Introduction II

Detector choice
RPC, simple, large signals, easy transverse segmentation

Readout
1x1cm$^2$ sampling, using digital ( =1 bit) readout

Use with RPC, but can be used for others (GEM, etc)

Goal: Try to make this work and prove feasibility for ILC

Transverse sampling is 1x1 cmxcm ➔ high channel count

Example: A 1m$^2$ plane has 10,000 channels = complete tilecal of ATLAS

A 1m$^3$ typical "module" for a testbeam consists of 40 planes ➔ 400K channels. This is a LARGE undertaking ( make stable and understood). Never done before.

Approach: Build a vertical slice, with the final components and data handling and collection system that will be used for a 1m$^3$ test, corresponding to ~2000 channels i.e. proof of principle

Goal: Verify that noise, random and coherent, is under control, that channels are stable, can be monitored and calibrated, proof stable operations, verify response to cosmics and testbeam.

After "proof of principle" build the 400,000 channel system on same technology

# Staged approach

I R&D on RPCs
Develop concept of digital readout system

→ **RPC Tests with cosmic rays and in particle beams** — **Done**

II Prototyping of RPCs for prototype section (PS)
Prototyping of all components of digital readout for PS

→ **Vertical slice test in particle beam** — **Planned for 2007**

III Construction of a 1m$^3$ Prototype Section with RPCs

→ **Detailed test program in Fermilab test beam** — **Planned for 2008**

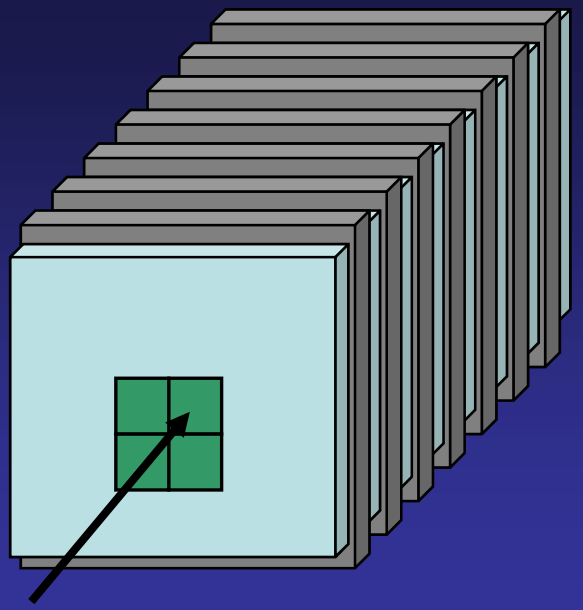
IV Further R&D on RPCs and electronic readout system — **Earliest in 2009**

V Scalable prototype

→ **Detailed test program in test beam** — **Earliest in 2010**

# Vertical Slice Test

# Vertical Slice Test



Uses the 40 DCAL ASICs from the 2nd prototype run

Equip ~8 chambers with 4 DCAL chips each

256 channels/chamber
~2000 channels total

Chambers interleaved with 20 mm copper - steel absorber plates

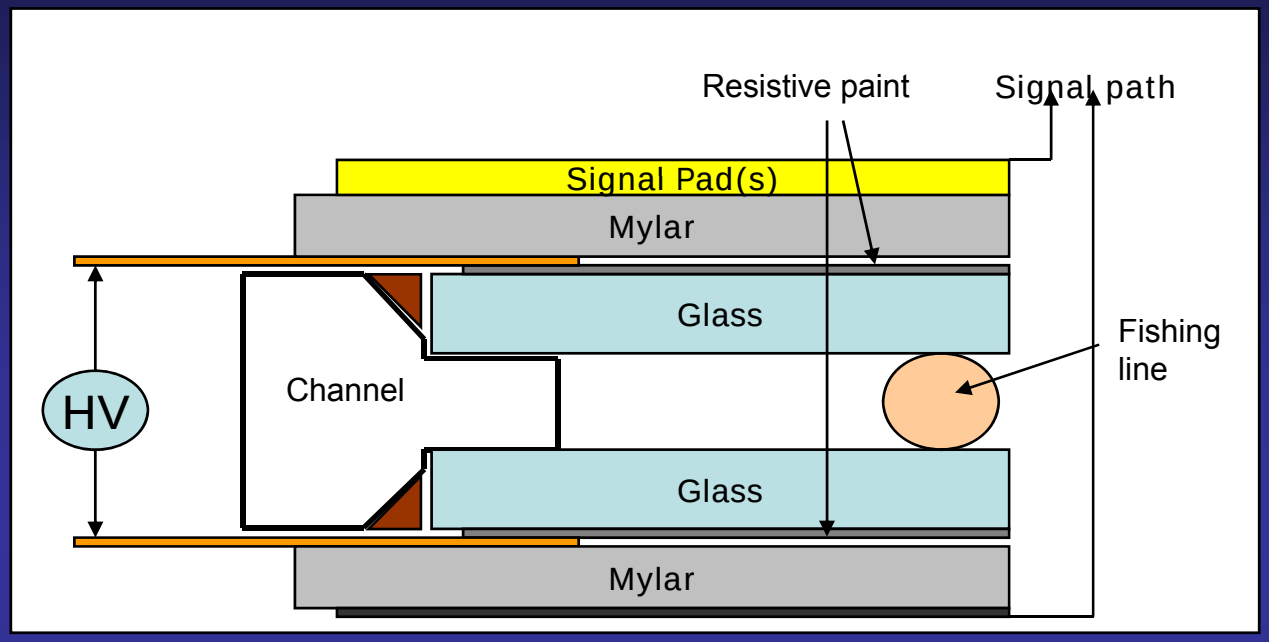
Electronic readout system (almost) identical to the one of the prototype section

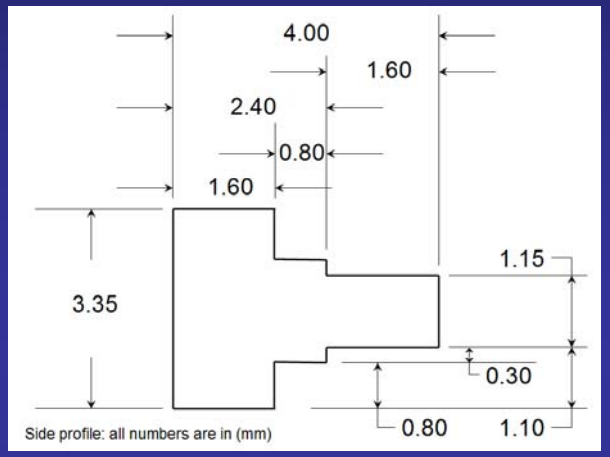
Tests in MTBF beam planned for Spring 2007

→ Measure efficiency, pad multiplicity, rate capability of individual chambers
→ Measure hadronic showers and compare to simulation

Validate RPC approach to finely segmented calorimetry
**Validate concept of electronic readout**

# Mechanical: RPC chamber design



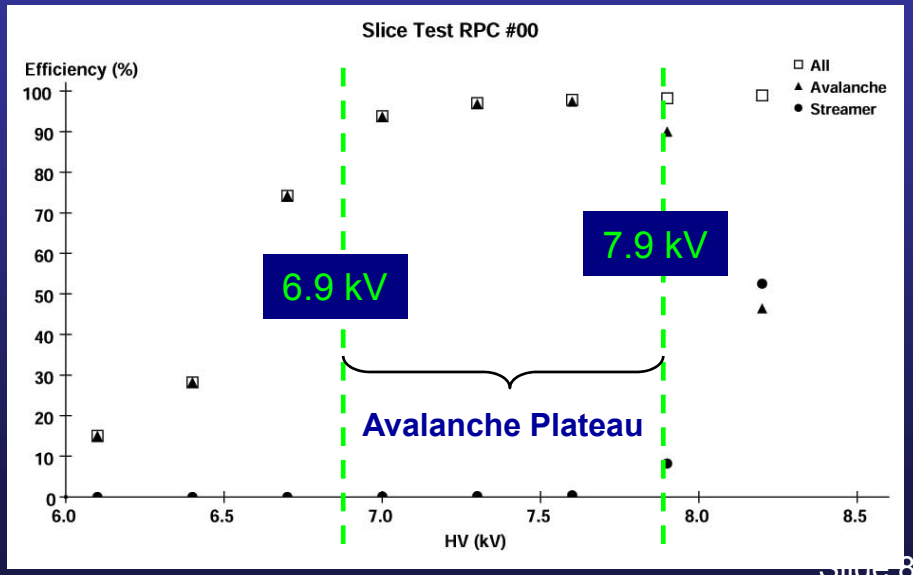

**New design** with simplified channels

**1st chamber assembled and tested**

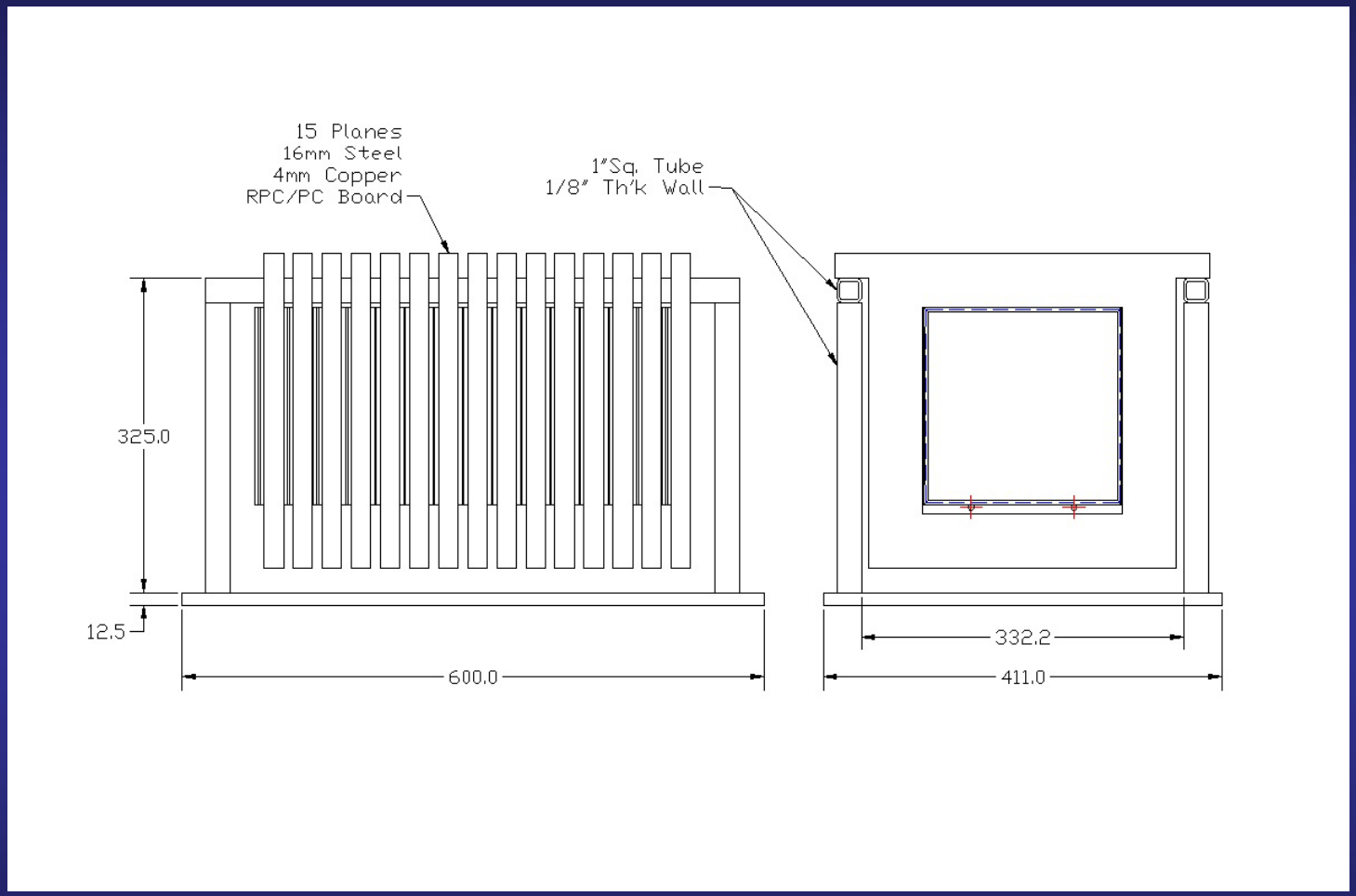
→ **Excellent performance**

**Thickness ~3.5 mm**

Material in hand for remaining chambers



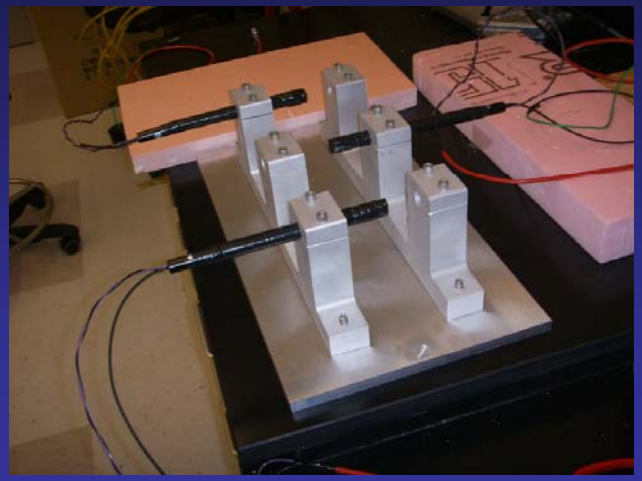
# Mechanical: Stack for Vertical Slice Test




Design accommodates 20 x 20 $cm^2$ RPCs as well as 30 x 30 $cm^2$ GEMs

Stack is assembled

# Beam telescope, HV, and gas



## Beam telescope

6 counters (3 x (1 x 1 $cm^2$) + 1 x (4 x 4 $cm^2$) + 2 x (19 x 19 $cm^2$)
Mounted on rigid structure
Counters in hand!

## HV modules

Need separate supplies for each chamber
Modules (from FNAL pool) being tested

With additional RC-filter perform similarly to our Bertan unit in analog tests (RABBIT system)
Digital tests satisfactory too

## Gas system

Need manifold for 10 chambers (in hand!)
Need approval for gas tanks (safety issue)

# Electronic Readout System for Prototype Section

Suitable for both RPCs and GEMs

40 layers à 1 $m^2$ → 400,000 readout channels

**More than all of DØ in Run I; ATLAS tilecal HCAL is 10,000 channels; ATLAS ECAL 200,000**

I Front-end ASIC

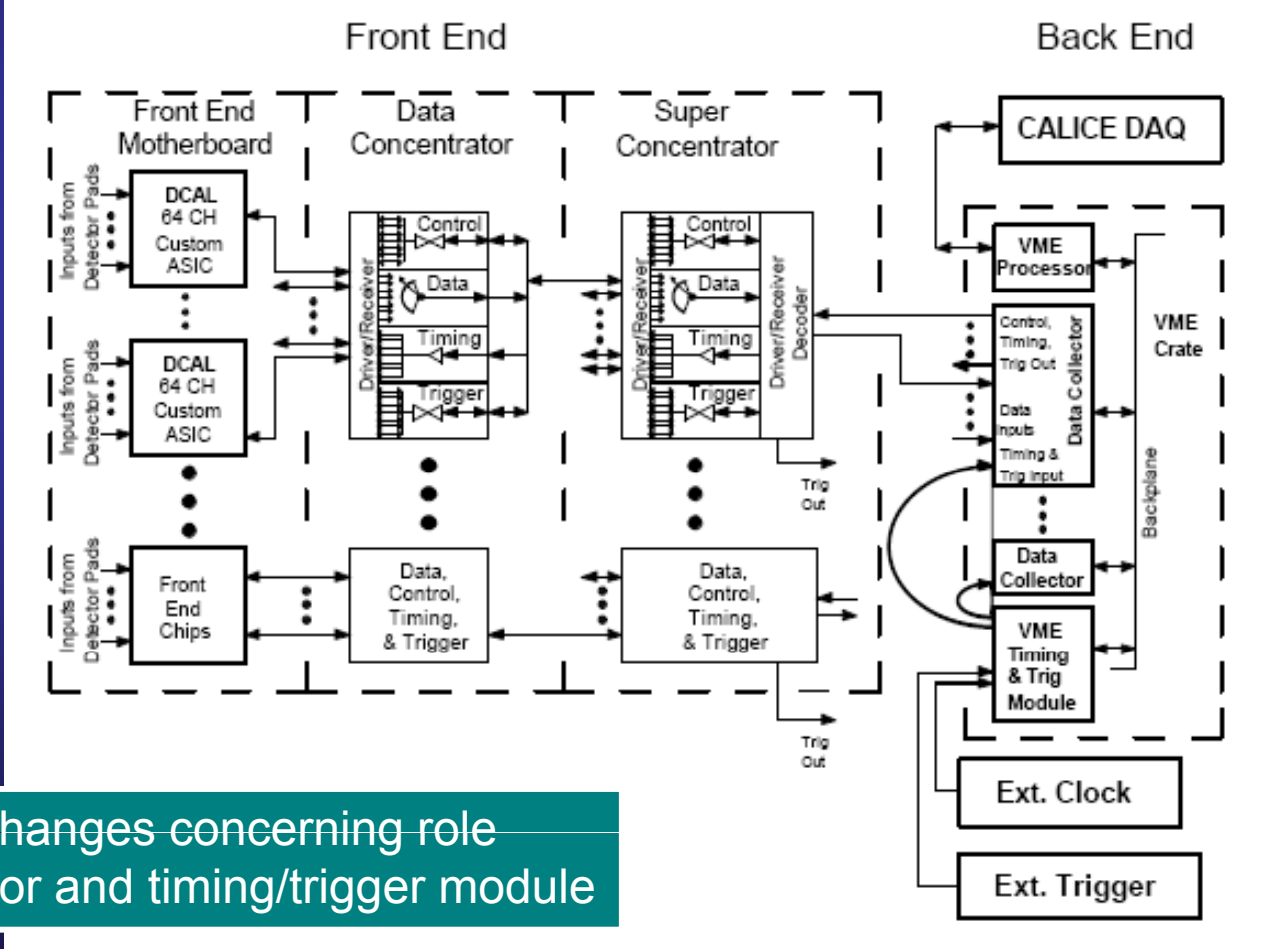
II Pad and FE-board

III Data concentrator

IV Super Concentrator

V VME data collection

VI Trigger and timing system




Some recent changes concerning role of data collector and timing/trigger module

# DCAL chip

**Design**

→ chip specified by Argonne
→ designed by Fermilab

**1st version**

→ extensively tested with computer controlled interface
→ all functions performed as expected

**Redesign**

→ decrease of gain by factor 20 (GEMs) and 100 (RPCs)
→ decoupling of clocks (readout and front-end)

**2nd version**

→ submitted on July 22nd
→ 40 chips (packaged) in hand

**Test board**

→ redesign of test board (changes in pin layout etc.□ complete
→ boards fabric□ted
→ chip mounted on tes□ board

**Testing (2/40)**

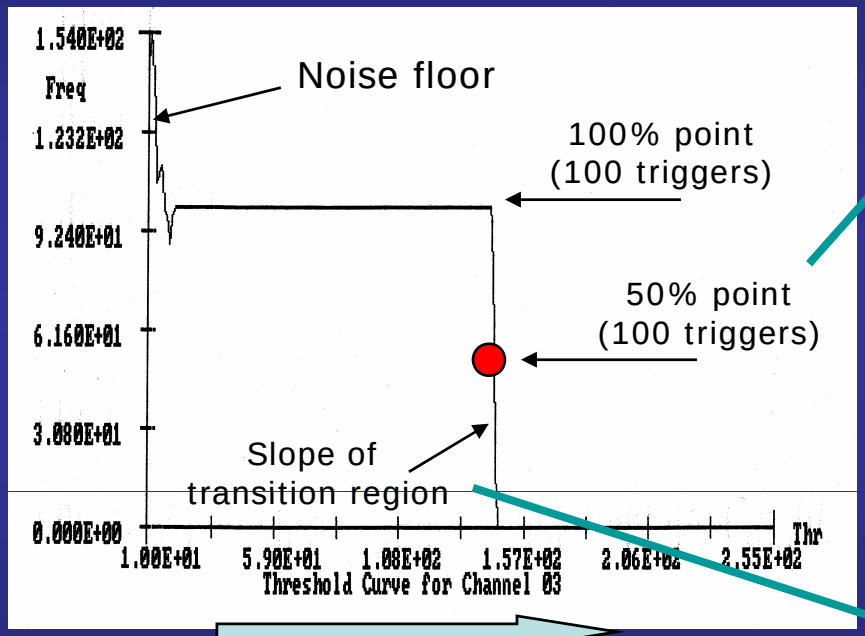
→□all software written
→ te□ts ongoing

Reads 64 pads
Has 1 adjustable threshold
Provides
- Hit pattern
- Time stamp (100 ns)

Operates in
- External trigger or
- Triggerless mode

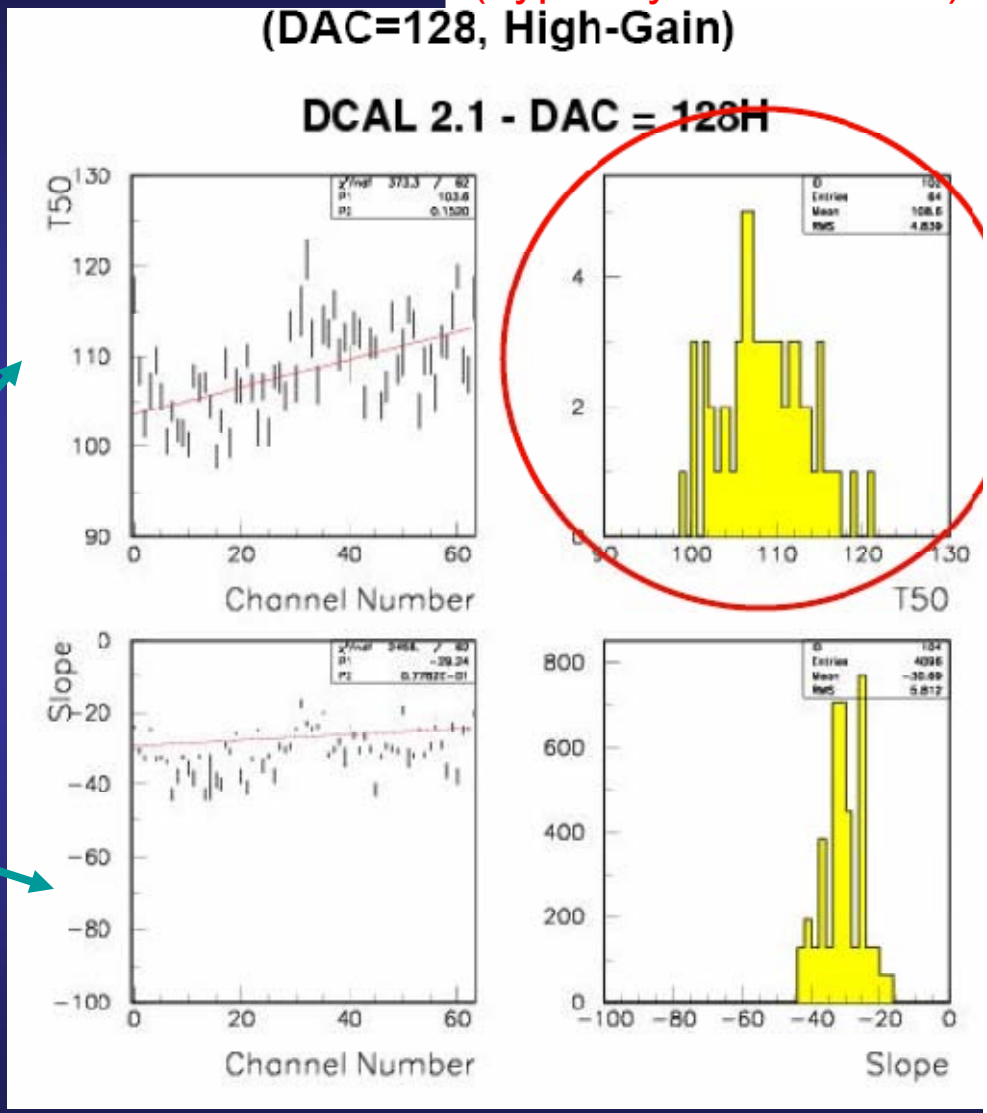
# DCAL2 Testing I

Threshold Response Tests
Typical Channel
(DAC=192, High-Gain)
On-board Q-inj, ext. trig., pipeline enabled



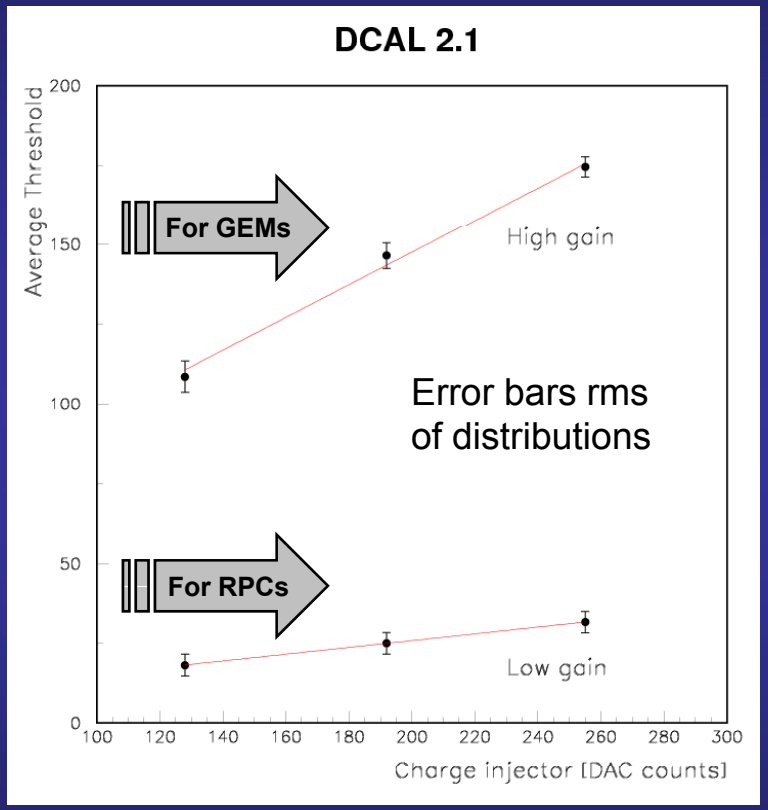

Threshold scan

Spread ~20 DAC Cnts
(Typically ~10-15 Cnts)




**Threshold scans…**
All channels OK, except
Channel #31 shows some anomalies
(understood, no problem)

# DCAL2 Testing II




Ratio of high to low gain

$R_{h/l} = 4.6 \pm 0.2$

(roughly as expected)

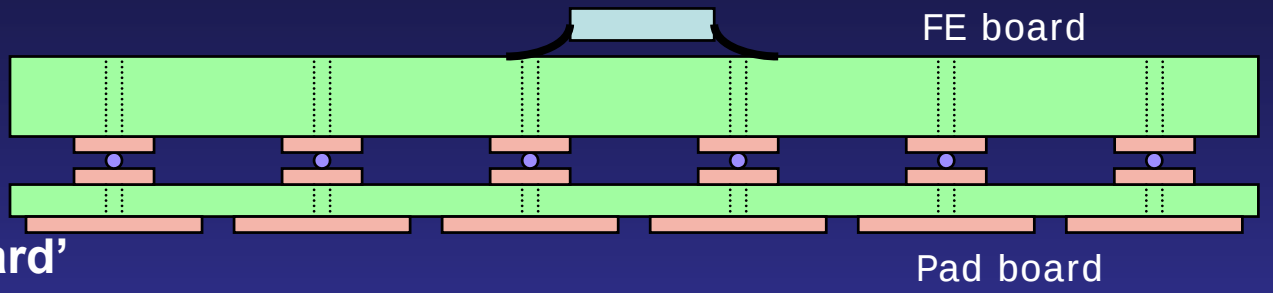
**Other tests**

- Sort out small problem with trigger
  (understood, can be circumvented)
- External charge injection
  (ongoing, first results look good)
- Noise floor
  (tests complete, results OK)

Chip can be used for vertical slice test
Small modifications still necessary for production

# Pad- and Front-end Boards I

**New Concept**

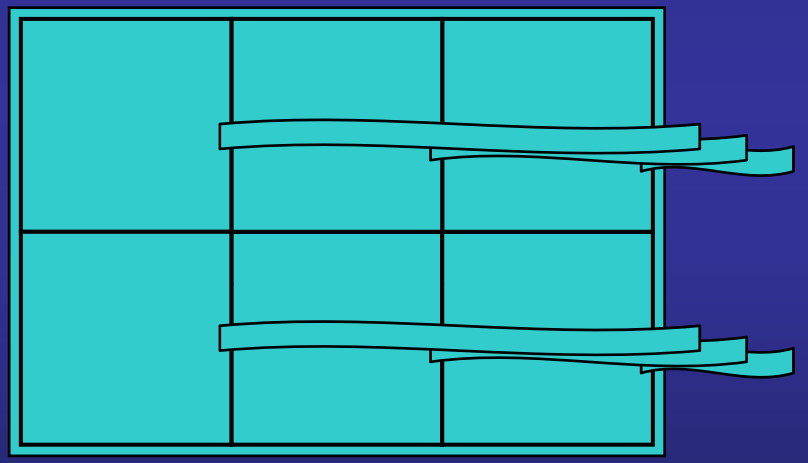



**Split old 'Front-end board'**

'front-end board' highly complex and difficult
blind and buried vias + large board => (almost) impossible to manufacture
split into two boards to eliminate buried vias

**Pad boards**

four-layer board containing pads and transfer lines
can be sized as big as necessary
relatively cheap and simple
vias will be filled



**Front-end boards**

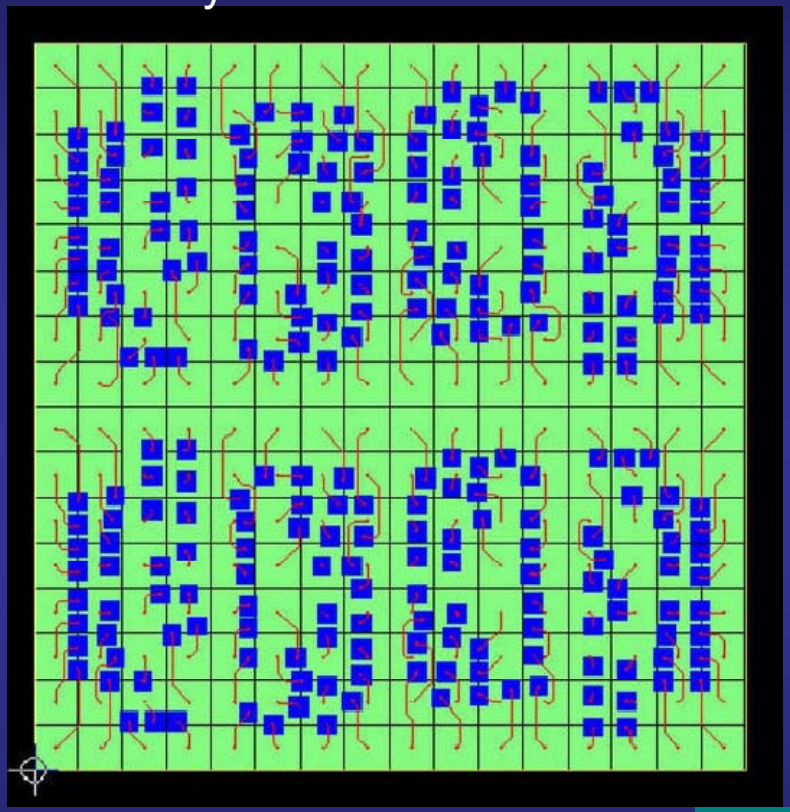
eight-layer board
16 x 16 $cm^2$
contain transfer lines, houses DCAL chip
expensive and tough to design

**Connections**

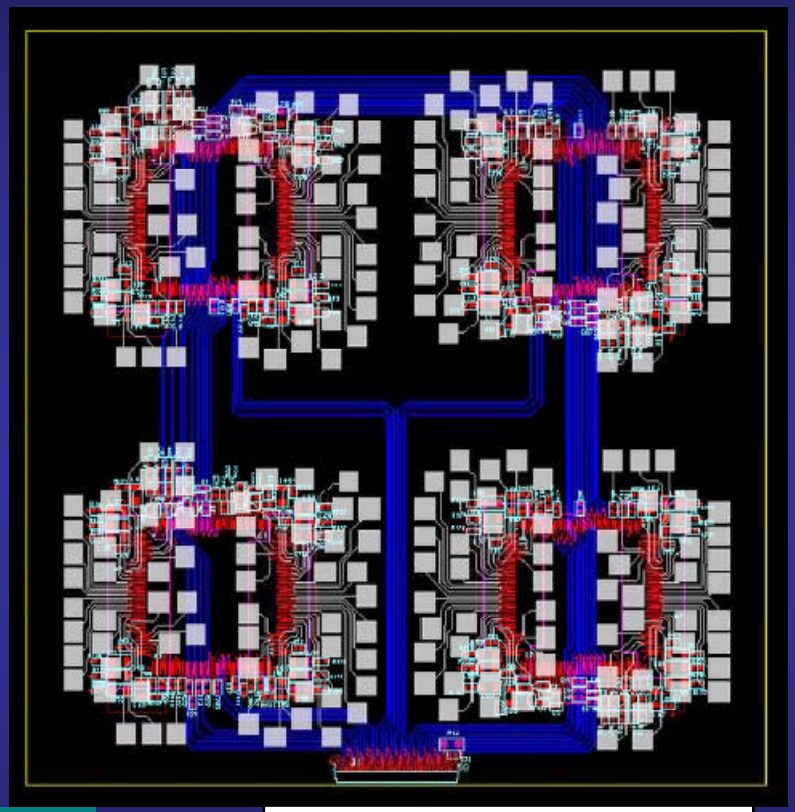
board to board with conductive glue on each pad (being tested)
cables for connection to data concentrators

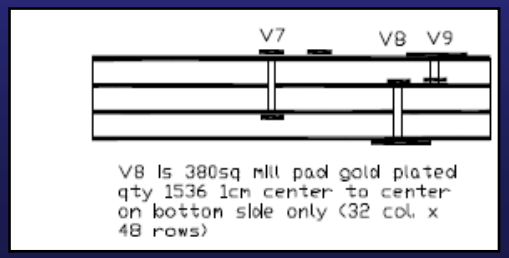
# Pad- and Front-end Boards II

Any size, multiple of 16x16 cm$^2$
4-layer Pad-board

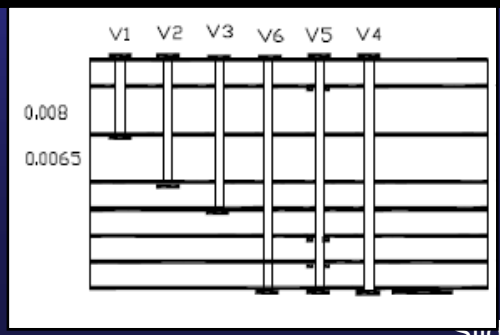


8-layer FE-board, 16x16 cm$^2$
All (almost) layers shown






Design completed
→ submitted




More complicated
than anticipated

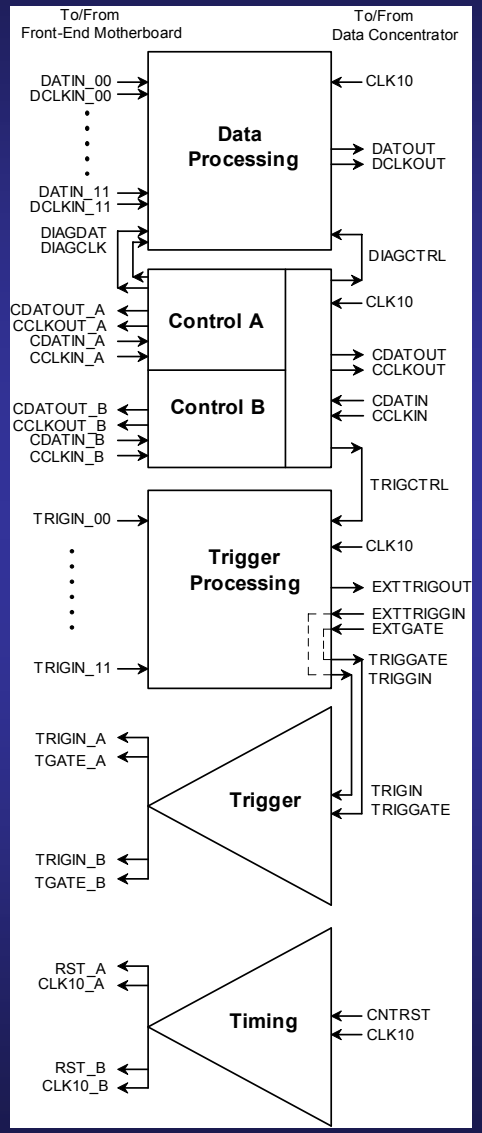
# Data concentrator boards

Functionality defined
Protocol to data collector defined

Design almost completed

# Timing and trigger module

**Functionality (almost) defined**
**Being designed by Argonne**



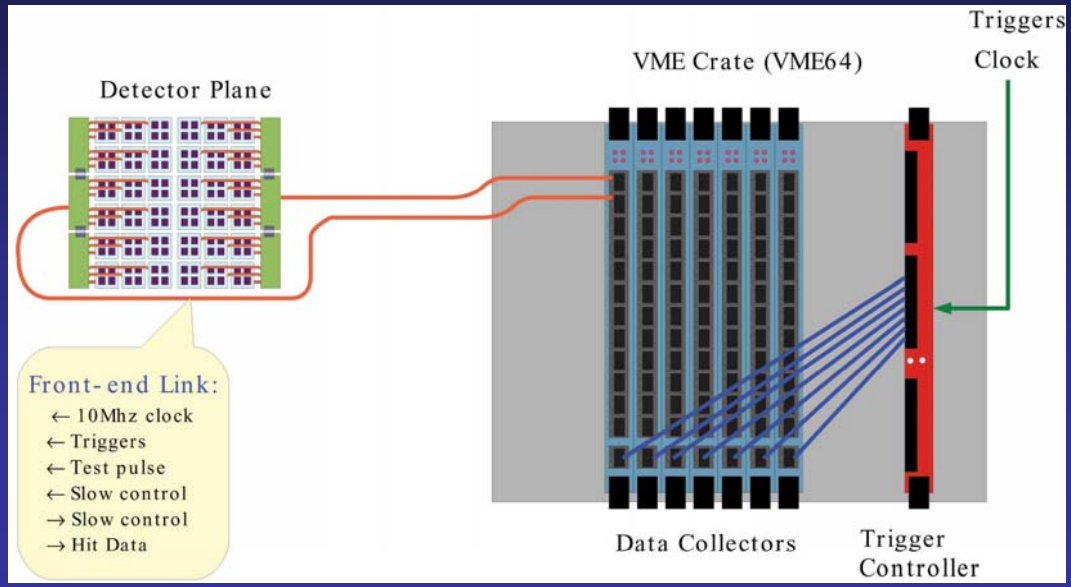
# Data collector boards

E Hazen (Boston)

**New Design Effort**

Boston Univ

**Fabrication of prototype this month**




## Functionality

**All data received as packets**

**Timestamp (24 bits) + Address (16 bits) + Hit pattern (64 bits)**

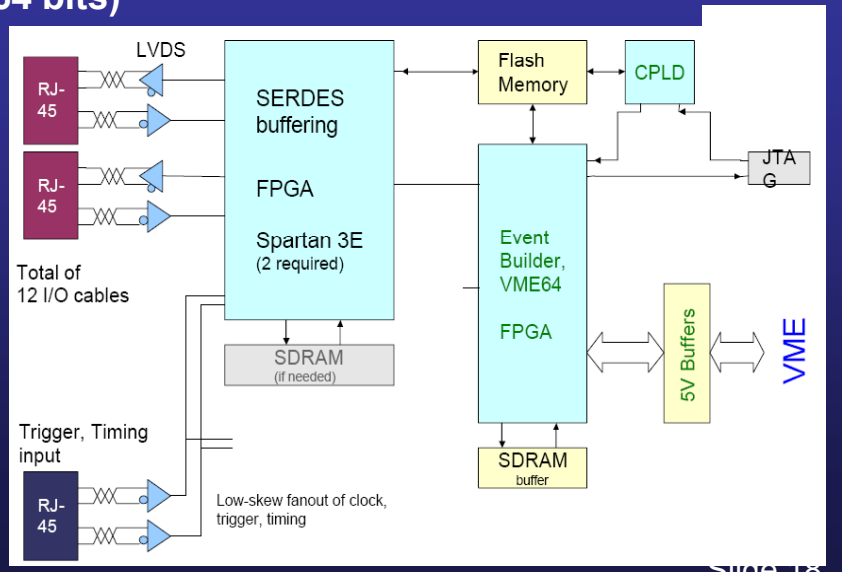
**Packets grouped in buffers by matching timestamps**

**Makes buffers available for VME transfer**

**Monitors registers (scalars)**

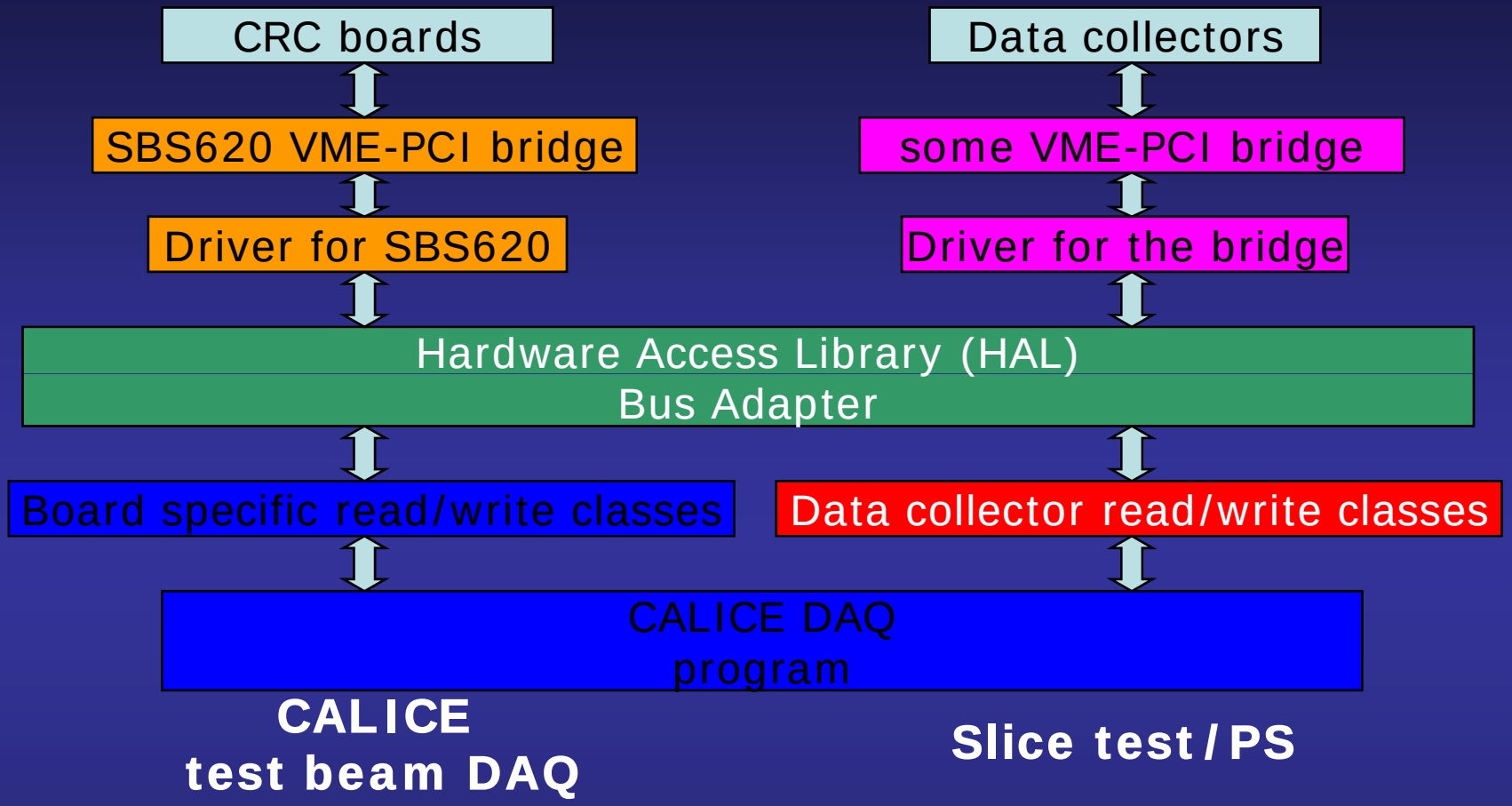
**Slow control of front-end**

**Allows read/write to DCAL chips or data concentrator boards**



# DAQ software

Particular challenge to be compatible with CALICE software

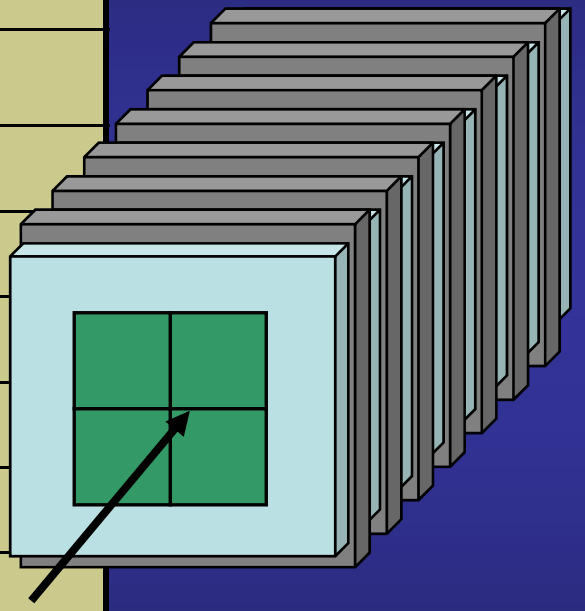



- Will be compatible with current CALICE test beam DAQ
- Use CALICE DAQ as much as possible to minimize the effort
  - Basically just need to supply some hardware specific I/O classes
- Currently focus on slice test, but will be used for 1m$^3$ PS as well

- Data format will follow existing CALICE convention

# Responsibilities and collaborators

| Task | Responsible institutes |
|---|---|
| RPC construction | Argonne, IHEP Protvino |
| Mechanical structure (slice test) | Argonne |
| Mechanical structure (prototype section) | DESY |
| Overall electronic design | Argonne |
| ASIC design and testing | FNAL, Argonne |
| Front-end board design | Argonne |
| Data concentrator design | Argonne |
| Data collector design | Boston |
| Timing and trigger module design | Argonne |
| DAQ Software | Argonne |
| HV and gas system | Iowa |
| Beam telescope | UTA |



# 1 $m^3$ Prototype Section

FUTURE

# Costs and Funding

**A) Slice test** is funded by LCDRD06, LDRD06 and ANL-HEP, and Fermilab

**B) Prototype section** not yet funded, but…

| Stack | Item | Cost | Contingency | Total |
|---|---|---|---|---|
| **RPC stack** | **M&S** | 607,200 | 194,600 | 801,800 |
| | **Labor** | 243,075 | 99,625 | 342,700 |
| | **Total** | **850,275** | **294,225** | **1,144,500** |
| **GEM stack*** | **M&S** | 400,000 | 165,000 | 565,000 |
| | **Labor** | 280,460 | 40,700 | 321,160 |
| | **Total** | **680,460** | **205,700** | **886,160** |
| **Both stacks** | **M&S** | 1007,200 | 359,600 | 1366,800 |
| | **Labor** | 523,535 | 140,325 | 663,860 |
| | **Total** | **1,530,735** | **499,925** | **2,030,660** |

* Reusing most of the RPC electronics

Proposal for supplemental funds for $500k/year over two years submitted to DOE
Help from ANL (LDRD), ANL-HEP, FNAL expected…

# Conclusions

**Finally gaining momentum!!!**

- Vertical slice test

  Funded (more or less)
  Concentrated effort with monthly meetings
  Goal: tests at MTBF in Spring 2007

- Prototype section

  Expensive!
  Funding appears possible
  Goal: RPC stack in 2008