Status of fast beam feedback systems

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- **ILC fast feedback prototype at KEK ATF/ATF2**
- **ILC electromagnetic background tests at SLAC/ESA**

FONT: Feedback On Nanosecond Timescales

Accelerator R&D for the International Linear Collider (ILC)

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Colin Perry
Javier Resta-Lopez

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Christina Swinson
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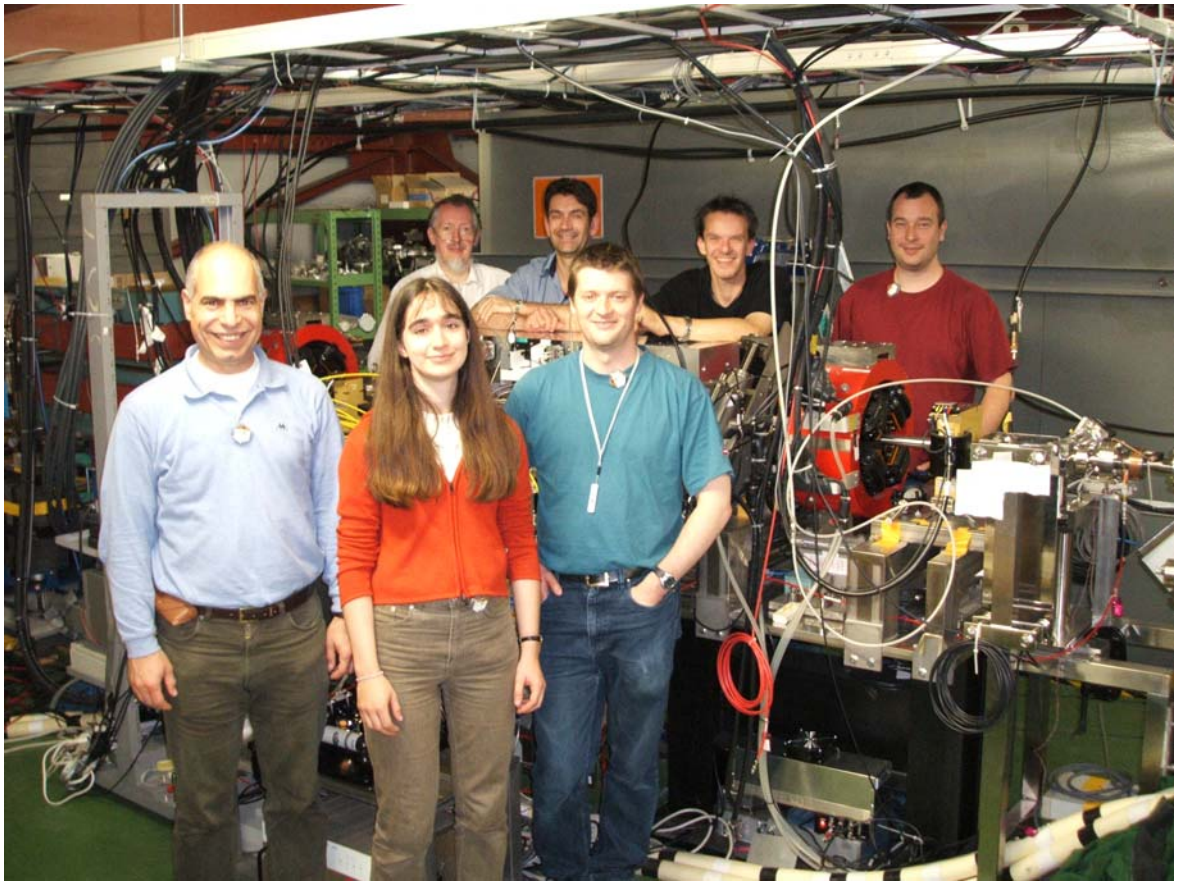
DESY, CERN
KEK, Tokyo Met, SLAC



Overview

Task: prototype beam-based (intra-train) feedback systems

Completed: ultra-fast analogue feedback prototypes

- **FONT2 / NLCTA: 54ns latency**
- **FONT3 / ATF: 23ns latency**

Originally developed in context of 'warm' LC, applicable to CLIC

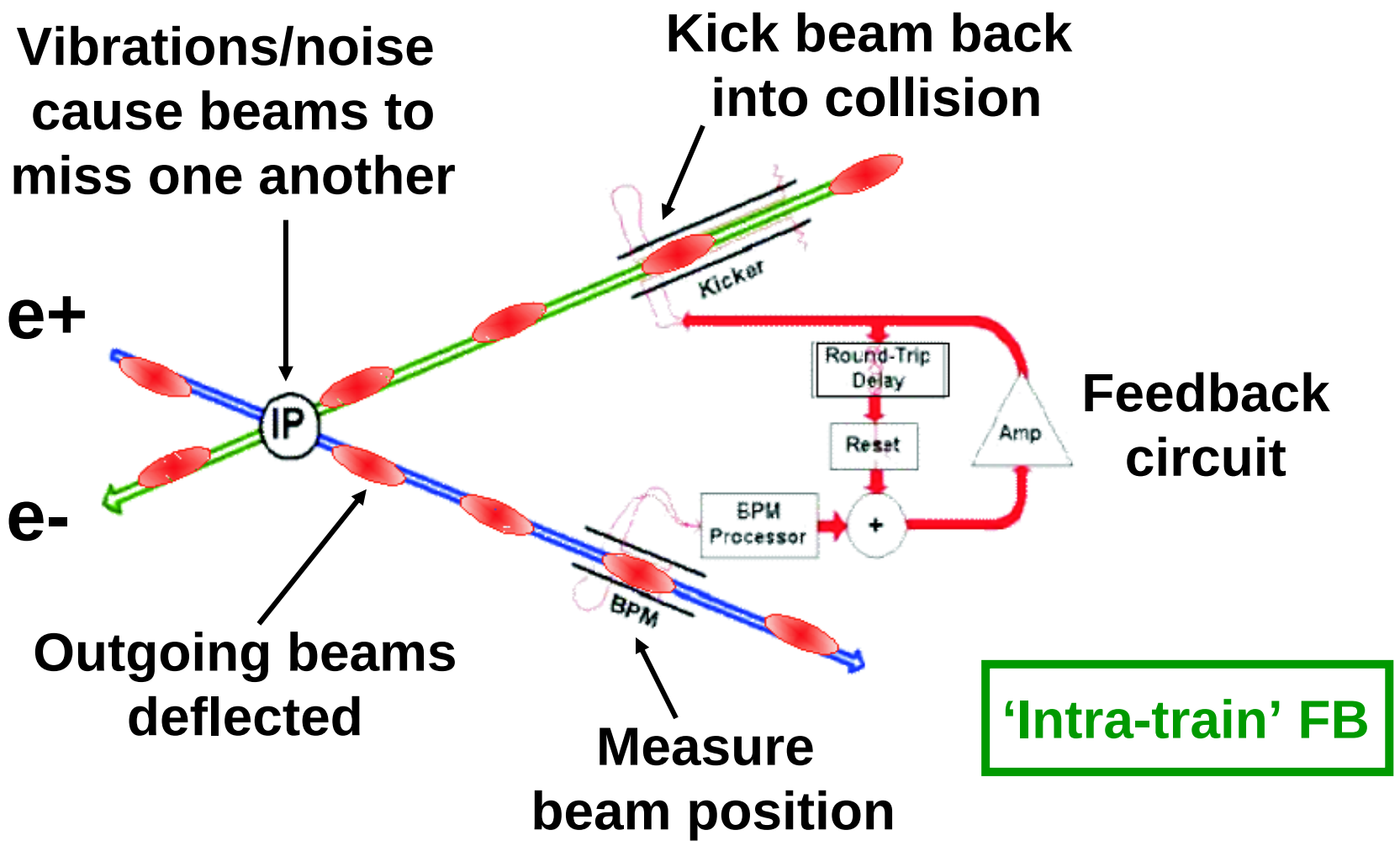
Ongoing: ILC digital feedback prototype

- **FONT4 / ATF: digital FB processor tests w. 3 bunches**
- **FONT@ESA: EM background impact on FB BPMs**

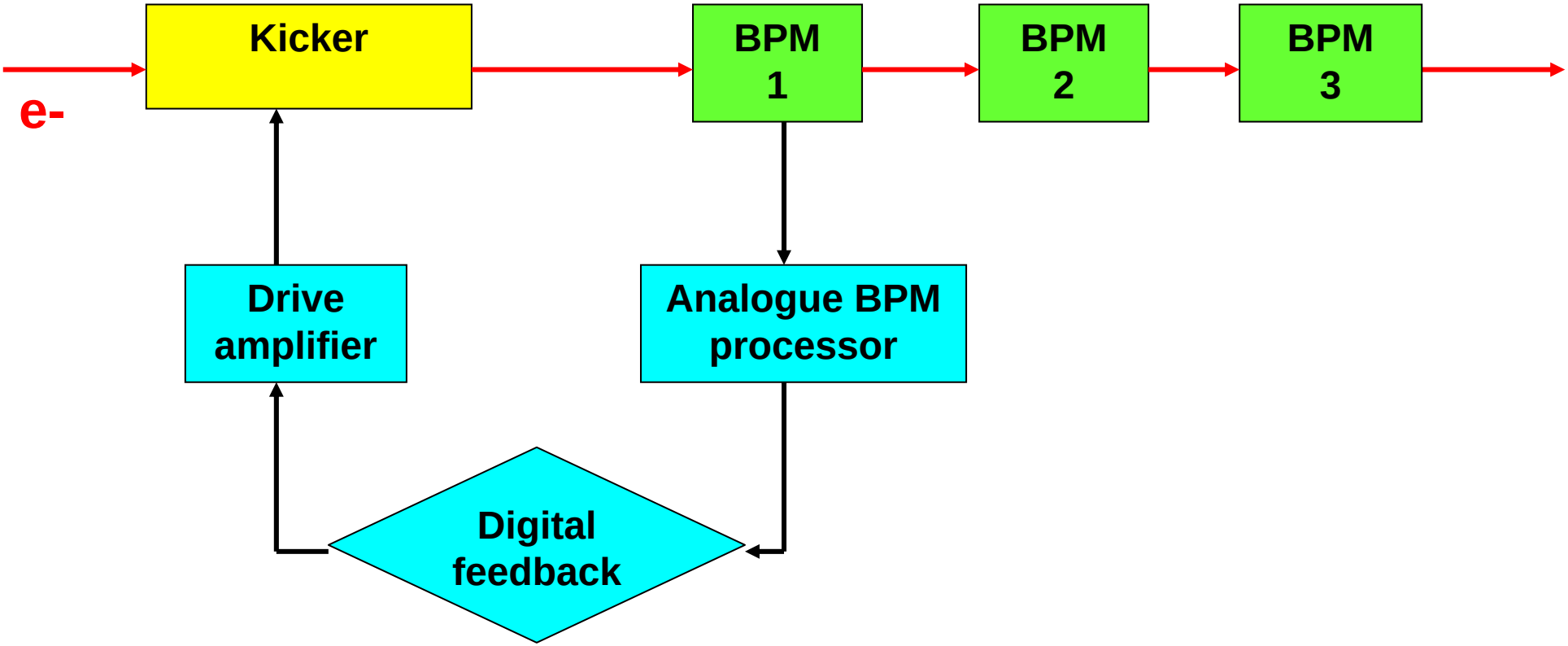
Future: Multibunch operations, algorithm tests

- **FONT5: ATF2 or FLASH**
- **(Feed-forward)**

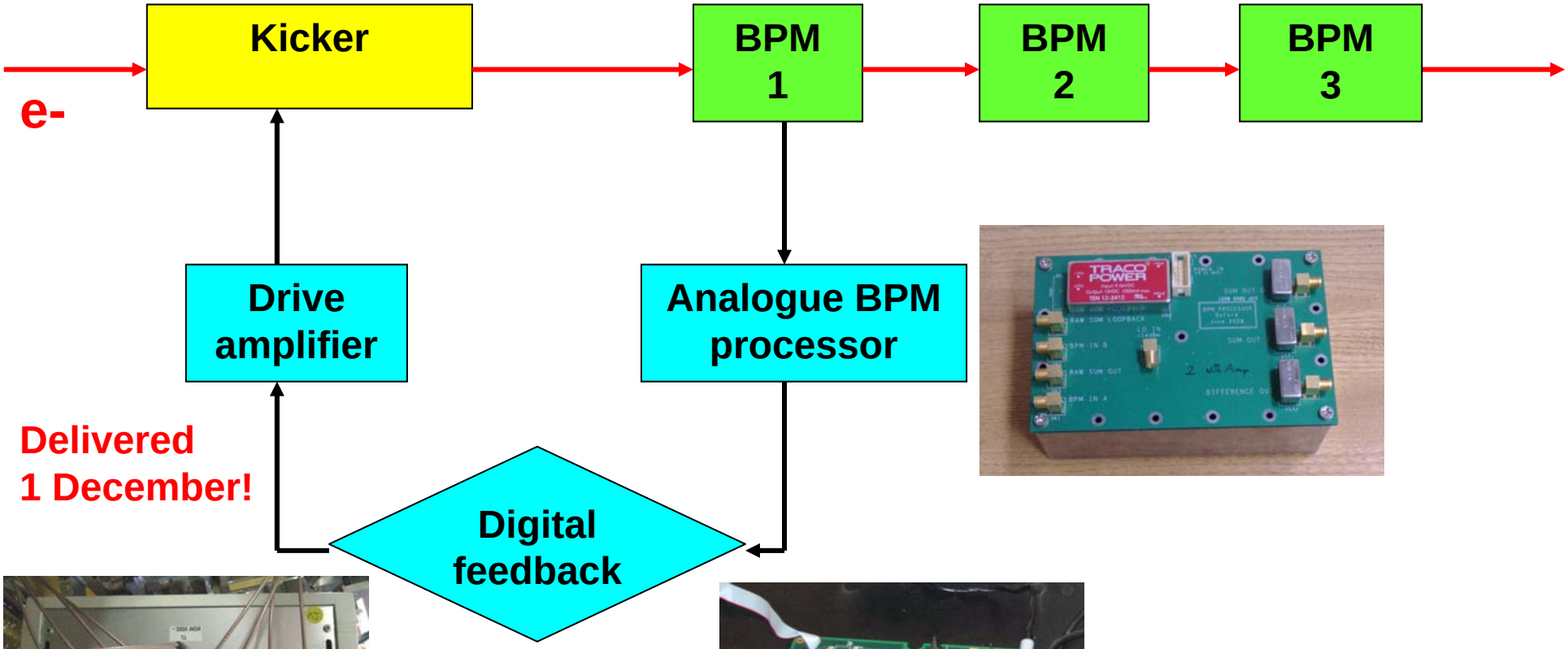
IP Intra-train Feedback Concept



ILC digital feedback prototype (FONT4)



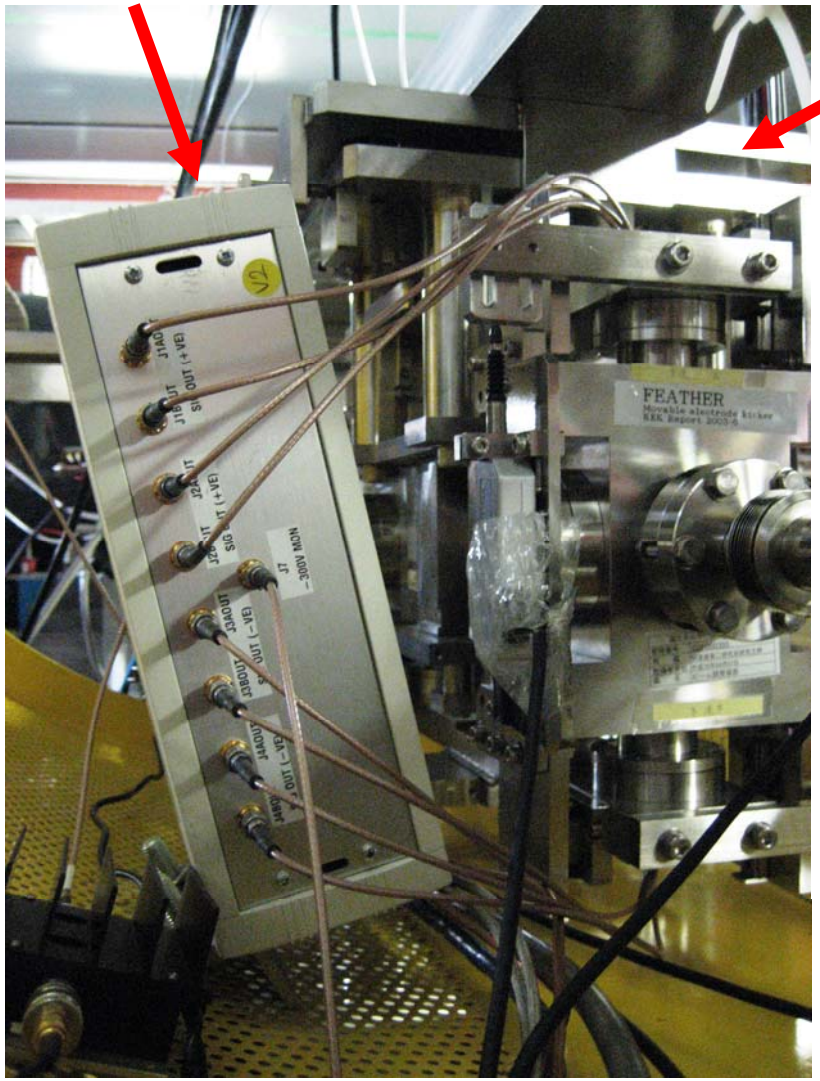
FONT4 hardware



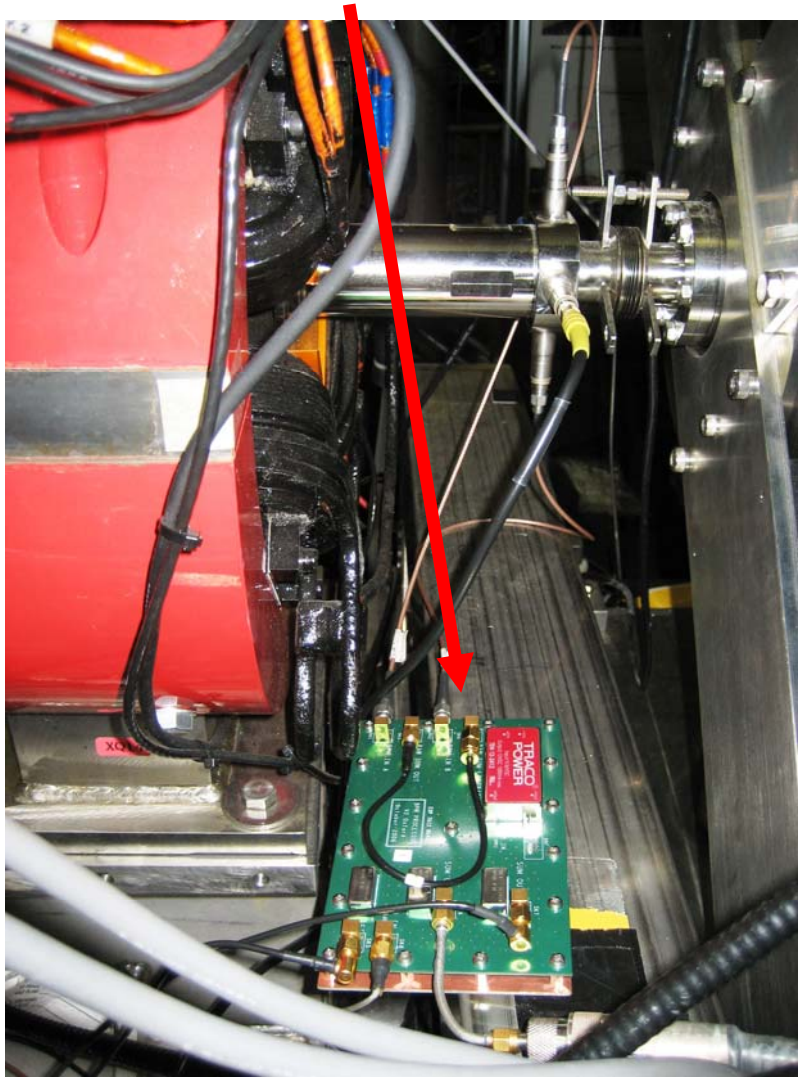
FONT4: beamline at KEK ATF (December 06)

Amplifier

FEATHER
Kicker



BPM processor board



FONT4: latency budget

- **Time of flight kicker – BPM: 7ns**
- **Signal return time BPM – kicker: 15ns**

  Irreducible latency: 22ns

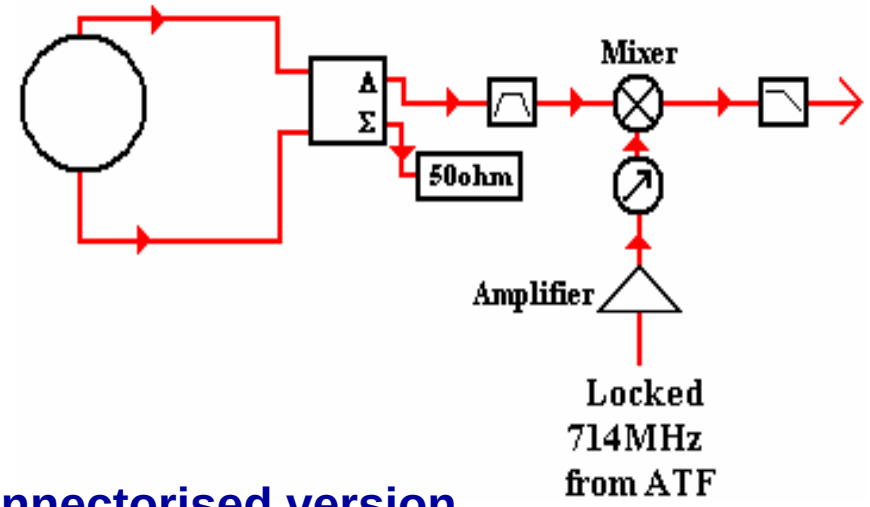
- **BPM processor: 7ns**
- **ADC/DAC (3.5 89 MHz cycles) 40ns**
- **Signal processing (8 357 MHz cycles) 25ns**
- **FPGA i/o 3ns**
- **Amplifier 40ns**
- **Kicker fill time 3ns**

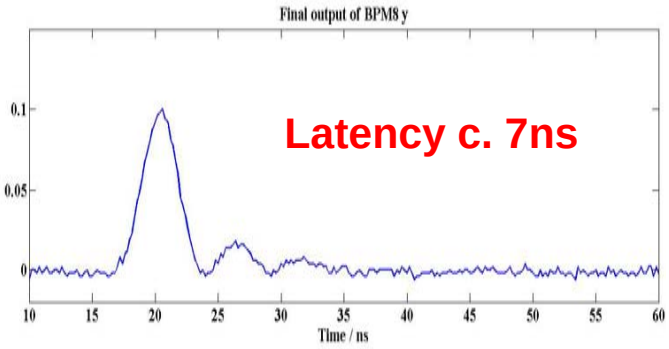
  Electronics latency: 118ns

- **Total latency budget: 140ns**

BPM processor

Single stage down-mix to baseband



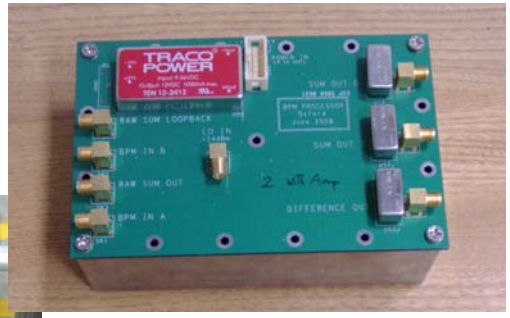


Latency c. 7ns

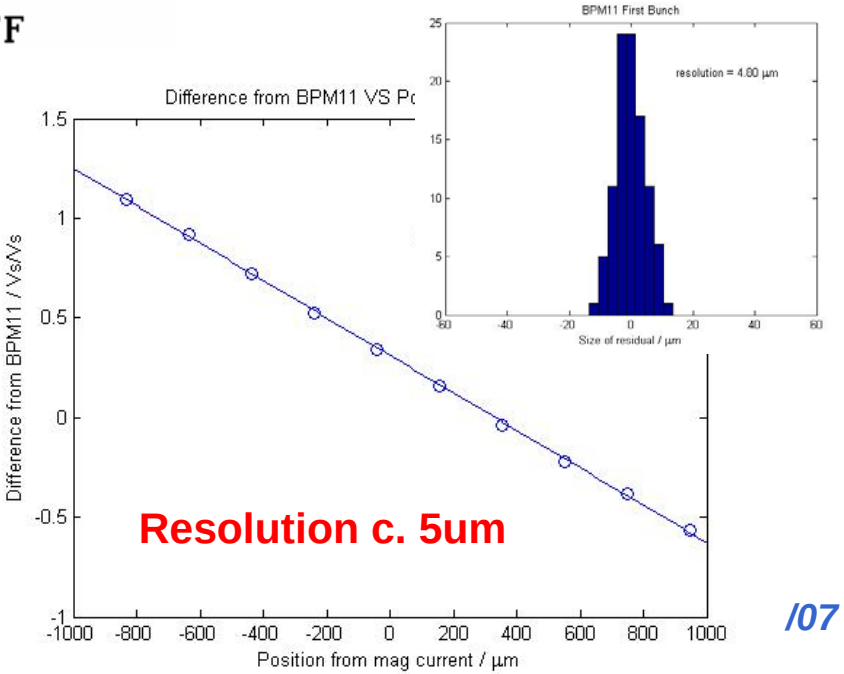
Replaced connectorised version with custom PCB – new version tested

November 2006

old

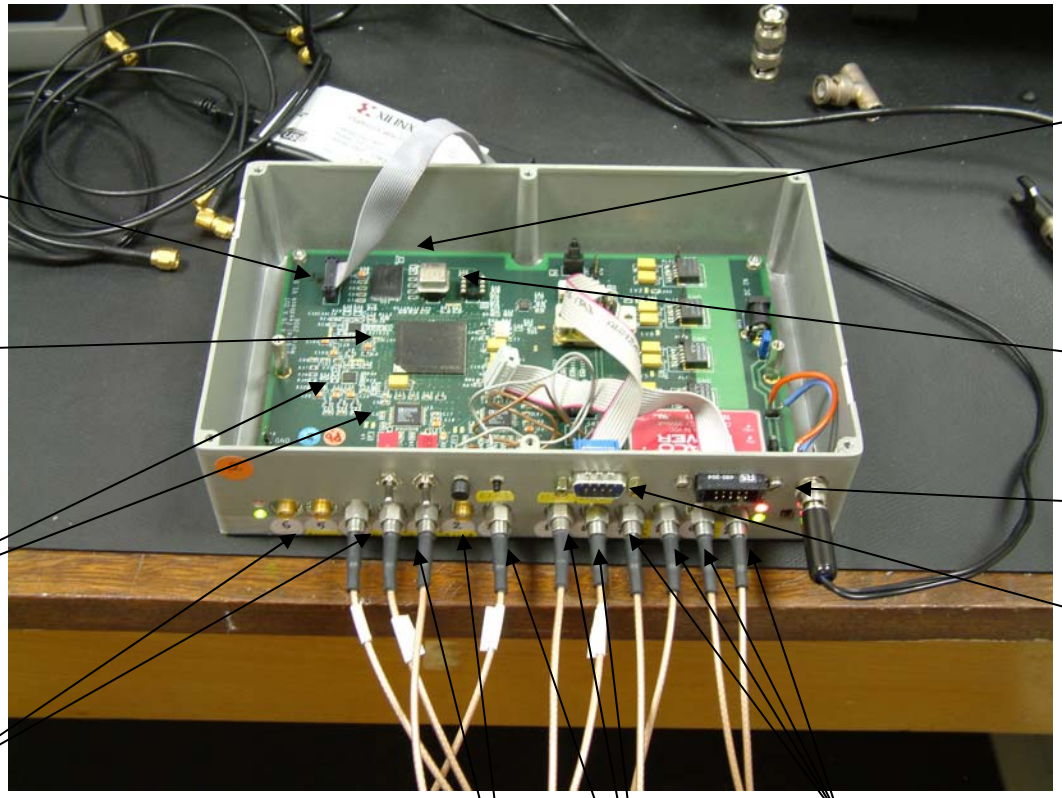


new

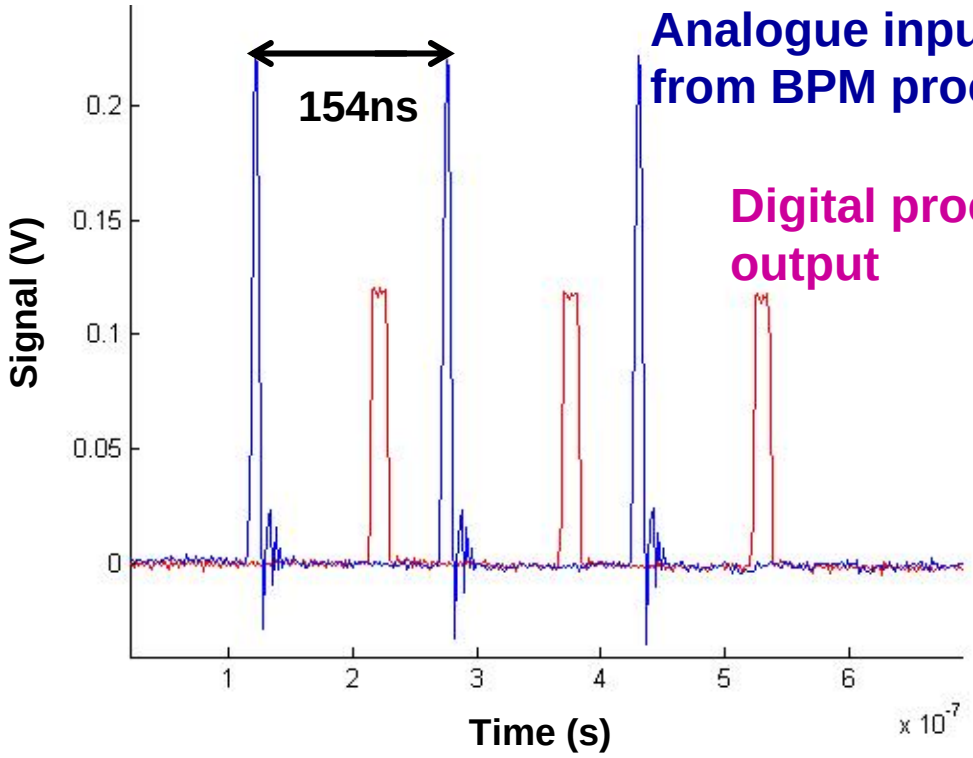


Resolution c. 5um

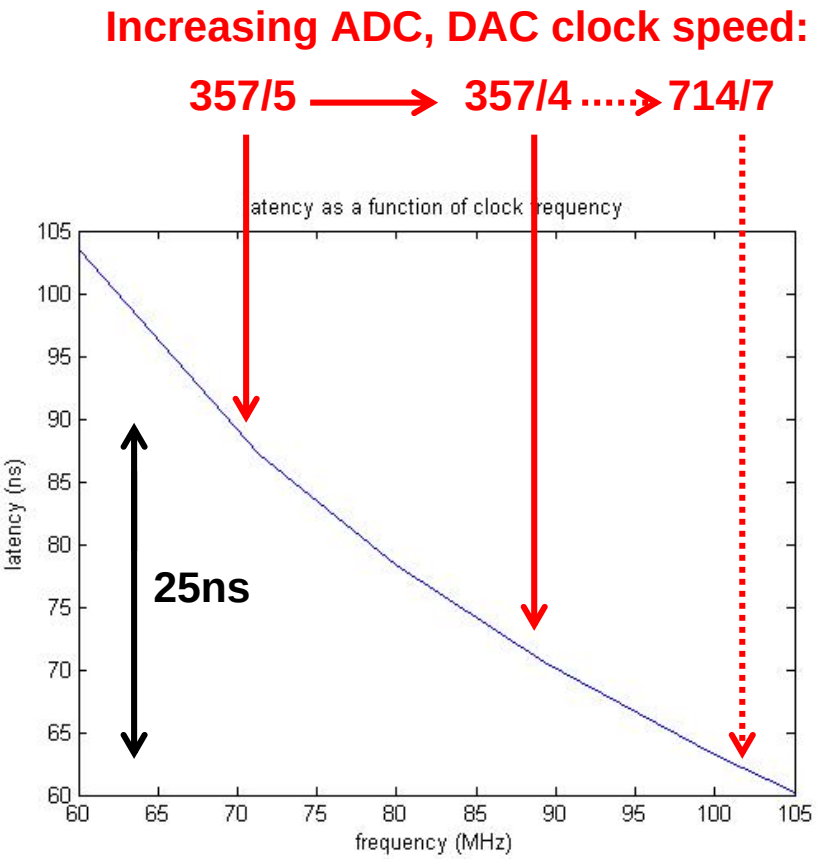
Digital Feedback Board



Beam test results (April – November 2006)



- Checked simple gain implementation
- Verified triggering, beam synchronisation, clocking …



Kicker driver amplifier

Specifications:

- **+- 15A (kicker terminated with 50 Ohm)**
- **+- 30A (kicker shorted at far end)**
- **35ns risetime (to 90%)**
- **pulse length 10 us (specified for 20-60 bunches)**
- **repetition rate 10 Hz**

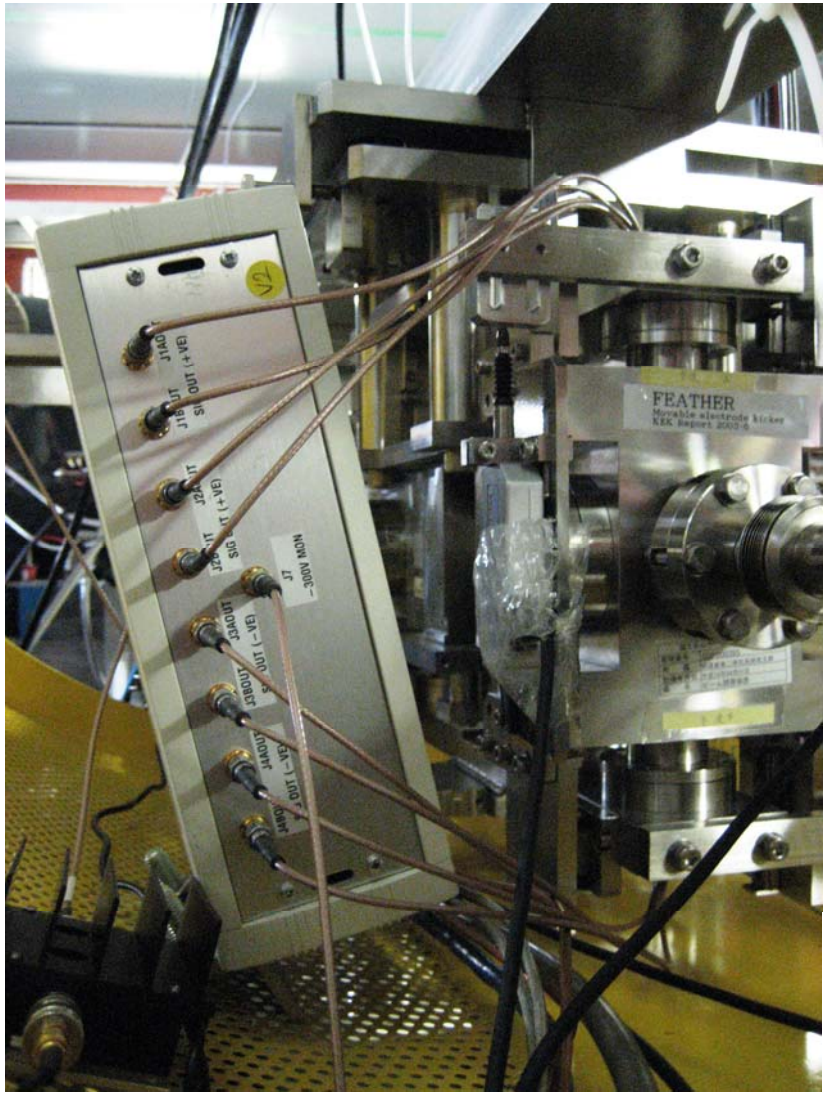
Order placed with TMD Technologies September 22

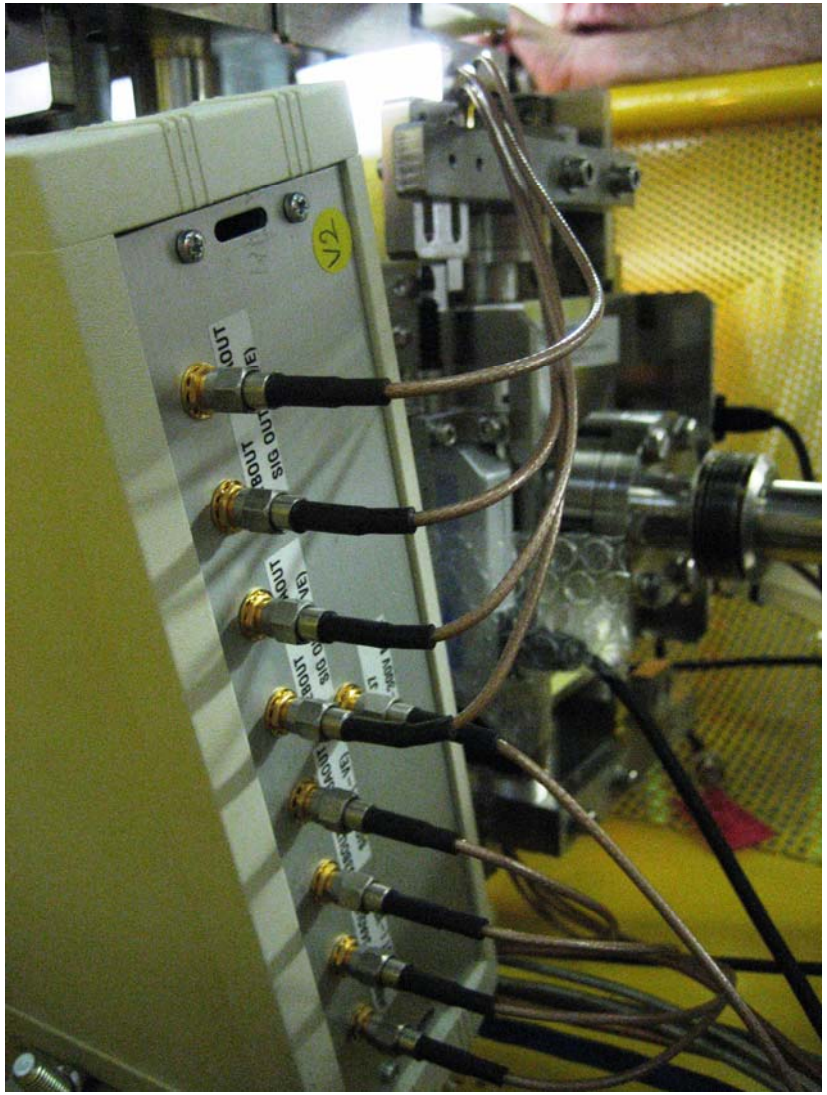
1st prototype unit delivered December 1

2nd prototype unit delivered December 8 (5ns faster)

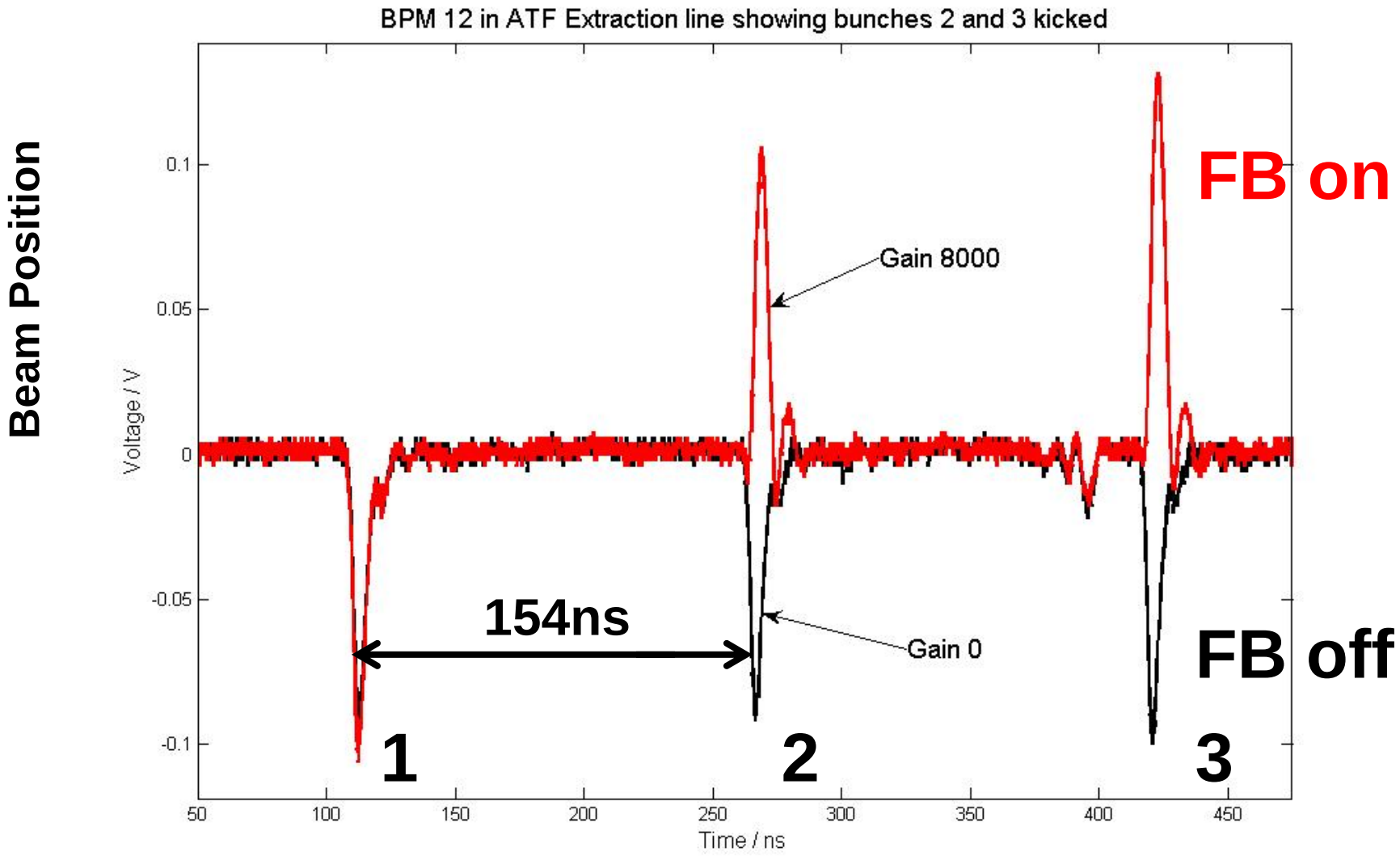
Tested with beam at ATF week of December 11!

Kicker driver amplifier in beamline





Kick on beam with loop closed (Dec 15 2006)



FONT4 test plan

June 2006:

- **1st test of PCB version of analogue BPM processor**
- **2nd tests of digital FB: timing, synchronisation, triggering, gain adjustment in FPGA (ADC clocking @ 714/10 = 71 MHz)**

December 2006:

- **1st test of FONT4 amplifier**
- **3rd tests of digital FB: ADC clocking @ 357/4 = 90 MHz**
- **2nd tests of PCB BPM processor**
- **Closed-loop FB**

Through 2007:

- **Closed-loop FB**

FONT5 test plan

The next major development would be FB tests using a long ILC-like train

(FONT4 amplifier was specified to allow this)

- **ATF: depends on success of fast-extraction kicker tests, 2008/9?**
- **Would allow us to address robustness of FB algorithms:**
  - **take into account bunch-bunch correlations along train**
  - **adaptive gain as beam conditions change (drift)**
  - **incorporate feed-forward information from upstream**
  - **add beam-related 'luminosity' signal for fast scanning?**
- **Could in principle be done at FLASH**

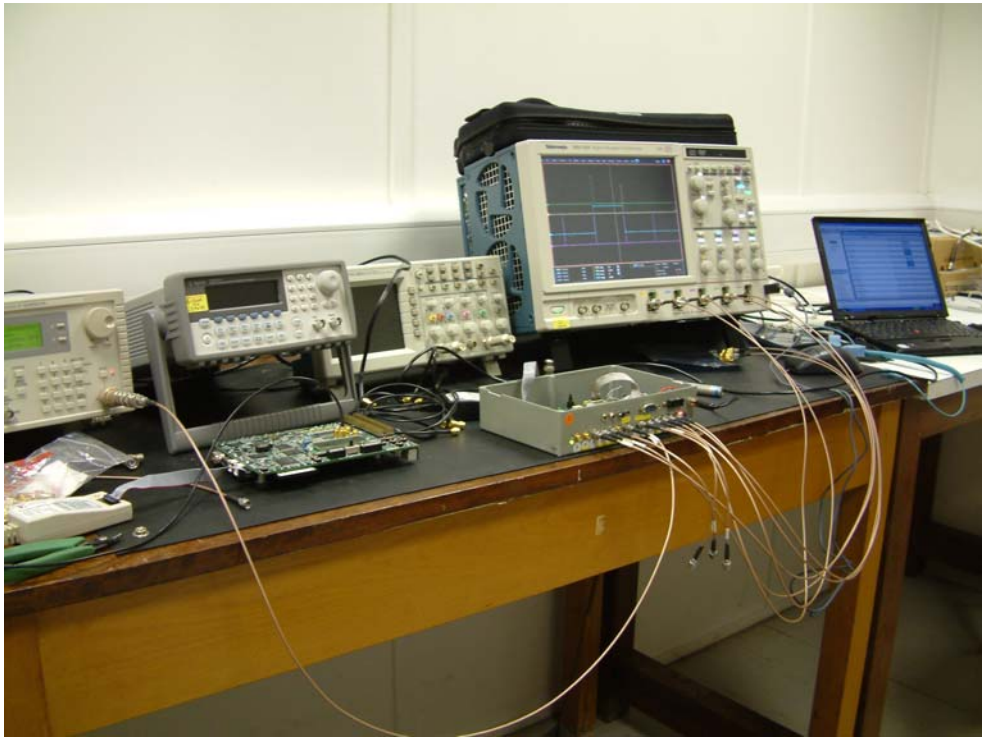
FONT bench test system

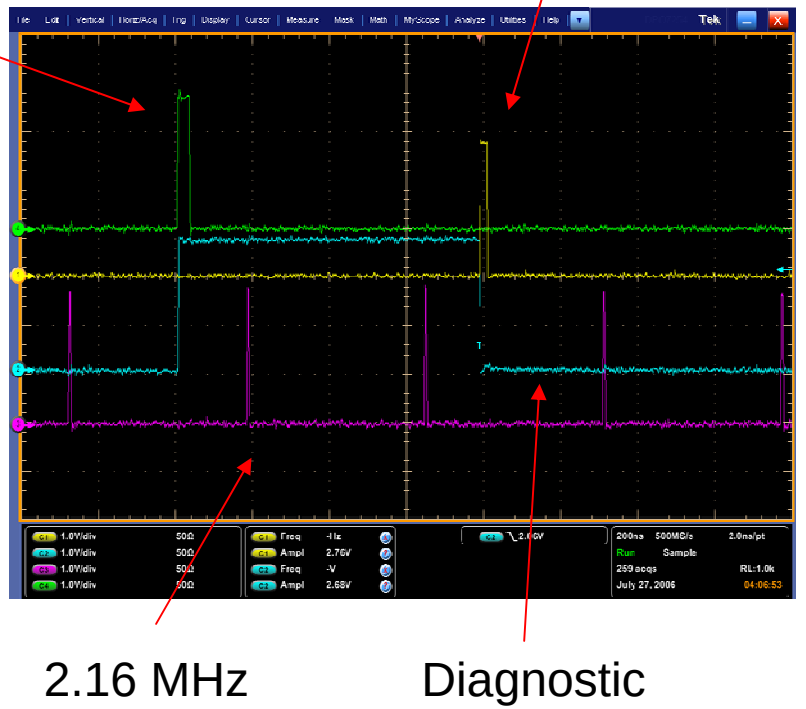
Manufacture synchronised ILC bunch-train, clocks, and trigger

Develop algorithms and program FPGA

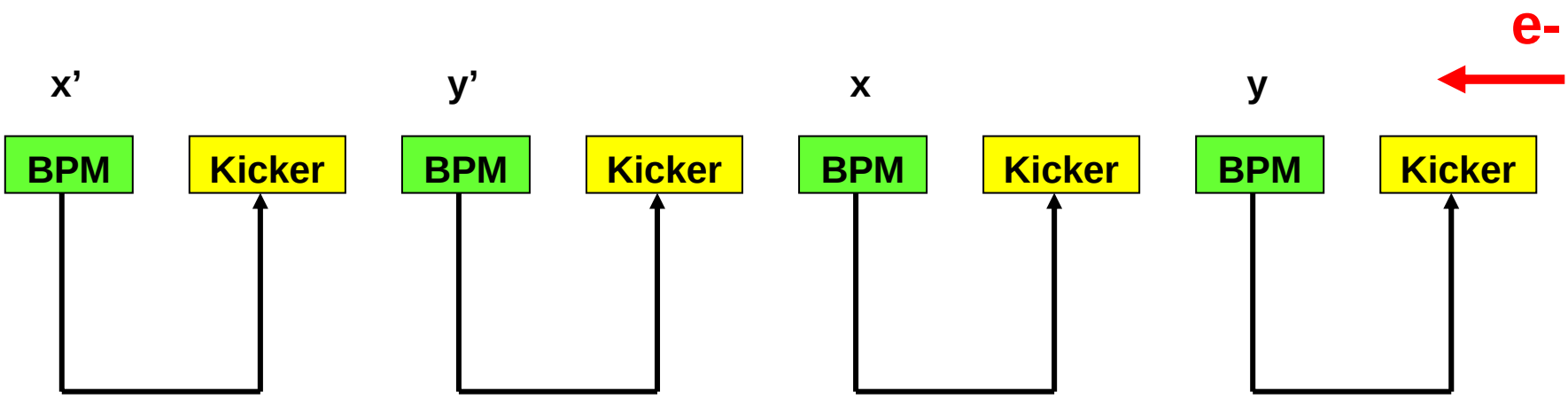
Close loop

(Include amplifier and dummy kicker also!)



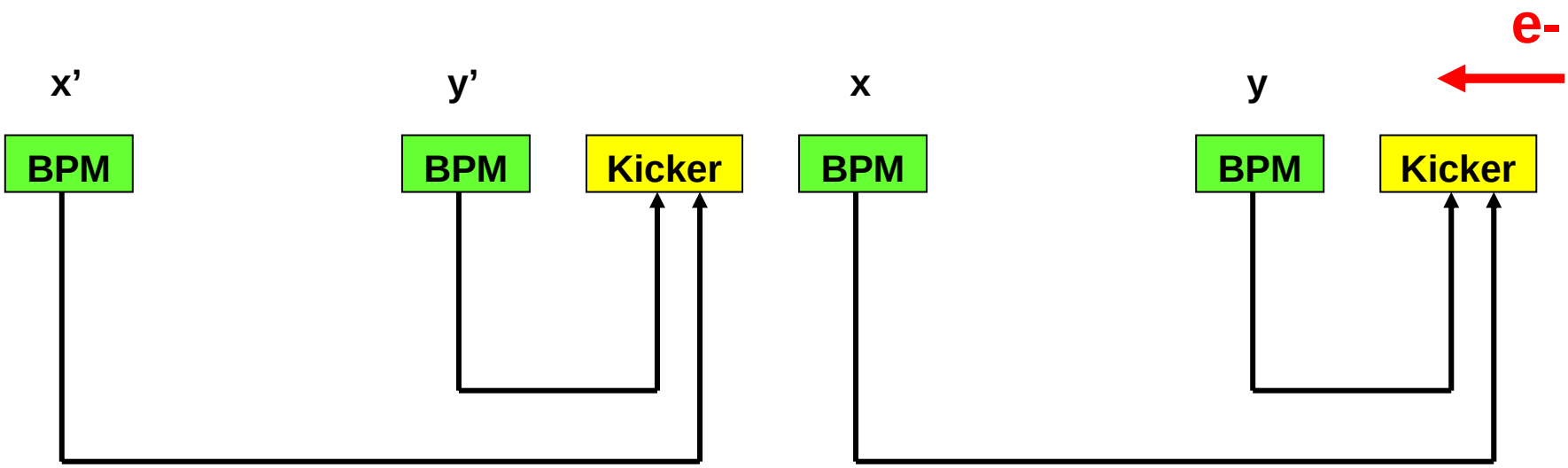


Schematic ATF2 feedback layout: 1

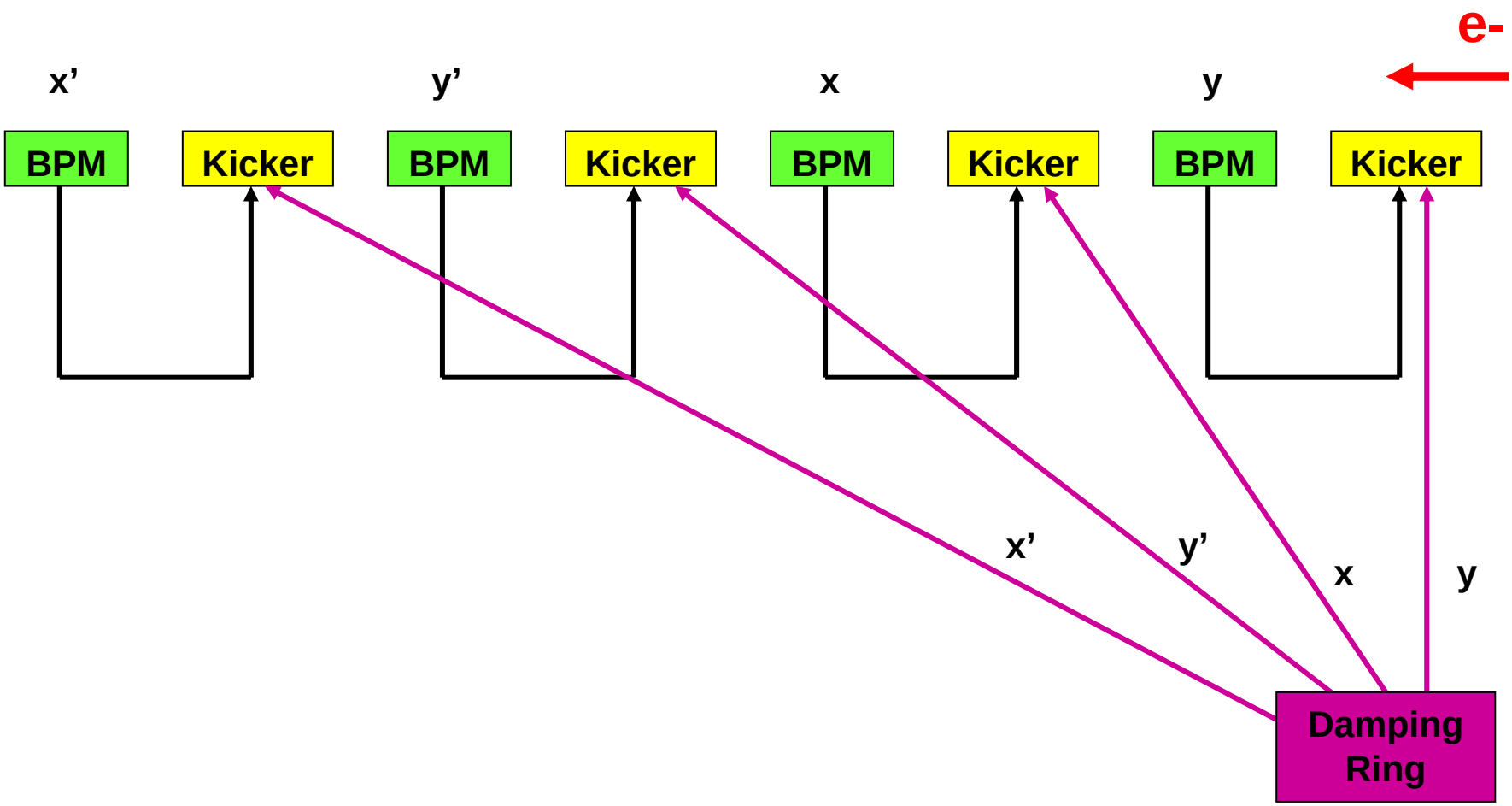


Schematic ATF2 feedback layout: 2

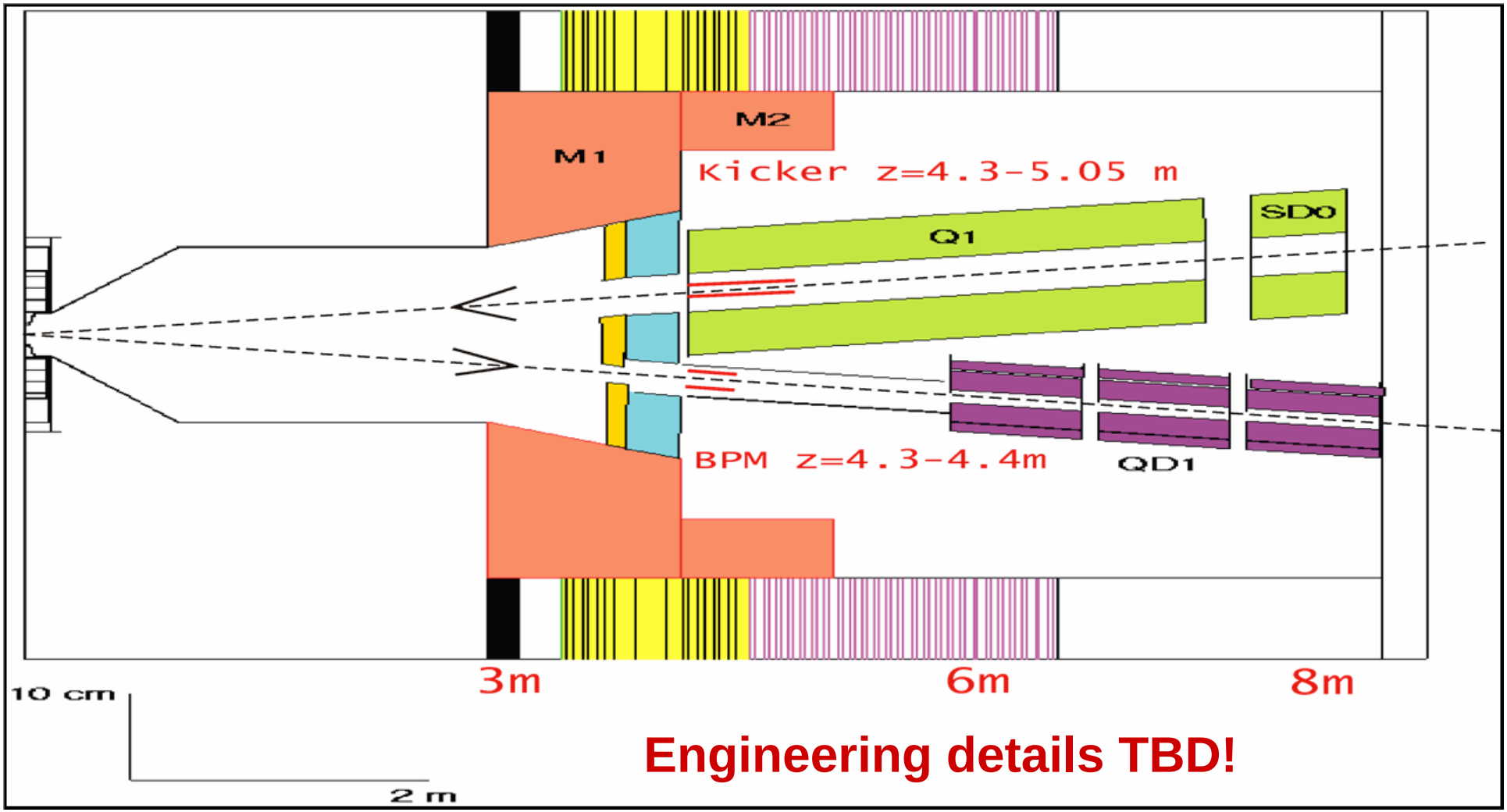
combined x-y kickers



Schematic ATF2 feedforward layout: 1

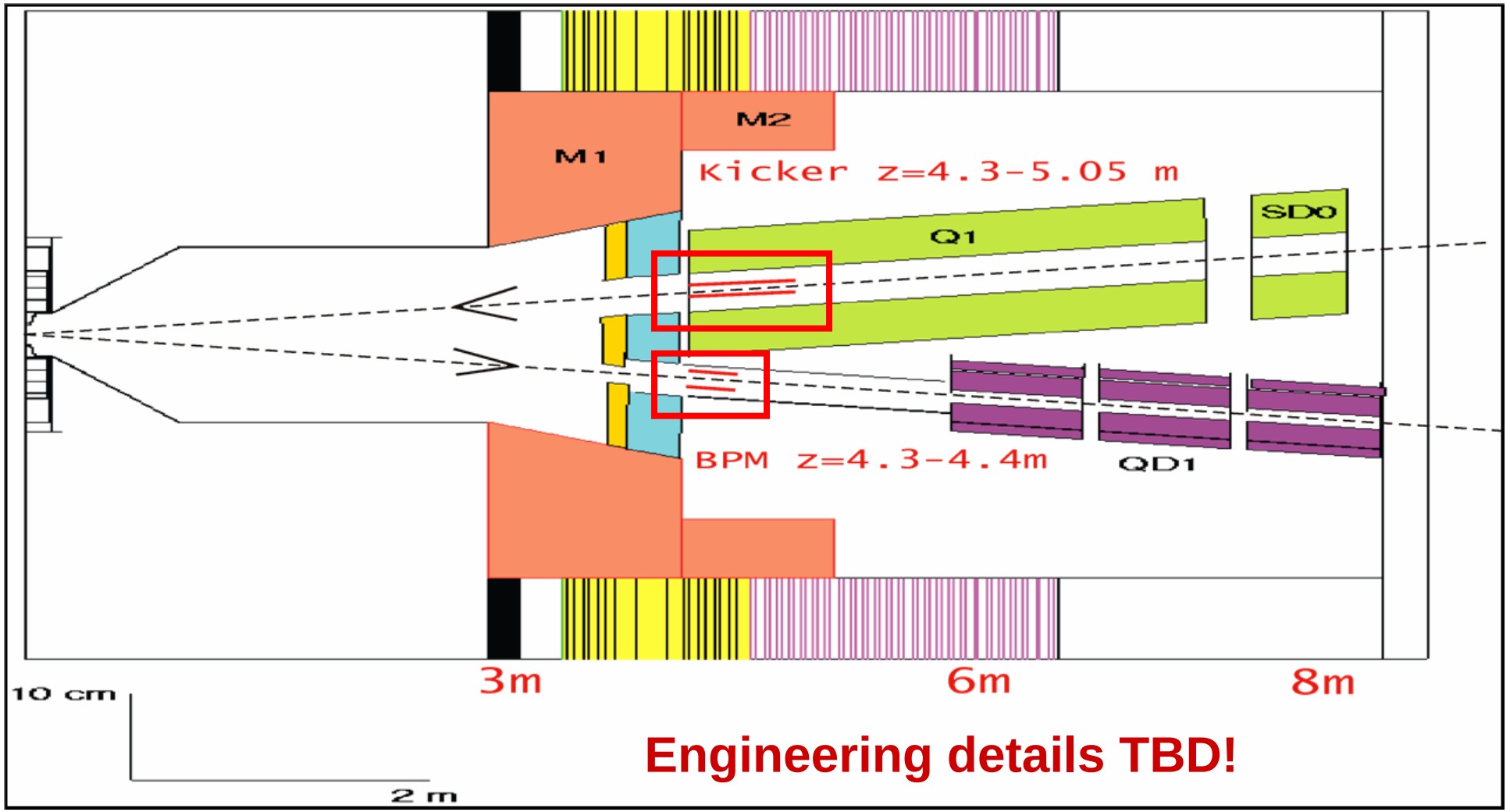


ILC interaction region



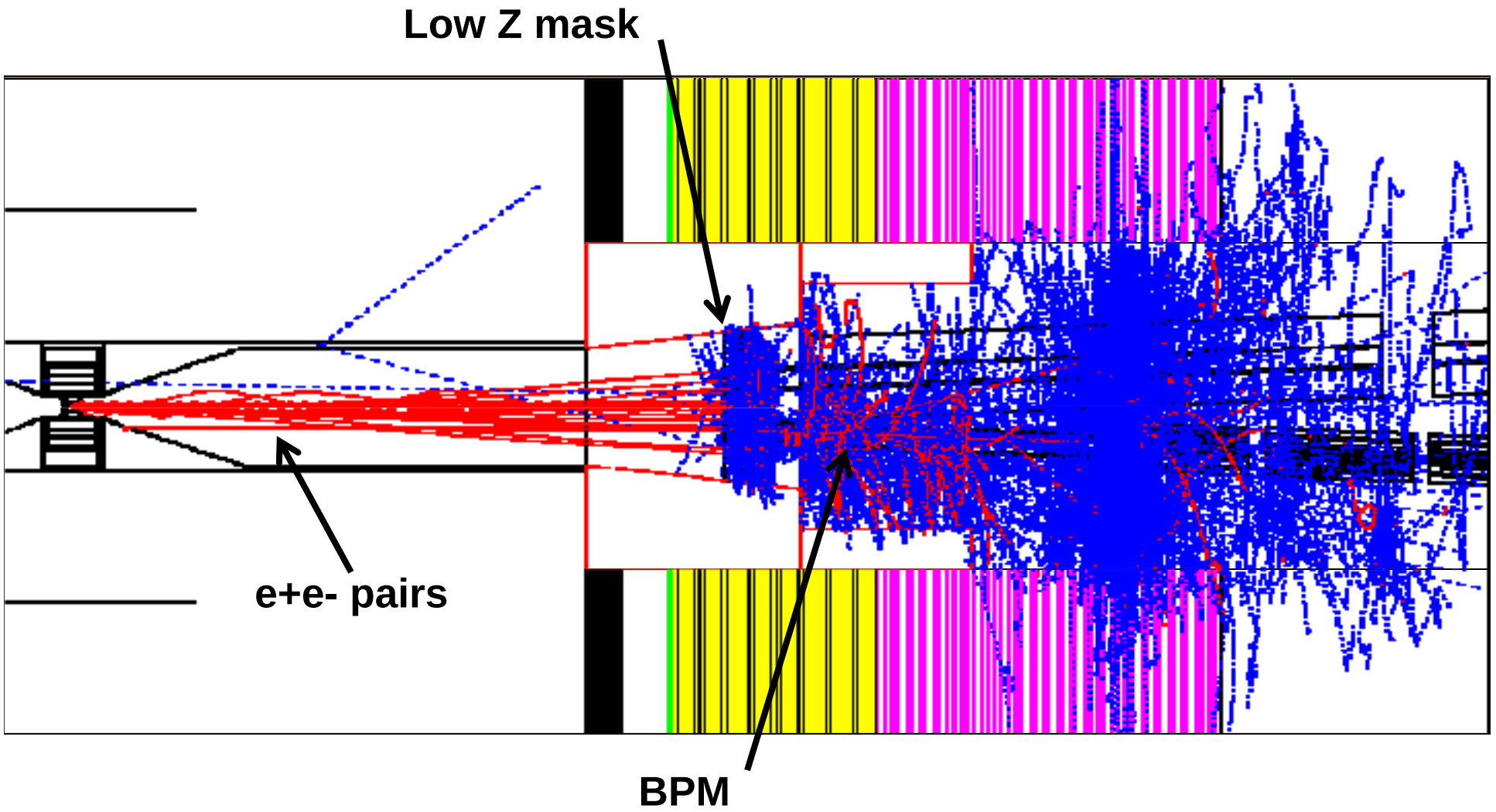
Engineering details TBD!

Nominal IP feedback hardware locations

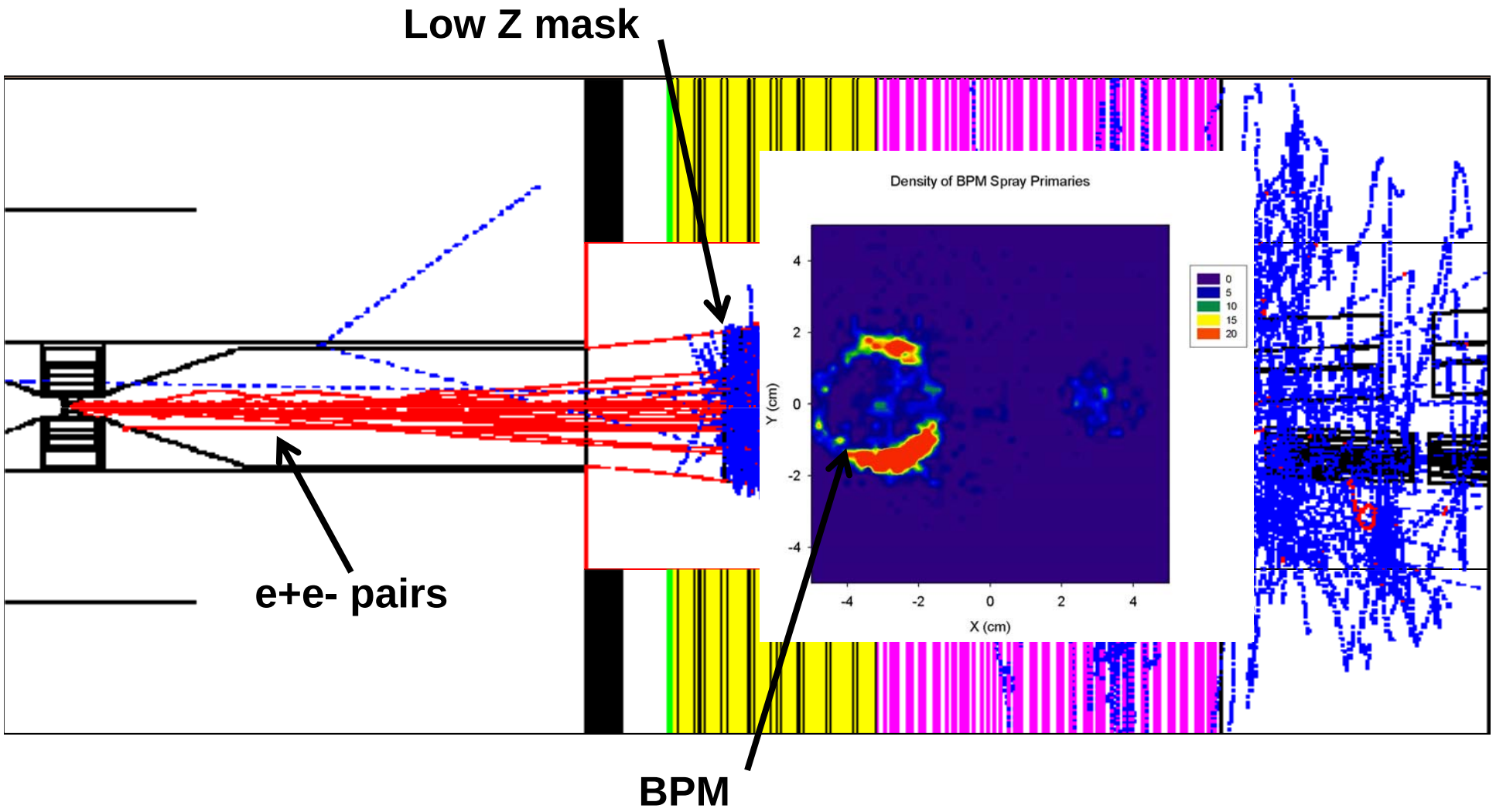


Engineering details TBD!

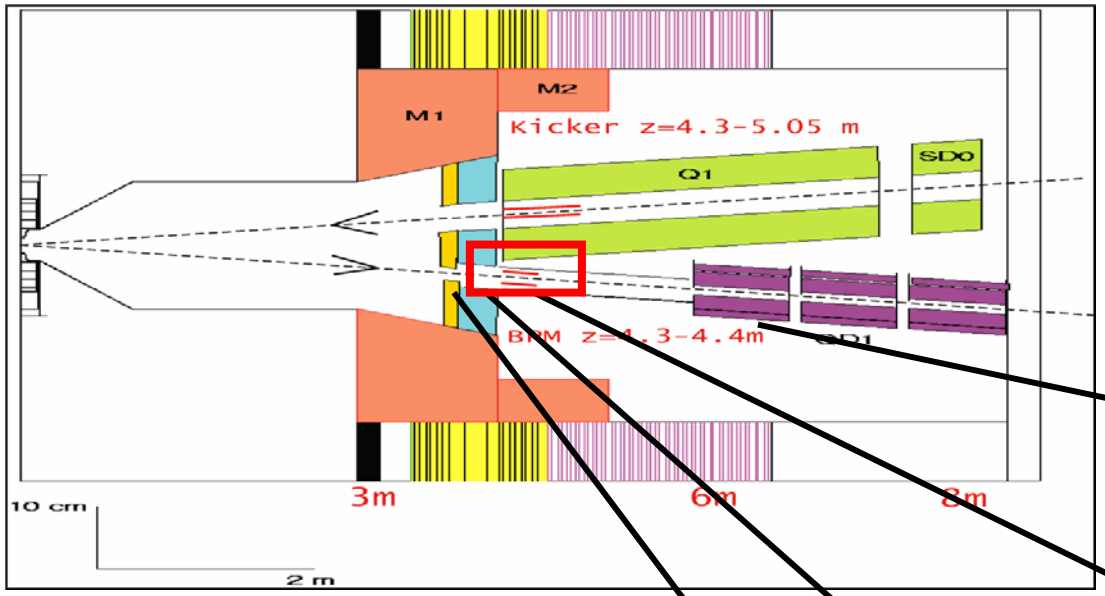
Pair-induced EM backgrounds



Pair-induced EM backgrounds



FONT Test Module for ESA



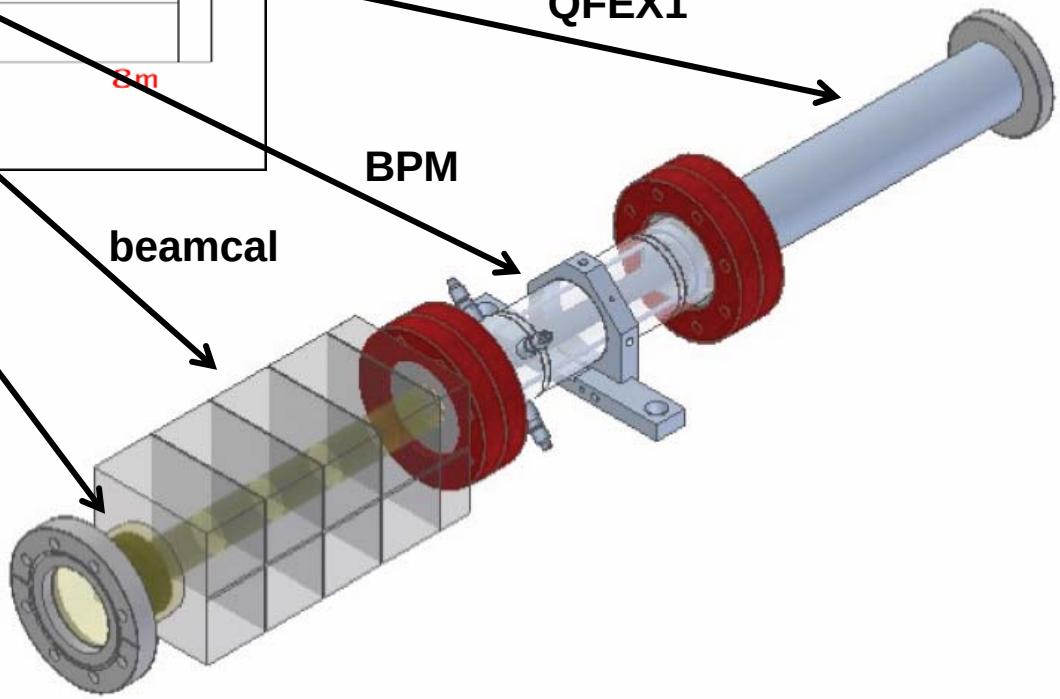
Material model of ILC outgoing beamline

QFEX1

BPM

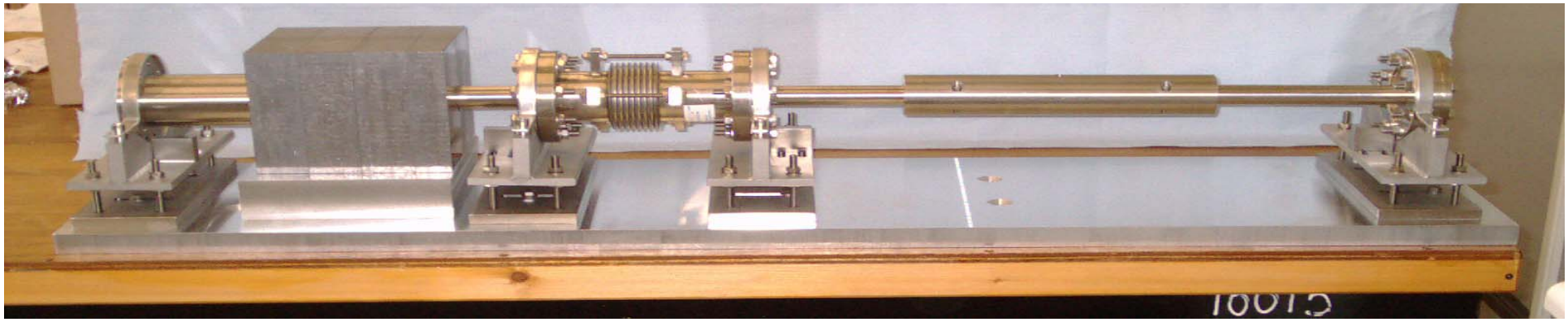
beamcal

low Z mask



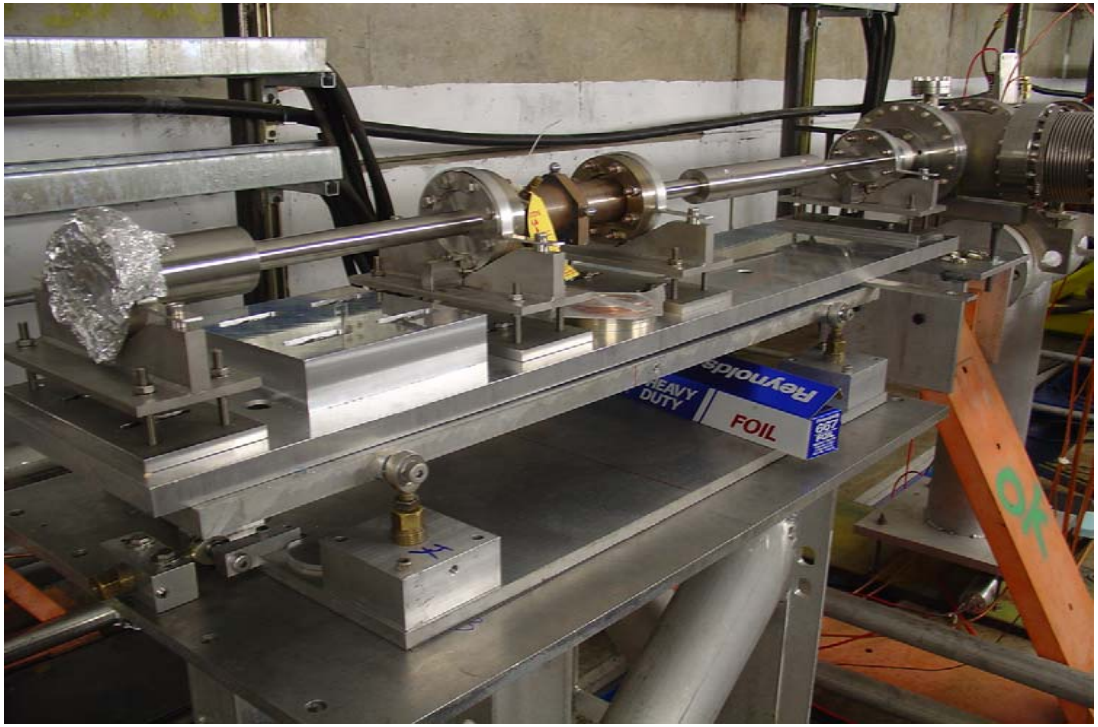
P.N. Burrows

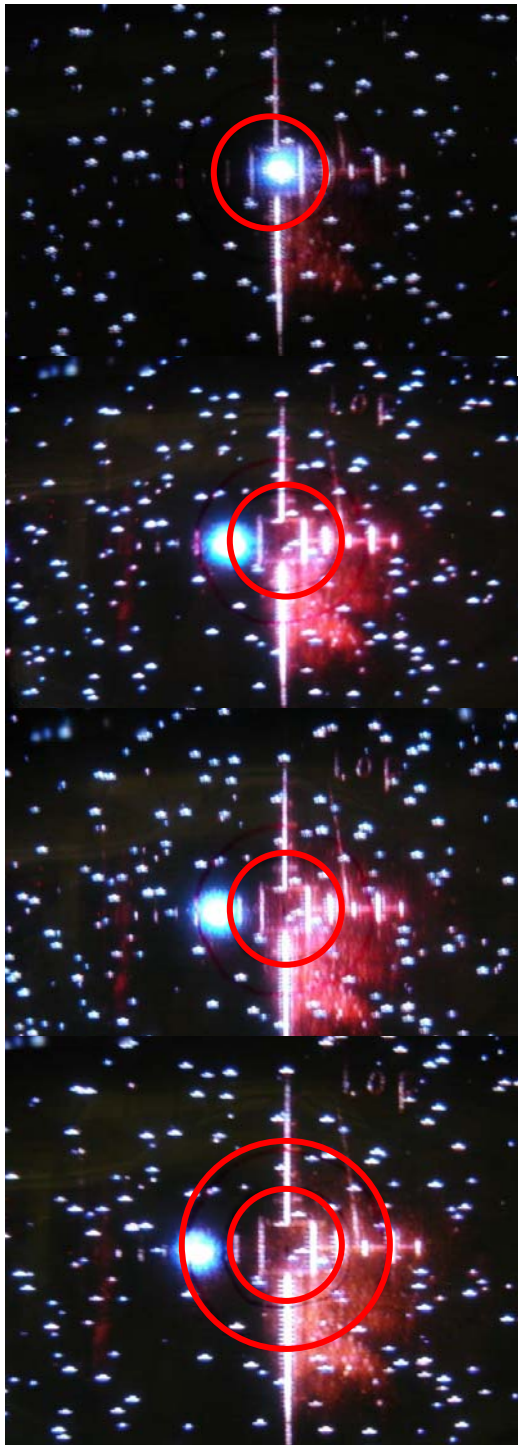
FONT Test Module (T-488)



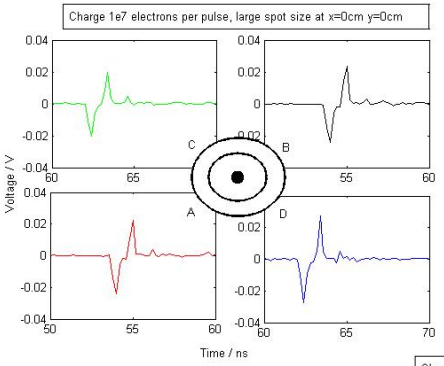
Beam

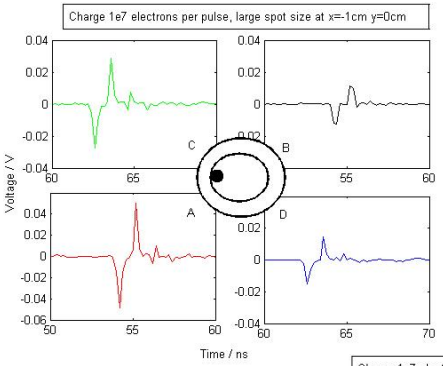
Installation at ESA



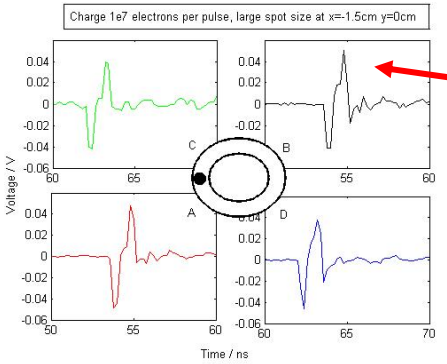


Beam scan across module (July 06)

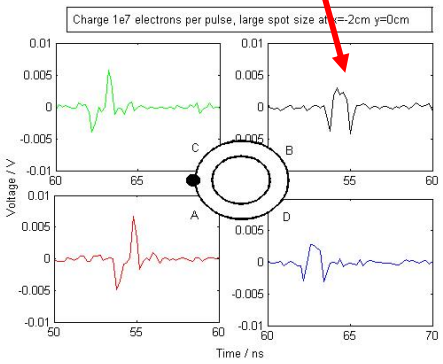




107 beam**



Noticeable degradation of signals



Modelling in progress - See Hartin talk

Summary

- **Hardware for ILC fast intra-train FB prototype has been built and tested with beam at KEK/ATF during 2006**
- **FB loop has been closed (December 2006)**
- **System will be further tested and optimised in 2007**
- **Planning for deployment of intra-train FB (+ FF) at ATF2**
- **Test system with long bunchtrain (ATF2, FLASH)**
- **Bench system for algorithm development + testing**
- **First beam tests of EM background environment for FB BPM at SLAC/ESA in 2006**

  - further beam tests March + July 2007