ATCA* for Machines

*Advanced Telecom Computing Architecture

LCWS 2007 DESY, Hamburg

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For the ILC Electronics Collaboration

Outline

1. What is ATCA and Why Should We Care?
2. Application to Machine Controls and Instrumentation
3. Note on Application to Detectors
4. Conclusions

- Appendix: Slides of ATCA & ILC High Availability R&D Applications

What is ATCA?

- A new Industry-developed modular open standard
  - *Large industry consortium called PICMG developed for telecom product "interoperability"*
  - *Released in 2005*
  - *Supported by ~250 companies*
  - *Several Telecom companies currently in development stage of implementing*
  - *Estimated $10B annual market potential (1 ILCU?) suggest very favorable costs for core products*

Why Should We Care?

- Current modular standards with parallel backplanes rapidly becoming obsolete so we will be forced to develop new platforms or adapt existing ones
  - *New chip level products now contain all parallel connections on-chip*
  - *Chip-chip communications via serial multi-Gb/s protocols now standard*
  - *Parallel bus bandwidth limited, represent many potential single points of failure*
  - *New ATCA serial interconnect crate opens architecture to unlimited scalability (e.g. Crate throughput 2 Tb/s with full mesh & today's Ethernet at 2.5 GB/s, increasing with time)*
  - *ATCA currently only viable candidate meeting our requirements*

What is ILC Availability Requirement?

Availability Defined

- *Availability:* Fraction of time machine/system is in "full production mode," i.e. *delivering design luminosity to user*[1].

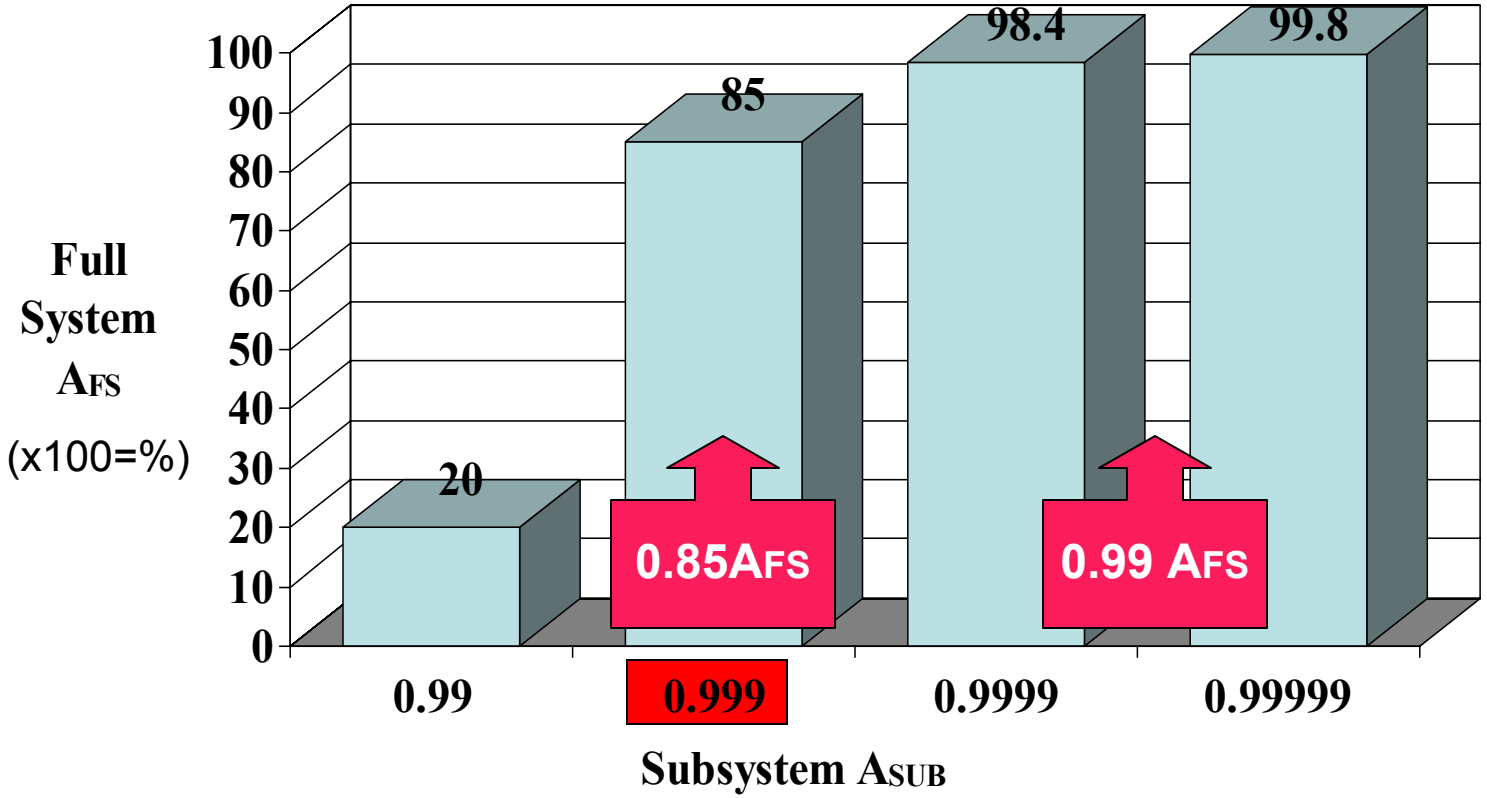
$$A = MTBF/(MTBF+MTTR) \leq 1$$

  - MTBF = Mean Time Before Failure (Reliability)
  - MTTR = Mean Time To Repair
  - Note: If MTTR→0, A →1 regardless of *Reliability*

[1] Most Machine Availability statistics do not account for times of degraded luminosity or time lost in getting from zero to full luminosity, which are significant.

Required Subsystem Availability A_{SUB} for Full System A_{FS} >0.85 = 0.999 Avg

Comprising 16 Systems, 10 Subsystems each System



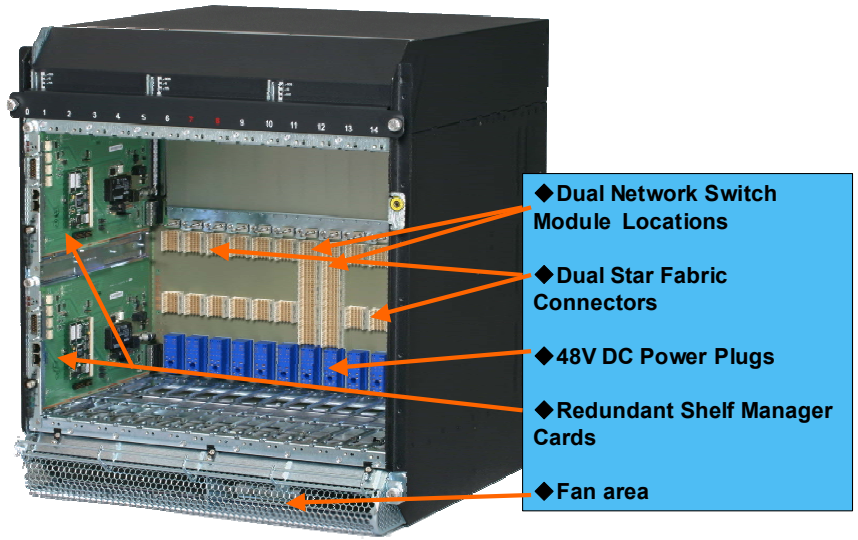
Ref: Larsen & Downing, 2004 IEEE NSS, Rome

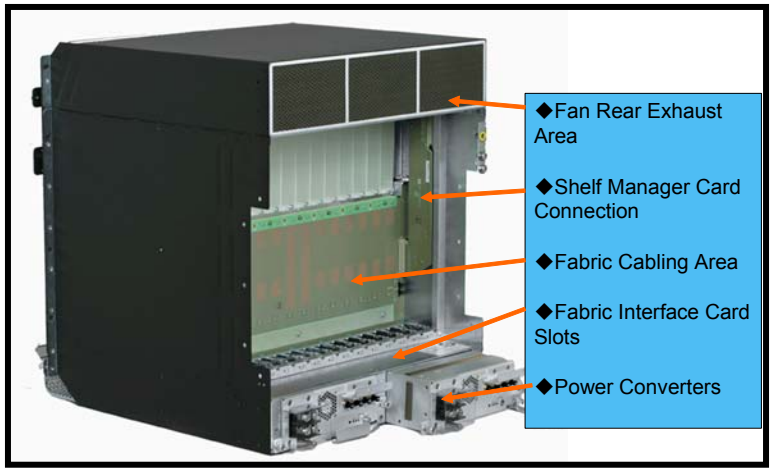
What Can ATCA Provide?

- A system building block of crate (Shelf) and 12-14 modules with vital features:
  - *Dual redundant communications node, processing core w/ auto-failover*
  - *Redundant 48V power supplies, fans*
  - *Serial power feeds to each module, serial I/O, Intelligent Platform Manager (IPM) to diagnose, isolate faulty modules, power or fans*
  - *Once isolated, faulty units can be replaced by technician without interrupting crate, controllers or remaining modules (Hot Swap capable)*
  - *Result:*

2004: Introduction of ATCA*

- Telecom Industry Open Standard
- Driven by $10B/year server and switching market
- *A=0.99999 = Downtime of 5 minutes/year*
- All Gigabit serial Dual Star or Mesh backplane
- Dual controllers, 48V PS, hot swappable,
- 200W/module air cooled, 3+1 Fans hot swappable
- Shelf Manager controls failover, power metering, hot swap





**Advanced Telecom Computing Architecture*

Courtesy PICMG-ATCA

More ATCA Features

- "High Availability" (HA)
  - *Telecom a high throughput business that must tolerate inevitable hardware & software failures*
  - *Clever strategies in architecture make rapid failover possible so another unit (module) automatically takes over job of a failed module (data processor)*
  - *Meanwhile, watchdog system ("Shelf Manager") detects faults, flags maintenance action, so modules, power supplies, fans and even entire crates can be replaced without interrupting data flow.*
  - *The ILC machine will never run with acceptable uptimes without using these kinds of design strategies (Ref. T. Himel's AvailSim studies).*

Crate & Module Power

- All power to crate is standard 48V DC
- Redundancy schemes can be dual or N+1 modular supplies
- All secondary voltages developed on-card!
  - *Trend for chips is ever lower voltages, higher functionality, higher currents*
  - *Whole new family of chip-size units on market provide range of chip voltages 0.5 to 12V*
  - *Power converter chips have their own IPM system!*
  - *Crate, existing modules remain compatible as new, different voltage devices introduced into new modules without rendering existing products obsolete*

ATCA Applicability to ILC

- Industry standard crates & modules can provide off-the-shelf core components today
- Industry developing HA software systems for IPM etc.
- Module format extremely versatile for custom applications
  - *Small daughter cards on carrier board, optional chassis sizes including "MicroTCA"*
- Extremely good grounding & shielding
- Dense robust connectors for multi Gb/s serial
- Manufacturer-flexible backplanes: Dual Star, Full Mesh, custom

Custom Designs Needed

- Highly precise timing, rf phase distribution modules and links
- Specialized front-end modules for machine instrumentation
- Modules also suitable for some power applications, slow instrumentation
- Interfaces to standard controlled machinery such as movers, vacuum etc
- Connector systems for Rear Transition Modules (RTM, like Fastbus rear entry, for hot-swap if rear signals being switched in fail-over operations)
  - *High density high bandwidth for digital; group coax for LLRF*

ATCA Work In Progress

- Purchased test systems: SLAC, FNAL,ANL, DESY
- Evaluation efforts of core systems underway
- DESY investigating TCA, MicroTCA for XFEL applications
  - *Controls. Protection, Low Level RF*
  - *Must make decisions in ~1yr*
- FNAL developing 12 Ch 500 MS/s 14 bit module for BPM's for SRF Facilities

Work in Progress 2

- SLAC contracted shelf manager evaluations, development of ATCA VME adapter to University of Illinois (UIUC)
  - *Ability to plug in existing VME instrument cards will make possible configuring test systems much more quickly, gain experience with core systems, software, do real work*
- ANL concentrating on system level 3 tier software, interfacing to EPICS and/or DOOCS
- ILC Controls & instrumentation cost model assumed ATCA as base system; used commercial pricing & applied large quantity learning curves
  –

IEEE RT2007 ATCA Workshop

- Held in late March 2007 at FNAL (1 day before conference)
- 85 paid attendees
- Industry inventor expert tutorials, papers by lab people, panel discussion
- ~ a dozen ATCA related papers presented at following conference
- High interest in following up with user group communications
- Interest among ILC, ITER and others in an ATCA-P (Physics) profile so labs can build interoperable modules (e.g. common protocols)
  - *Much easier with common protocol serial I/O system!*

What About Detectors?

- Off-the-shelf ATCA hardware has clear applicability to Trigger-DAQ, Event Builders
- Architecture lends easily to front-end designs
- Power systems, new products will be extremely useful at many levels
- Architecture most valuable for inaccessible applications
  - *Will have to invest in radiation hard device designs, radiation protection schemes, or remote access schemes for robotic replacement (e.g.) for buried applications*

Summary Challenges

- Need R&D to decide feature set, evaluate performance of ATCA as instrument platform, prototype example critical hardware-software applications.
  - *HA requires large investment especially in software systems.*
  - *Need international project electronics collaboration for best results, industry support for both machines and detectors.*
  - *ILC, ITER, light sources, astrophysics, future experiments in all areas*

Conclusions

"Design and build systems that do not interrupt operation when components fail."

- HA design strategy well accepted in the ILC
  - *HA principles apply to all systems, not just I&C but power electronics, magnet systems etc.*
  - *ICL has large program in these areas*
- *ILC Subsystem A → 0.999 needed for overall A → 0.85*
  - *But human errors, system & configuration management must be very well controlled as well*
- Readiness of ATCA Platform potentially huge payoff for research communities
  - *Labs could not afford such a huge development effort*
  - *Imperative to move forward rapidly to explore applications for all machine, experimental systems*

Acknowledgments

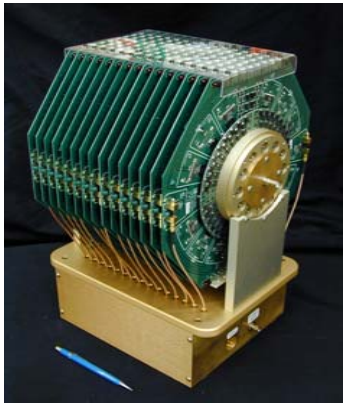
A large team is engaged in various aspects of the ILC High Availability electronics programs at SLAC, Argonne, Fermilab, Lawrence Livermore, KEK, DESY, Pohang, University of Illinois (UIUC).

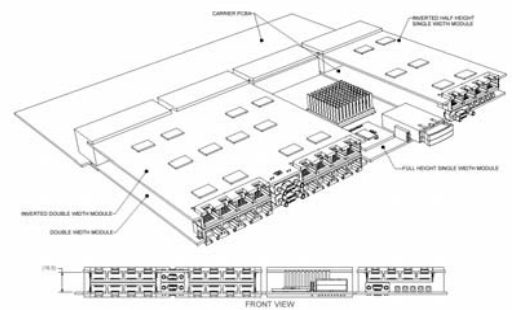
John Carwardine of ANL heads the ILC Controls collaboration; Kay Rehlich, Stefan Simrock the DESY-XFEL initiatives; Shin Michizono the KEK efforts. R. W. Downing formerly of UIUC is a consultant for the program.

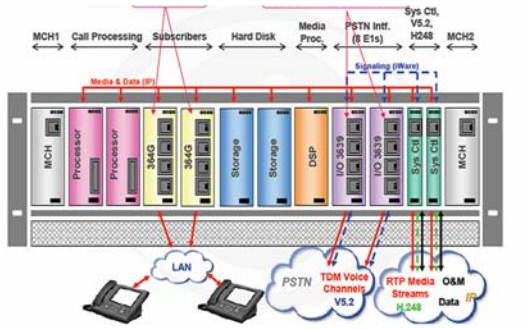
Many others in labs and universities have pilot programs underway to gain new insights. Check the program of IEEE Real Time 2007 (Margaret Votava of FNAL, Chair) for information on abstracts.

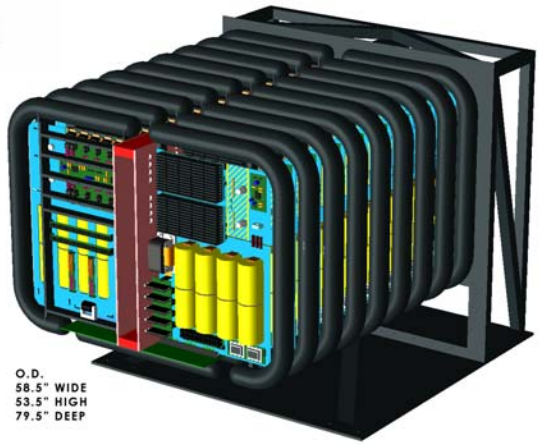
Appendix

- Slides of ATCA hardware, module options, backplanes, power systems, new HA architectures for other ILC components such as magnet power, modulators, diagnostics layer.



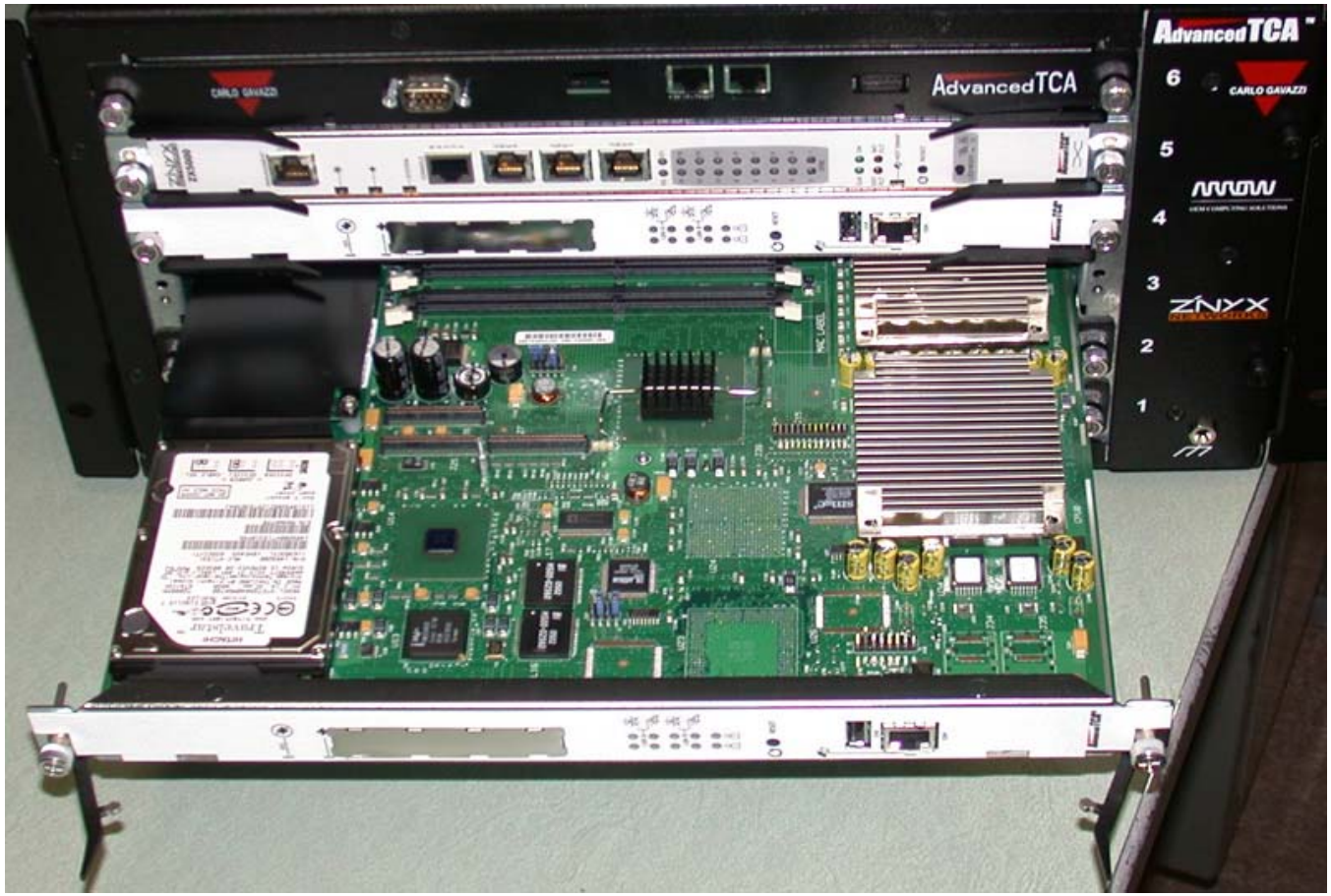






DETAIL, MARX MODULATOR CORE

II.5-Slot Crate (Shelf) Starter Kit



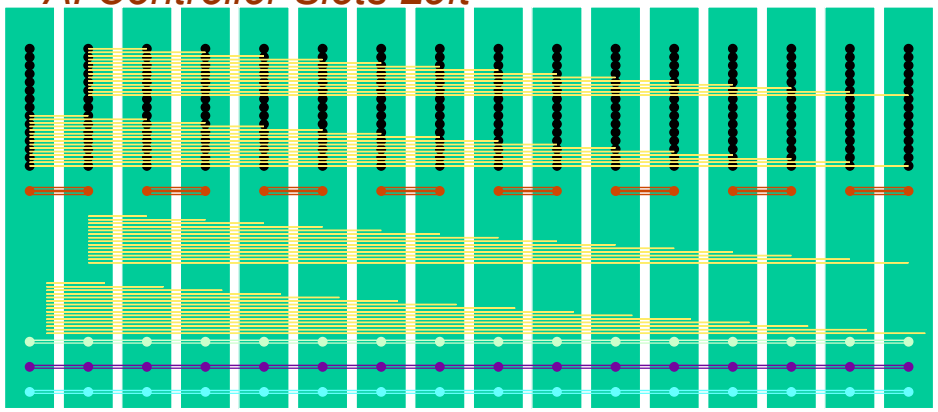
2 Processor Blades, 1 Fabric Switch 3.125 Gb/s, Shelf Manager (Inside box, not shown)

-Arrow Electronics

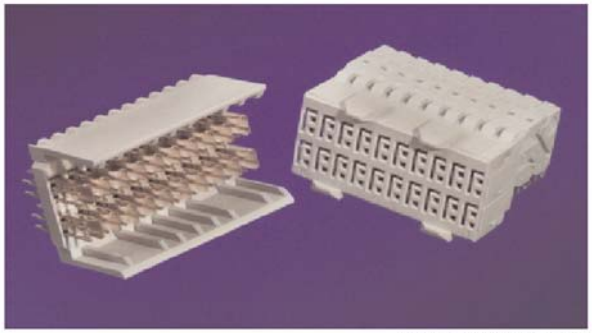
II. Dual Star Backplane & Fabric Connector

AdvancedTCA Backplane Routing Dual/Dual Star

A. Controller Slots Left



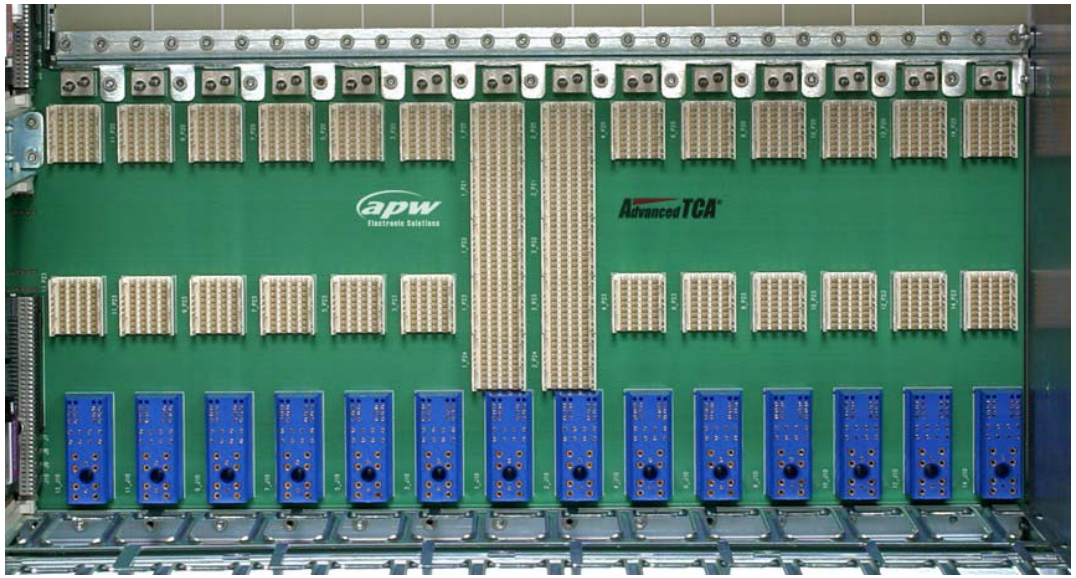
Full Mesh Fabric
Update Channel
Base Interface
Analog & Test Bus
System Management Bus
Power



20 Pair Header and Receptacle

- Data Fabric, Update Channel, and Timing Clocks
- Up to 3.125Ghz clock rates
- Pins protected by ground shield from bending
- Up to 5 connectors can be used on a backplane per slot

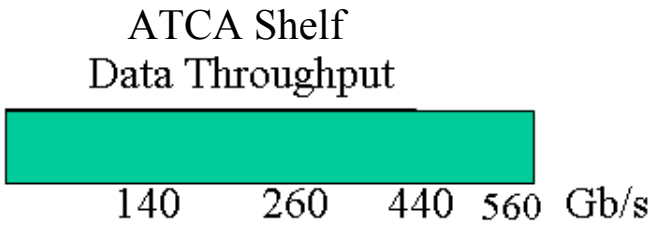
B. Controller Slots Center

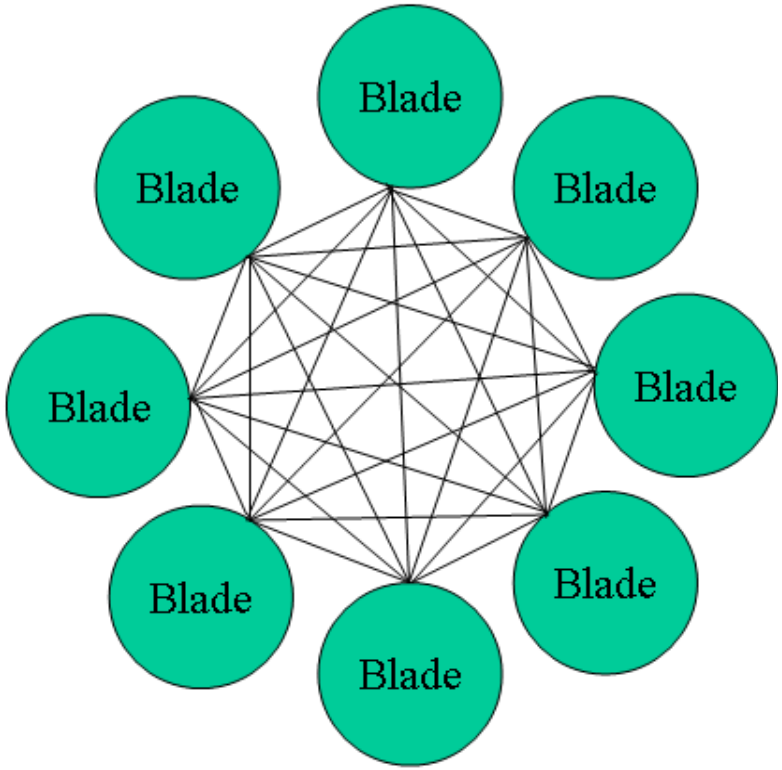


Courtesy PICMG-ATCA Consortium

II. ATCA Topology Options

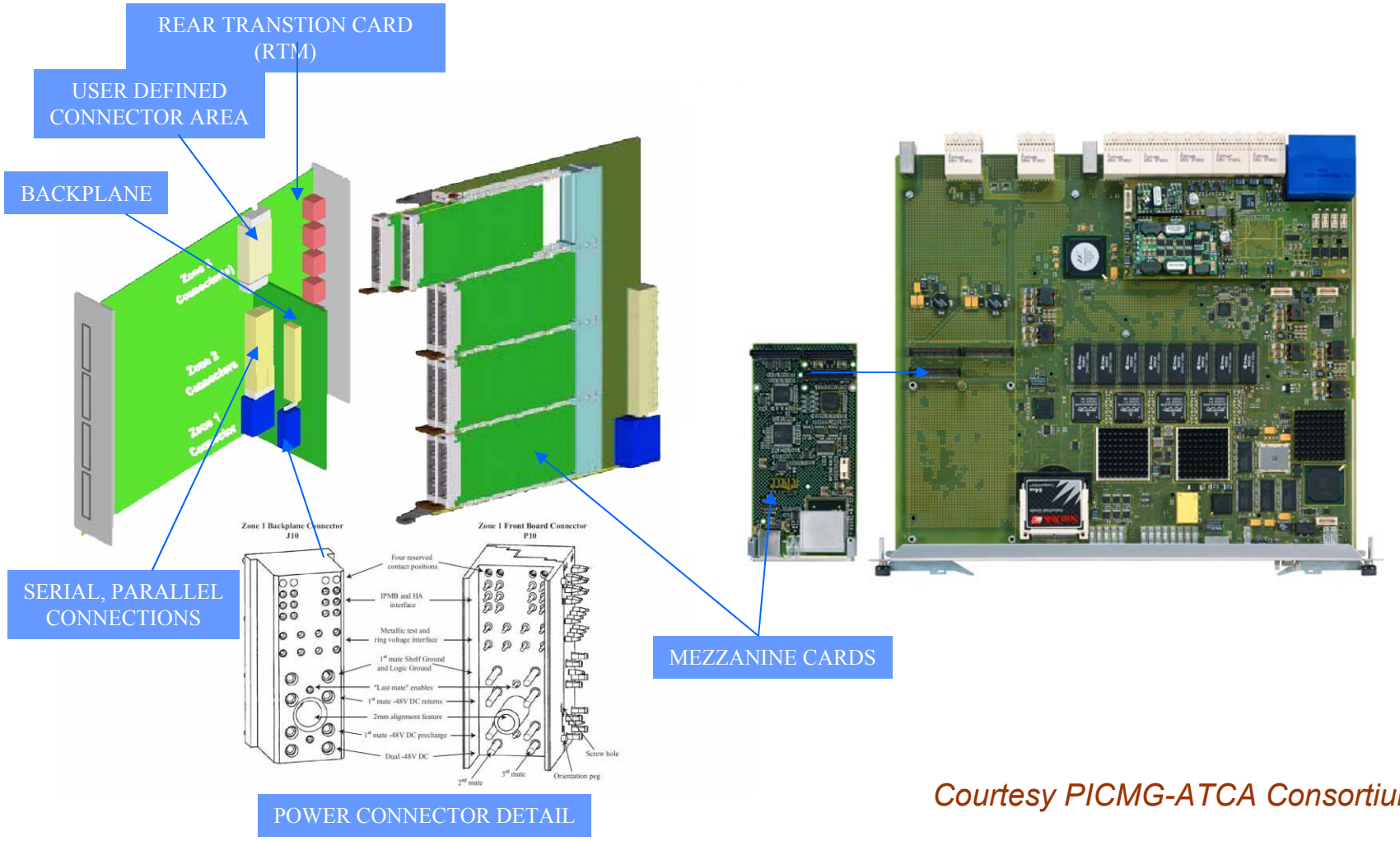
- PICMG 3.0 supports multiple topologies
  - Star (140 Gb/sec in 8 slots)
  - Dual Star (280 Gb/sec)
  - Full Mesh (560 Gb/sec in 8 slots)
- A 14 slot ATCA shelf could support data rates to 2.1Tb/s





Courtesy PICMG-ATCA Consortium

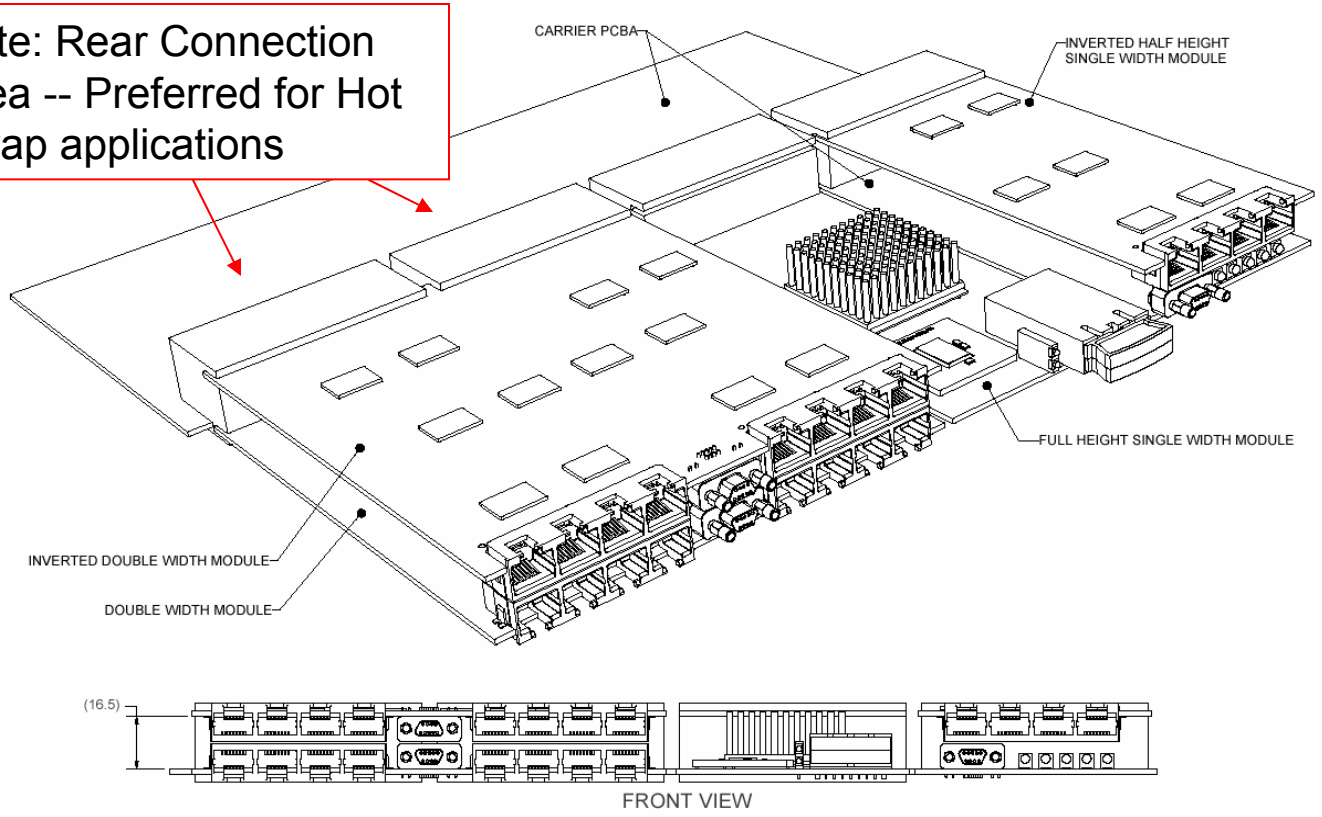
II. ATCA Card Options



Courtesy PICMG-ATCA Consortium

II. ATCA Carrier & Mezzanine Cards

Note: Rear Connection Area -- Preferred for Hot Swap applications

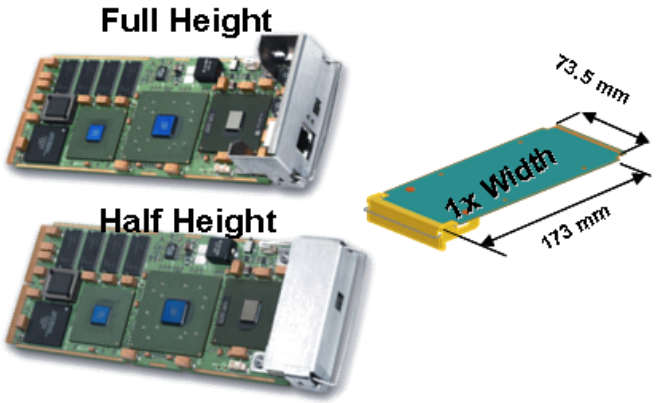


Courtesy PICMG-ATCA Consortium

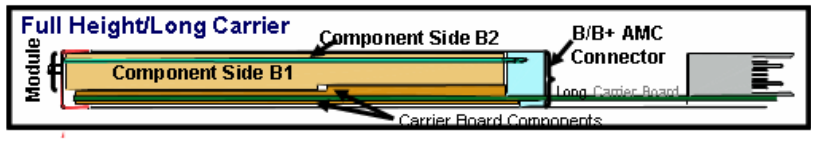
II. Advanced Mezzanine Card

Full Height & Half Height

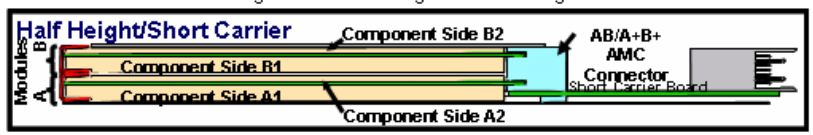
- What's an AMC?
  - A next generation mezzanine standard optimized for ATCA and high-speed interconnects such as PCI Express and Advanced Switching
- What's it good for?
  - Design simplification
  - Reduced board complexity
  - Increased throughput
    - 21 duplex ports @ up to 12.5 Gbits/s each
    - Designed to also enable SPI-4.2
  - Increases high availability with IPMB and Hot Swap
  - Modularity increases system density and improves TTM
    (due to less baseboard redesign)



Photos Courtesy of Artesyn Technologies



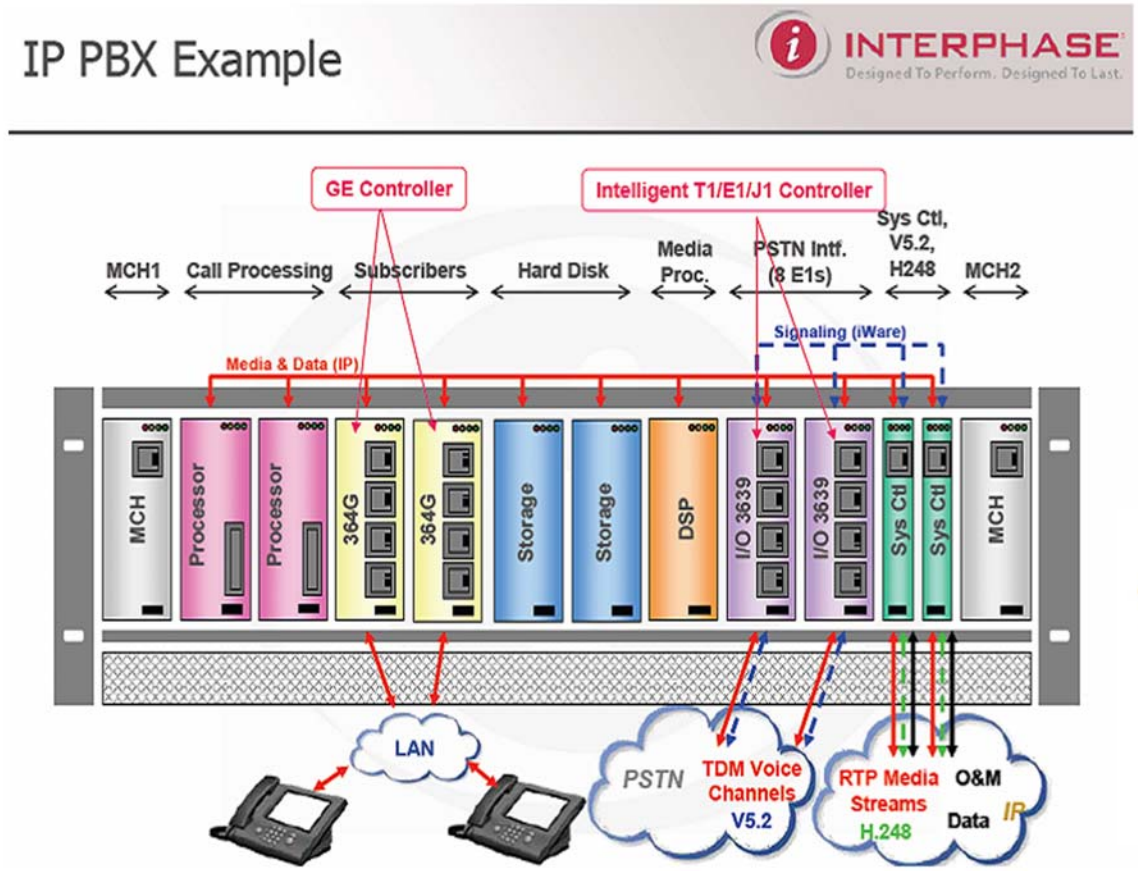
Note: Half Height Modules can go into Full Height Connectors



IPBM=Intelligent Platform Management Board
TTM = Time To Market

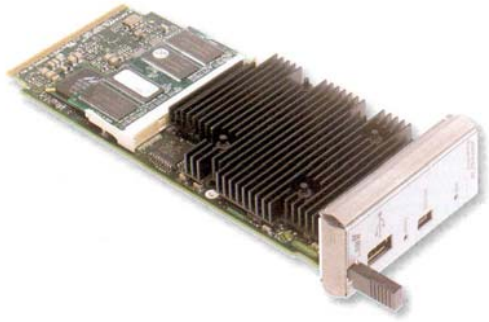
Courtesy PICMG-ATCA Consortium

II. MicroTCA Chassis



MicroTCA

Platform designed for standard Mezzanine cards in separate low profile package. Current design is NOT rear-only connection.



Courtesy Interphase Corp.

II. Commercial DAQ Instruments Example

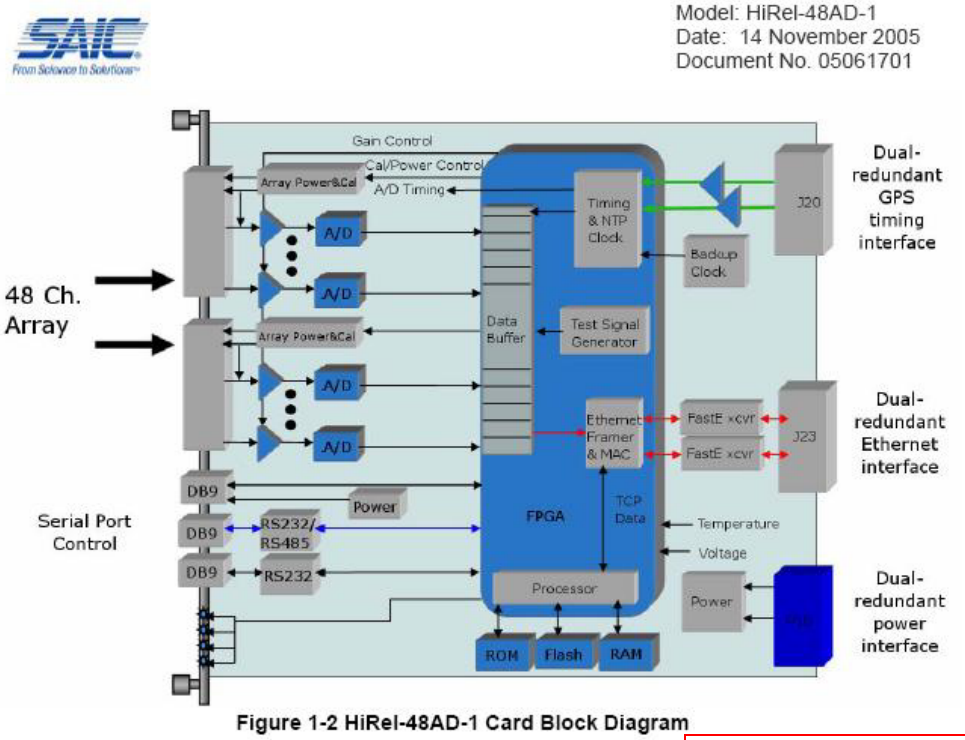
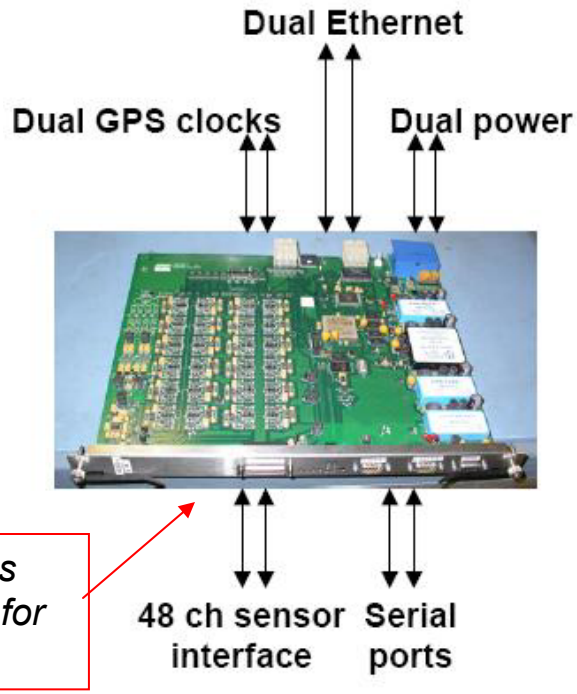


Figure 1-2 HiRel-48AD-1 Card Block Diagram

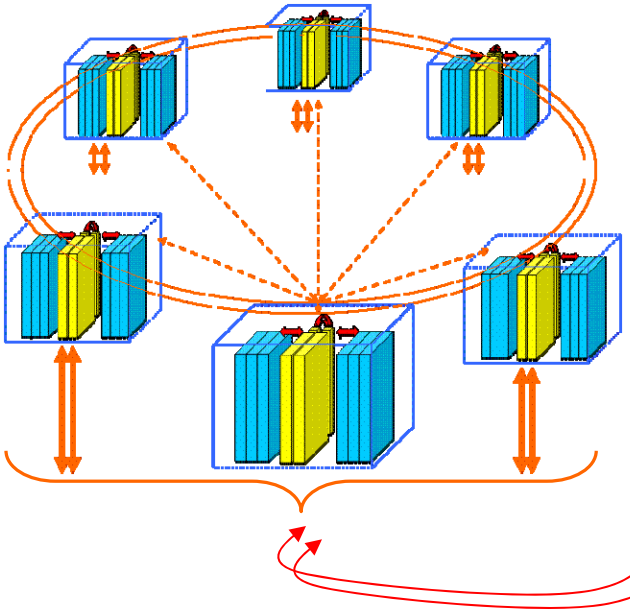
Designed for large array underwater sonar experiment, early ATCA, redundant for high reliability, 10W total board power, GPS timing.

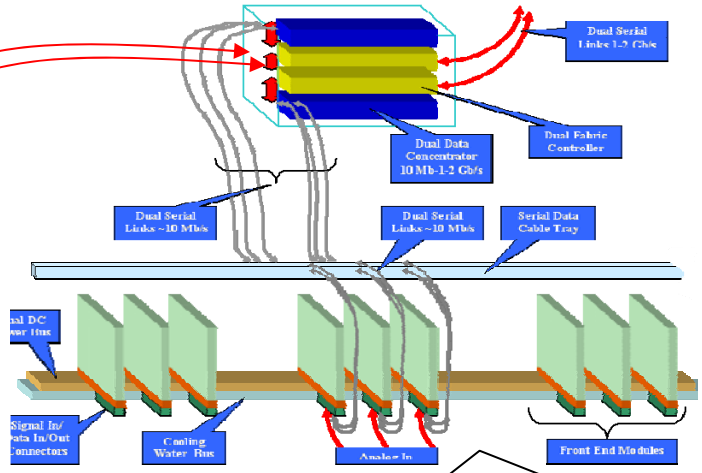


Note – FP connections can be moved to rear for hot-swap.

II. Proposed ILC Applications

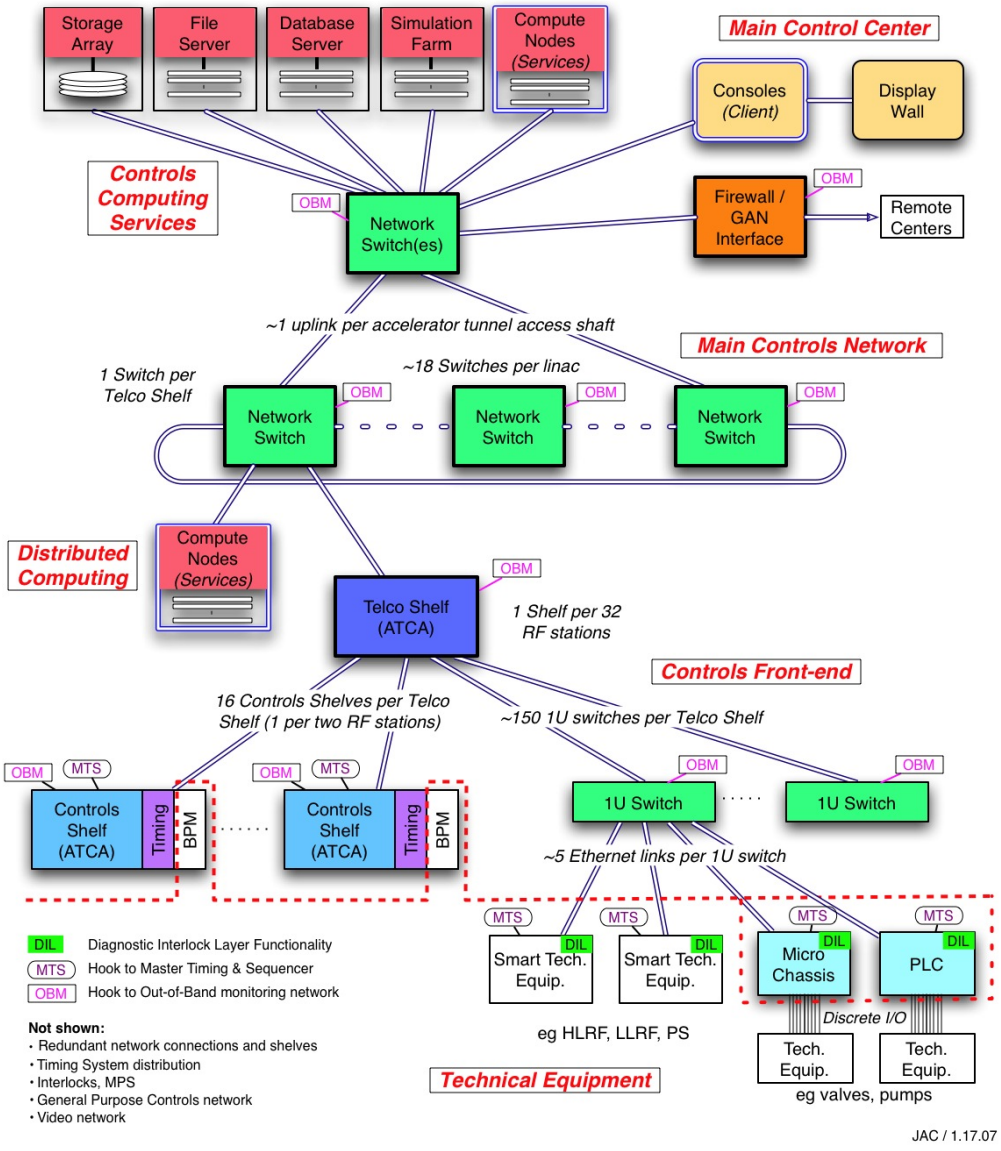
- Controls Backbone
- Main Control
- Remote Sector Nodes
- Front End Instruments





Front End Instruments in standard crates & racks or special structures, e.g. Detectors

II. ILC Controls Architecture Details



Courtesy J. Carwardine Argonne National Lab

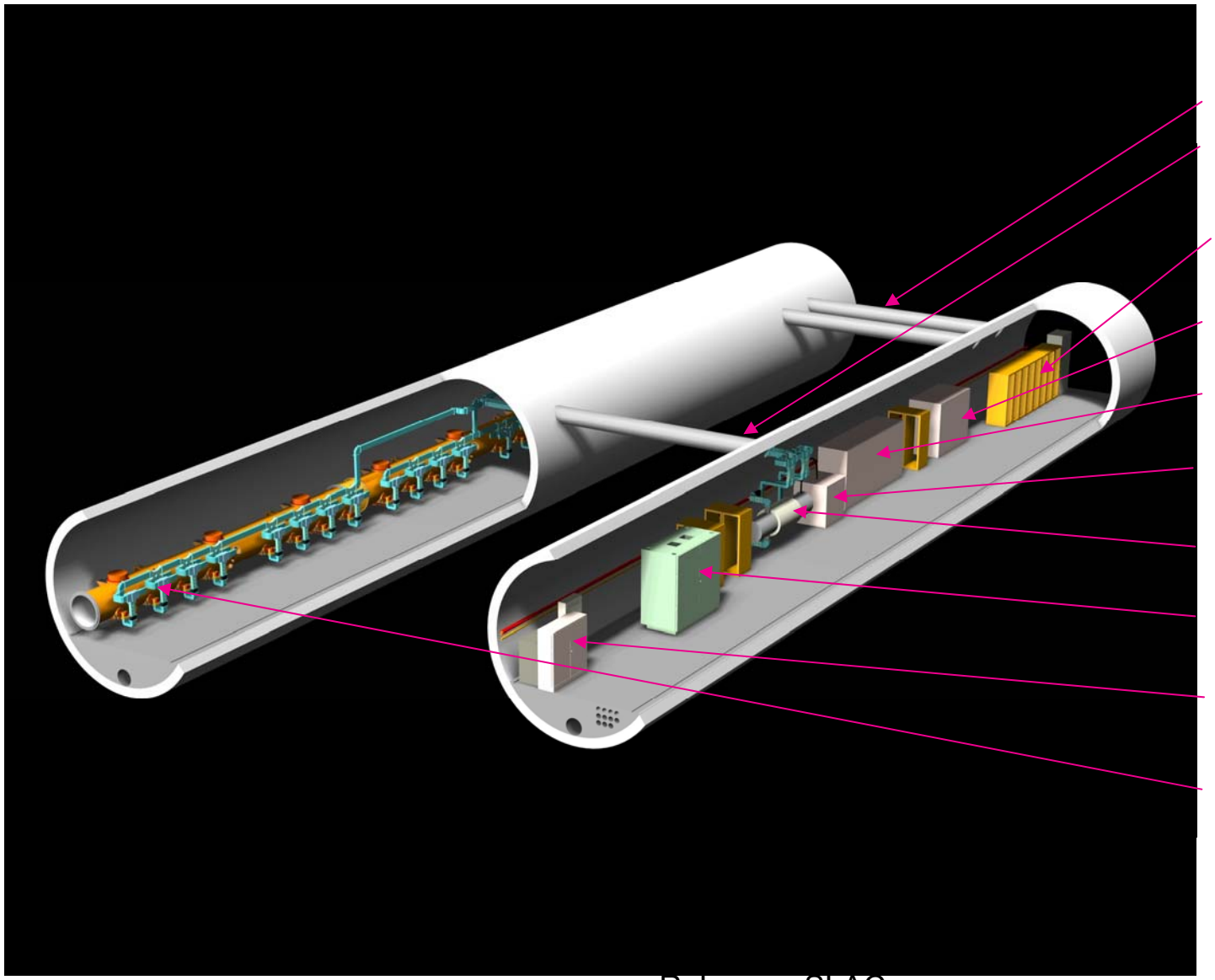
III. Power Systems Architectures

- 1. Crate & Card-Level Power Systems
- 2. DC Magnet Constant Current Power Supplies
- 3. Marx Klystron Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer

III. Main Linac RF Power

- Dominate electronic systems costs:
  - *~650 10 MW 1.3 GHz RF Stations (modulators, klystrons, waveguide distribution)*
  - *~5000 equipment racks for LLRF, BPM, magnet supplies, vacuum, tuners etc*
  - *~1,500 ATCA crates.*
- Main limitation to availability:
  - *RF power, DC power systems*

ILC Baseline: 38m 10 MW Linac RF Station



Penetrations:
Cable & Plumbing
Waveguide

LLRF, Controls,
Protection Racks

Charger

Main Modulator

HV Pulse Transformer

Horizontal Klystron

LCW Chiller for Racks

HV Supply Switchgear

Waveguide
Distribution
System

Courtesy: J. Liebfritz, FNAL

III. Power Systems Architectures

- 1. Crate & Card-Level Power Systems
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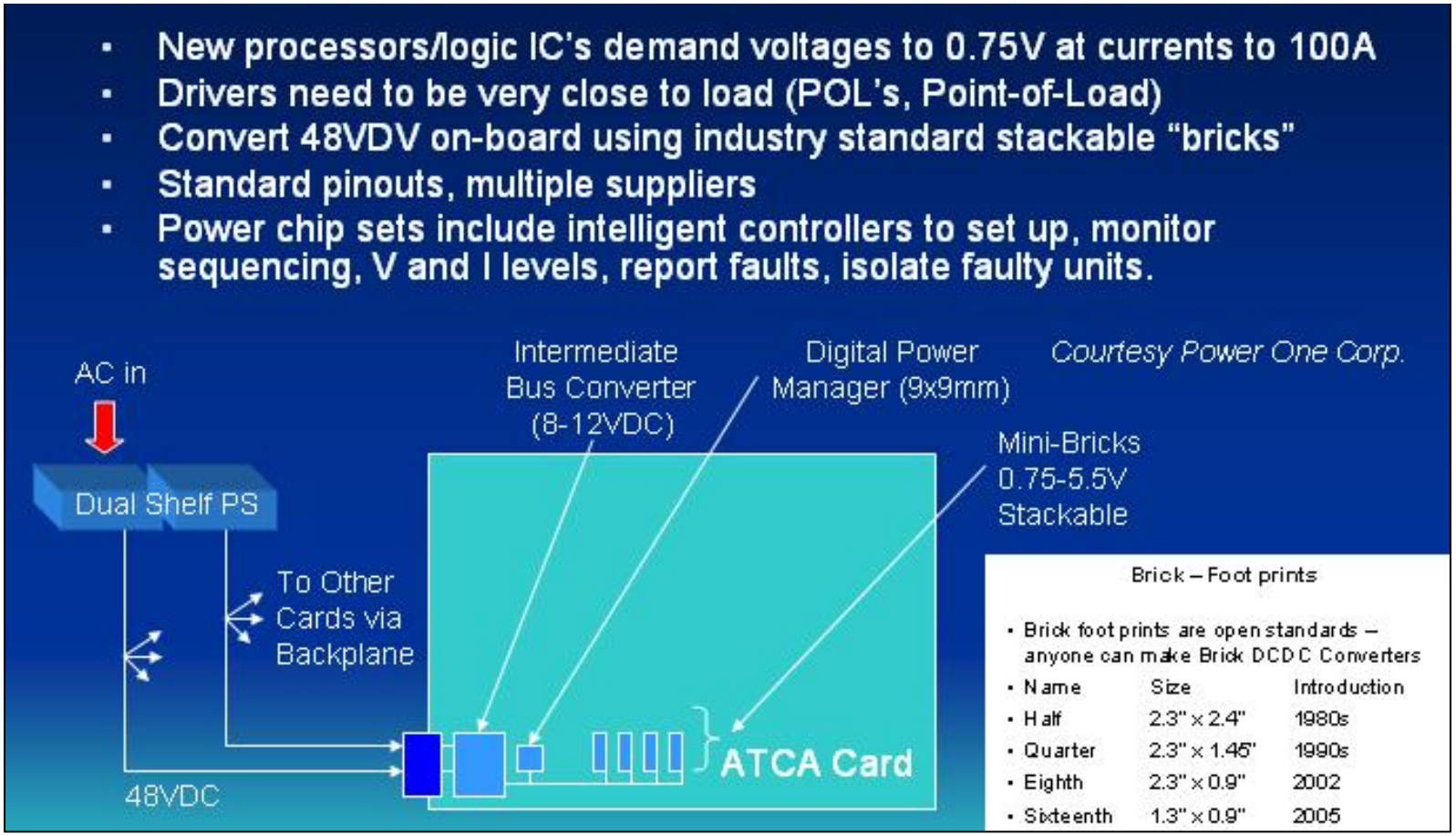
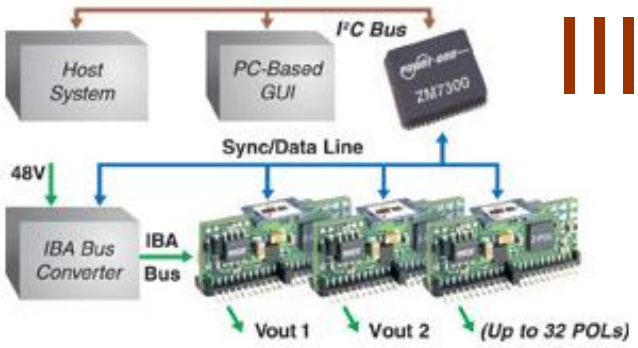
III-1. Card Level Power Systems

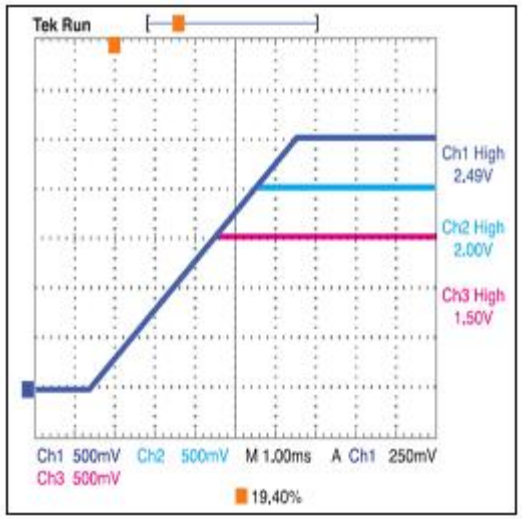
Commercial Solutions from Telecom Industry



III-1. Power Converters*



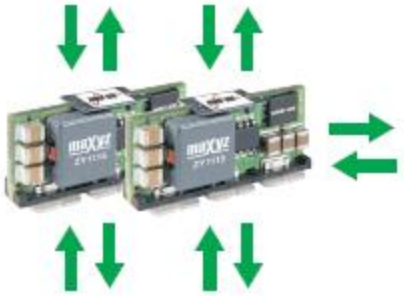
Z-One® Digital Power is a multi-source open-architecture power solution that optionally utilizes an industry-standard I²C interface.



No-Bus™ Z-1000 POLs feature guaranteed tracking between multiple outputs

Output Voltages and Currents

- Output voltages (0.5 to 5.5V) and turn-on delays are configured with an external resistor and a capacitor, respectively.
- Up to ten Z-1000 POLs can current share using a single control trace.
- Z-1000 POLs can start up with pre-biased outputs.
- Sink and source current capabilities for active bus termination.



Signals and Protections

- Reporting of output current and temperature via signal pins.
- Thresholds for overvoltage, undervoltage, and Power Good track the output voltage settings.

Coordination and Optimization via Simple Pin Strapping

- Frequency synchronization and phase interleaving reduce EMI.
- Comprehensive sequencing and cascading management.
- Feedback loop compensation and enable logic.
- Frequency synchronization, fault propagation, and current sharing are implemented, without external components, by interconnecting the respective pins on the Z-POLs being coordinated.

*Courtesy Power-One Corp.

III-1. Intelligent Power Application - Beijing*

Xinwei Configures Z-One® Digital Power for "Big Smart" Wireless in Under 10 Minutes

DC-DC Converters Quick Links

The Z-One® POLs pictured below provide point-of-load power for Beijing Xinwei Telecom's "Big Smart" SCDMA wireless service. SCDMA incorporates advanced technologies, such as smart antenna, software radio, and synchronous wireless access protocol, to target a Chinese market projected to grow from 3 million users in 2005 to over 20 million by 2007. This extremely complex application requires six different voltages, from 1.3 to 3.3VDC, with peak currents approaching 60 amps.

Xinwei's Chief scientist, Dr. Guanghan Xu commented, "Using the Z-Series graphical user interface, we were able to configure a power system in less than ten minutes.

This is extremely impressive considering that the diverse range of functionalities we implemented included paralleling, turn-on cascading, and fault management. Z-One Digital Power saved weeks of design time compared to analog power management. The complex power requirements of our base station control board, combined with our need for on-the-fly reconfiguration, would have been extremely difficult to support without Power-One's revolutionary Z-One Digital Power."

III. Power Systems Architectures

- 1. Crate & Card-Level Power Systems
- 2. DC Magnet Constant Current Power Supplies
- 3. Marx Klystron Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer

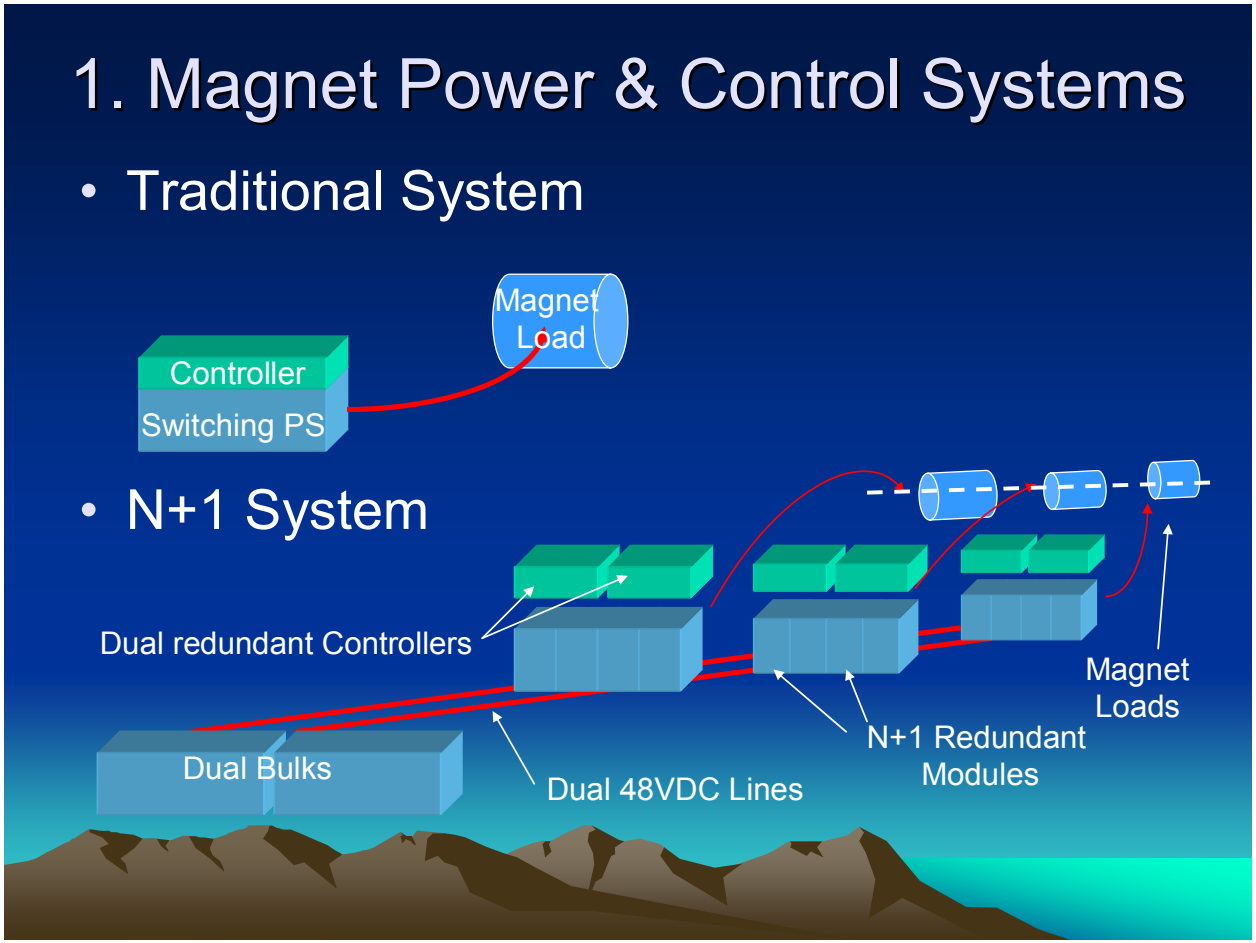
III-2. HA High Power Systems R&D

- *Pulsed & DC Power Systems are major limitations to achieving High Availability in current machines.*
  - *HA principles being applied to all ILC power systems.*
  - *Goal is >0.99 for RF Power System, DC Magnet Power System*
- 1/n Redundancy at 3 levels in Magnet PS, Modulators & Kickers:
  - *High current/power switches*
  - *Modular construction*
  - *System level or Unit level hot spares or hot-swap*
- Intelligent Diagnostics Layer
  - *Minimize Mean Time to Repair, monitor health at card level.*

- *Goal: Keep operating with 1-2 failed cells; change failed cells while machine keeps running if possible.*

III-2. DC Magnet Power & Control Systems

- *For A=0.99, need redundant Bulk, Modules & Controllers*



**Modular Supplies <1 to 60 kW*
**Current stability to .01% typical.*
**Strings & Single magnet applications*

III. Power Systems Architectures

- 1. Crate & Card-Level Power Systems
- 2. DC Magnet Constant Current Power Supplies
- 3. Marx Klystron Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer

III. Marx Modulator

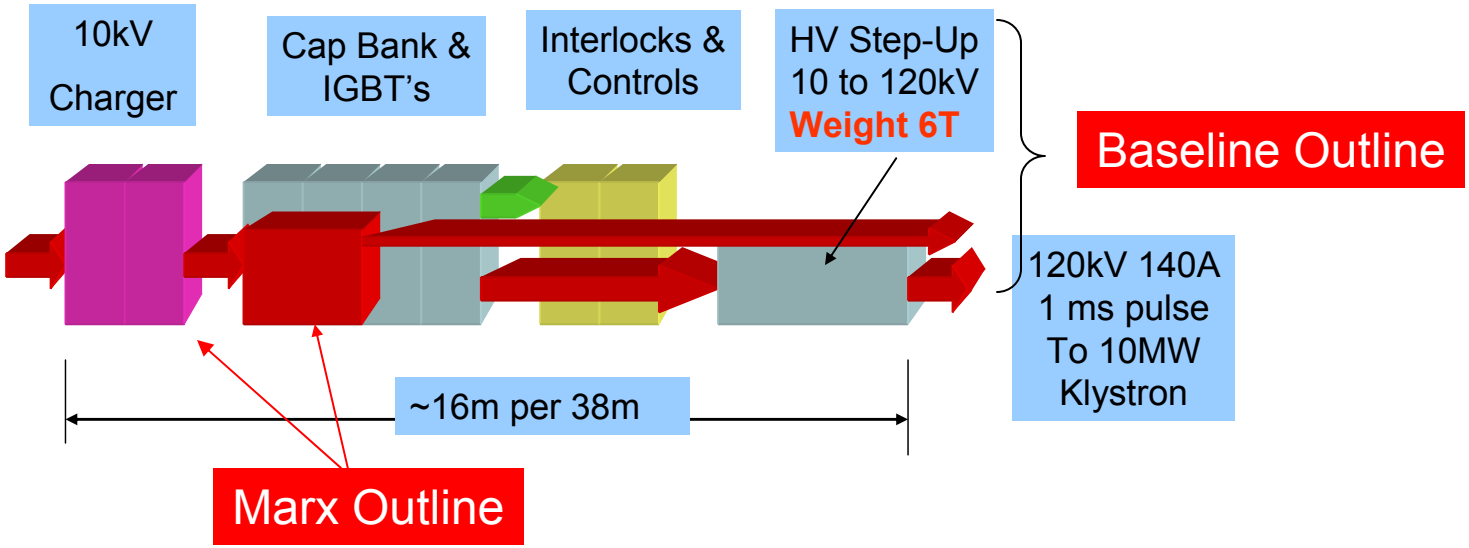
- Being investigated as alternate design to present switched cap "Bouncer" design

Goals:

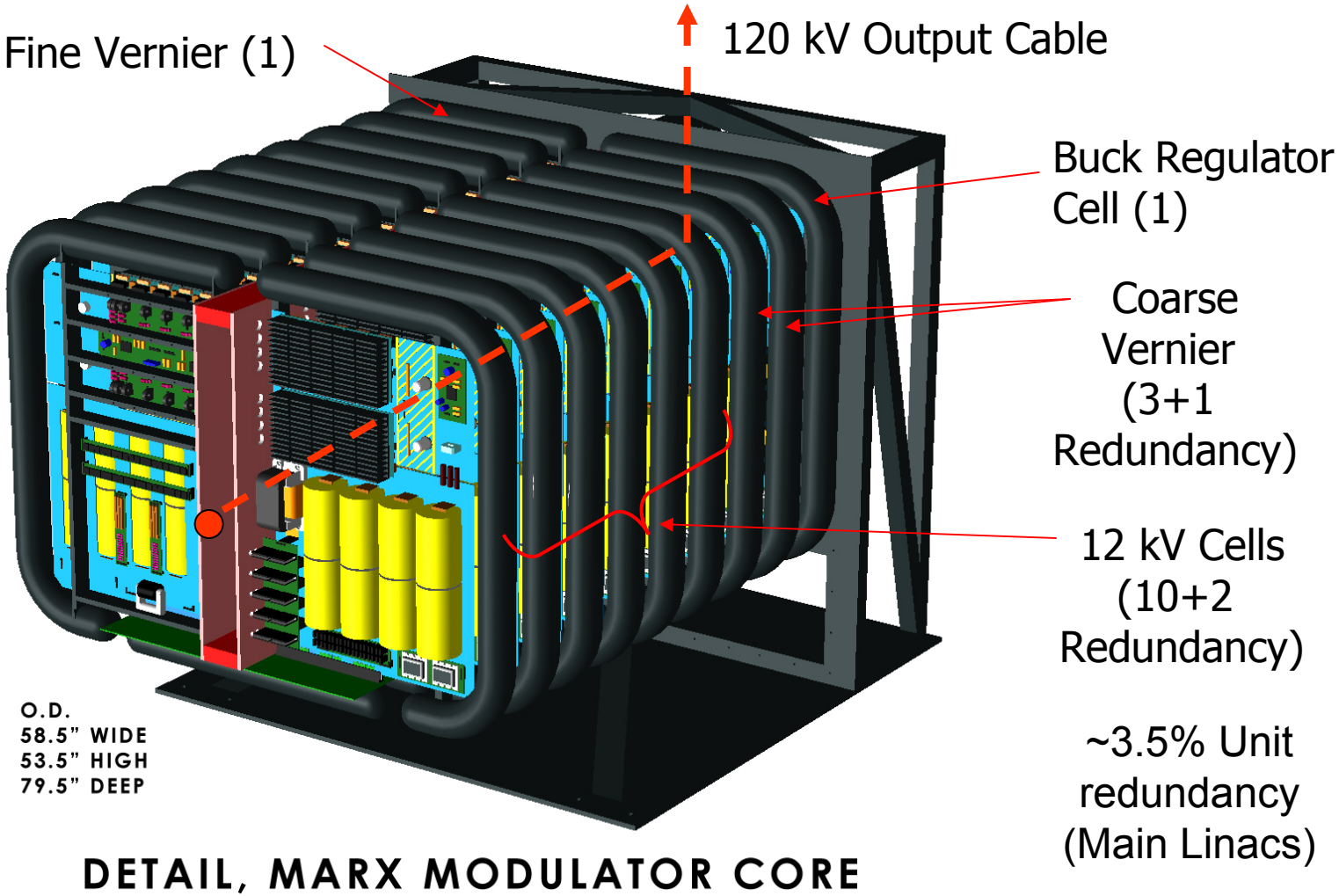
Reduce size, weight, space by 3-4X
Reduce cost by >2X
Increase efficiency
Demonstrate operation in 2007.

Specifications:

120 kV, 140 A, 1.63 ms, 5 Hz
125 kW output power to klystron
Efficiency from wall-plug ~90%



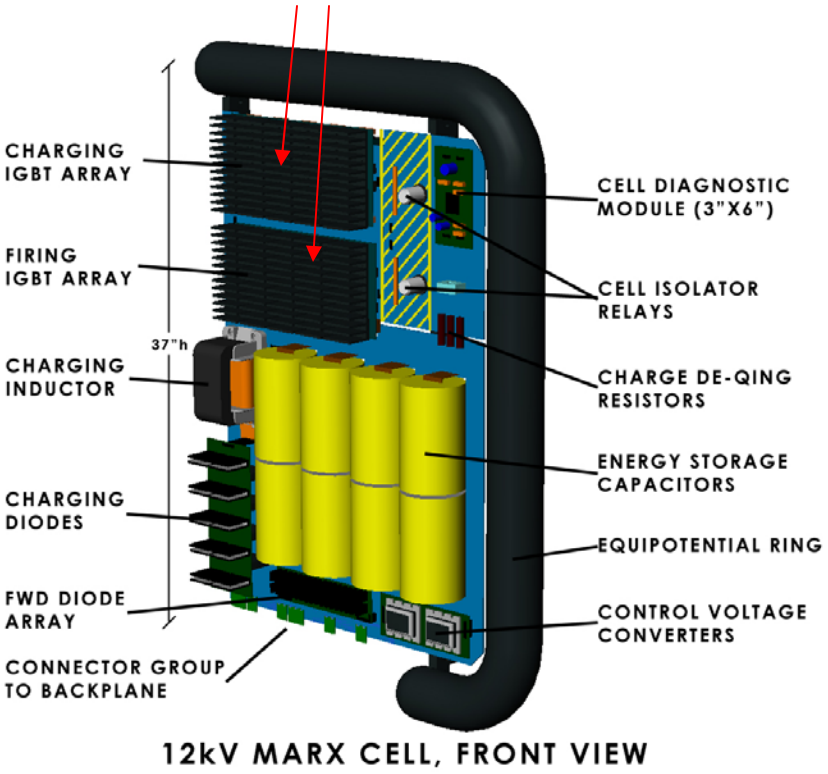
III. Marx Assembly Overview*



*Courtesy G. Leyh, SLAC

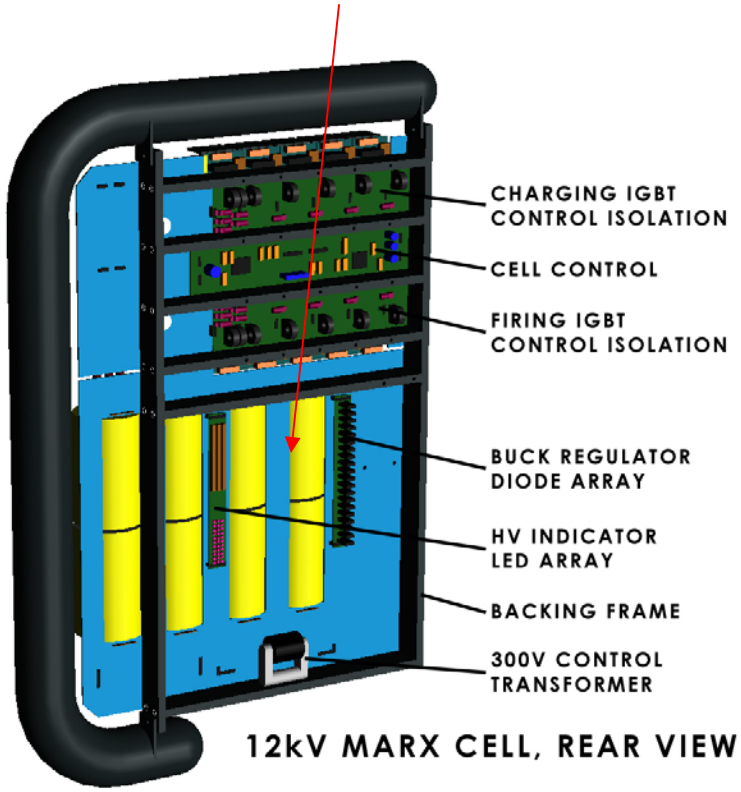
III. 12 kV Cell Detail*

4+1 Redundant Switch Arrays for charge, discharge



12kV MARX CELL, FRONT VIEW

6+2 Redundant Capacitors



12kV MARX CELL, REAR VIEW

III. Power Systems Architectures

- 1. Crate & Card-Level Power Systems
- 2. DC Magnet Constant Current Power Supplies
- 3. Marx Klystron Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer

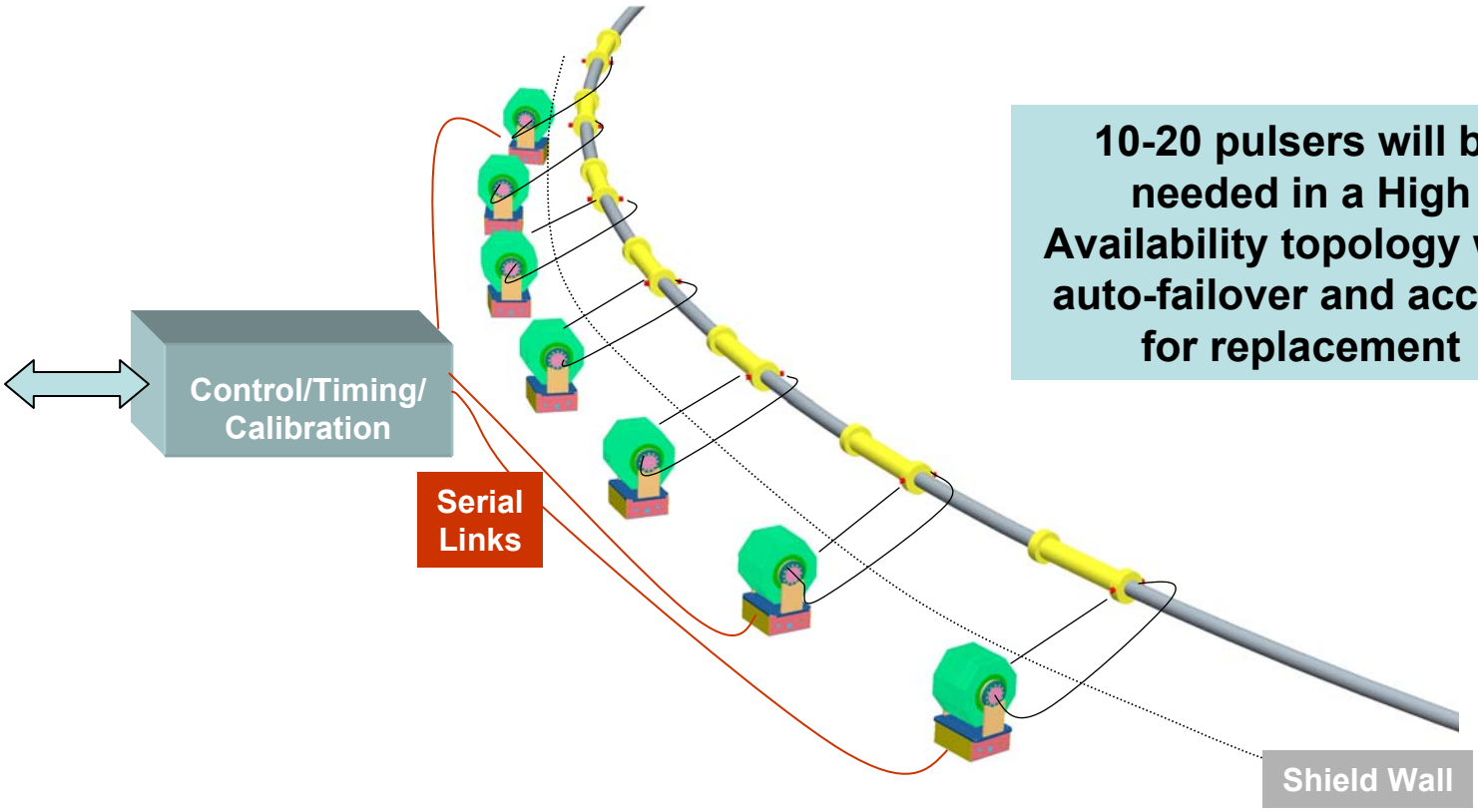
III-4. Damping Ring Kickers

- Damping Ring pulser performance directly related to size of the rings.
- Currently assuming can operate with 6 km circumference largely based on extrapolations of pulser performance.
- Architecture requires a large number of stripline pulsers to develop total kick.

III-4. Damping Ring Kickers

- Goals:
  - *Reduce size, cost of damping rings with 20 nsec beam interleave performance.*
  - Limit size of DR to ~ 6 km circumference.
- Specifications:
  - *Tr, Tf 1ns to +/-5-10 kV,*
  - *3 MHz constant beam extract rate*
  - *Amplitude matching, timing to <0.1% stability long term*
  - *Multiple units needed in tandem*

III-4. Kicker System Topology



10-20 pulsers will be needed in a High Availability topology with auto-failover and access for replacement

Dwg by C. Brooksby BN/LLNL

III. Power Systems Architectures

- 1. Crate & Card-Level Power Systems
- 2. DC Magnet Constant Current Power Supplies
- 3. Marx Klystron Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer (DIL)

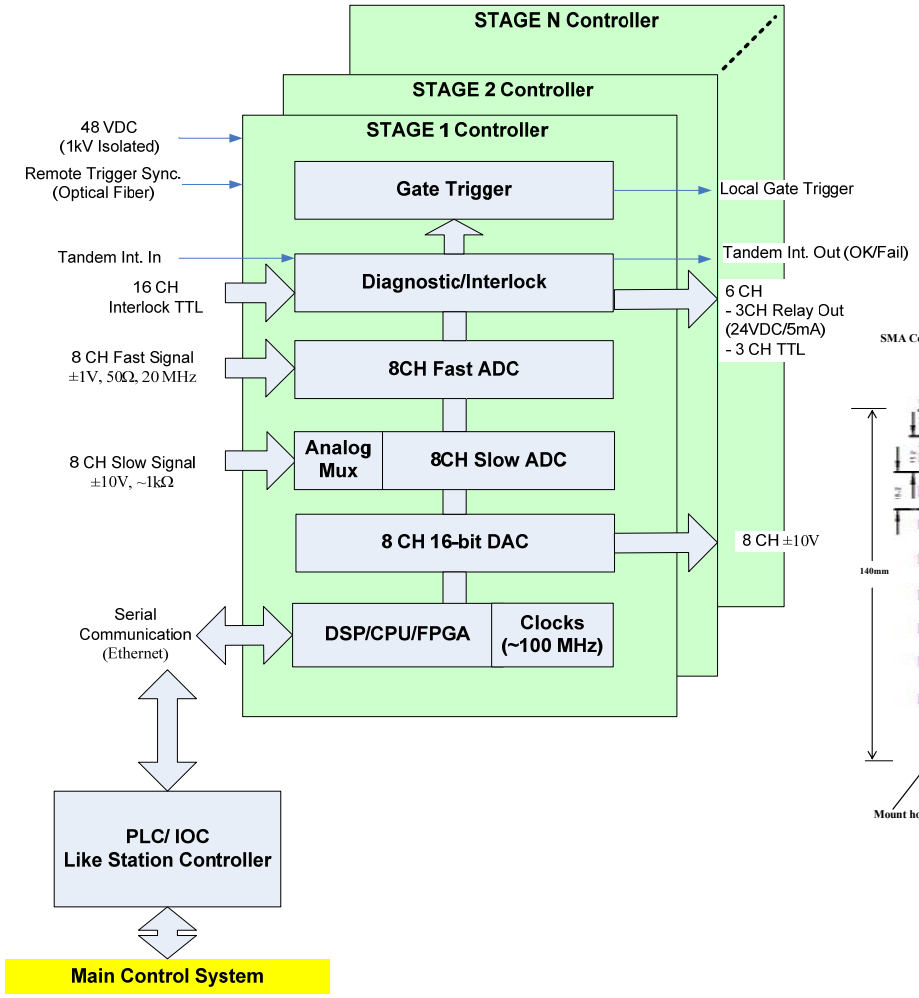
III-5. Diagnostic Interlock Layer

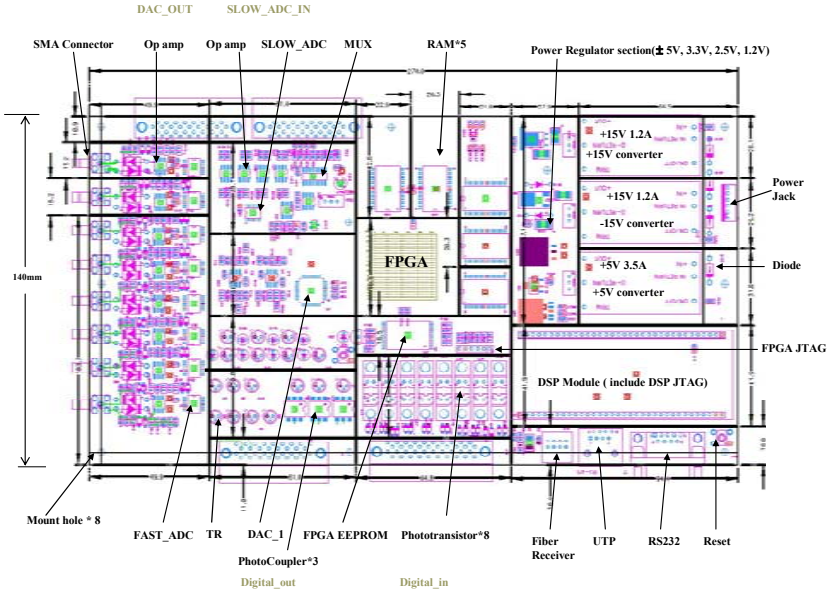
- DIL Goal: Help achieve near-zero MTTR
  - *All power systems will have a "DIL" card or hybrid circuit in each power cell.*
    - Similar in function to ATCA Shelf Manager for Controls crates but with added controls features such as interlock management, waveform capture and memory.
  - *Gathers diagnostic information to view in control room: Interlock set points vs. actual levels; fast and slow waveforms.*
  - *Enables evasive action to avoid trips: Reduces load, adjusts set points if permitted; "safes" system in case of failure.*
  - *Manages Hot-Swap operation if feasible or module swap operation in case of trip.*

III-5. Diagnostic Interlock Layer Concept

- DIL Functions (Typical)
  - *Combination digital controller and memory of small size imbedded into power circuits such as power supplies, modulators*
  - *Captures power conversion waveforms in ADCs to detect early failures in switching circuits*
  - *Captures fast & slow waveforms, stores recent results to local memory*
  - *Monitors interlocks, controls trip settings*
  - *Monitors temperatures of critical components*
  - *Provides fast timing and trigger control & monitoring*

III-5. DIL Prototype Functional Design





Courtesy S. Nam, Pohang Light Source

IV. Ongoing HA R&D Programs

- 1. ATCA Evaluation
- 2. DC Magnet Power Systems
- 3. Marx Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer

IV. Ongoing HA R&D Programs

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IV-1. ATCA Collaboration R&D

- Hardware/software tests of starter kit, shelf manager, auto-failover of controllers, VME adapter development
  - *SLAC with University of Illinois*
- Control system architecture, hardware & software modeling, commercial product search, integrated system search, racks & cooling
  - *ANL, FNAL, SLAC*
- ATCA Adaptation to front end instruments for LLRF, Detectors
  - *DESY, FNAL, BNL, Yale*
- Overall system cost estimates
  - *ANL, FNAL, DESY, KEK, SLAC*

IV. Ongoing HA R&D Programs

- 1. ATCA Evaluation
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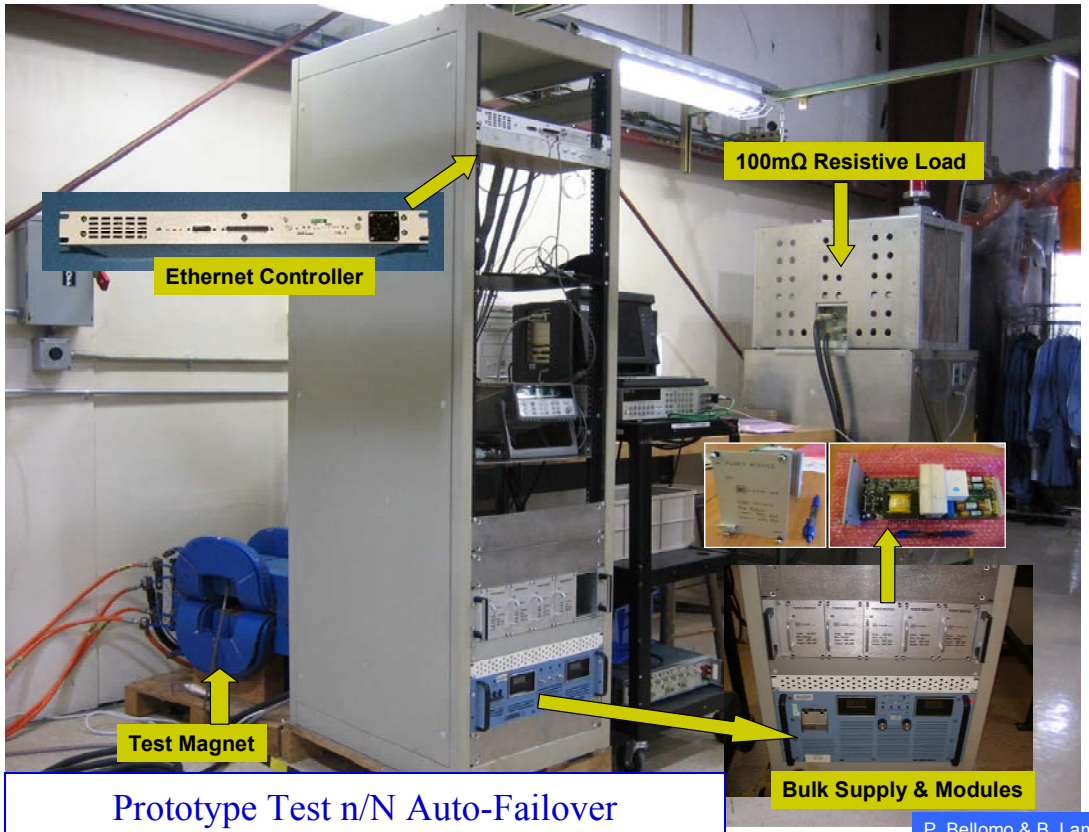
- 5. Diagnostic Interlock Layer

IV-2. DC Magnet Power Systems

- Study of commercial products in prototype 5kW system to demonstrate redundant N+1 architecture, auto-failover, current sharing stability
  - *SLAC*
- Application to system of 41 magnet supplies for ATF2 at KEK
  - *SLAC with KEK, due to complete in 2008*
- Development of dual redundant diagnostic controller for magnet supplies
  - *SLAC*
- Study of low voltage commercial products for crate, board level applications
  - *SLAC, RW Downing Inc.*

IV-2. Magnet PS Prototype R&D

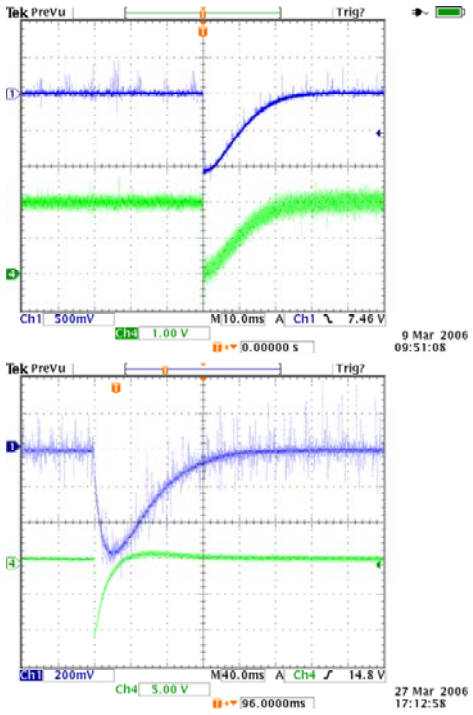
- Approx. 18,000 magnets & supplies in all systems
- FY07-09 Goals: Demonstrate all HA features on multiunit test system in KEK ATF2.



Prototype Test n/N Auto-Failover

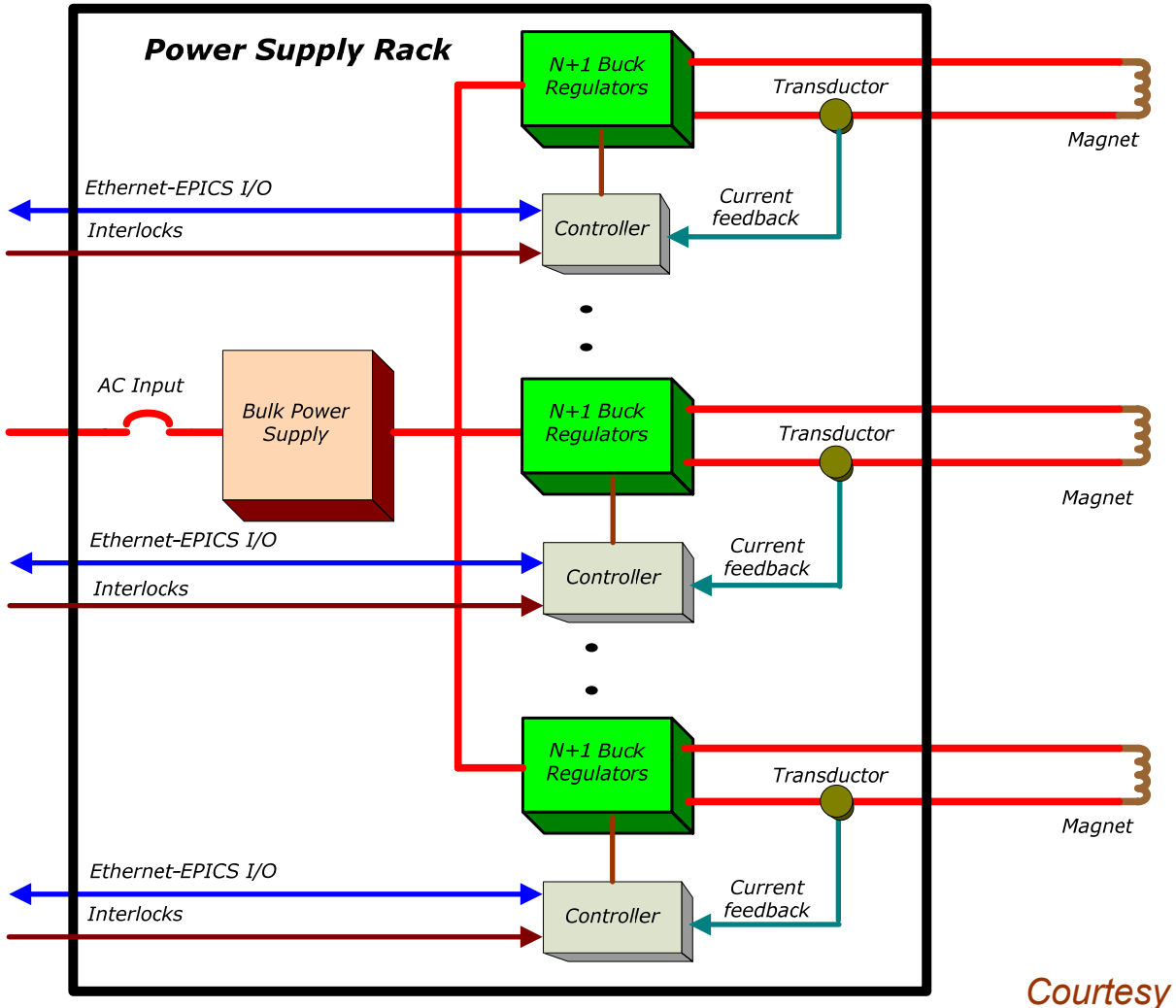
P. Bellomo & B. Lam

Transient Recovery
1 Module Switched Off



Top: Resistive Load, 10 ms/cm
Bottom: Magnet Load +100mΩ, 40 ms/cm

Typical System Block Diagram



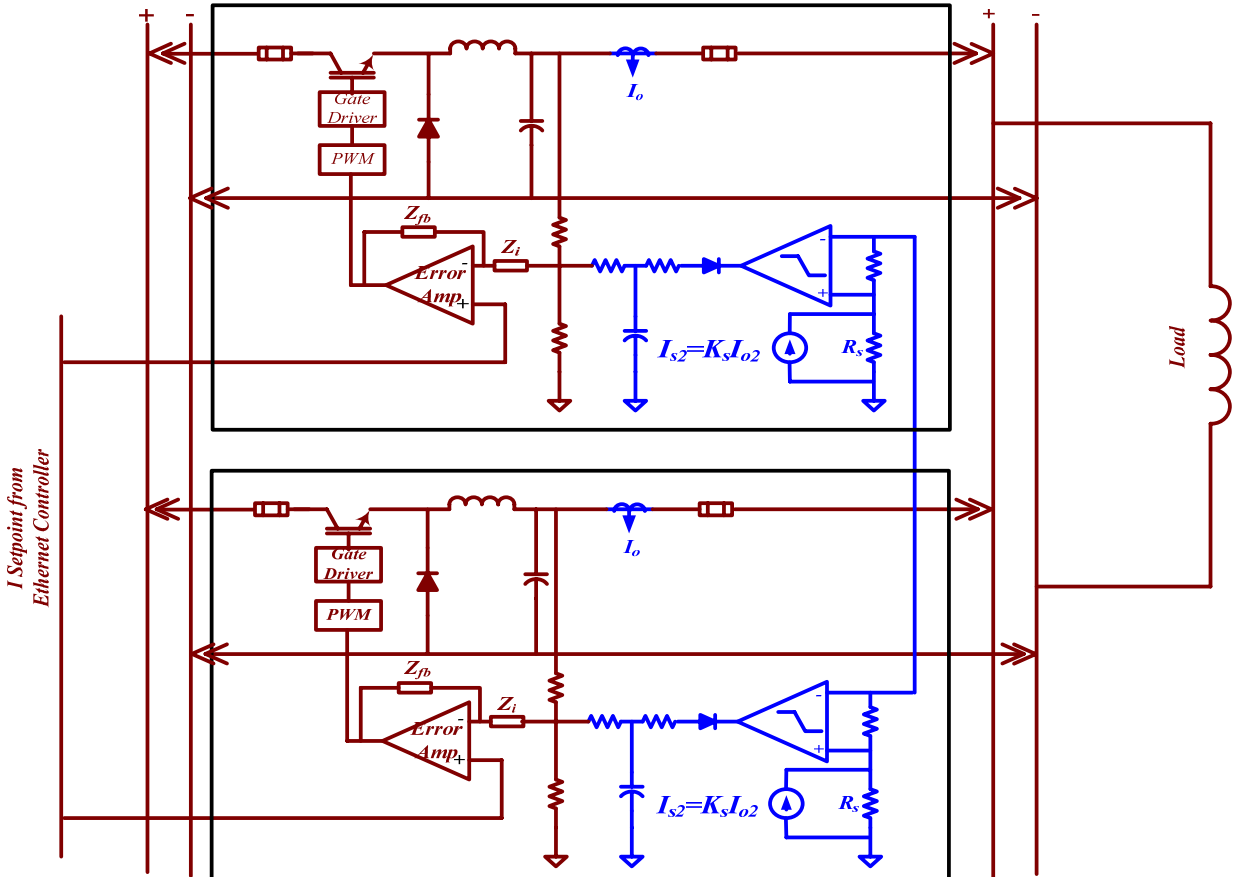
Courtesy P. Bellomo & B. Lam, SLAC

Bulk Power Supply Mfgrs

Elgar Electronics Corporation
9250 Brown Deer Road
San Diego, CA 92121
Website: www.elgar.com
IE Power
12 Falconer Drive, Unit 15
Mississauga, Ontario
Canada L5N 3L9
www.iepower.com
Lambda-EMI
Aroma Square Bldg 5F
Kamata, Ohta - Ku
Tokyo 144-8721 Japan
www.densei-lambda.com
***Matsusada** - Shiga Headquarters*
745 Aoji-Cho,
Kusatsu -City, Shiga, 525-0041
Japan
www.matsusada.com

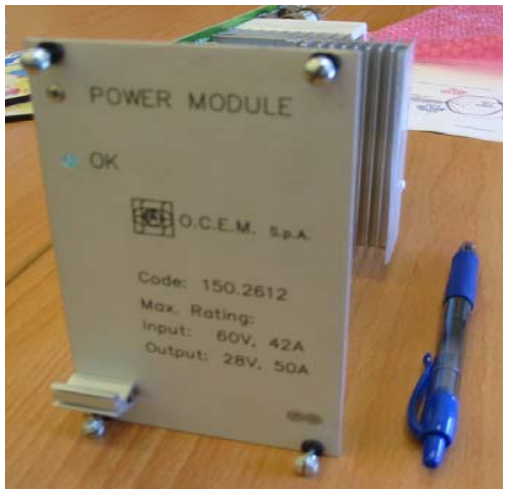
Courtesy P. Bellomo & B. Lam, SLAC

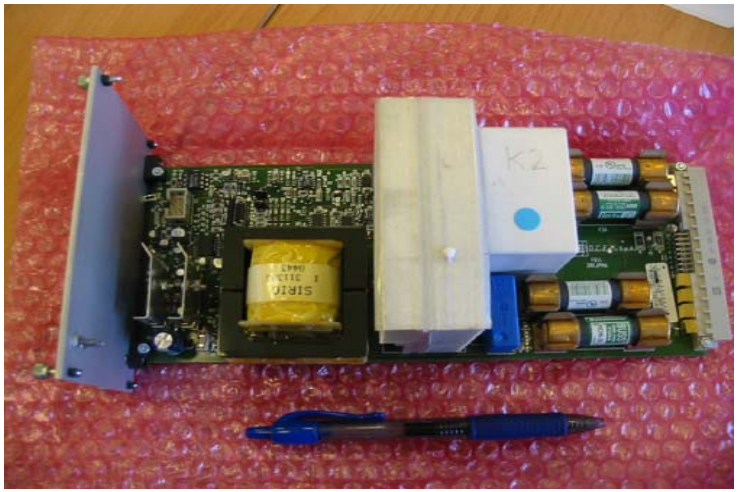
Democratic Current Share Circuitry



Courtesy P. Bellomo & B. Lam, SLAC

Commercial Power Modules





- *Purpose – current regulation of magnet current*
- *All 20V, 50A*
- *Parallel for current share and redundancy*
- *OCEM Italy IE Power Canada*

Courtesy P. Bellomo & B. Lam, SLAC

Ethernet Power Supply Controller

Note: Dual Redundant Controller with DIL features development started 2007

Purpose

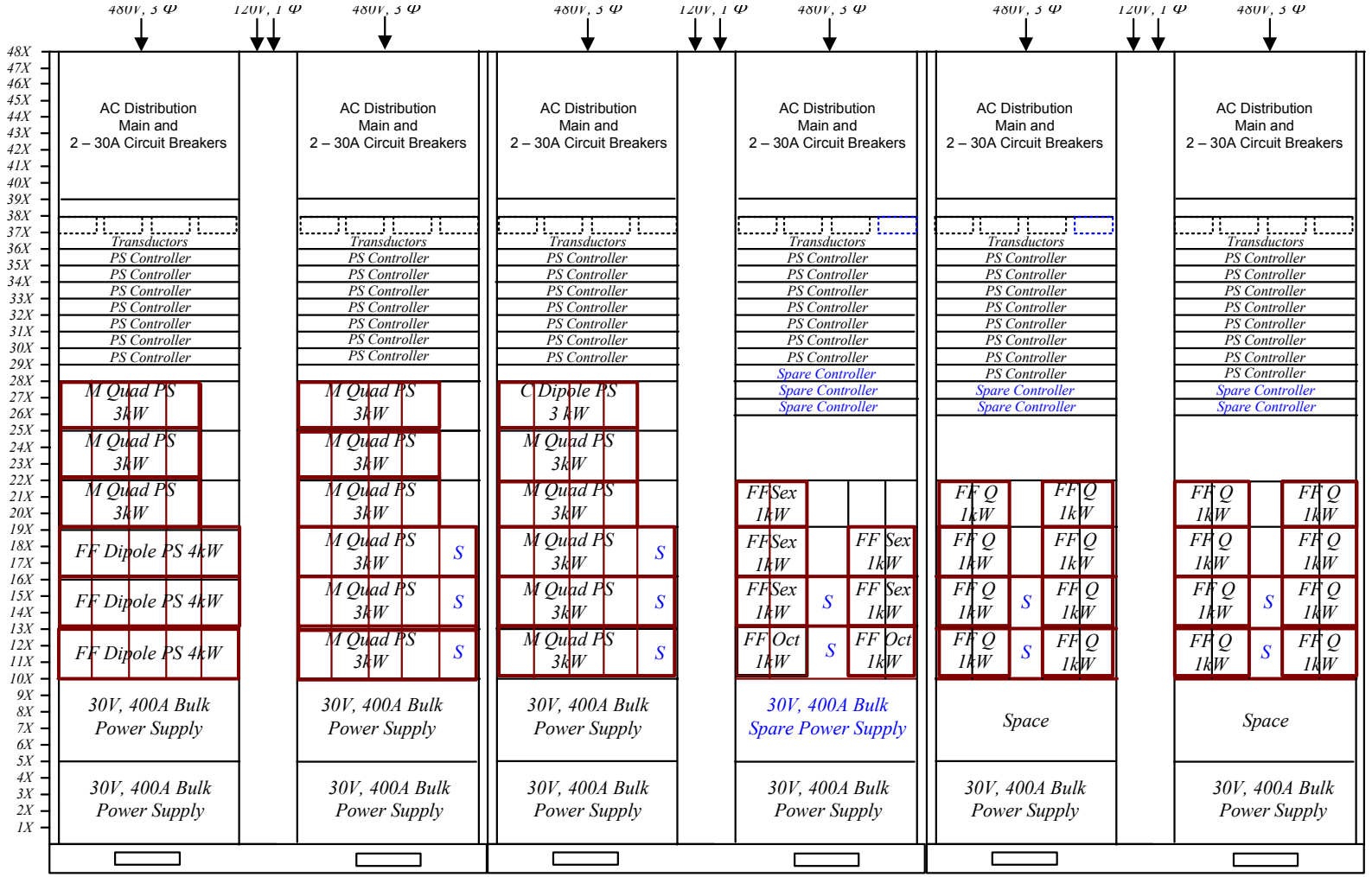
- *Interfaces remote computer to power supply*
- *Closed loop control for current setting and regulation*

Features

- *Integrated EPICS IOC*
- *100Mbps TCP/IP communications via UDP protocol*
- *SLAC-Built for PEP and SPEAR, ≥ 300,000h MTBF.*
- *Controllers slated for LCLS project use.*

Courtesy P. Bellomo & B. Lam, SLAC

Configuration of 41-Supply System



Courtesy P. Bellomo & B. Lam, SLAC

IV. Ongoing HA R&D Programs

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- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer

IV-3. First Marx Assembly Underway

G. Leyh, Designer

Tested Prototype Cell

First 2 Production Cells under initial test

IGBT subassembly plugs

IV-3. 8-Cell Output Waveforms

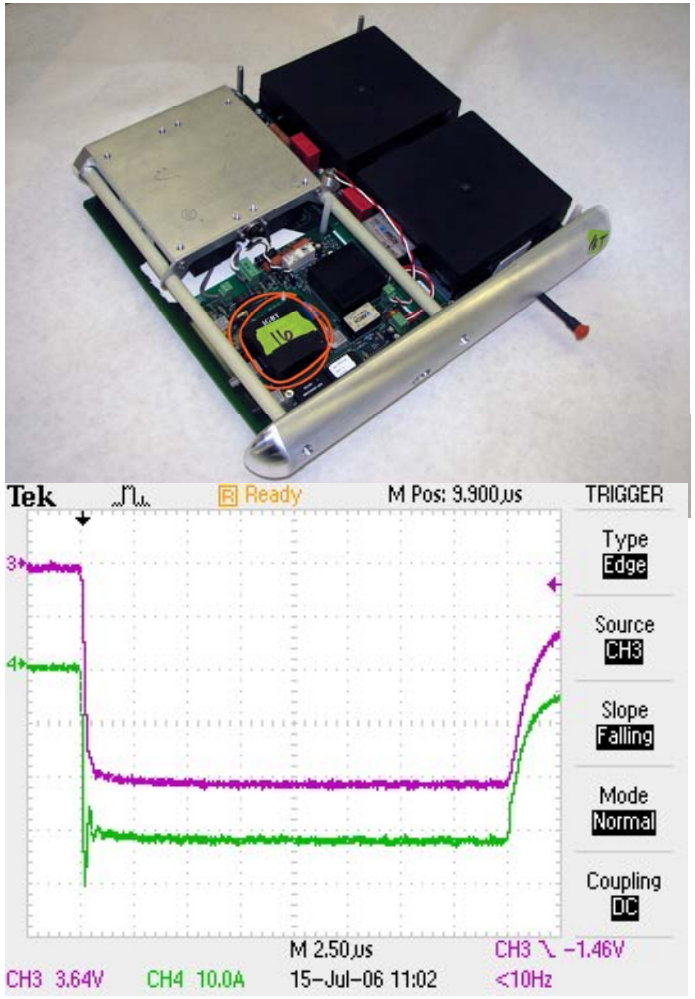
Goal: 120 kV
Reached:
80kV
1/25/07.

Courtesy G. Leyh, SLAC

Industrial Marx Efforts

- Two industrial SBIR's underway (Phase I).
- One company received contract for military agile radar application & successfully lab-tested first unit.
- Similar in power to ILC Marx, but shorter (variable width) pulse, higher (variable) trigger rate, lower voltage (90 kV max c.f. 120 kV for ILC.
  Significant demonstration of viability of Marx.

Commercial Marx Demonstration



•Output Specifications:
Resistive Load
90 kV 50A
100µsec 125 kW

•Waveforms shown:
Klystron Load
81kV ~30A
20µsec

Courtesy R. Cassel, SLAC & Stangenes Industries, Palo Alto CA.

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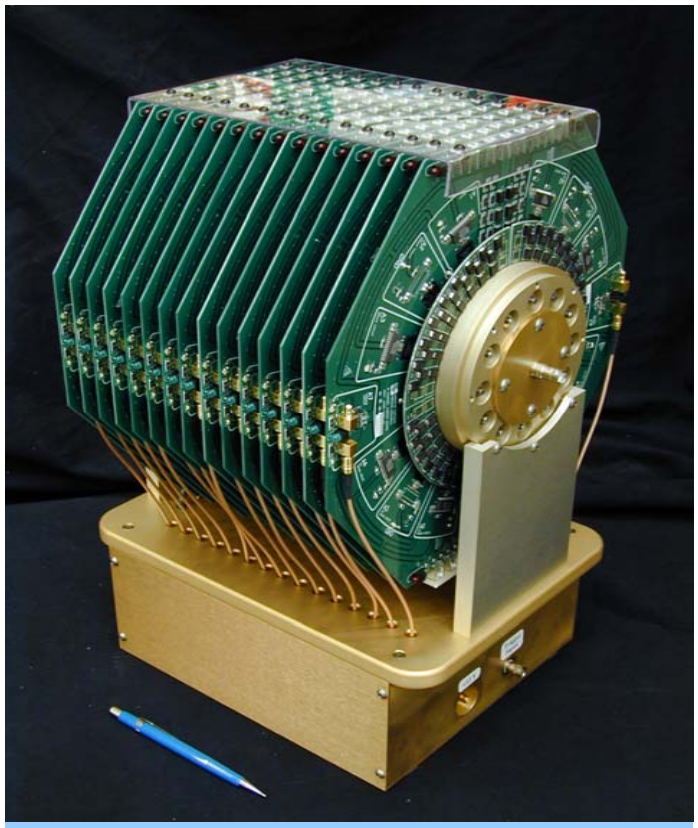
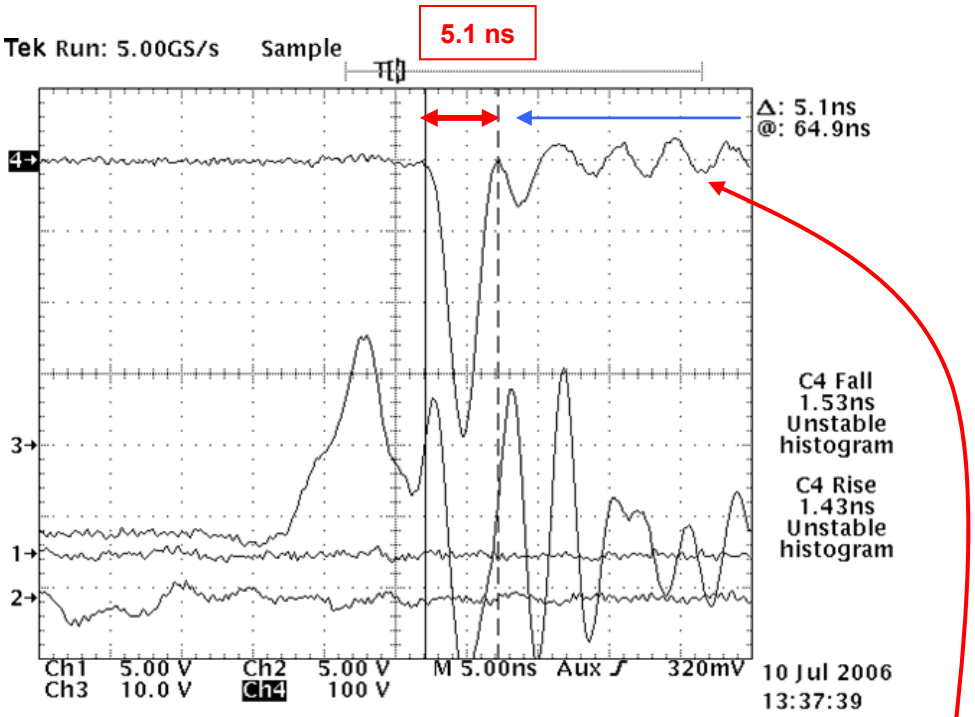
IV-4. LLNL Induction Kicker



LLNL Kicker Tested at KEK ATF



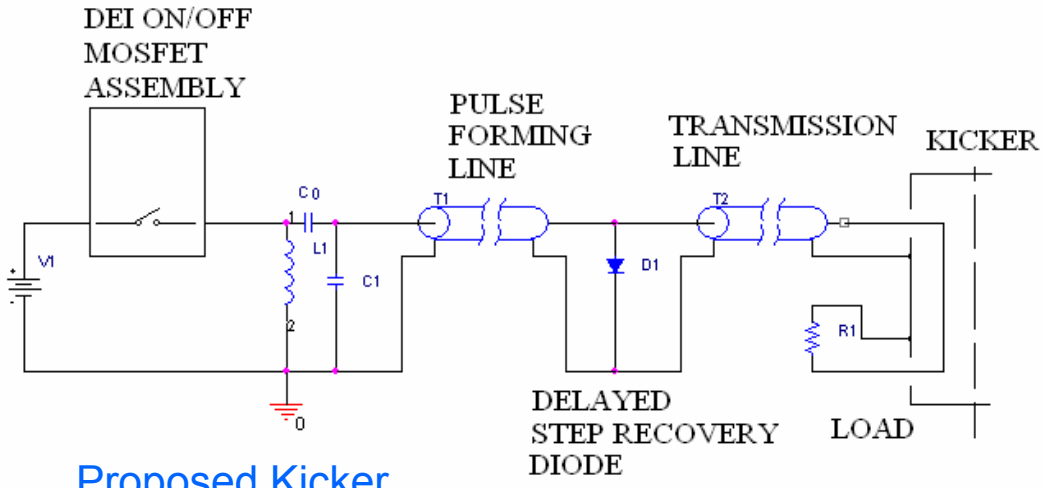
- Unit has 15 MOSFET-driven induction cells
- Type C Coax cables connected to each side produces +/-8 kV bipolar pulses
- Does not yet achieve desired Tr, Tf, clean tail

Courtesy E. Cook LLNL

IV-4. DSRD R&D

- Parallel R&D started on *Drift Step Recovery Diode (DSRD)* circuit, possibly using Induction unit as "pump."
- Tr, Tf of 1-2 nsec 5 kV into 50 Ω demonstrated on bench.
- Note- DSRD's used are samples. Commercialization is in progress.

Packaged Unit
Ioffe PTI,
St. Petersburg

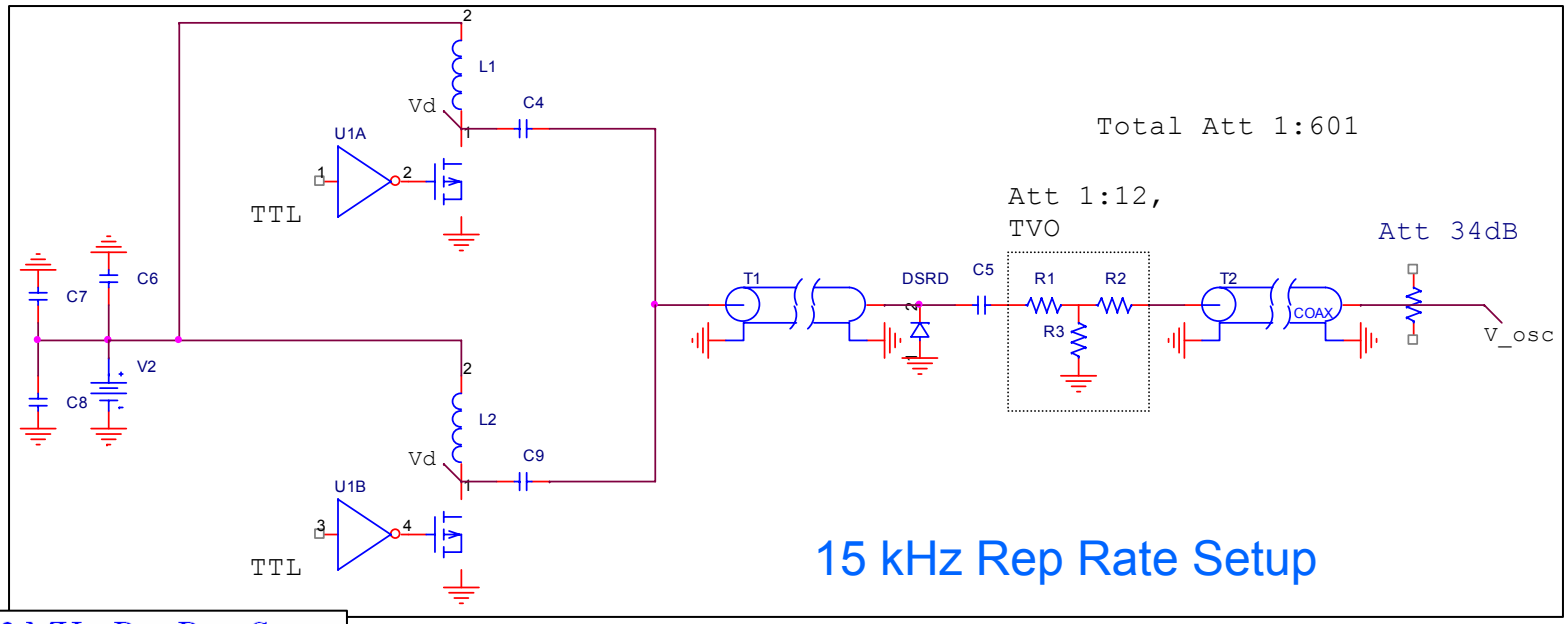


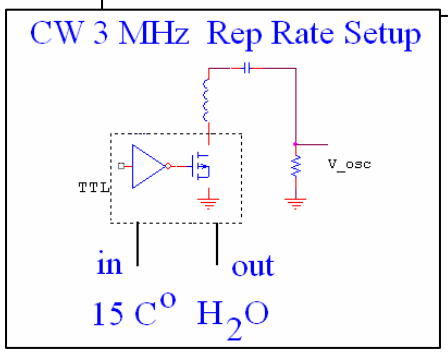
Proposed Kicker
(one side shown)

Courtesy A.Krasnykh, SLAC &

A. Kardo-Sysoev, Ioffe PTI

IV-4. DSRD Test Circuits

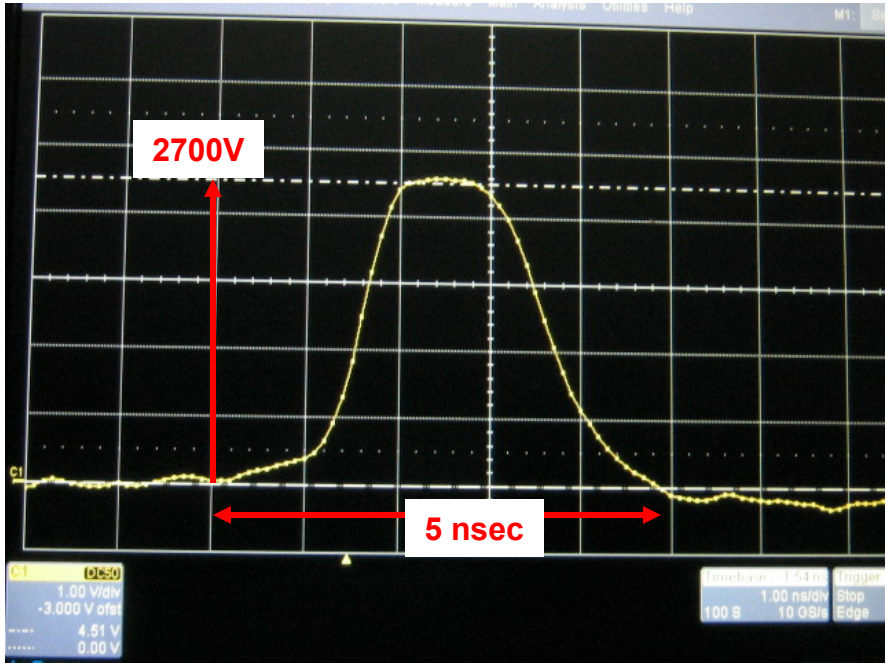


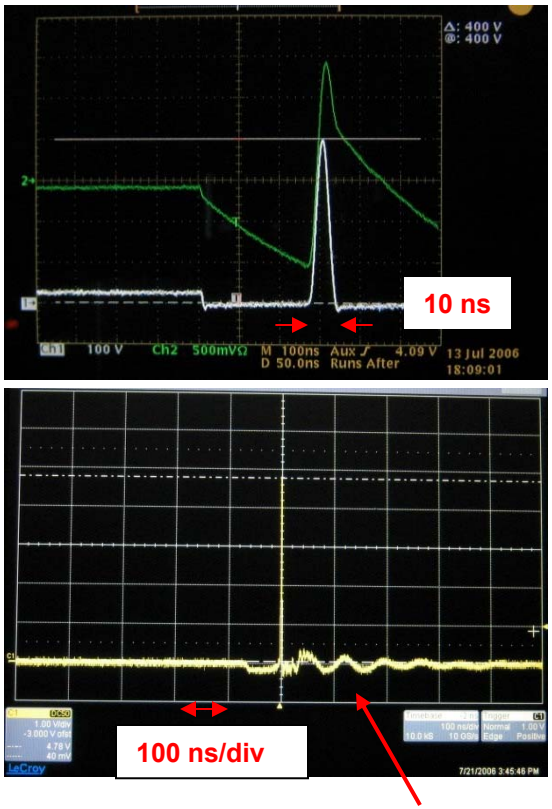


Courtesy A.Krasnykh, SLAC

A. Kardo-Sysoev, Ioffe PTI

IV-4. Test Circuit Waveforms





A_out = 4.5 x 600 = 2,700 V H=1 ns/cm

LeCroy @ 10GS/s

Tail effects need to be reduced

Courtesy A.Krasnykh, SLAC

A. Kardo-Sysoev, Ioffe PTI

IV. Ongoing HA R&D Programs

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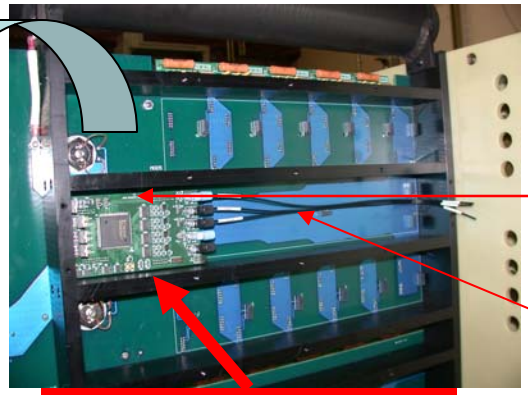
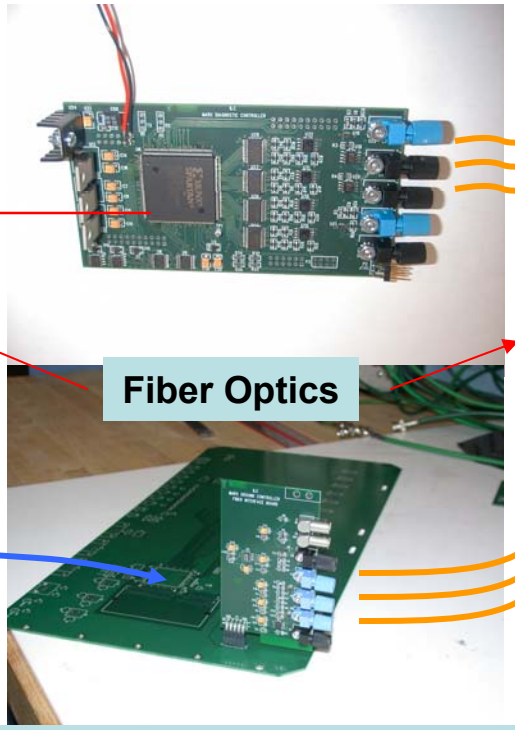
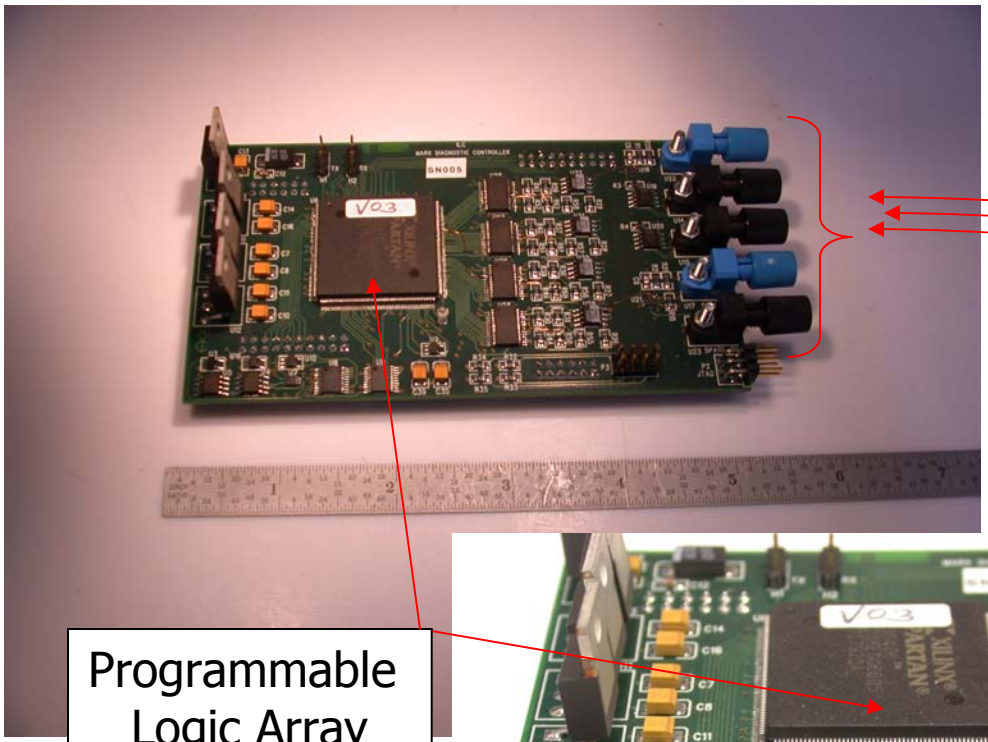
IV-5. Marx DIL Controller

- DIL had to be designed for very low power
- Operates on cell control power from charged capacitor
- Board floats up to 120 kV at output (*80 kV achieved to date*)



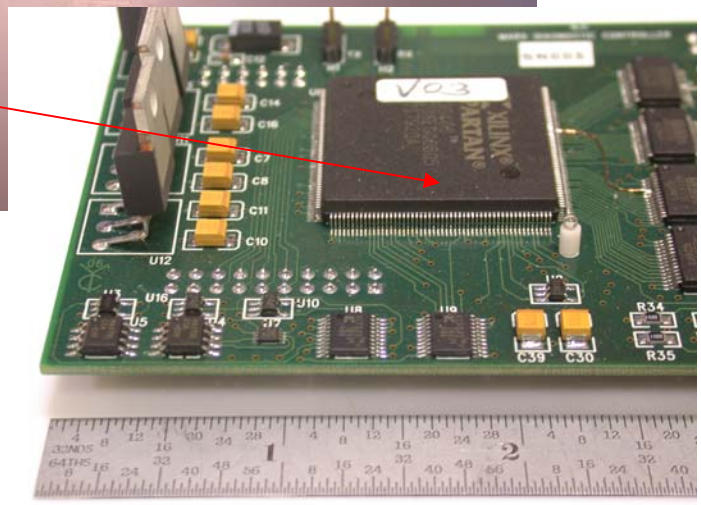


IV-5. DIL Controller Details

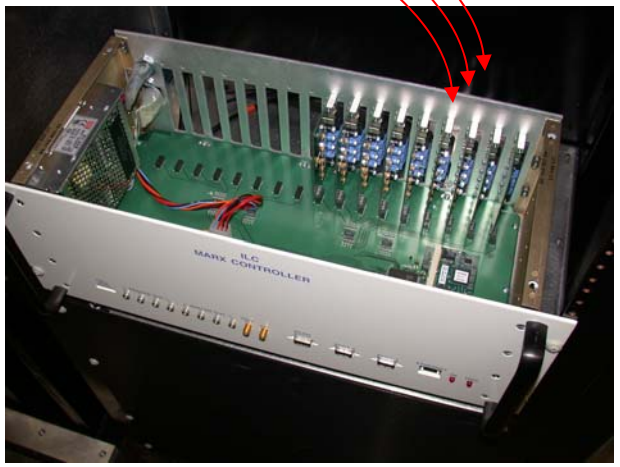


Dual Fiber Optic Timing & Data Links

Programmable Logic Array



Duplex Timing & Data Channels Each Cell (Mounted on Rear)



16 Ch Ground Station