Status of gaseous DHCAL R&D in Europe

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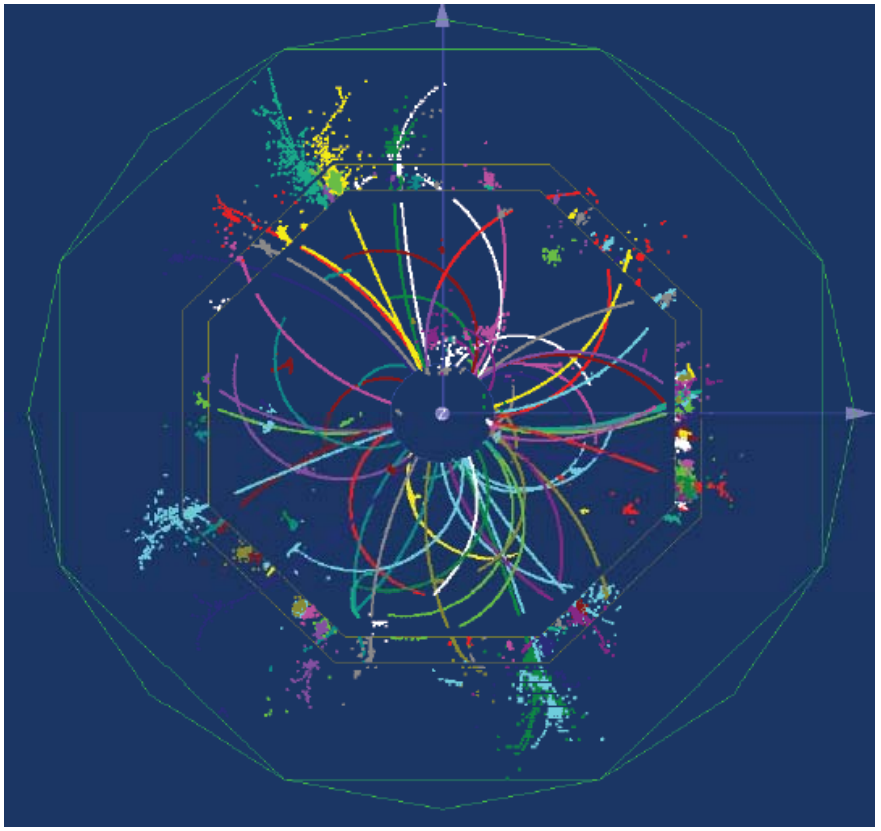
IPNL,LAL, LAPP, LLR, SACLAY
CIEMAT, DESY, IHEP, UK DAQ groups
Cooperation

Outline

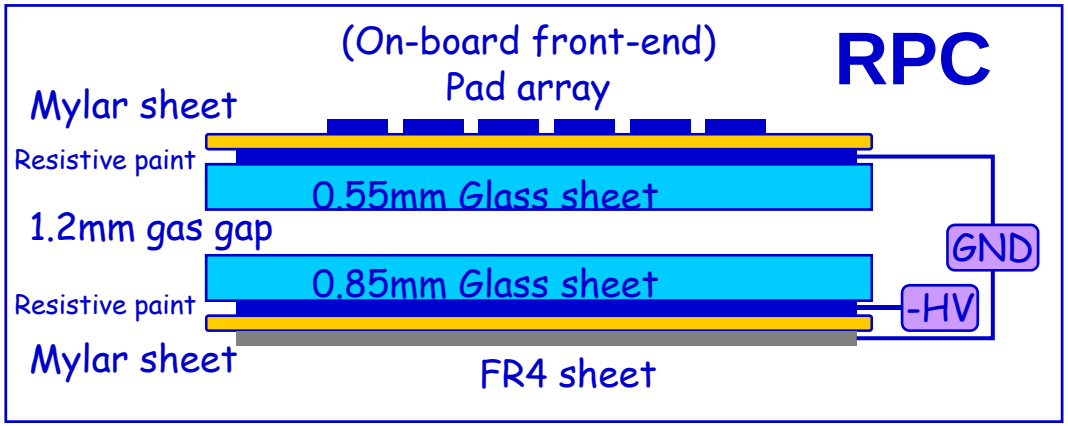
- **R&D with small gaseous prototypes**
- **Toward ILC DHCAL prototyping**

DHCAL motivation

- **Particle Flow Approach requires high longitudinal and transverse granularity in calorimetry for precise jet measurement**
- **It implies highly segmented steel sandwich hadron calorimeter (HCAL)**
- **Digital Hadron Calorimeter (DHCAL) may provide fine segmentation (~1cm^2) with simplest yes/no read out system which is enough for neutral hadron pattern recognition and muon ID**



Gaseous active medium candidates



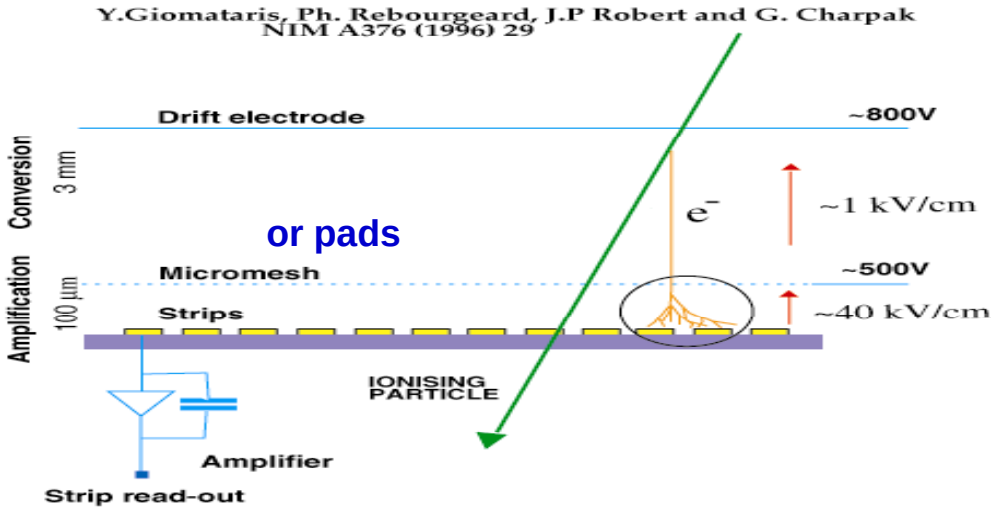
gain ~10^8, low rate

IHEP (Protvino) + collaborators

R&D is advanced

MicroMegas

gain ~10^5, high rate



LAPP (Annecy) + collaborators

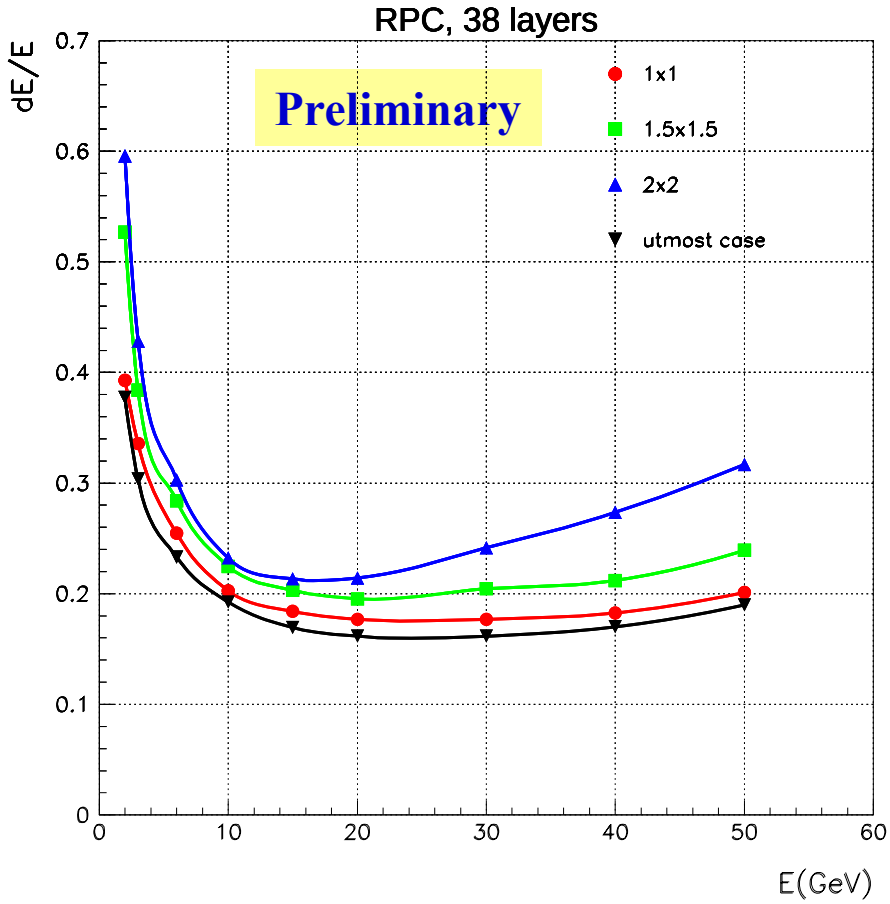
R&D is started

DHCAL RPC performance

RPC pad size

GEANT 3.2 simulation
of DHCAL response for pions

- 38 layers – 2cm SS absorber,
  6.5 mm RPC
- RPC – 1.2 mm gas monogap,
  TFE gas, glass as resistive plates
- MIP/2 cut
- nonlinearity is taken into account



1x1 cm2 pads case is compatible when all hits are counted

$R_M \sim 1.65$ cm

DHCAL RPC performance

It was choosen in beam tests in IHEP with small 4x4 pads RPCs

5 GeV/c h^+ beam

RPC samples

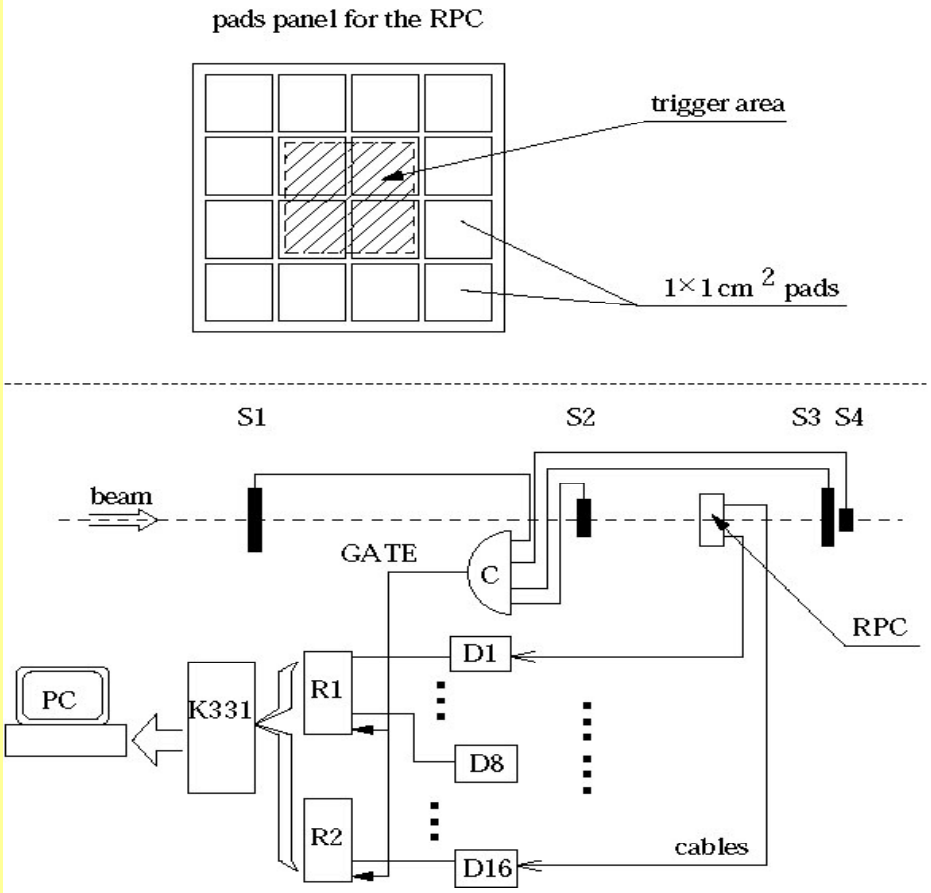
- **1.2, 1.6, 2.0 gaps**
- **10^{13} Ω·cm window glass**
- **4x4 pads of 1x1 cm^2**

In saturated avalanche and streamer modes with TFE based mixtures:
avalanche: TFE/IB/SF6=(90-93)/5/(5-3) %
streamer : TFE/IB/Ar or N2=80/10/10 %

Trigger S1·S2·S3·S4 for 2x2 cm^2 area

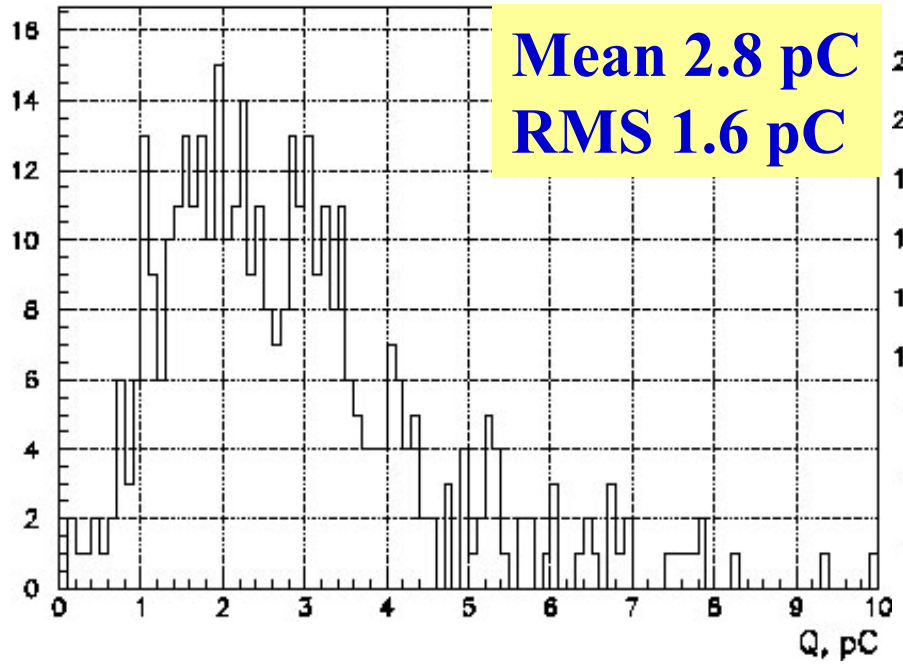
$FE(D_i)$ – 16 ch. preamp+disc based on discrete elements, on side

Avalanche mode was selected

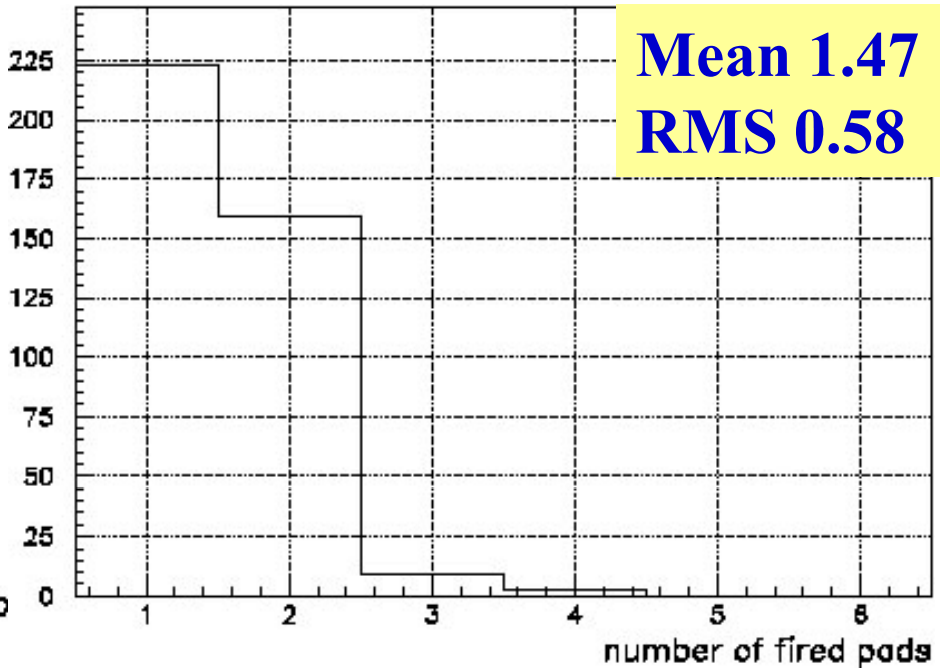


RPC in avalanche mode

Typical Q and m distributions
1.2 mm, 2% SF_6, 8.4 kV - working point, 2.2 mV thr



Mean 2.8 pC
RMS 1.6 pC



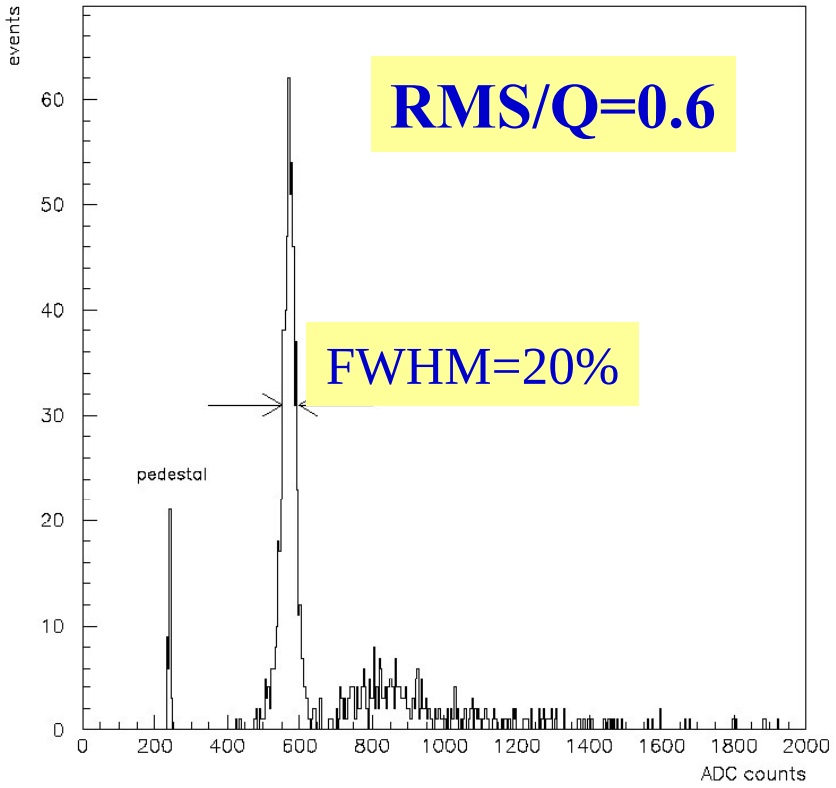
Mean 1.47
RMS 0.58

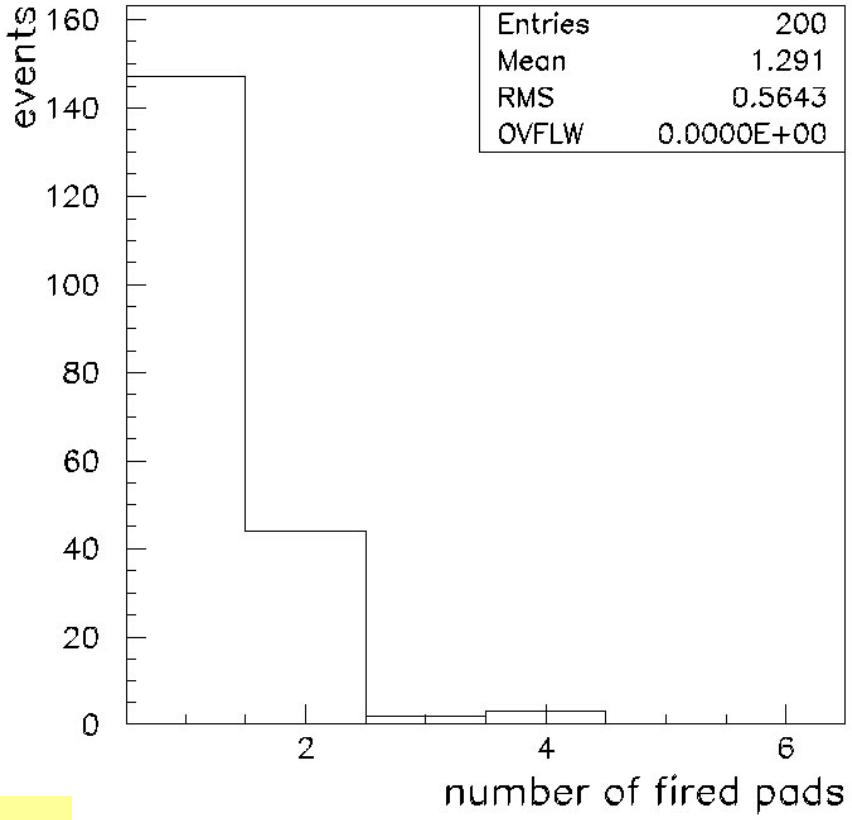
Q ~ 10^7 e

2 adj pads

RPC in streamer mode

Typical Q and M distributions, 200 V above knee
1.2 mm gap, TFE/Ar/IB=80/10/10





No ways to suppress multi streamer tail

Comparison of avalanche and streamer modes

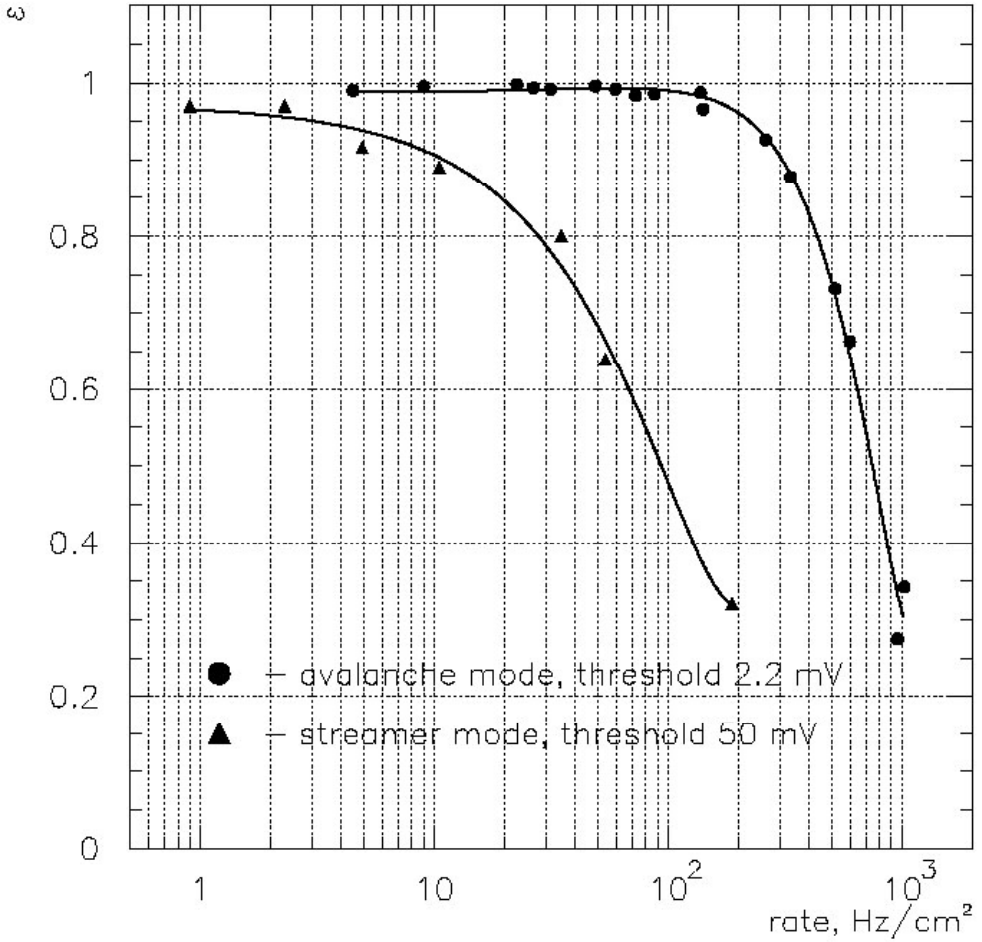
Rate capability

streamer ~2-3 Hz/cm²

avalanche ~100 Hz/cm²

It is hard to work in streamer mode even for usual beam conditions

Streamer is suitable only for very low rates like e+e⁻ ILC



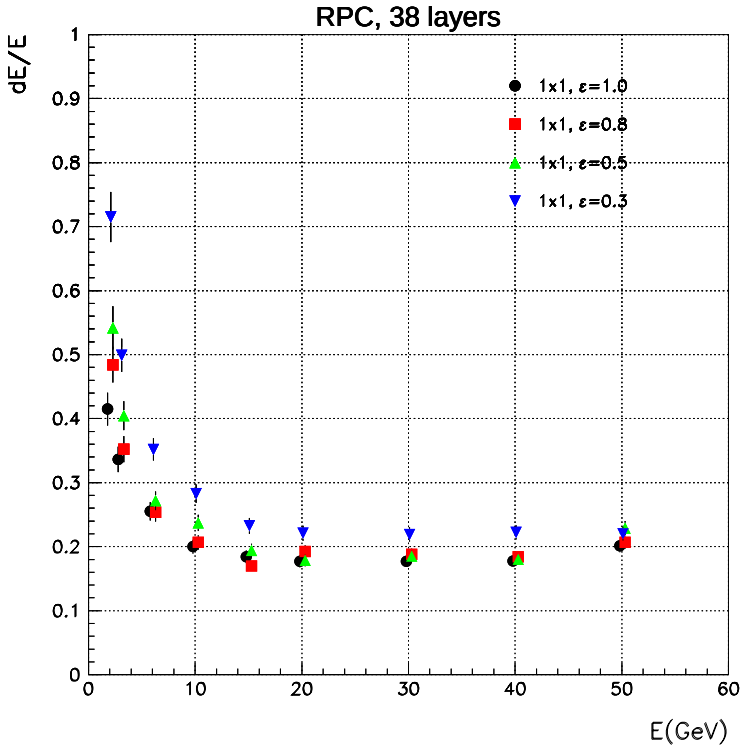
Comparison of avalanche and streamer modes

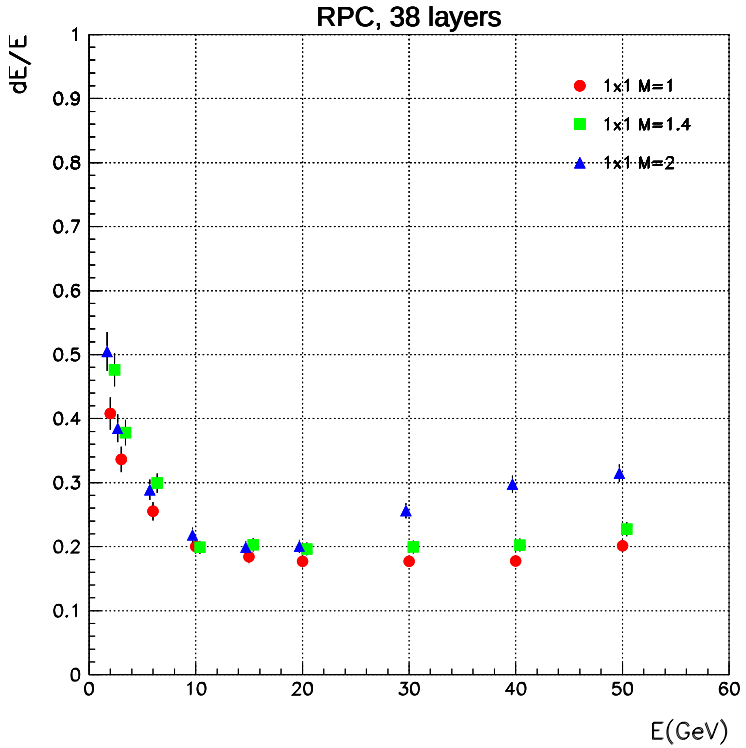
As example, for 1.2 mm gap

№	Item	avalanche	streamer
1	Working mixture	TFE/Iso/SF6=93/5/2	TFE/Iso/Ar=80/10/10
2	HV working point, kV	7.4	7.4
3	Induced charge, pC	3.4	400
4	Threshold on 50Ω, mV	1-2	300
5	Efficiency, %	~98	~95
6	σ_Q / Q	~ 0.9	~ 0.6
7	Pad multiplicity	1.4-1.5	1.2 - 1.3
8	Noise, Hz/cm^2	~ 0.7	~ 0.1
9	Rate capability, Hz/cm^2	100	2 - 3

DHCAL RPC features

Geant3 simulations





It seems eff down to 80%
does not hurt resolution much

It seems <m> up to 1.4-1.5
does not hurt resolution much

Summary of RPC features

№	Item	Value	Comments
1	Pad size	1x1 cm2	
2	Number of gaps	monogap	
3	Mode of operation	saturated avalanche	
4	Working mixture	TFE/Iso/SF6=93/5/2	
5	Gas gap	1.2 mm	1.6 mm can be
6	Resistive plates	thin glass,10^13 Ω·cm	used
7	HV working point, kV	7.4	
8	Induced charge, pC	~3	
9	Threshold on 50Ω, mV	1-2	
10	Efficiency, %	~98	
11	HV plateau	~600 V	
12	σ_Q / Q	~ 1	
13	Pad multiplicity	1.4-1.5 ?	
14	Noise, Hz/cm^2	~ 0.5	
15	Rate capability, Hz/cm^2	≤100	
16	Resistivity of HV coverage	> 10^6 Ω/ sq	
17	Control of RPC work	Q RO of cathode strips	
18	Maximal own RPC thickness	6 mm	try to keep 5 mm
	with 2 mm SS cups	10 + 0.5 mm	14 mm AHCAL

Combined RPC

Our results confirm first observation of ANL group about combined RPC – low hit multiplicity, <m> ~ 1.1 at 95% with 400 V plateau.

It seems that the combined RPC is promising option for the DHCAL. Long term stability study of combined RPC is underway.

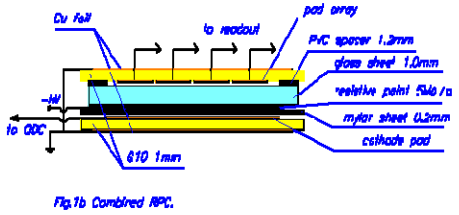


Fig.1b Combined RPC.

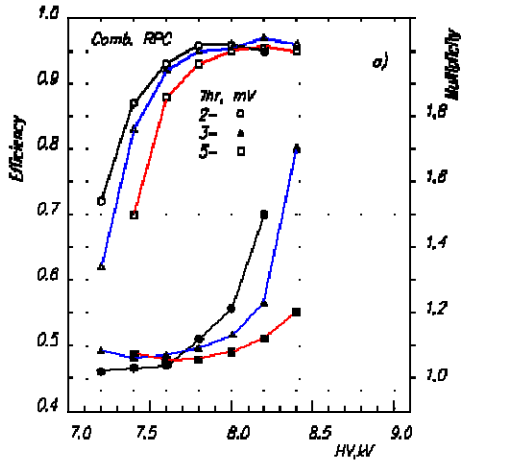


Fig. 3

RPC performance selection and design

1.2 mm monogap glass RPC, saturate avalanche mode

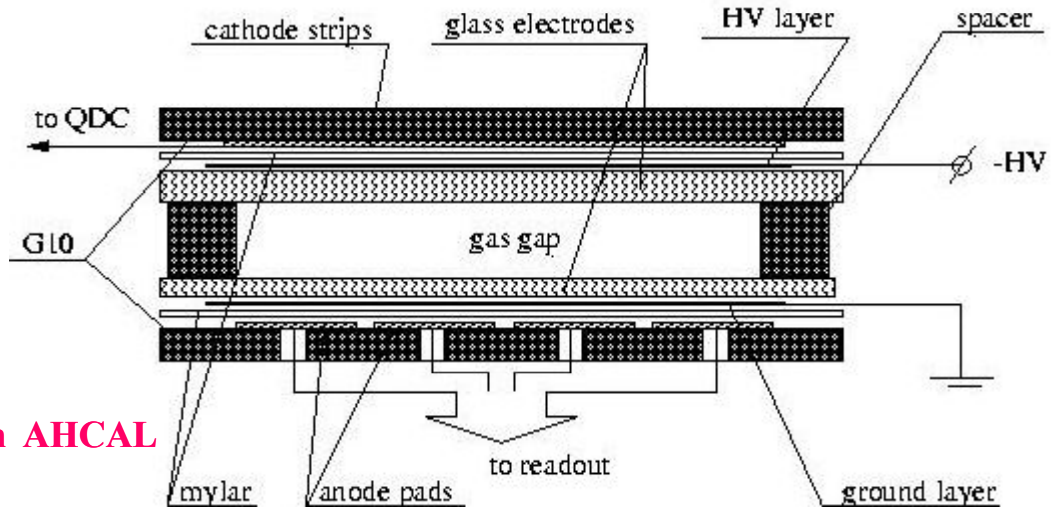
98% eff , 1 kV plateau, ~1.4 mult

Combined RPC – mult < 1.1

N	Item	Thick, mm
1	Anode printed board	1.0
2	Insulated mylar	0.05
3	Graphite coverage	0.05
4	Glass anode	0.55
5	Gas gap	1.2
6	Glass cathode	0.85
7	Graphite coverage	0.1
8	Insulated mylar	0.2
9	Cathode PB	0.5
	Thickness budget	4.5
	Max thickness	<8.0
	Room for FEE	~ 3.5

Anode PCB – internal surface for pads, external one for RO electronics

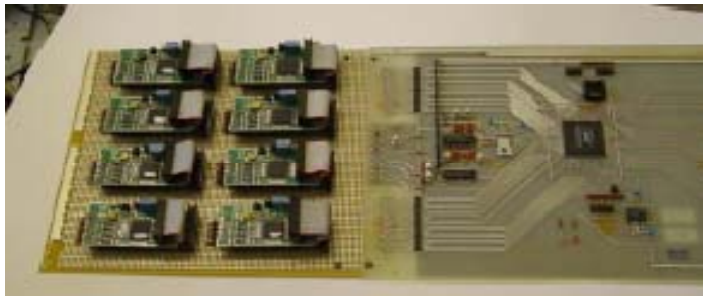
Cathode PCB – internal surface for long strips for QDC read out (control)

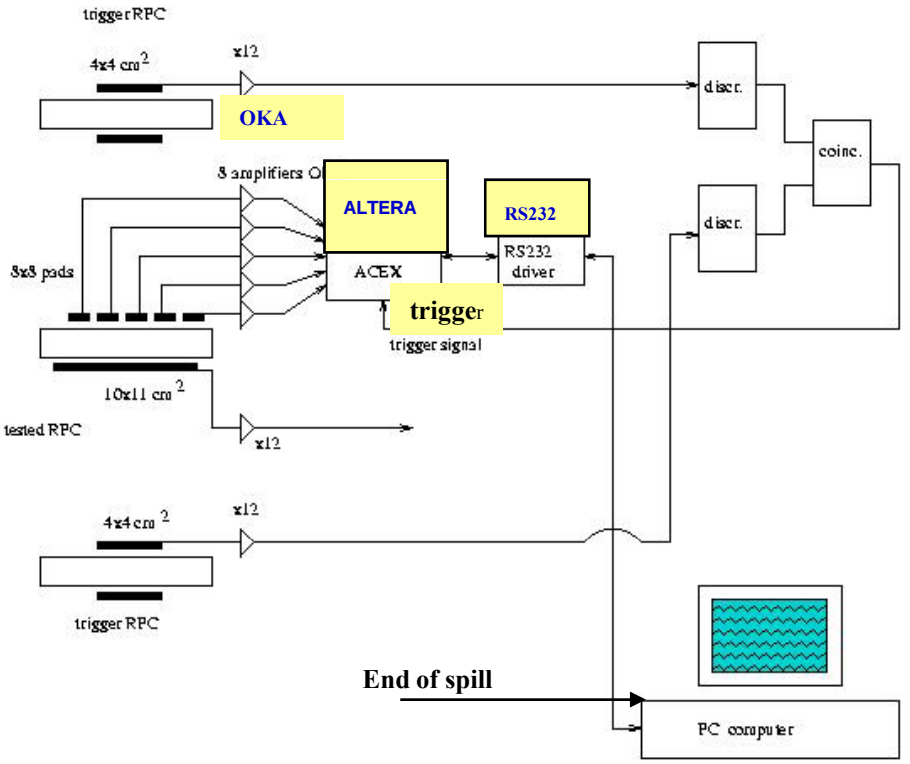


10 mm AHCAL

Tests of 64 channels RPCs in 5T mag field

RPCs with 8x8 pads of 1x1 cm2 area were tested with new specially designed 64 channel FEE





PCB is on side of RPC and

includes 8 channel MINSK chips OKA (amp.+disc.),

ALTERA EP1K50 as FPGA

and RS232 driver for sequental read out with PC

FPGA

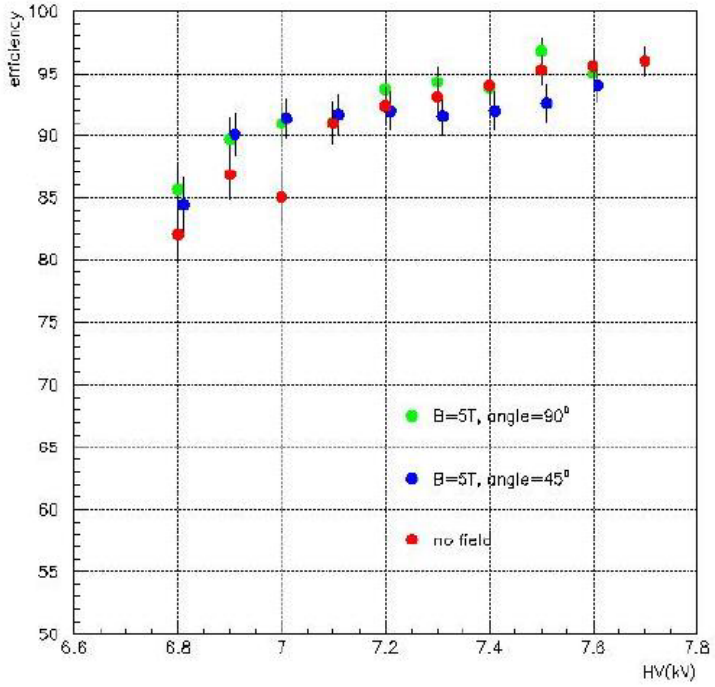
-Signals written on coincidence with trigger
64 bits for signals + 10 bits for trigger N

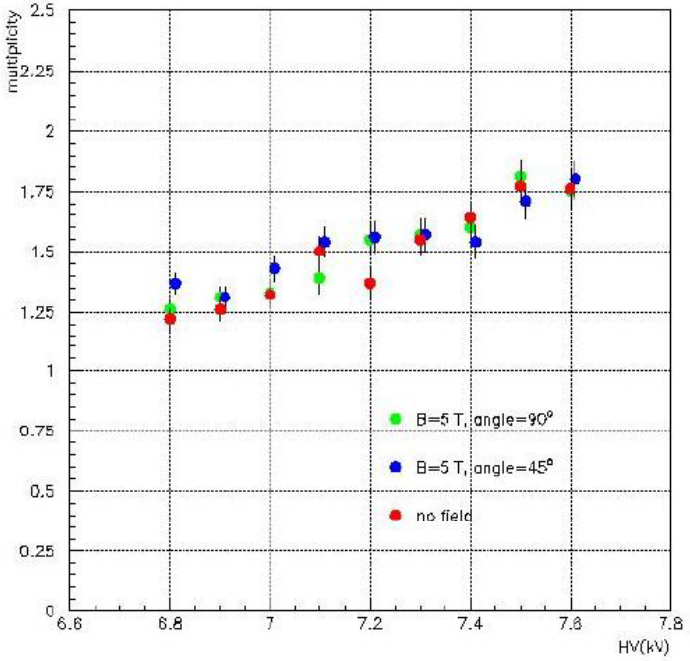
-Info is storaged in FIFO

-Read out by PC with end of spill signal

Tests of 64 channels RPCs in 5T mag field

There is no evidence of the 5Tmagnetic field influence on the RPC performance



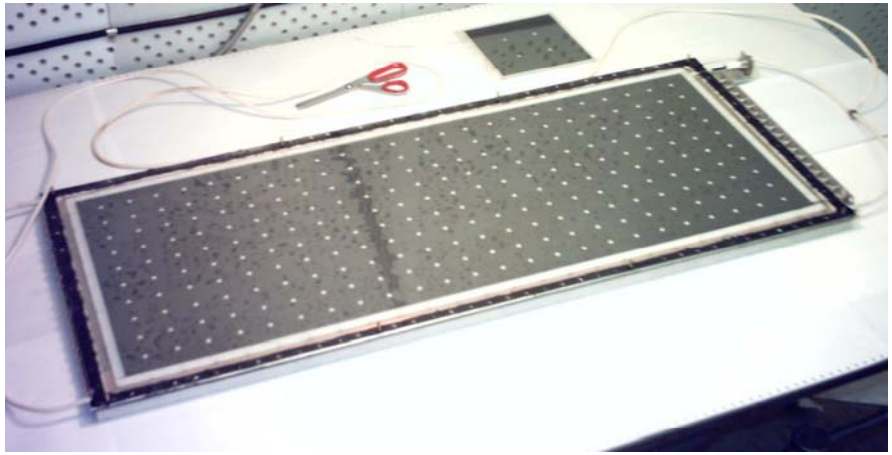


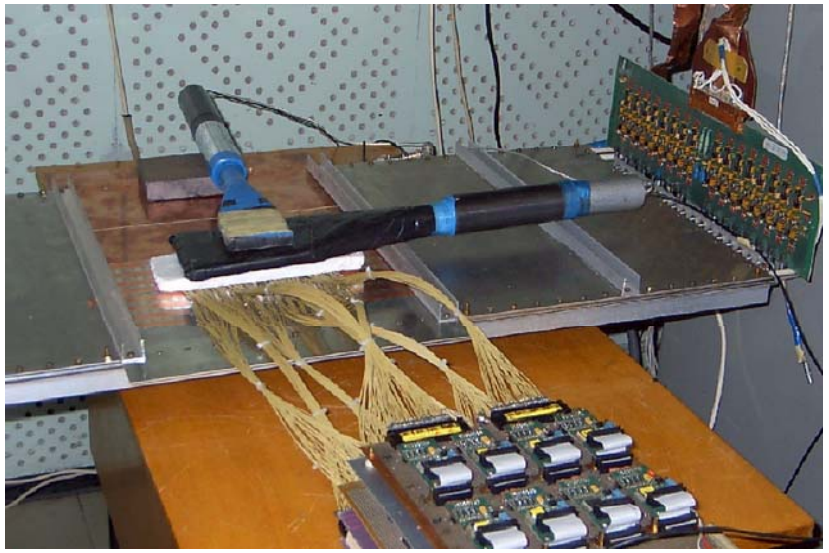
Tests of 32x32 pads RPC

RPC with sensitive area of 36x96 cm2 was produce to incorporate 32x32 =1024 pads of 1 cm2 area.

For read-out the 2 anode PBs with 16x32=512 pads were used.
Connections between pads and the 64 ch. FEE are made by microcoax 50 ohm cables.
Cosmic ray tests were done due to lack of beam time.

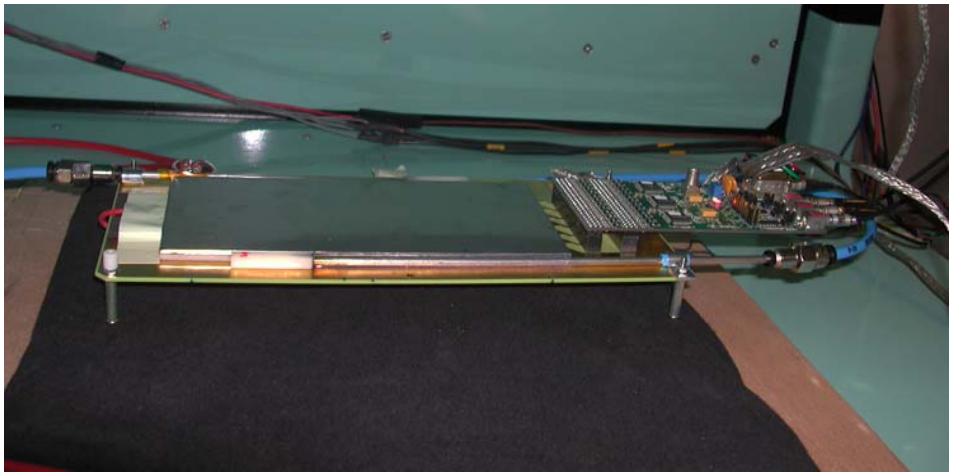
It was concluded that on side FEE is dead end for 1 m2 plane.
Special on board ASIC with serial output is needed.





DHCAL µMEGAS Study

R&D is ongoing for **µMEGAS** chambers with 8X8 pads, 6X16 pads, 50X50 pads of 1cm2 *(collaboration with Saclay)* *to select the performance for DHCAL*



6X16 pad **µMEGAS** chamber(LAPP,IPNL)

1m^3 DHCAL prototype

It is intended to construct ~1m3 DHCAL prototype with solutions near ILC detector requirements:

- **Single active layer plane (no dead zones)**
- **ASIC with power pulsing**
- **On board front end**
- **CALICE DAQ2 system**
- **Integrated gas, HV, LV systems**

Furthermore it is needed to validate gaseous approaches, to compare with MC simulations and Sc. HCAL

If 1x1 cm2 cells and 40 layers with 20 mm steel plates as absorber then ~400,000 channels are needed

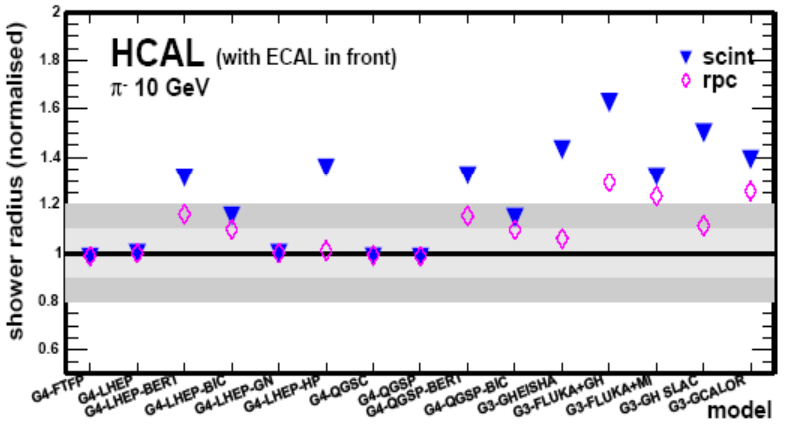
Existing mechanical structure can be used

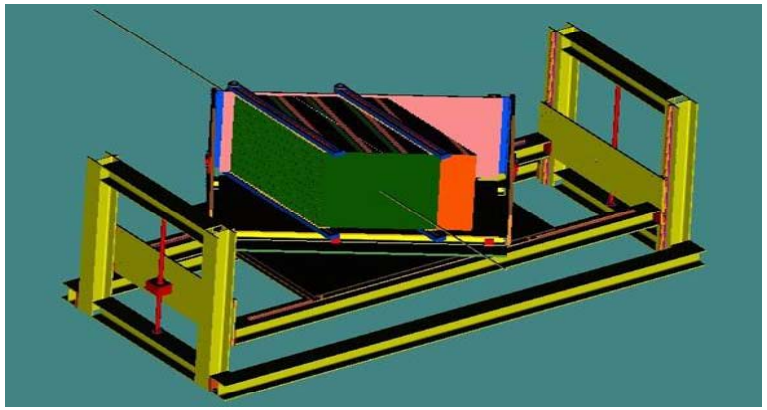
Key question is FE ASIC

Two steps in realization:

- **Slab construction and tests**
- **Full ~1m3 construction and tests**

Comparison of hadron shower simulation codes by G Mavromanolakis





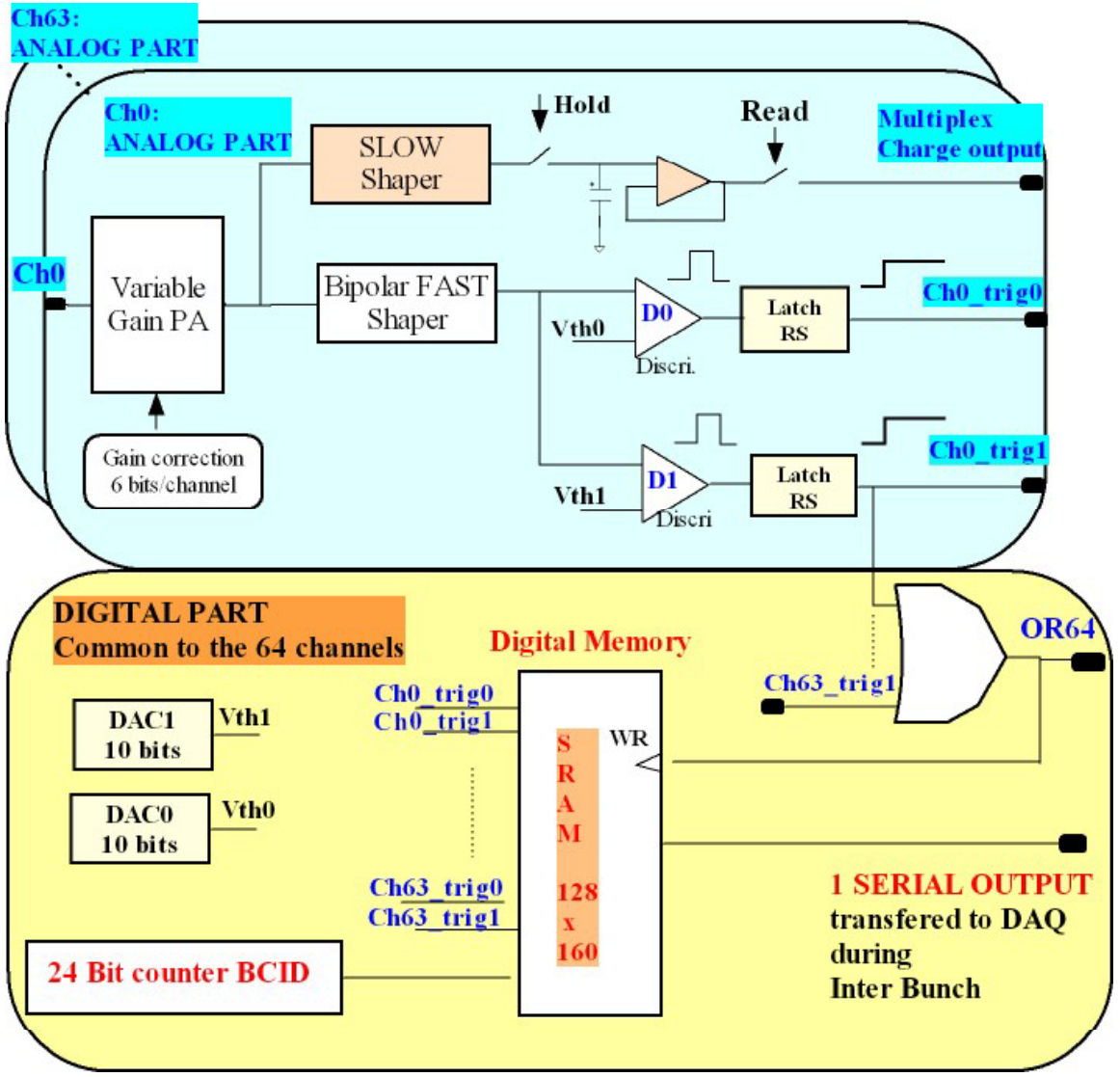
ASIC – HARDROC1

NSM

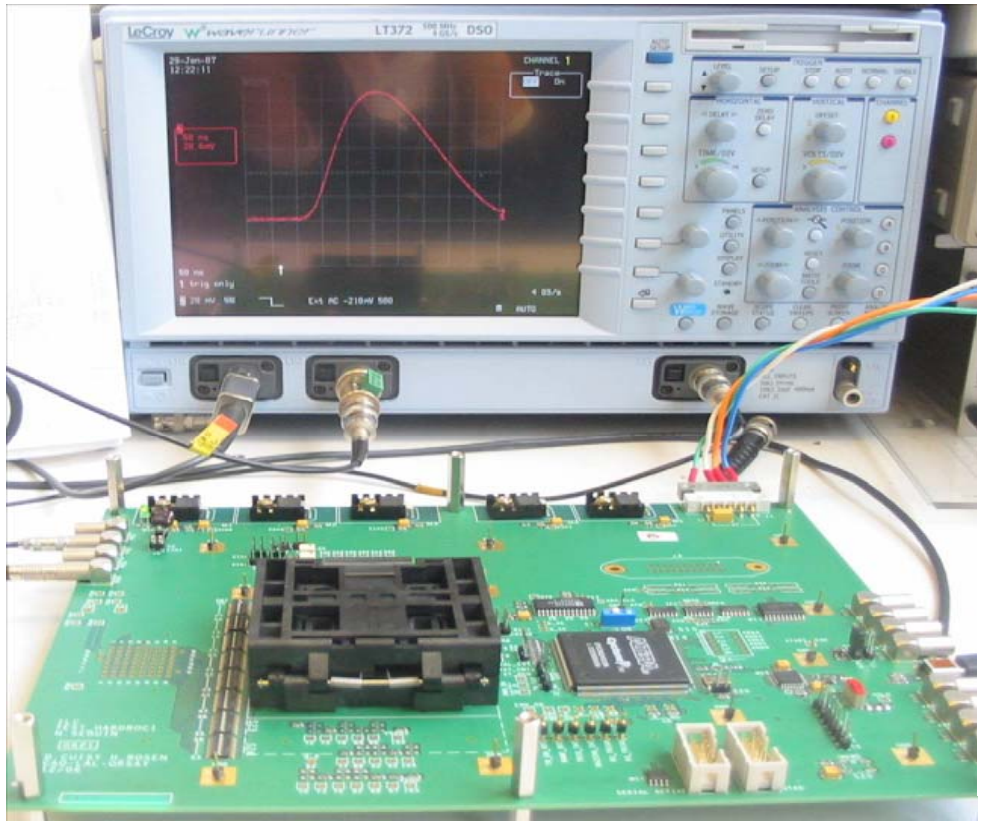
Was produced and tested successfully

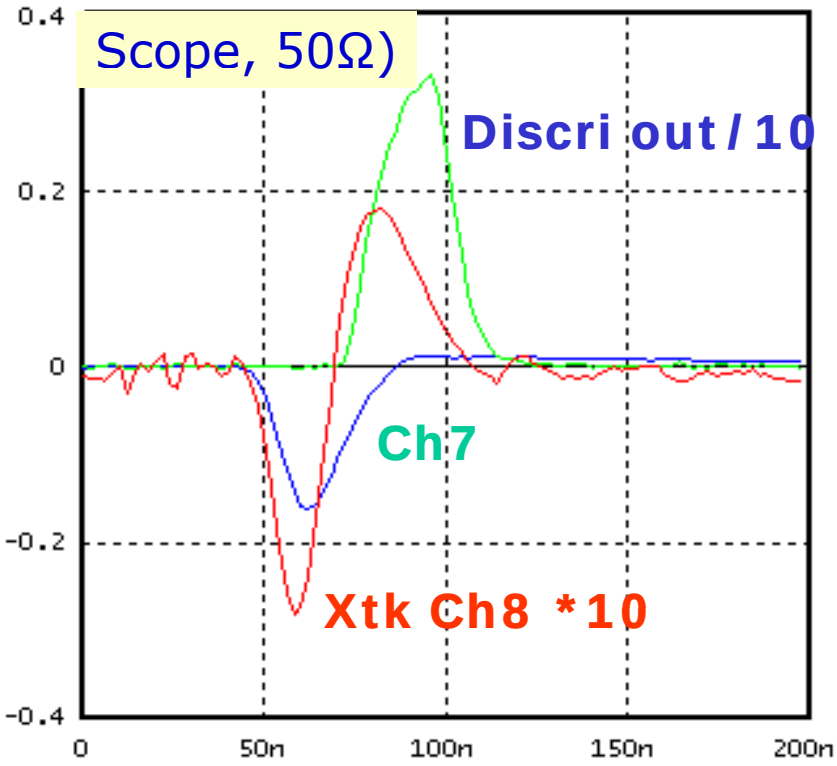
LAL, IPNL, LLR

- Full power pulsing
- Digital memory: Data saved during bunch train.
- Only one serial output
- Store all channels and BCID for every hit. Depth = 128 bits
- Data format : 128(depth)*[2bit*64ch+ 24bit(BCID)+8bit(Header)] = 20kbits
- Sequential readout @ 1 MHz



Test board with packaged HaRDROC chip

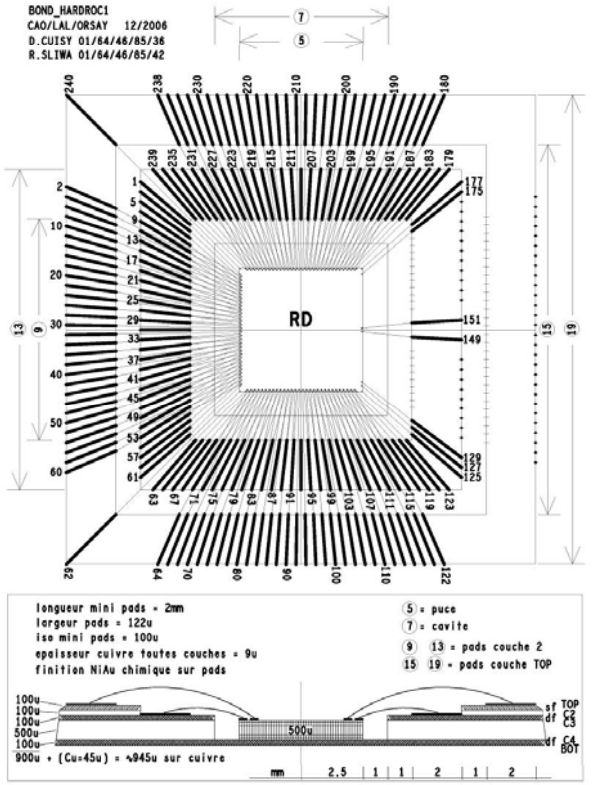




Chip performance are found as expected. Low channel-to-channel X-talk (<2%)

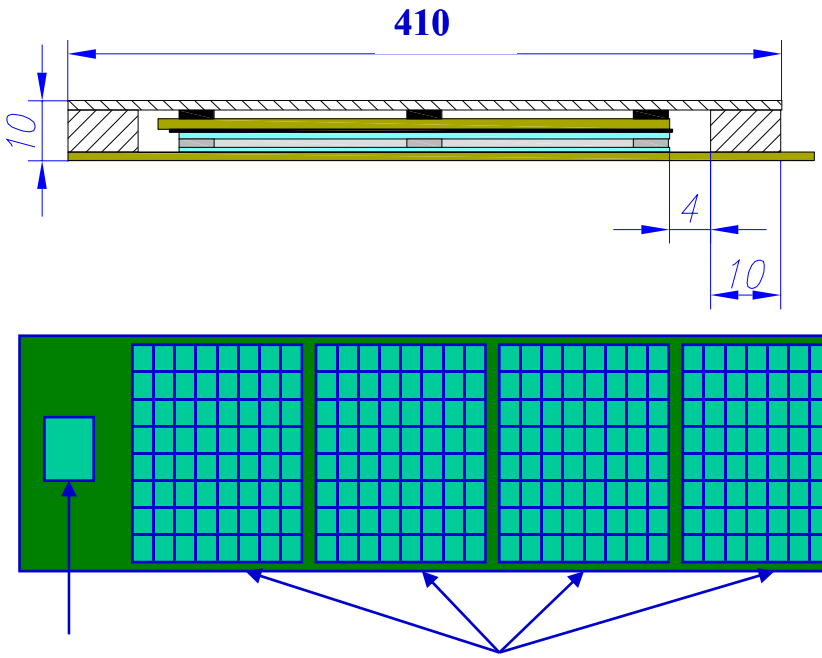
HARDROC1 PERFORMANCE SUMMARY

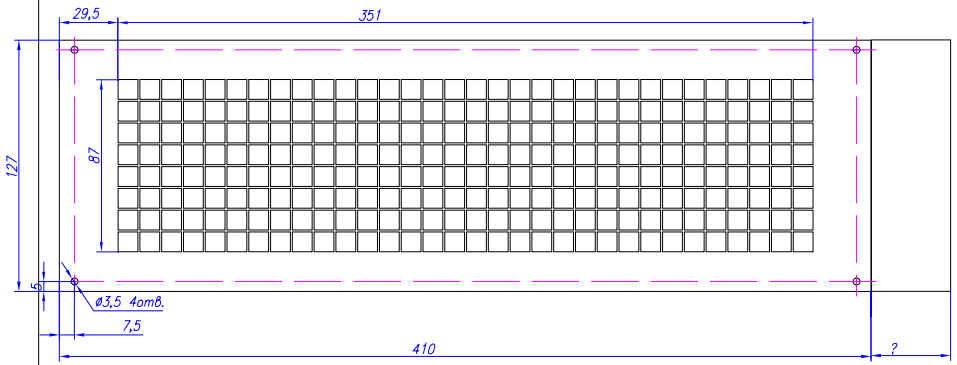
Number of inputs/outputs	**64 inputs, 1 serial output**
Input Impedance	**50-70Ω**
Gain Adjustment	**0 to 4, 6bits, accuracy 6%**
Bipolar Fast Shaper	**≈3.5 mV/fC tp=15ns**
10 bit-DAC	**2.5 mV/fC, INL=0.2%**
Trigger sensitivity	**Down to 10fC**
Slow Shaper (analog readout)	**≈50 mV/pC, 5fC to 15pC , tp= 50ns to 150ns**
Analog Xtk	**2%**
Analog Readout speed	**5 MHz**
Memory depth	**128 (20kbits)**
Digital readout speed	**5MHz or more**
Power dissipation (not pulsed)	**100 mW (64 channels)**



Slab study

8x32 pads RPC/µMEGAS





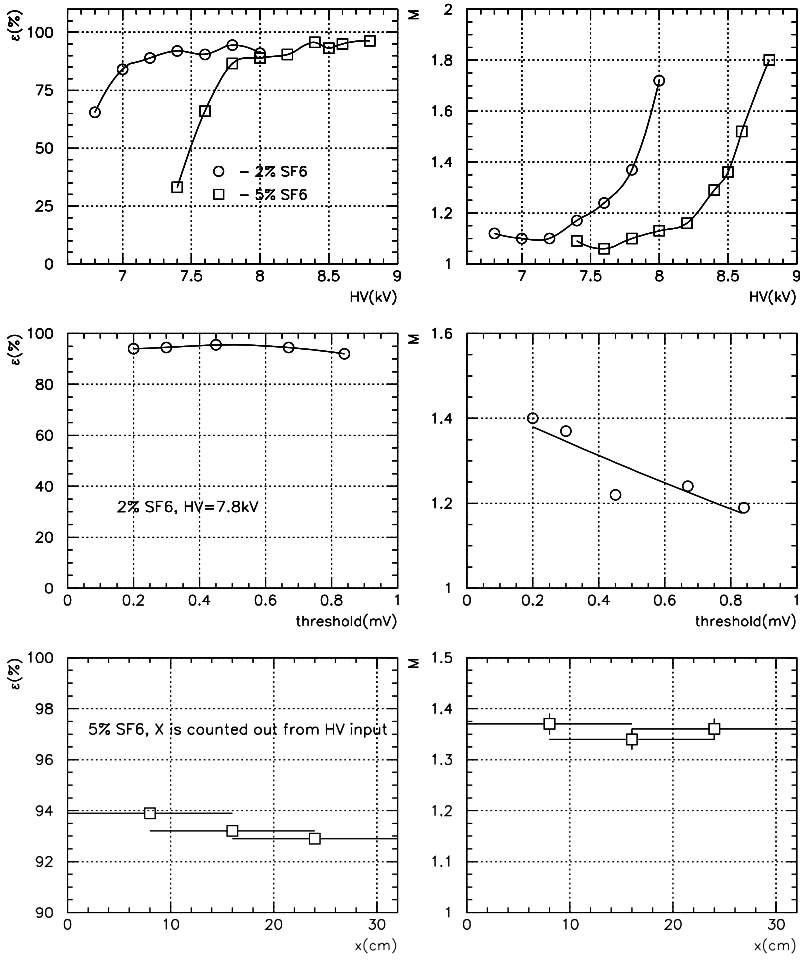
FPGA

4 areas of 64 pads of 1 sq cm : bottom layer

Hardroc external components : top layer

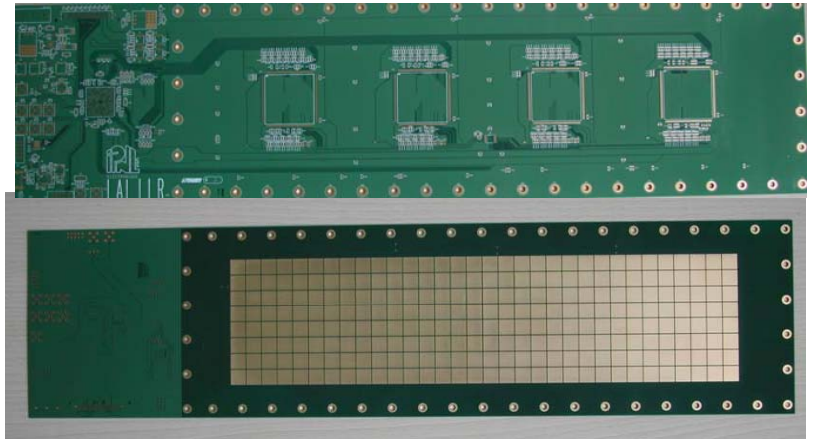
8x32 pads RPC

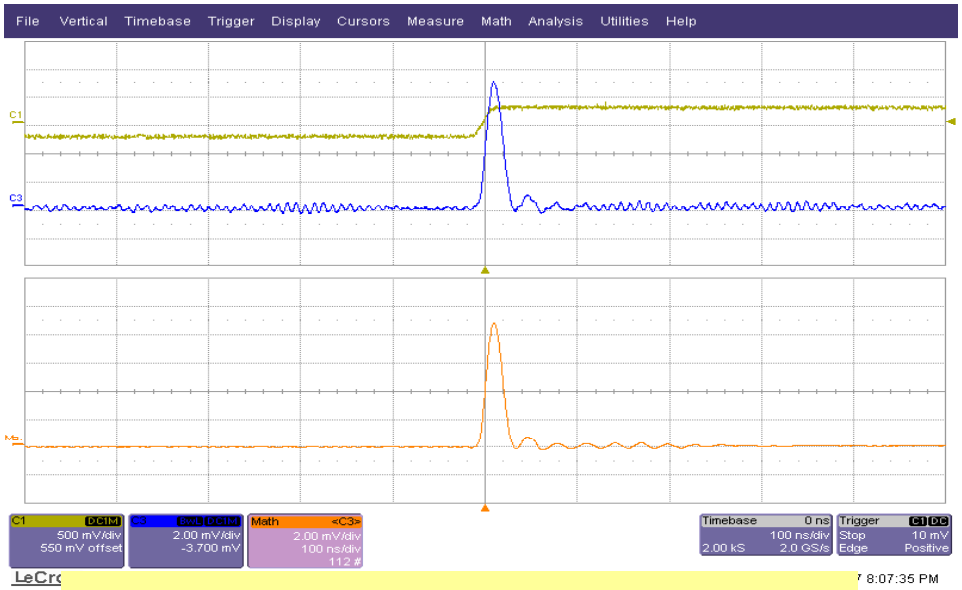
4 RPCs with 8x32 read out pads were produced. One chamber was sent to Lyon.
Chambers are waiting for anode PCBs with HADROCK chips

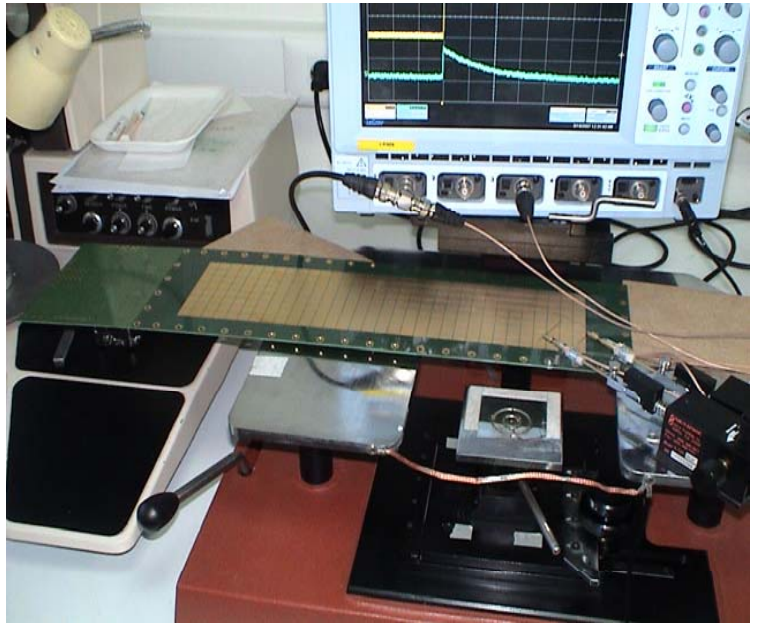


8x32 pads PCB

- 800 μ thick 8-layers PCB with blind and buried vias
- 8X32 pads, 1 cm2 surface with 500μ separation between pads
- 6 PCBs were produced

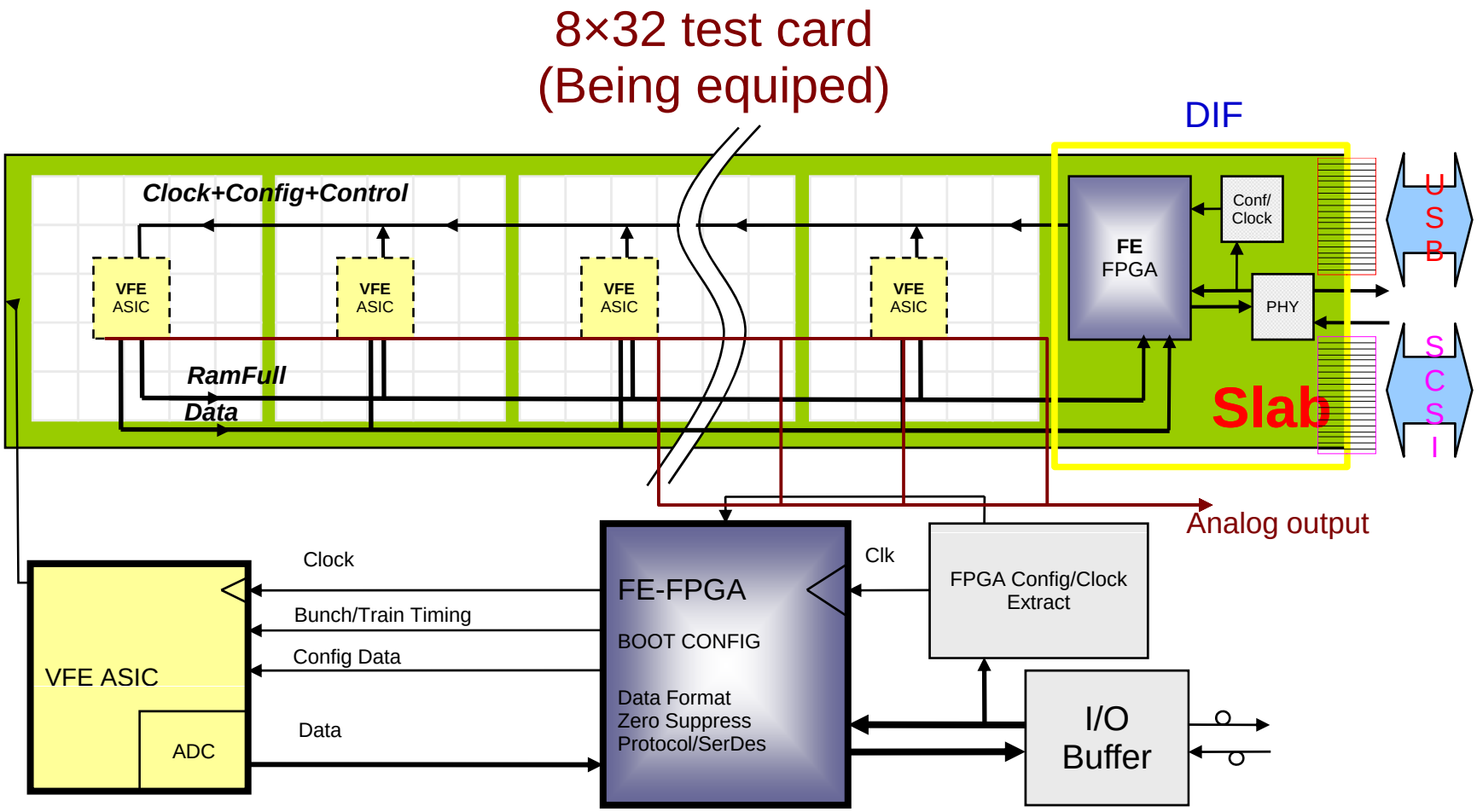






X-talk measurement (<0.3 %)

DAQ for Slab


8×32 test card
(Being equiped)
DIF
Clock+Config+Control
VFE
ASIC
VFE
ASIC
VFE
ASIC
VFE
ASIC
FE
FPGA
Conf/
Clock
PHY
USB
SCSI
RamFull
Data
Slab
Analog output
Clock
Bunch/Train Timing
Config Data
Data
VFE ASIC
ADC
FE-FPGA
BOOT CONFIG
Data Format
Zero Suppress
Protocol/SerDes
Clk
FPGA Config/Clock
Extract
I/O
Buffer

Time schedule 2007 for Slab study

- Assembly (soldering) of 3 PCBs — June 10
- Check of soldering PCBs — June 15
- Development of the DAQ — June 15
- Full assembly of one 8x32 RPC — end of June
- Tests with cosmics — July CRITICAL
- Tests in e beam at DESY — September
- Tests of µMEGAS Slab in cosmics — October
  Comparison of RPC and µMEGAS performance

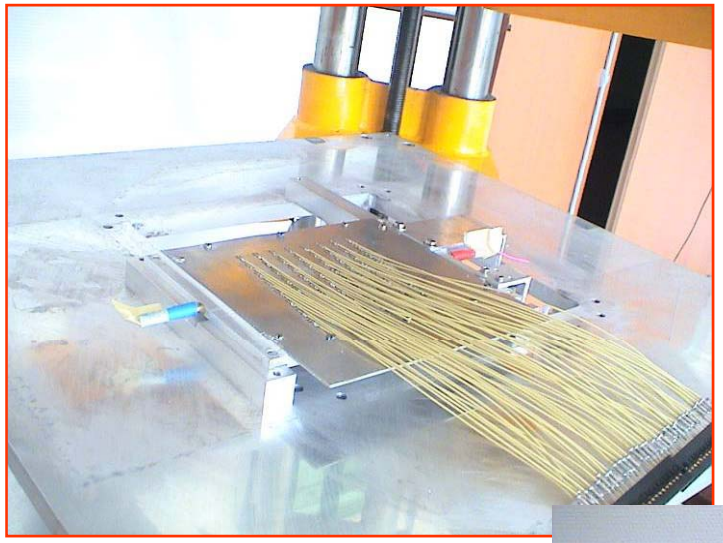
N.B : The PCB was conceived to be compatible with µMEGAS detector as well.

~1m3 DHCAL prototype

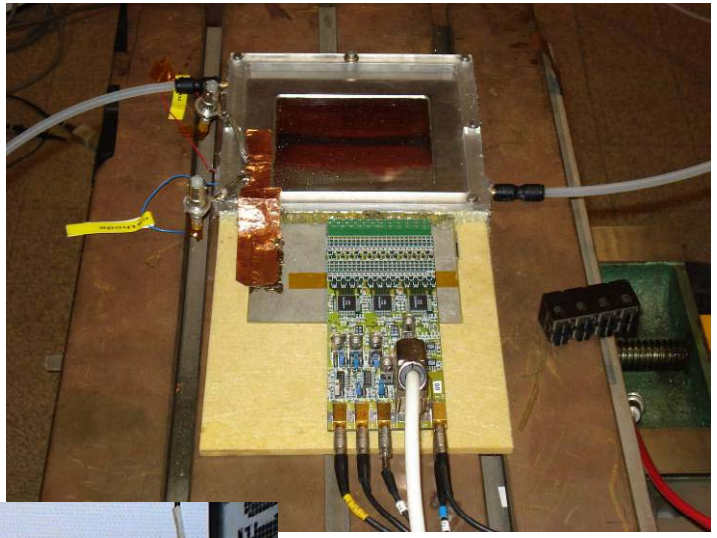
If Slab tests are OK and funding is available then roughly:

- **Construction, cosmics tests of 1st 1m2 RPC plane with strips in IHEP, sending to Lyon. The same for μMEGAS in Annecy. Dec07**
- **Construction of cosmics stand for tomography of pad 1m2 RPC planes in Lyon Dec07**
- **Comparison between RPC/μMEGAS performance in Lyon with cosmics stand to select the proper active media for the DHCAL prototype. Final Hardrock, PCB, DAQ Jan08**
- **Build elements of DHCAL prototype Dec08**
- **Assembly and beam tests of the DHCAL prototype Jun09**

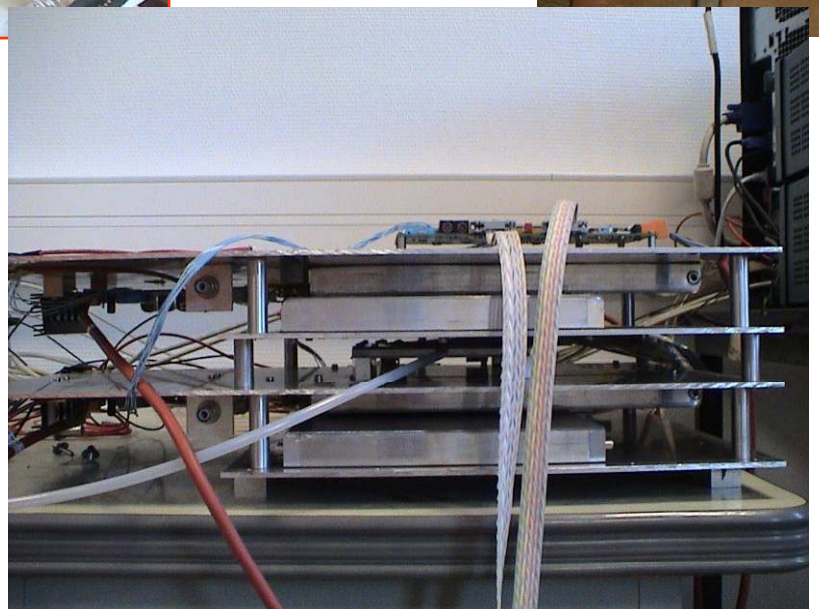
IPNL(Lyon) starts to be DHCAL center



RPC

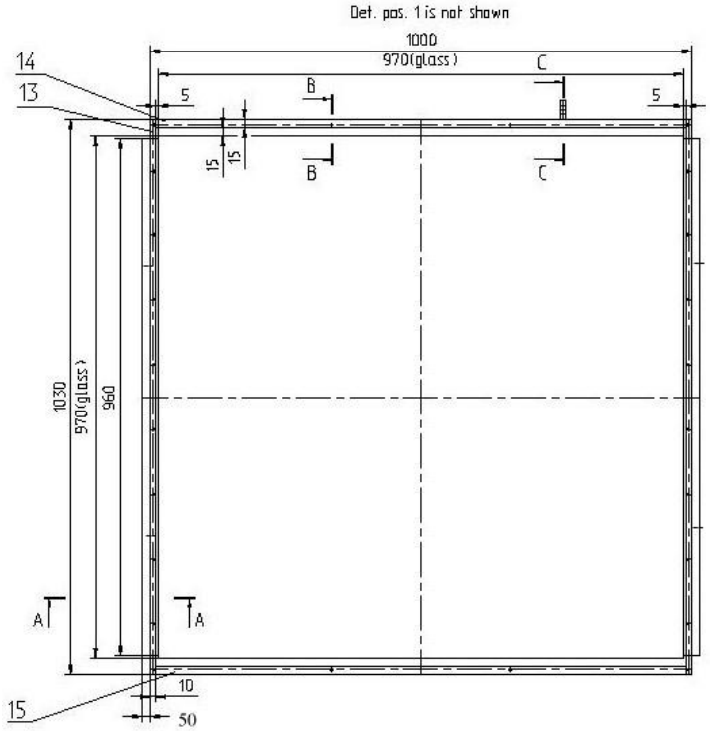


µMEGAS

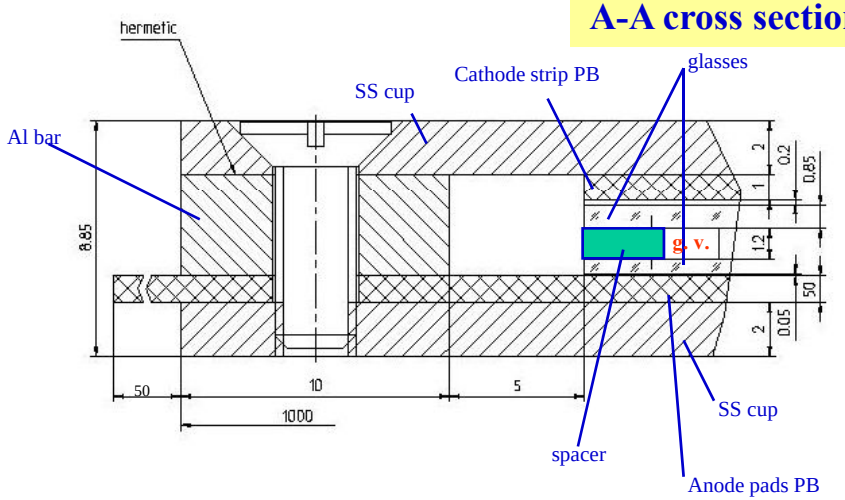


1m² RPC plane

As prototype for 1 m3 DHCAL prototype



A-A cross section



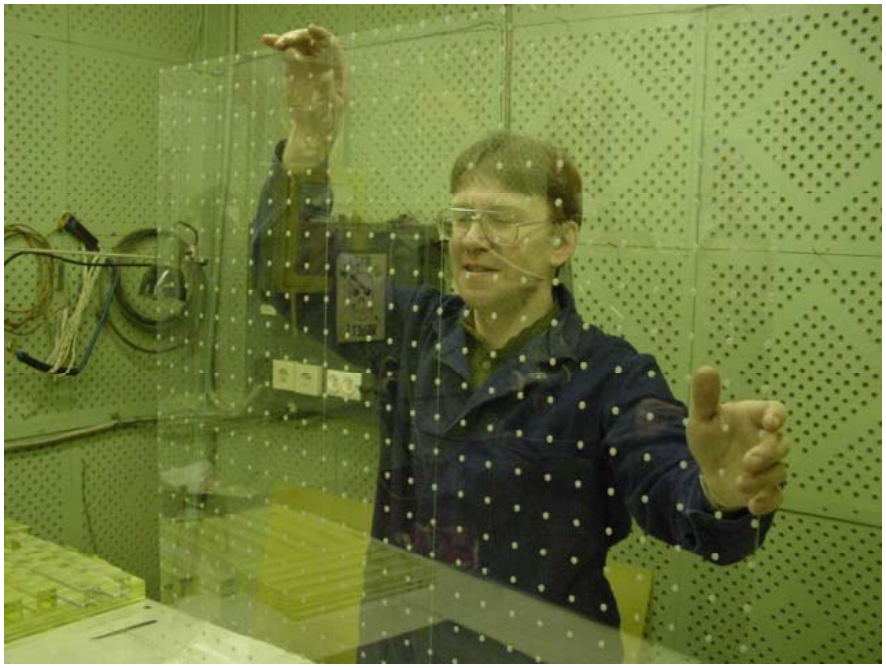
1000x1030 mm2 - lateral dimensions
970 x 970 mm2 – glass area
960 x 960 mm2 – sensitive area
Weight ~ 40 kg

96x96 = 9216 anode pads in total
24 anode PCBs of 80x530 mm2
8x48 = 384 pads on each = 6 Hardrock ASIC

SS cups and Al bar frame form hermetic box.
It prevents glass break due to gas overpressure.

1m² RPC plane with strip read out

Construction of 1 m2 RPC plane



Gas volume: anode glass – 0.5 mm thick, cathode glass – 0.8 mm thick, 1.2 mm gas gap, 6 mm dia spacers

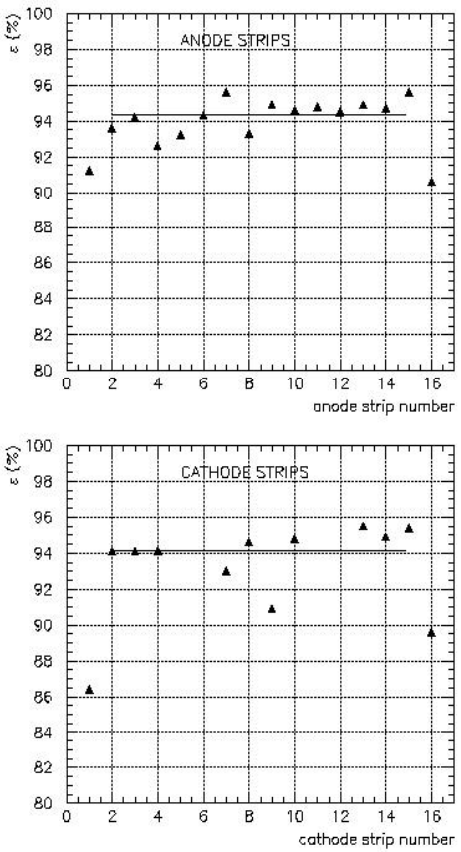
96x6 cm2 strips for read-out
16 anode (x) strips
16 cathode (y) strips

Tests of 1m^2 RPC plane with strip read-out

Detailed study of the plane was performed in cosmic rays.

In general :

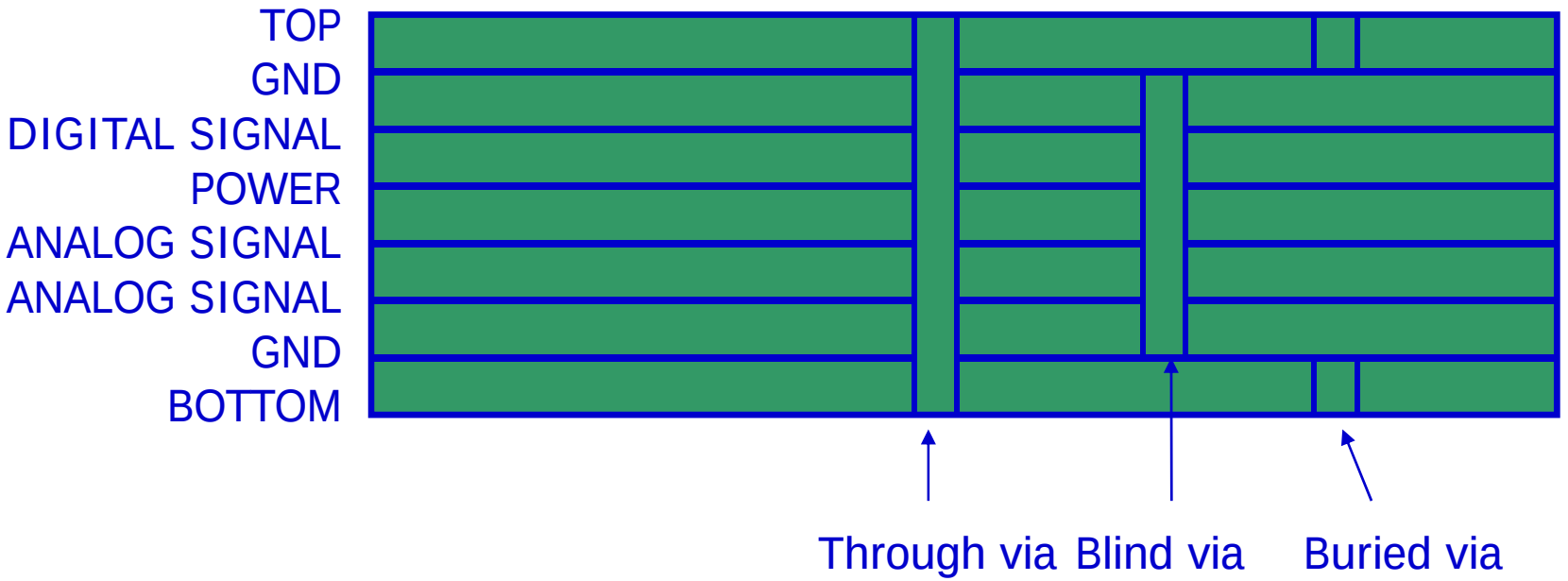
- the plane is robust and hermetic;
- inefficiency of about 6% is compatible with the geometrical one due to spacers;
- uniformity of efficiency on the large scale (0.06 m2 area) is (94+/-2)%;
- current in HV circuit is 1 μA;
- noise at the plateau knee of about 0.45 Hz/cm2 is acceptable.



Conclusion

- **Many efforts on gaseous DHCAL are going on in Europe.**
- **European DHCAL project has the ambition to be as close as possible to ILC detector requirements.**
- **European project is complementary to the american one .**
- **It is hoped that the two projects merge in the future.**

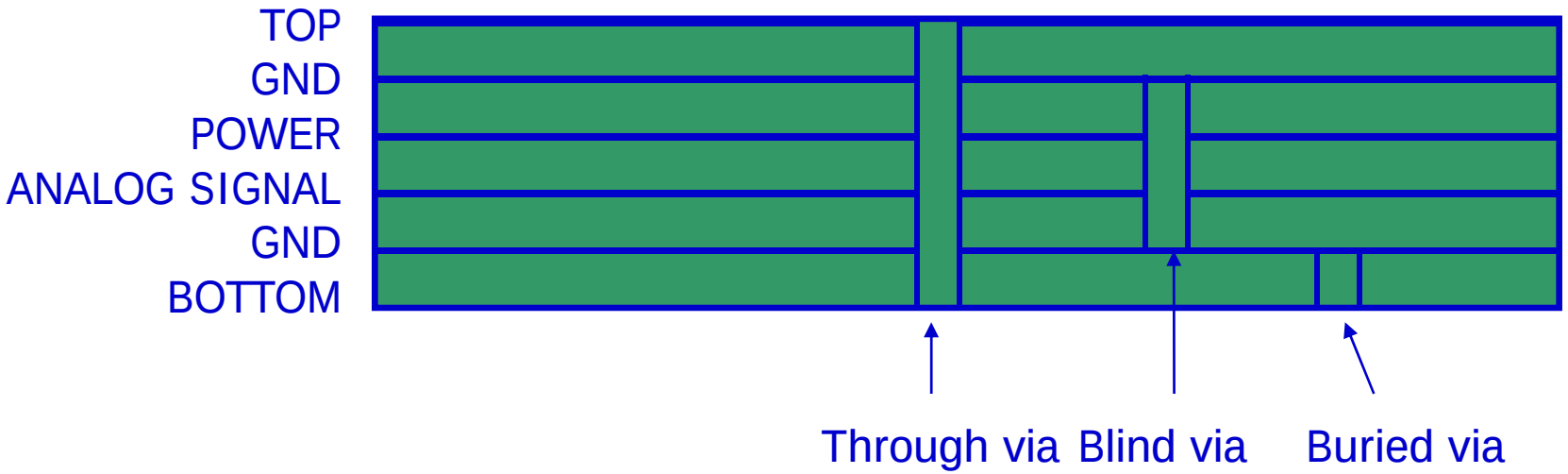
Layout in 8 layers (solution1)



Layer definition (except FPGA area)

TOP LAYER	: Component layer
GND	: Ground layer and access to internal layers
DIGITAL SIGNAL	: Layer to interconnect between hardroc and FPGA
POWER	: Power to hardroc
ANALOG SIGNAL	: Layer to interconnect pad signals
BOTTOM	: RPC pads layer

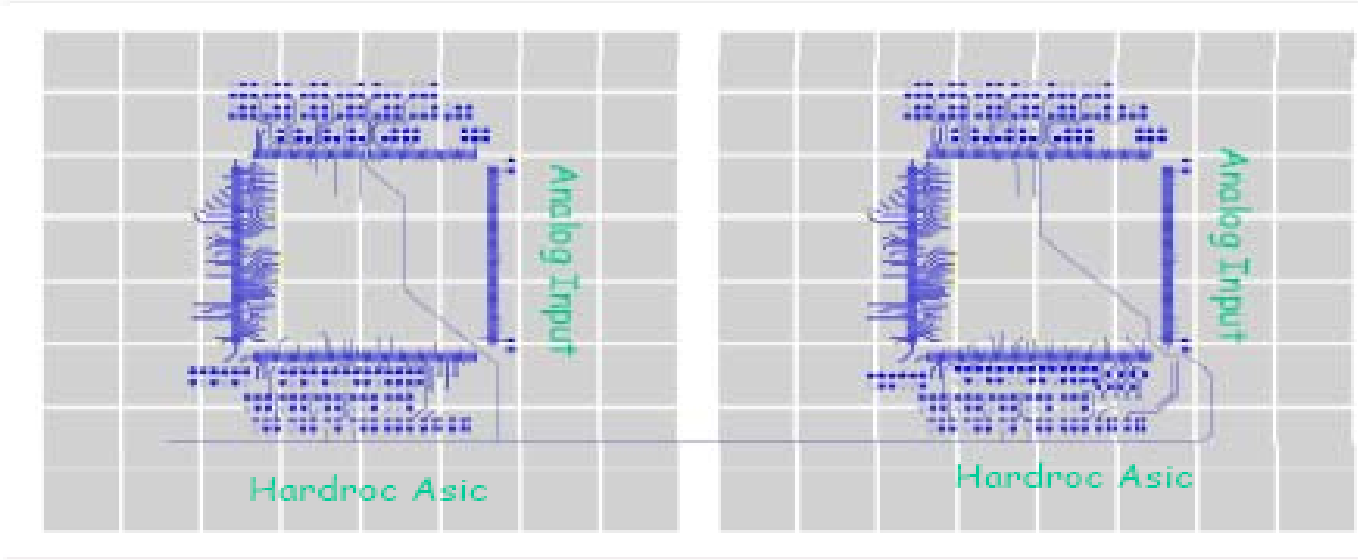
Layout in 6 layers (solution2)



Layer definition (except FPGA area)

TOP LAYER	: Component layer+interconnect between hardroc and FPGA
GND	: Ground layer and access to internal layers
POWER	: Power to hardroc
ANALOG SIGNAL	: Layer to interconnect pad signals
BOTTOM	: RPC pads layer

Top layer and Pads (8 layers)



DAQ2 (needed for the m³)

- DIF: Det. Specific. FE
  - To be defined next...

Constraints (M. Wing):

- LDA: concentrator card
  - 1 Gbits/s output
  - Up to 50 DIF input (#pins of the FPGA)
    ➔ 20 Mbits/s per DIF
- ODR: readout card
  - Can reads 2 LDA @ 1 GB/s
  - Links are expensive