Vertex Detector System Design

This talk will concentrate on the topics of power, mechanical support, interconnections. I will try to be sensor technology-independent - but in general sensor technologies drive, and are driven by, cooling and power choices.

Contents:

- Requirements
- Candidate technologies
- Mechanical Studies
- Power Distribution
- EMI
- Summary

Physics Needs

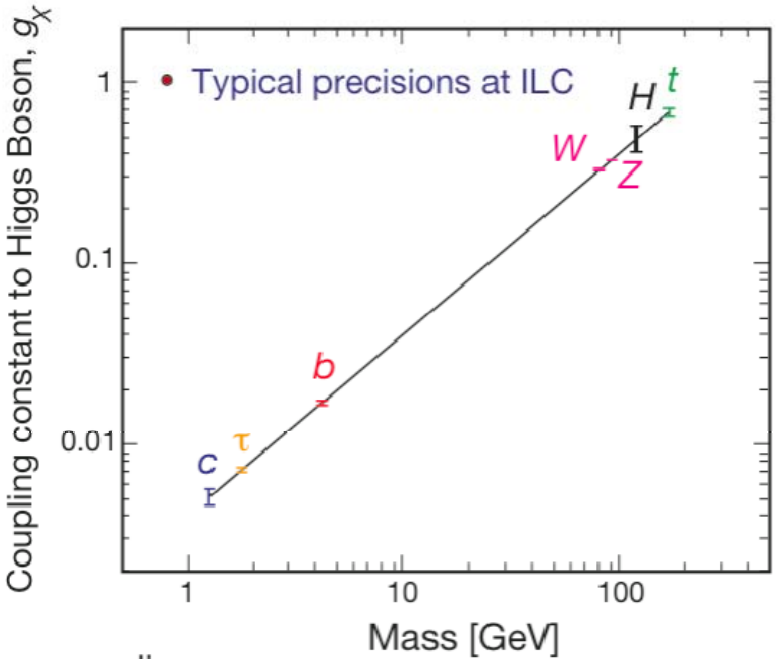
ILC is designed to do precision physics

- Higgs couplings
  - Require excellent separation of b/c/light quark vertices
- Higgs self coupling:

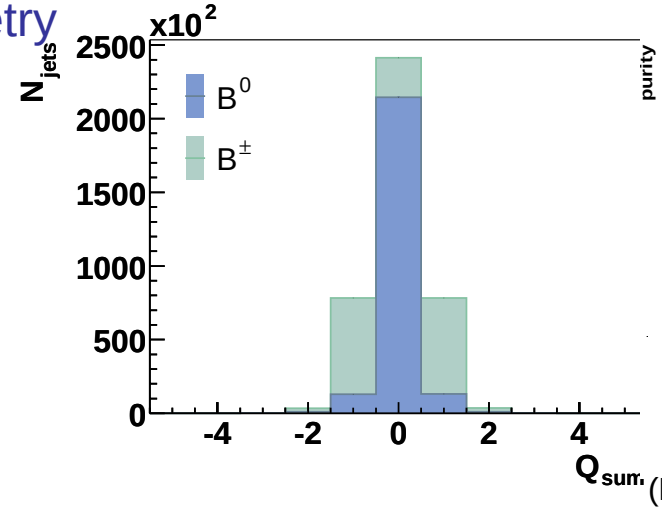
$$e^+e^- \to Z^0H^0H^0 \to qqbbbb$$

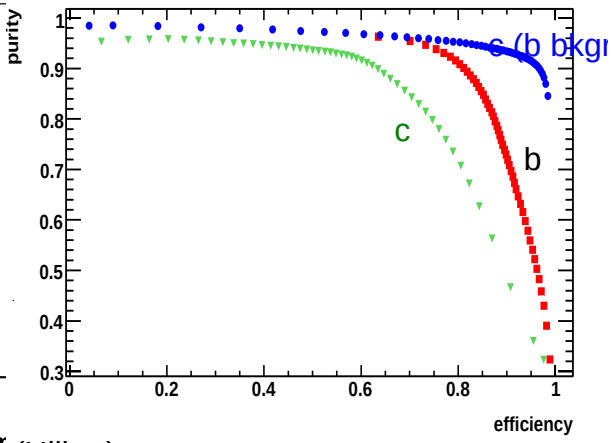
$$backgrounds: tt \to bb\,\mathrm{csc}\,s, ZZZ, ZZH$$

  - B quark ID within jets



- Forward-backward asymmetry
  - Flavor tagging
  - Vertex charge
  - Forward tracking





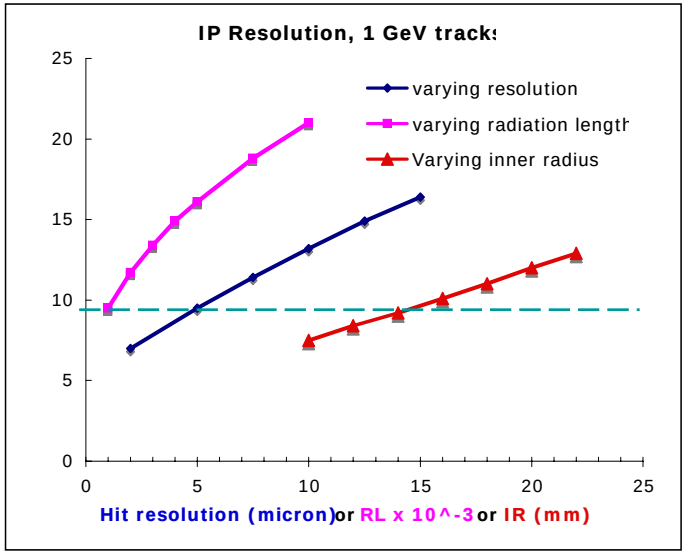
Detector Goals

- Good angular coverage with many layers close to IP
- Excellent spacepoint precision (< 5 microns)
- Superb impact parameter resolution ($5\mu m \oplus 10\mu m/(p \sin^{3/2}\theta)$)
- Transparency (~0.1% X_0 per layer)
  - Power constraint based on minimal mass (< 50 Watts)
- Integration over <150 bunch crossings (45 μsec)
- Electromagnetic Interference (EMI) immunity
- Moderately radiation hard (<1 MRad)
- Track reconstruction

Difficult to satisfy all of the constraints, especially power and time resolution

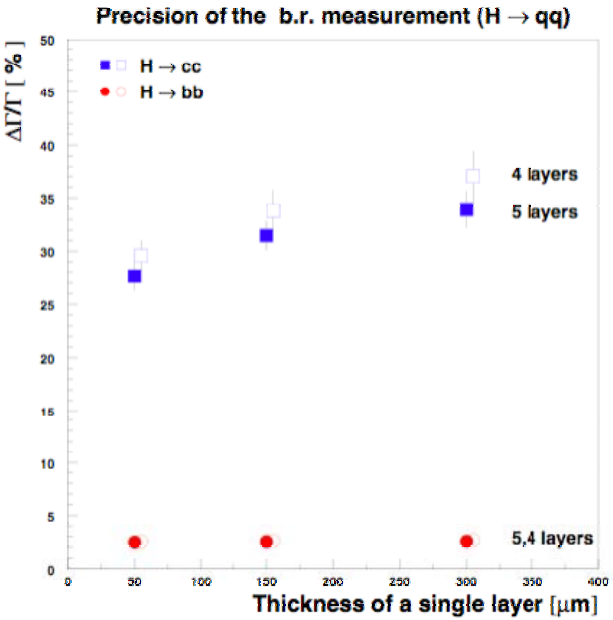
Optimizing Vertex Performance

- Inner radius
- Material
- Position resolution (<5 microns)
  - Binary or analog readout
  - Charge collection by diffusion (MAPS) or drift (3D, SOI)
- Optimizing vertex performance has significant physics impact
  - 5 μm resolution or better is possible with current sensor technology
  - Minimal mass is crucial - this implies constraints on power to enable air cooling.



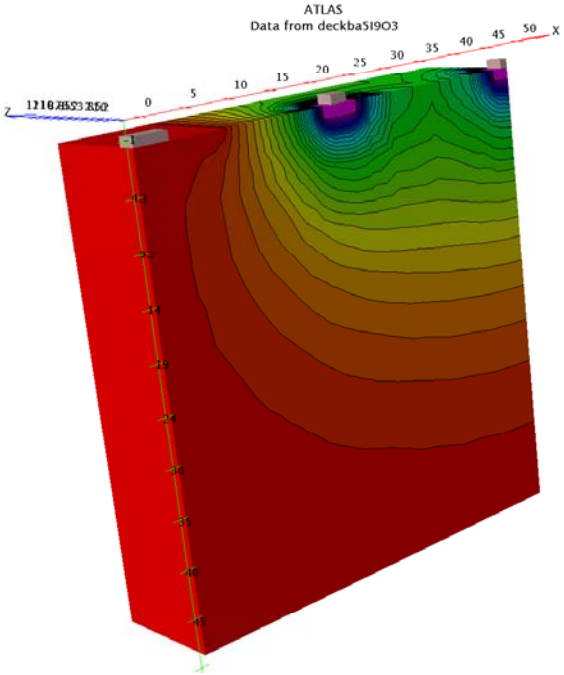
Parametric simulation assuming:
- 0.1% RL per layer
- 5 micron resolution
- 1.4 cm inner radius

Varying each parameter



Technology

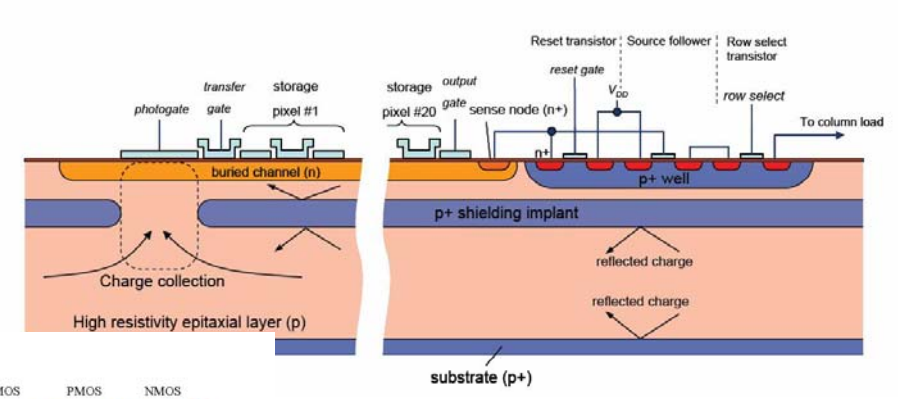
- Technologies being developed by the semiconductor industry are directly applicable to ILC vertex detectors
  - Thinning (standard for many applications)
  - Integrated sensors and CMOS (digital camera)
  - Focal plane sensor development - “edgeless” sensors
  - “Virtual Wafer Fab” simulation software
  - Access to CMOS processing variants



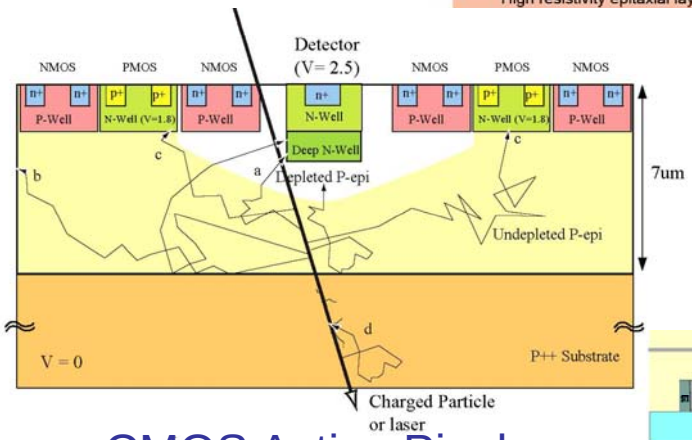
- We can engineer detectors in ways we never could before.

Candidate Technologies

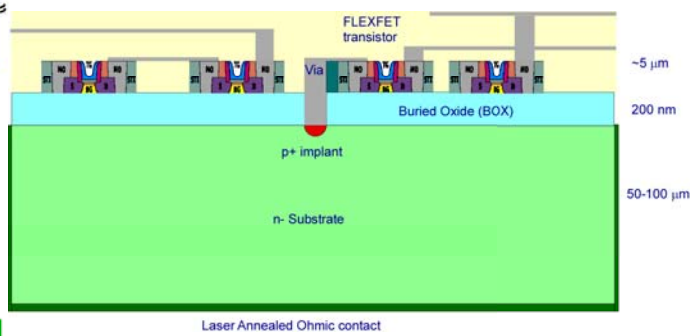
- CCDs
  - Column Parallel
  - ISIS
  - Split Column
  - Fine Pixel
- CMOS Active Pixels
  - Chronopixel
  - Mimosa
  - LCRD 1-3
  - INFN
- SOI
  - American Semiconductor
  - LCRD-SOI
  - KEK
  - SUCIMA
- 3D
  - VIP1 (FNAL)
- DEPFET



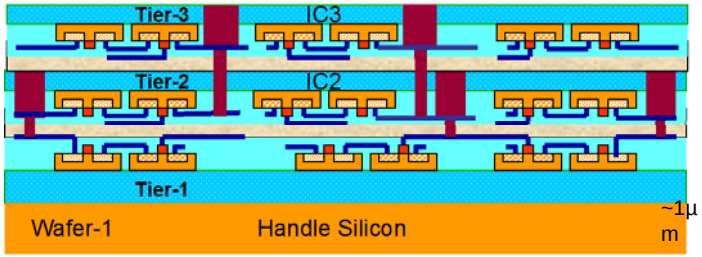
CCD



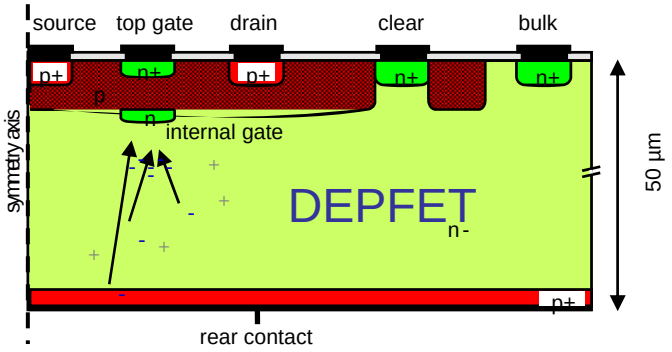
CMOS Active Pixels



SOI

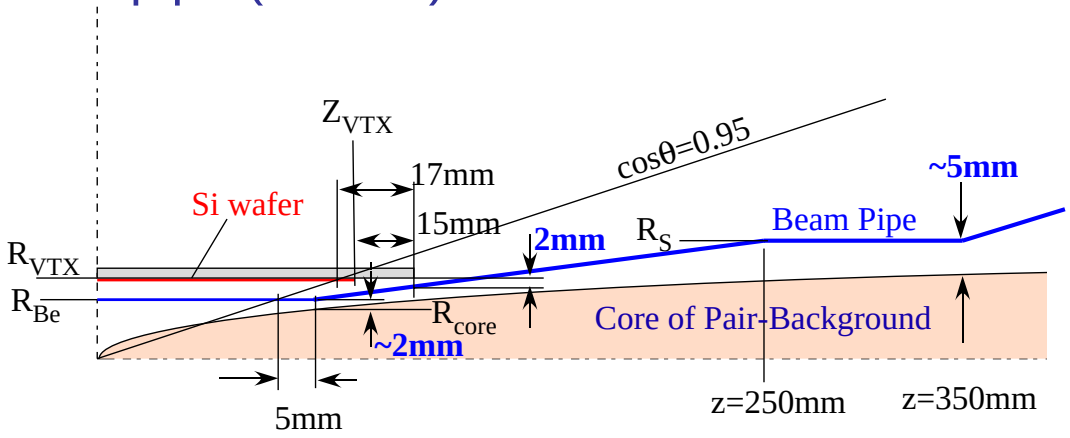


3D

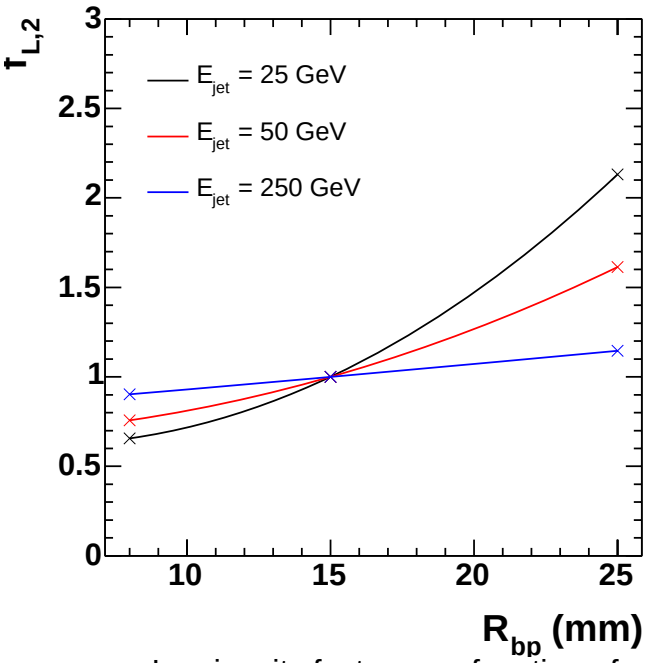


Geometry

- Inner radius important to IP resolution, vertex charge, vertex reconstruction
  - Determined by magnetic field, machine parameters
- Beam pipe must flare to accommodate disrupted beam fragments
- Vertex enclosure also supports the beam pipe (for SID)

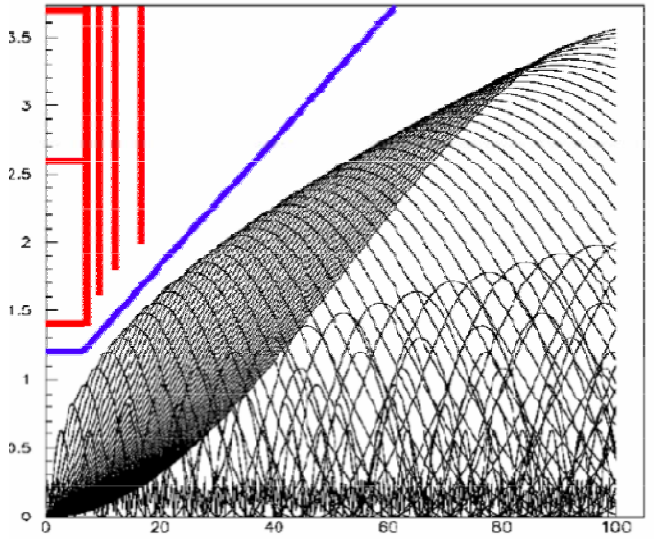


(GLD)



Luminosity factor as a function of radius for processes requiring vertex charge for 2 jets

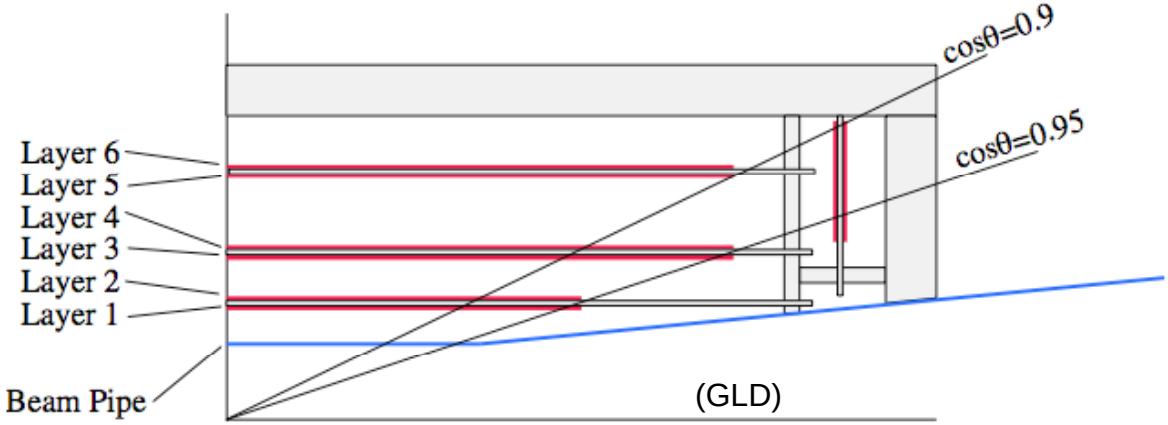
(Hillert)

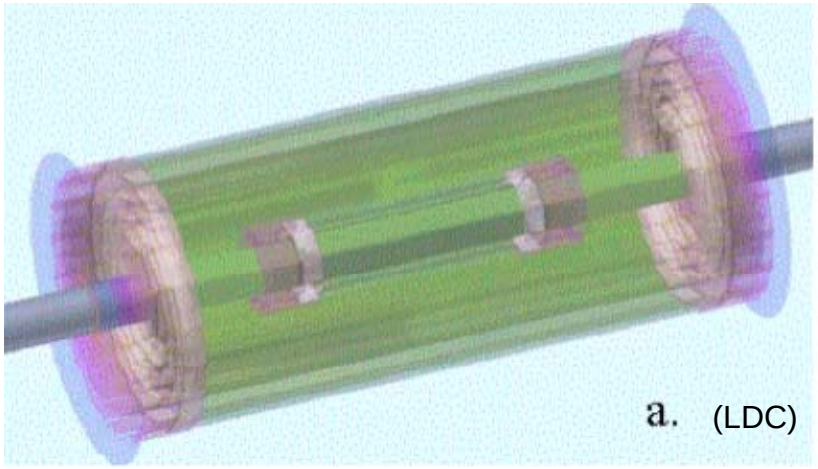


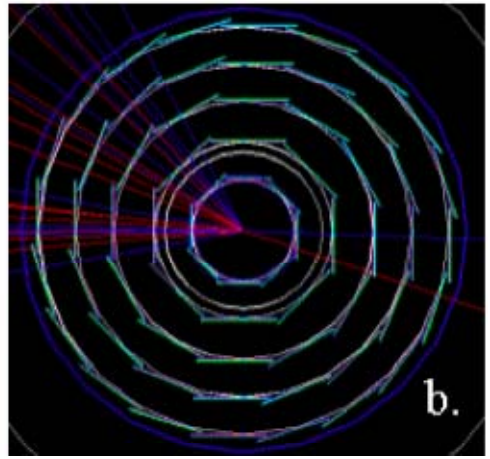
Design Features

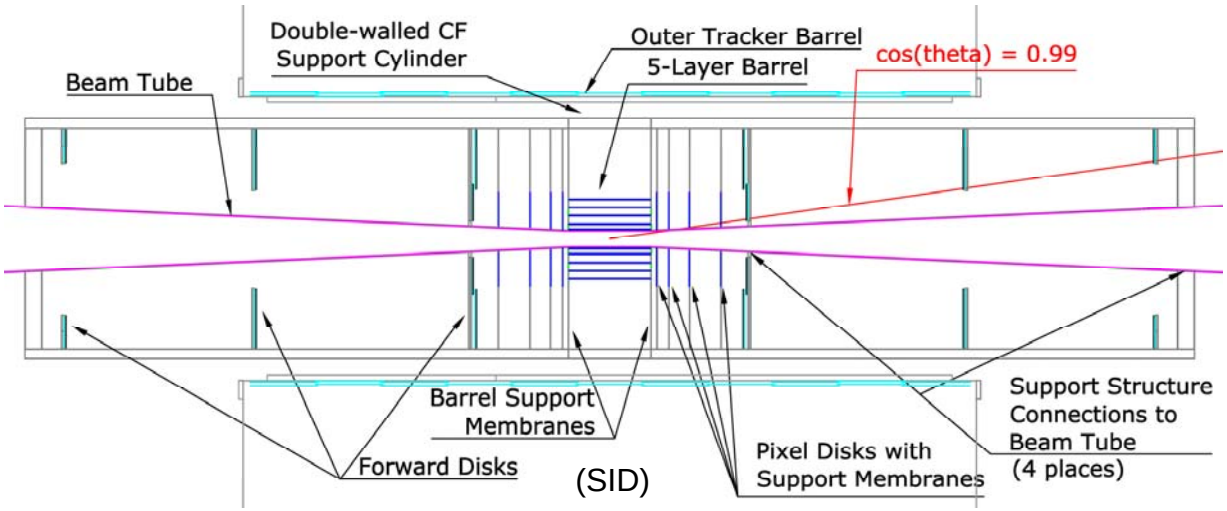
- Outer radius ~ 6 cm
- Barrel length ~ 14 cm
- Ladder widths 1-2 cm
- Disks to cover forward region

A bit larger than this



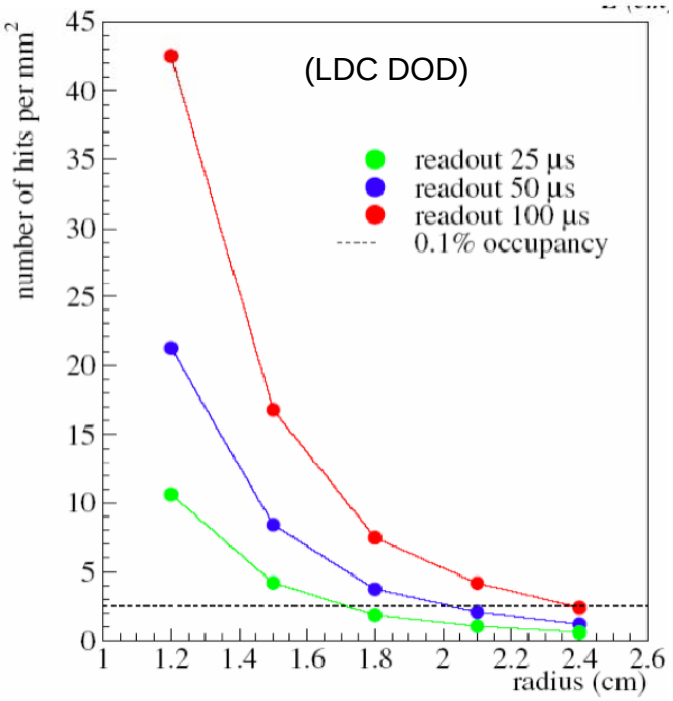


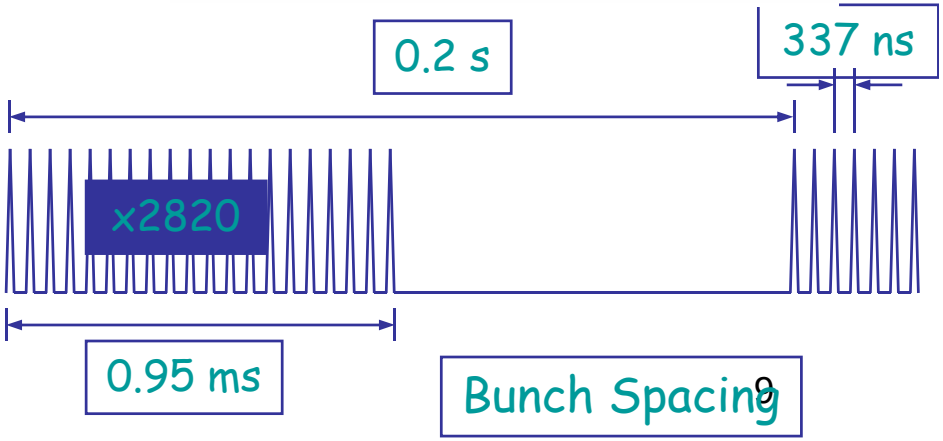




Time Resolution

- Need set by inner layer beam-based occupancy - how many crossings do we integrate over?
  - Stand-alone pattern recognition?
  - Timing information from outer tracker?
  - Overall background hit tolerance?
- Better than 50μs resolution generally agreed (the more precise the better)
- Time is power (FE current, more clock cycles …)
- Read out during or after bunch train
- Differs by technology
  - Rolling shutter
  - Multiple analog samples
  - Explicit time stamps
  - Buffers per pixel

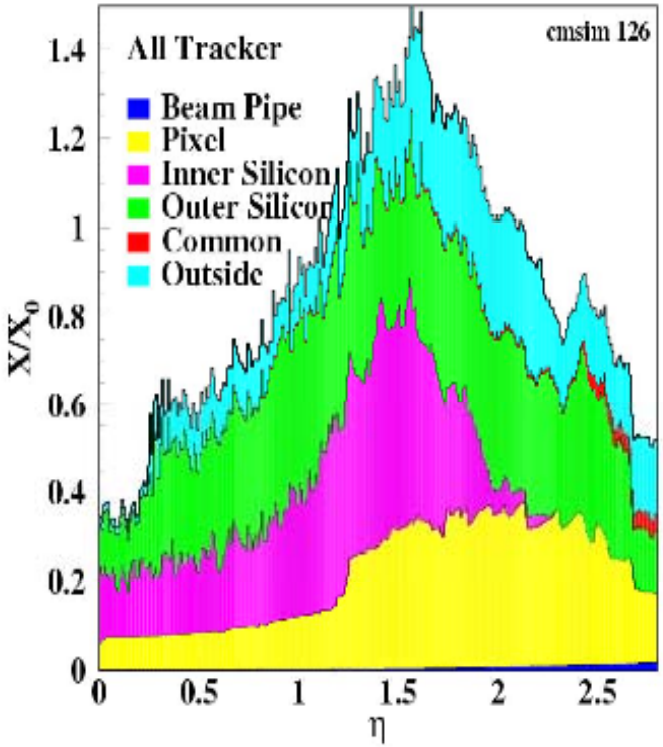


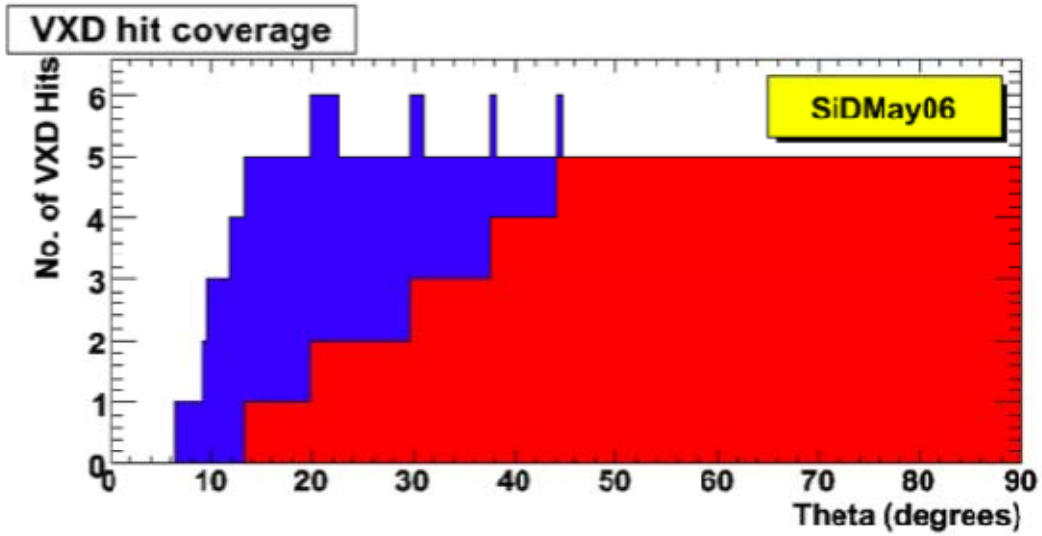


Material

- To achieve ILC goals we must improve RL/layer by ~20 x

LHC





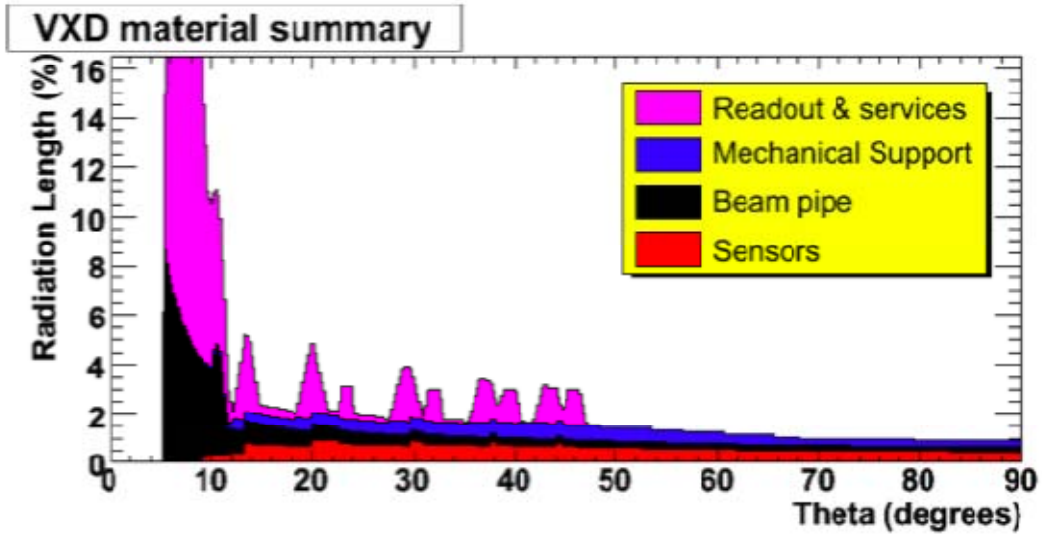
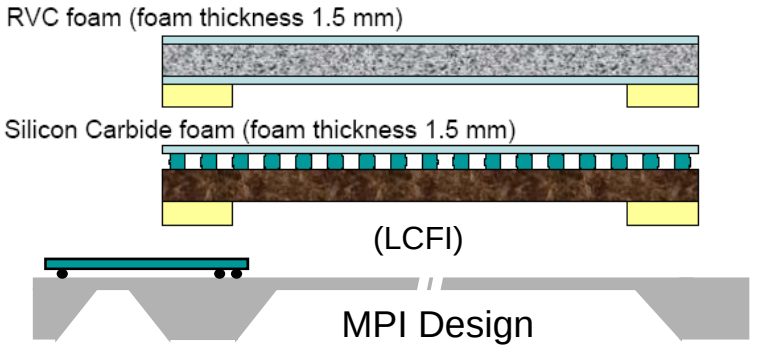


Figure 33 VXD hit pattern and material summary as a function of polar angle.

Mechanical Support

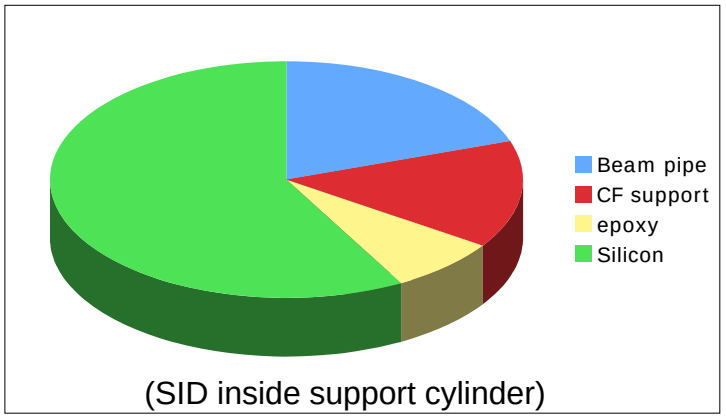
- Several options – range in ambition
  - Carbon fiber-based supports, similar to D0 layer 0
  - Foam-based (SiC, RVC) supports
  - Silicon picture frame (MPI)
  - Pure silicon?
- System Issues
  - Planarity of the sensors
  - Bonding to thin silicon
  - Thermal bowing
  - Connection to external cables
  - Full size (~12 cm) sensors (CCD, DEPFET) or mosaic of ~2 cm reticules (CMOS, SOI, 3D)?

(University of Washington)



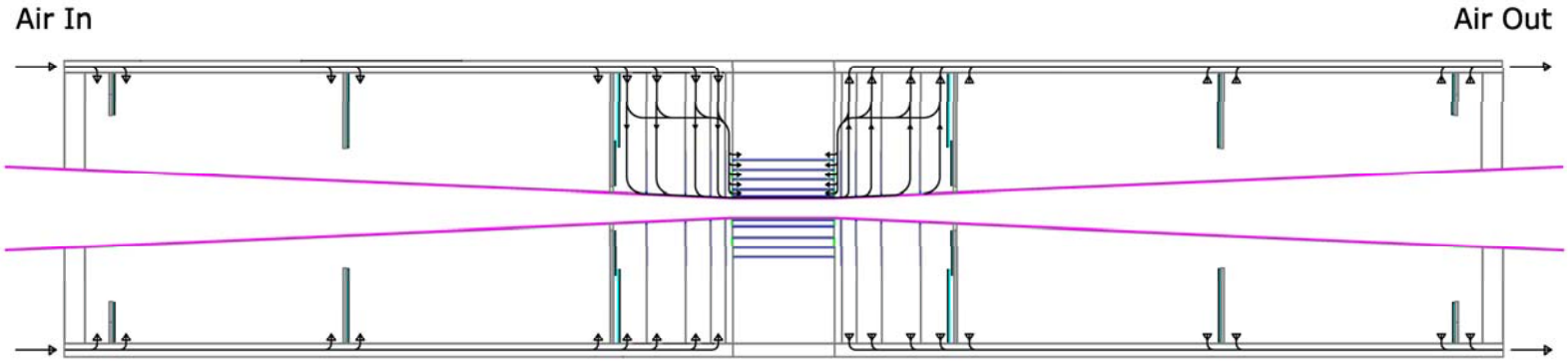
(LCFI)

MPI Design



(SID inside support cylinder)

Air Cooling



(Cooper, SID)

- Air cooling is crucial to keep mass to a minimum
  - implies a limit on power dissipation
- Require laminar flow through available apertures
  - This sets total mass flow – other quantities follow
- For SiD design
  - Use the outer support CF cylinder as manifold (15mm Δr)
  - Maintain laminar flow (Re_{max} = 1800).
  - Total disk (30W) + barrel (20W) power = 50W *average*
    - For SiD ~ 131 $\mu W/mm^2$.
    - Max ΔT ~ 8 deg

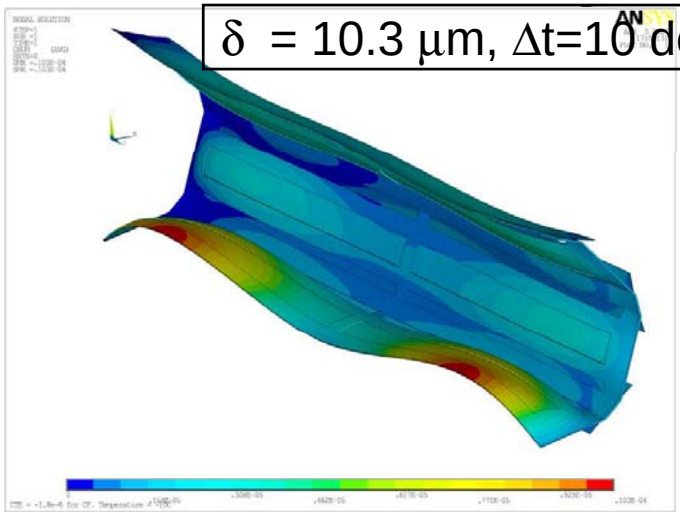
Alignment and Stability

Planarity

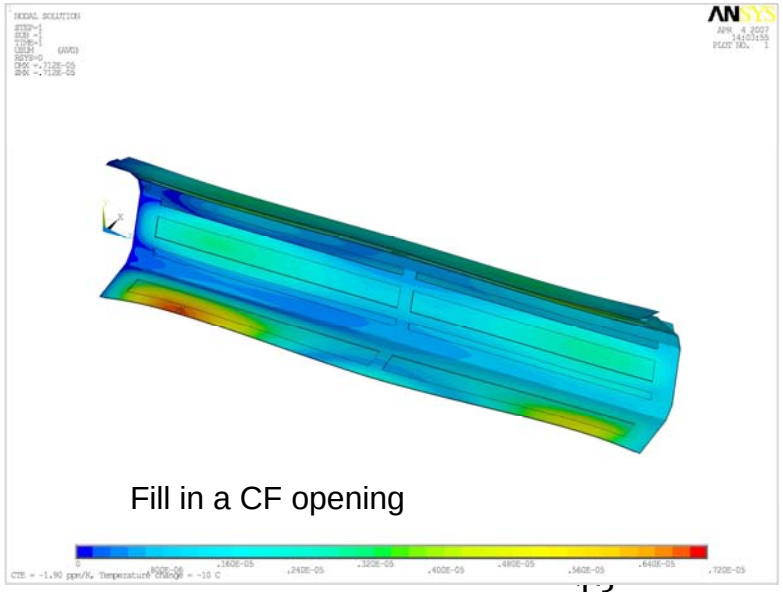
- Depending on technology, thinned sensors may have built-in stresses and differential CTEs
- Could be stiffened by support structure (mass)

Interconnections

- Wirebonds can be made to silicon thicker than ~50 microns
  - Wirebond compliance separates sensor from cable moments
- Minimize number of connections
- Does the bulkhead contain
  - Bypass capacitance?
  - Serial power routing?
  - Stiffness to absorb cable torque?
  - Position monitoring?



FEA of SID CF support with thin silicon and openings to reduce mass (Cooper, U Washington)



Fill in a CF opening

(U. Washington)

Technology and Power

CCD	Requires cryostat, low temperature operation, power dominated by clock driving high capacitance CCD planes (100nf x 3.0Vx 20MHz=6A/phase/sensor)
CMOS MAPS	Dominated by FE transistor, can be power cycled
SOI/3D	Dominated by FE transistor, can be power cycled
FE power	1 μa FE current, 20 μm pixels, 1/80 duty factor, SID size (1.6×10^5 mm^2) -> 5 W for the barrel, power cycling crucial
DEPFET	Low power, FE transistor only on when being read out, ~6 Watts for the barrel, power cycling unnecessary

Noise and Power

For pixel amplifier-based devices the FE amplifier usually dominates power consumption:

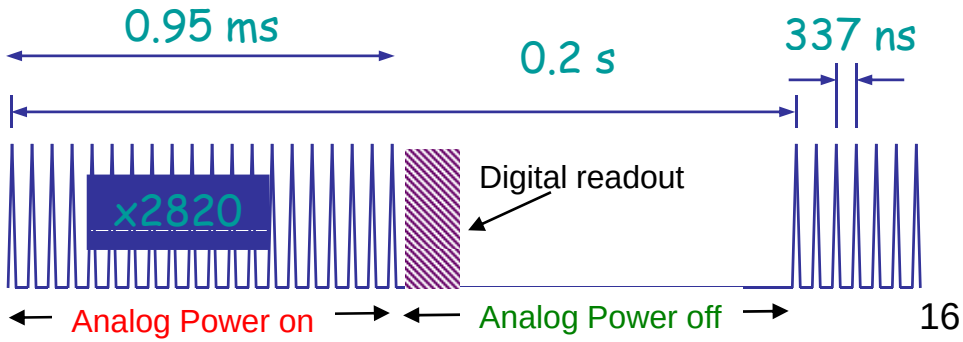
- Series white noise:

$$ENC^2 = (C_{\det} + C_{gate})^2 \frac{a_1 \gamma 2kT}{g_m t_s}$$

- Noise scales as C and 1/sqrt[transductance (g_m)]
- Pixel front end transistors will operate in weak inversion - where g_m is independent of device geometry and ~(I_d/nV_T).
- Assume 130 μW/mm^2 , 20 micron pixel, duty factor ~ 100
  - 5.2 μW/pixel
  - 3.5 μA @ 1.5 V
- Acceptable low current operation (<1 μA) requires long shaping and/or low node capacitance
  - For t_s = 100ns, I_d=1 μA C_d ~ 100 ff noise ~ 35-50 e
  - ~10 ff should be achievable in SOI devices, 20-40 in MAPS

Power Distribution

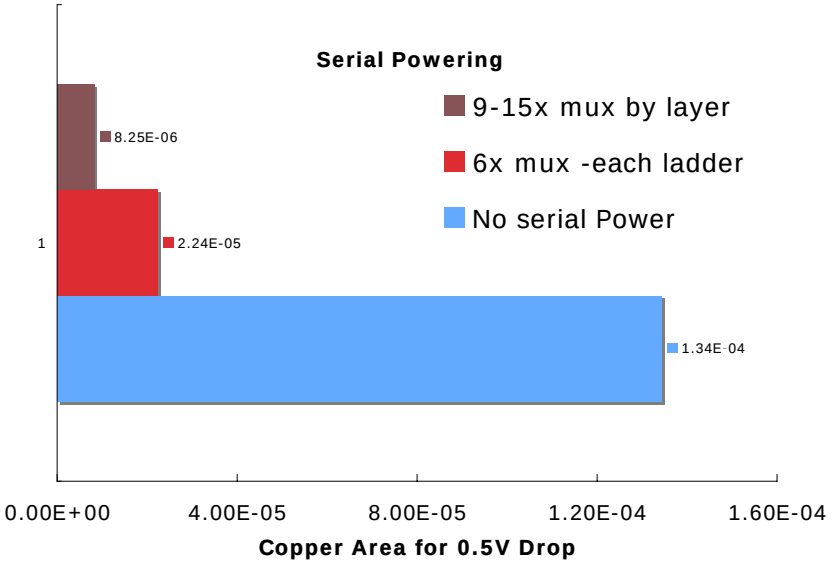
- Peak and average power are both crucial issues for the vertex detector
  - CCD 20 amps x 200 modules = 4000 amps of clock
  - MAPs, SOI ~ 1μa/pixel x 1V x $4x10^8$ pixels ~ 400 Watts
- Power pulsing for FE chips - just turn power on during 0.95/200 ms
  - Maximum duty factor ~200, assume ~100 may be practical
    400 W=> 4 W (average) (let's assume 20W)
  - But I_{peak} is still the same - 2000A if we saturate the 20W limit
- High peak currents => more conductor to limit IR drop => Mass
- Lower CCD capacitance, ISIS (read CCD during beam-off), DEPFETs or other technologies which reduce FE power
- Serial powering (think Xmas lights) can lower instantaneous current



Serial Power

Peak current can be reduced by providing power at higher voltage and locally regulating ladder voltage (current sharing)

- Peak currents reduced by number of ladders per string
- Conductor volume set by IR drop is reduced
- Needs:
  - Near-sensor regulation - perhaps integrated with sensors
  - Ramped current supplies
  - Study of power regulation losses



- Local regulation relaxes the IR constraints (50 mV => 0.5 V?)
- For copper cable with 0.5 V drop the equivalent shell at 6 cm radius is:
  - 0.5% Radiation length for normal power
  - 0.04 % for serial power (should be acceptable)

Serial Power II

Most work on serial power to date has been done for sLHC

- ATLAS power loss in cables 3x detector power, CMS tracker 2x
- Demonstrated serial power in ATLAS pixel modules
  - Local shunt/linear regulators
  - Constant current supply
- Major concerns
  - Increased vulnerability to failures in the string
  - Increased coherent noise sensitivity due to lack of ability to interconnect local grounds with low impedance (ok in initial ATLAS tests)
  - Increased interconnect complexity, bias distribution
  - AC isolation to readout (optical)

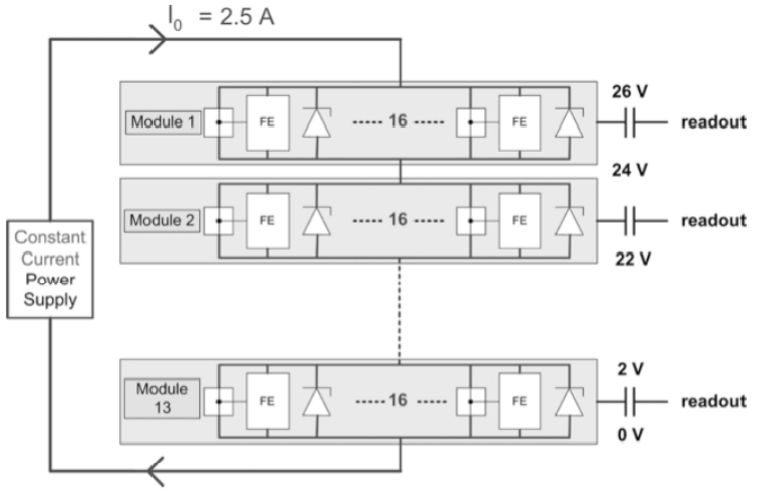


Fig. 1. Basic scheme of serial powering. A power supply provides a constant current which is fed into a chain of modules. In each module a shunt generates a constant voltage from the constant current. Additional linear regulators are used if more than one supply voltage is needed.

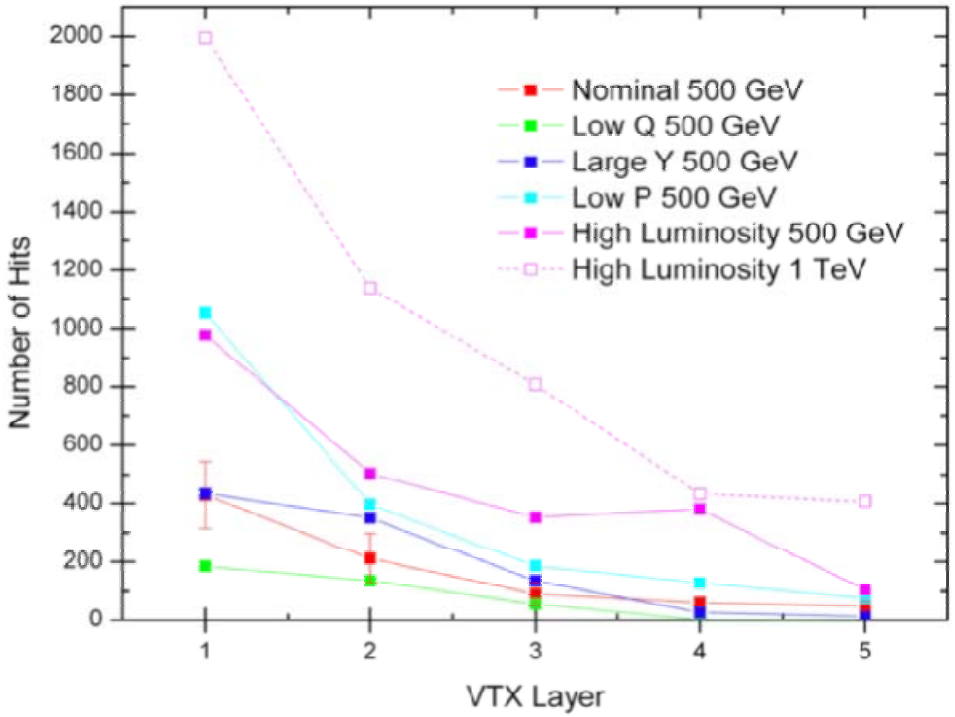
Atlas SLHC design

The price seems small compared to the benefits - should be focus for ILC R&D

DC-DC conversion is an alternative, but less promising

Data Readout Power Load

- Assume ~ 1 TeV high luminosity
- Cable power = f x C x V^2
  - Assume 30 bits/hit ~ 1.4x10^7 hits/train ~
  - 2 Gbit/sec, 1 V, 3 m
  - If total c_{clock}~15 nf (system) p ~ 30 Watts (too much)
- Power for optical drivers
  - ATLAS ~ 10 mW/line(lowest)
  - For 96 ladders ~ 1 W
- Where are the cables routed?
  - Outer support cylinder
  - Along BP?
  - Transition to high mass cables



(LDC)

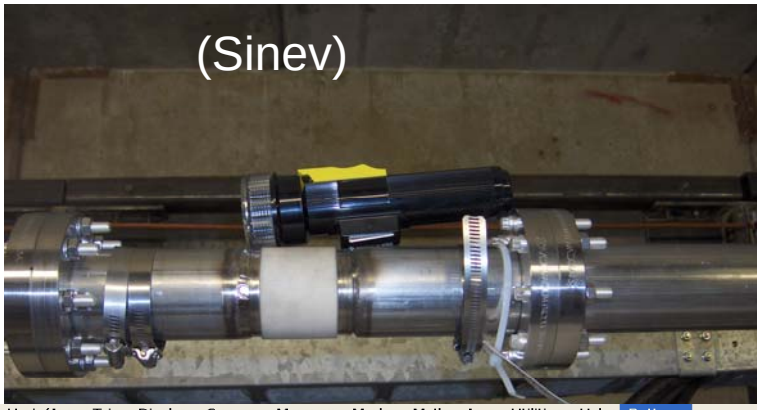
EMI Studies

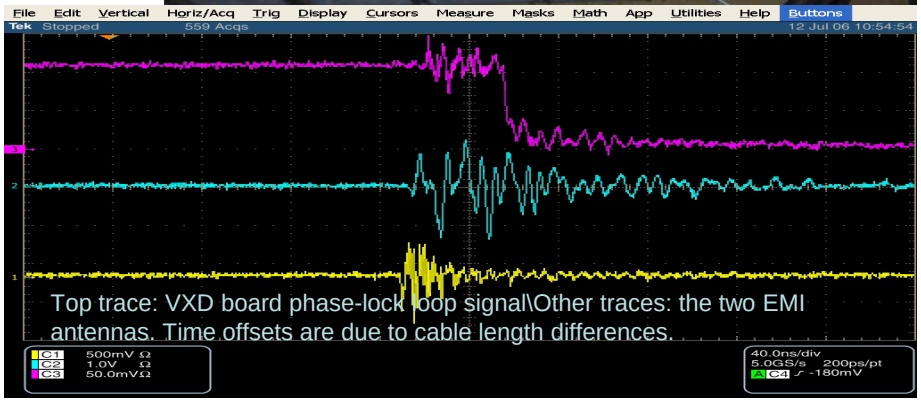
SLD saw significant electromagnetic interference associated with the SLC beam crossings

- amplifiers saturate, PLL lost lock
- This can have a major effect on vertex (and all electronics) design
  - Better to read out between bunches
  - Avoid active electronics during train

End Station A study of beam-induced EMI

- Antennas placed near (~1 m) gaps observed pulses of EMI in the high MHz range with strengths up to ~20 V/m.
- The pulse amplitudes varied in proportion to the bunch charge, independent of the bunch length.





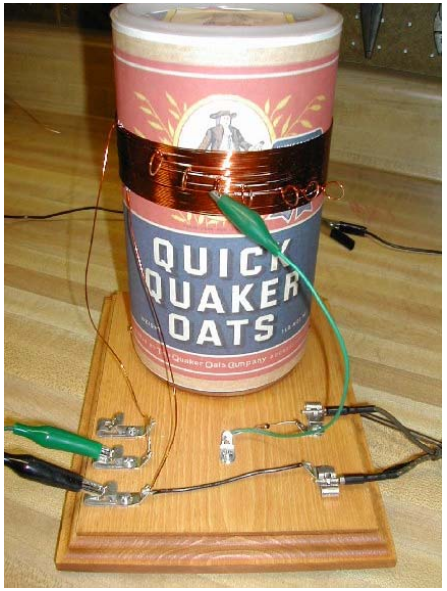
- A single layer of 5mil aluminum foil placed over the ceramic gap and clamped at both ends reduced the signal amplitude by >x10 (eliminated?)
- A 1 cm hole in the al was enough to cause the PLL to fail, failures stopped at .6 cm

Is there any need to have gaps in the pipe?, How close to the IR?

To what extent is this a design constraint on the vertex and tracking?

Conclusions

- Combination of sensor technology, new materials, power pulsing, serial powering should be able to achieve a very low mass, precise vertex detector
- Achieving the 0.1%/layer RL goal will require a substantial engineering effort
  - Understand thinned materials and supports
  - Power cycling
  - Power distribution
  - Interconnections
- I have not mentioned:
  - Forward direction
  - Lorentz forces
  - Vibrations
- Technology drives many ultimate design decisions but we can make real progress on supports, power delivery, and cooling in parallel with sensor R&D.

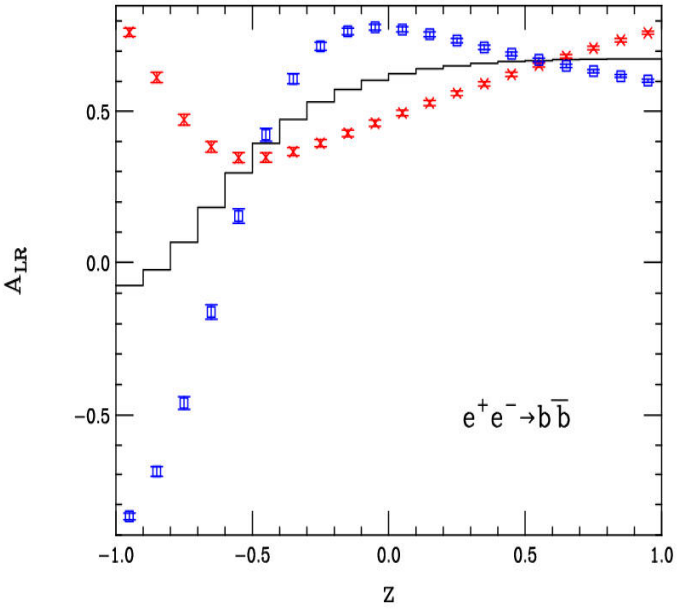


Forces

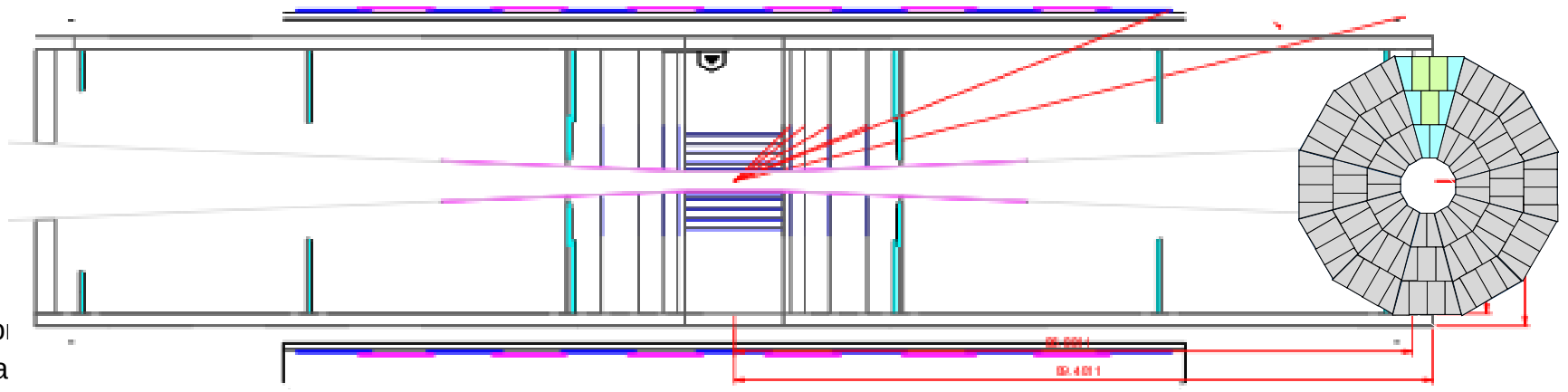
- Thinned silicon can be distorted by modest forces
  - Lorentz force due to unbalanced currents
    - Vibrations induced by power pulsing
  - Limit transmission of support and cable moments to silicon
  - Thermal distortions => limit temperature rise?

Forward Region

- A_{fb}, $Z\gamma$, $\nu\nu h$ all require good, low mass forward vertexing and tracking
- Assuming pixels for the forward region?
  - What are we asking of the forward vtx?
    - IP resolution - dominated by barrels
    - Pattern recognition
  - Integration with forward silicon design
  - Pixel size
    - Maximum size -> minimum power
    - Support and geometry



KK graviton exchange with jet-charge info
$\sqrt{s}$ = 500 GeV, Λ = 1.5 TeV, 500 fb^{-1}
(Hewett)



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Sensor Thinning

- Becoming a standard service in the semiconductor industry
- A number of techniques are available
  - Backgrinding and polishing
  - Chemical etching (MPI)
  - Reactive ion etching (RTI)
- Working chips demonstrated to 15 microns, sensors to <50 microns
- Laser annealing techniques have been developed to form backside contacts after thinning