Carleton/Montreal Electronics development

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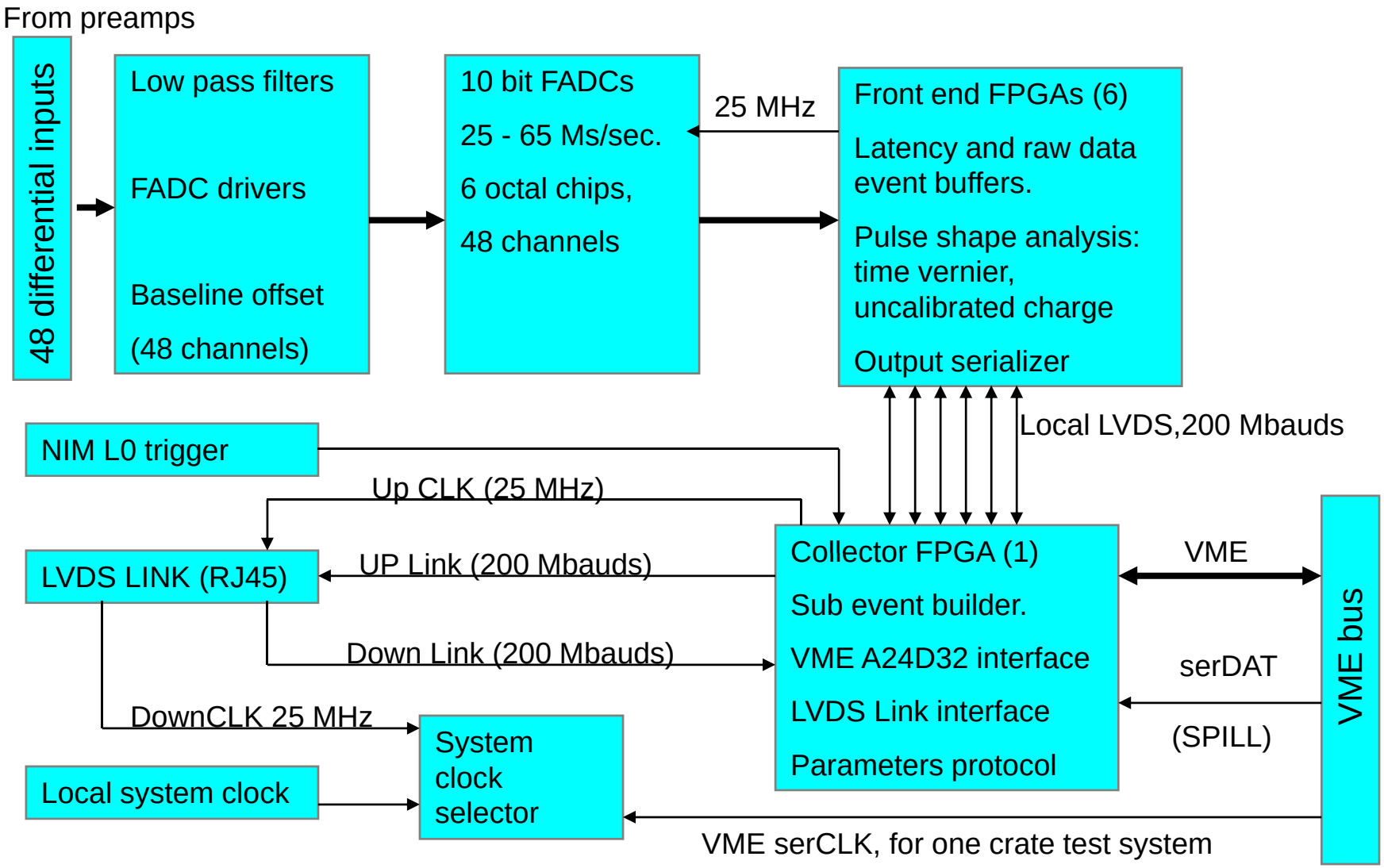
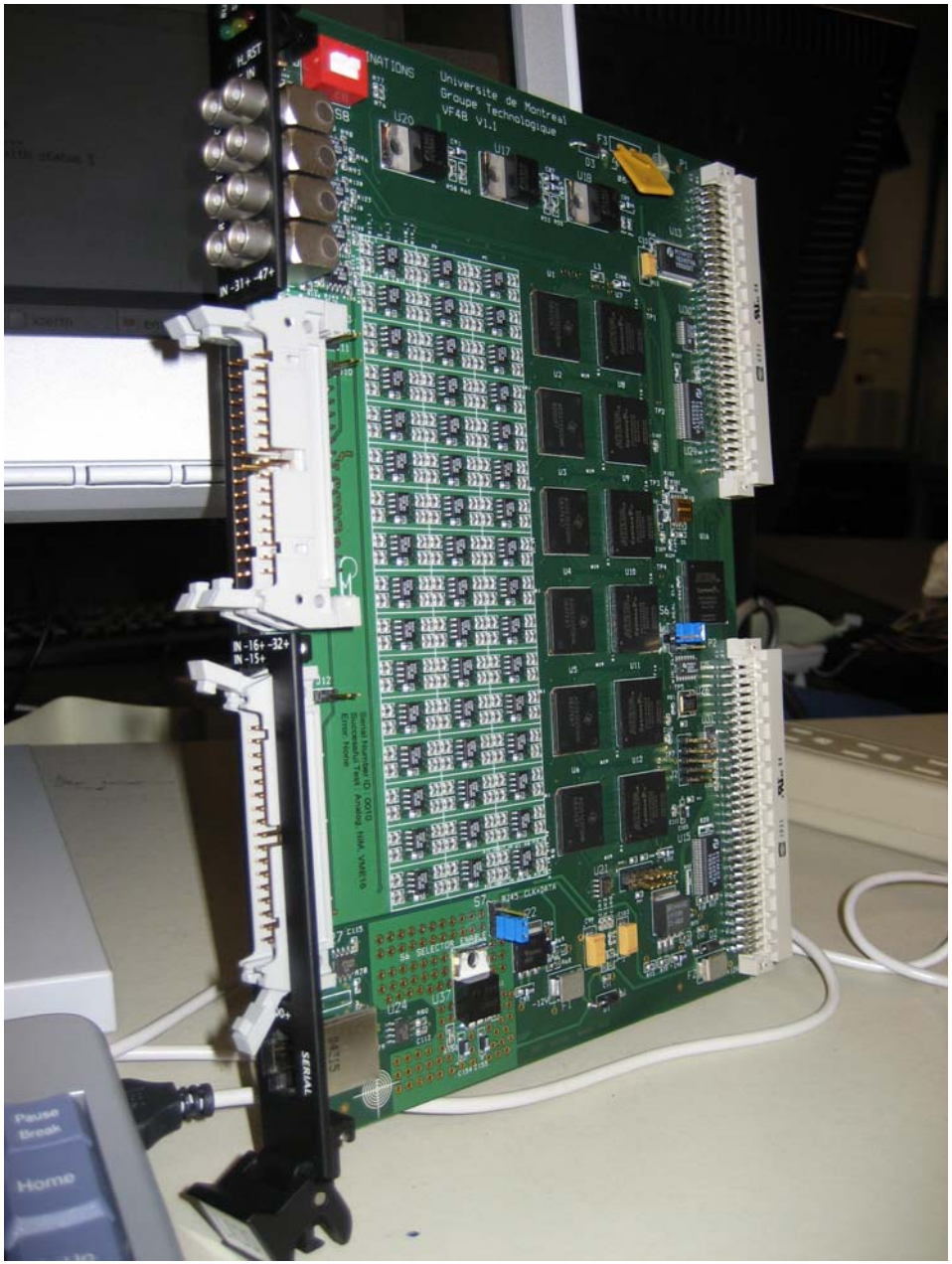
Development based on KOPIO VF48 prototype readout card




Universite de Montreal
Groupe Technologique
VF48 V1.1
IN -31+ -47+
IN -16+ -32+
IN -15+
SERIAL
Pause
Break
Home

General specifications

Input: 48 differential pairs, 100 position connector, fine pitch
flat cable. (now 3 X 34 position normal pitch connectors)
Analog conditioning: - fixed gain (1x to 20x practical)
- low pass filter (Nyquist)
FADC: 10 bits, +- 0.5Volts full scale.

Trigger window: 0 to 100 microseconds
Hit detector pulse shape segments: 0 to 4 microseconds,
retriggable
Firmware digital filters/shapers

VME A32D64 interface

- New TPC readout cards being developed, will be more closely related to the LTPC requirements.
- New generation of 12-bit 50MS/sec FADCs (the one with LVDS serial output at 600 MHz).
- A small 16-channel prototype with an USB interface to study the problems related to 600 MHZ serial readout of new FADCs has been designed
  - Test cards fabricated
  - Presently being assembled
  - Will incorporate power pulsing in next generation
- Combine tests of new electronics with proposed 2008 Fermilab TPC tests in 1-2 T magnet with ILC beam structure.