R&D for a 2nd generation AHCAL prototype

Mathias Reinecke

on behalf of the AHCAL partners

Current AHCAL Testbeam Prototype

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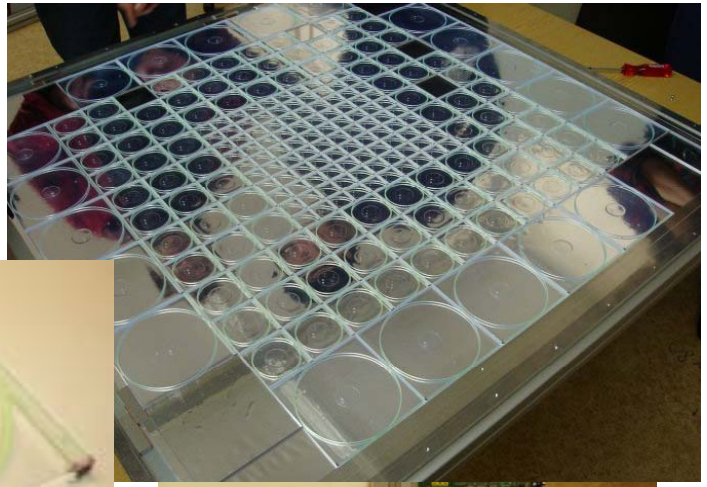
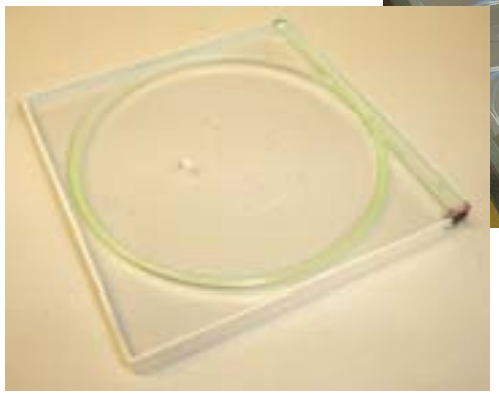
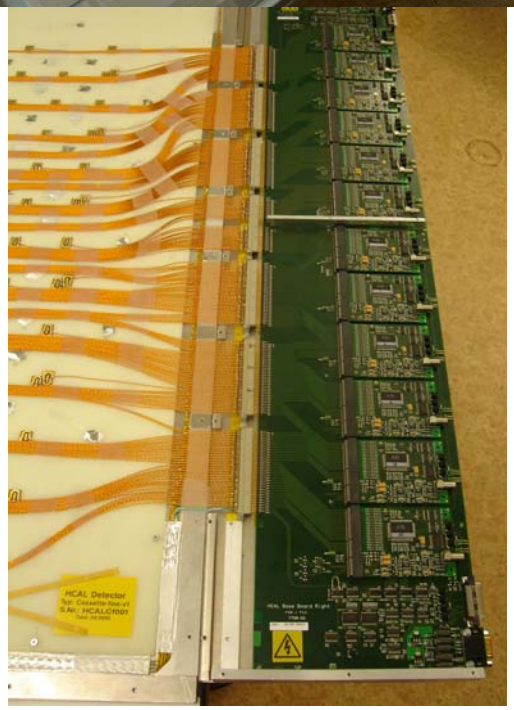
-8000 Tiles with SiPMs in 38 layers
-New Readout Electronics
-LED Calibration System







<u>BUT: not scalable to a full detector:</u>

-Electronics (ASICs), Tiles and Calibration System not integrated into layer
-Electronics not optimized for SiPMs
-Assembly to complicated (time, cost)
-ADC not in Front End ASIC

Mechanical Constraints

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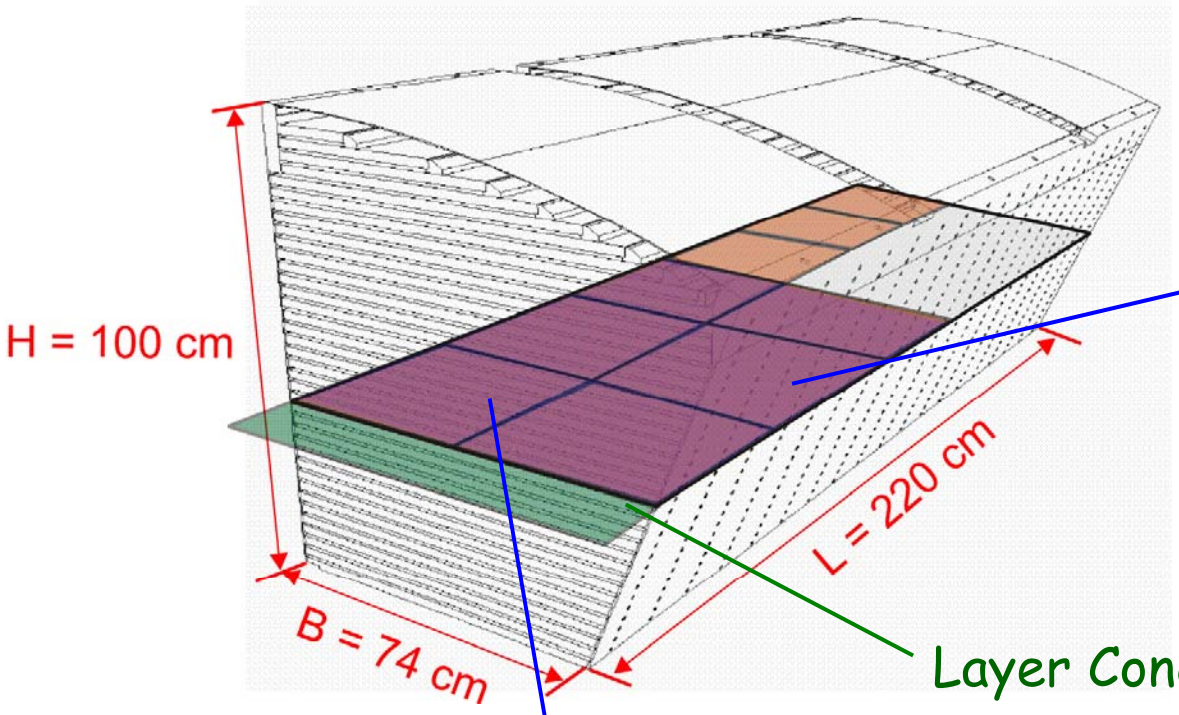
AHCAL Half-Sector with 38 layers



Combine many HBUs to **layer-units** for assembly.

Layer Concentrator (Signals / Power)

HCAL Base-Unit (HBU):

- typical HBU: 12 x 12 tiles (36 x 36 cm²)
- Tiles and Electronics together on a PCB

Mechanical Constraints

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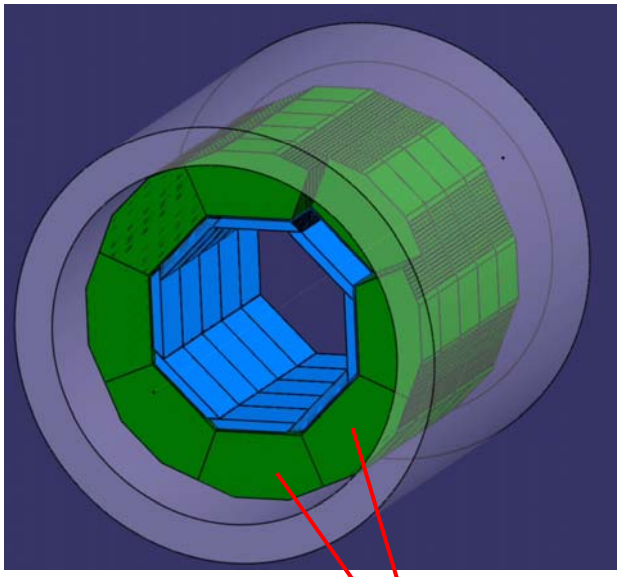

HCAL: 2 x 8 Sectors
2,432,000 Tiles

Requirements for a HCAL Base-Unit (HBU) from the Barrel's mechanics:

-As large as possible (assembly time)

-As thin as possible (barrel diameter)

-Easy de-/installation of single units (repair)

-Rail System needed (Sector walls ?)

-Minimize dead area

Tiles in the HBU

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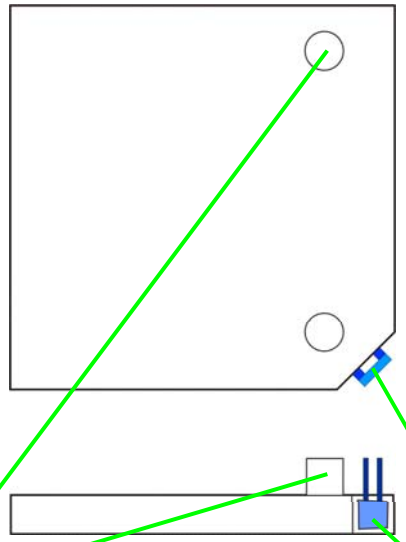
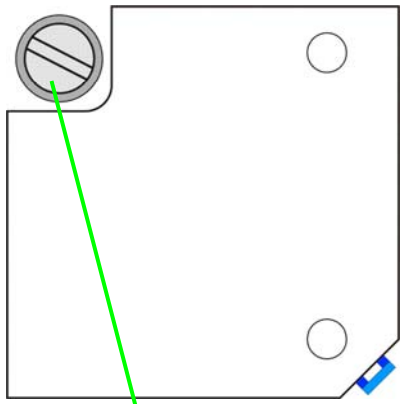
Standard Tile:
30 x 30 x 3 mm³



Tile Alignment Pins
(integration to HBU)

SiPM Carrier

Mechanics Tile:
HBU interconnection and HBU module setup



Minimum:
8 of 144 tiles
in a HBU

6mm bolt with
M3 thread inside

See last talk from Mikhail Danilov (ITEP)

HBU – How could it look like ?

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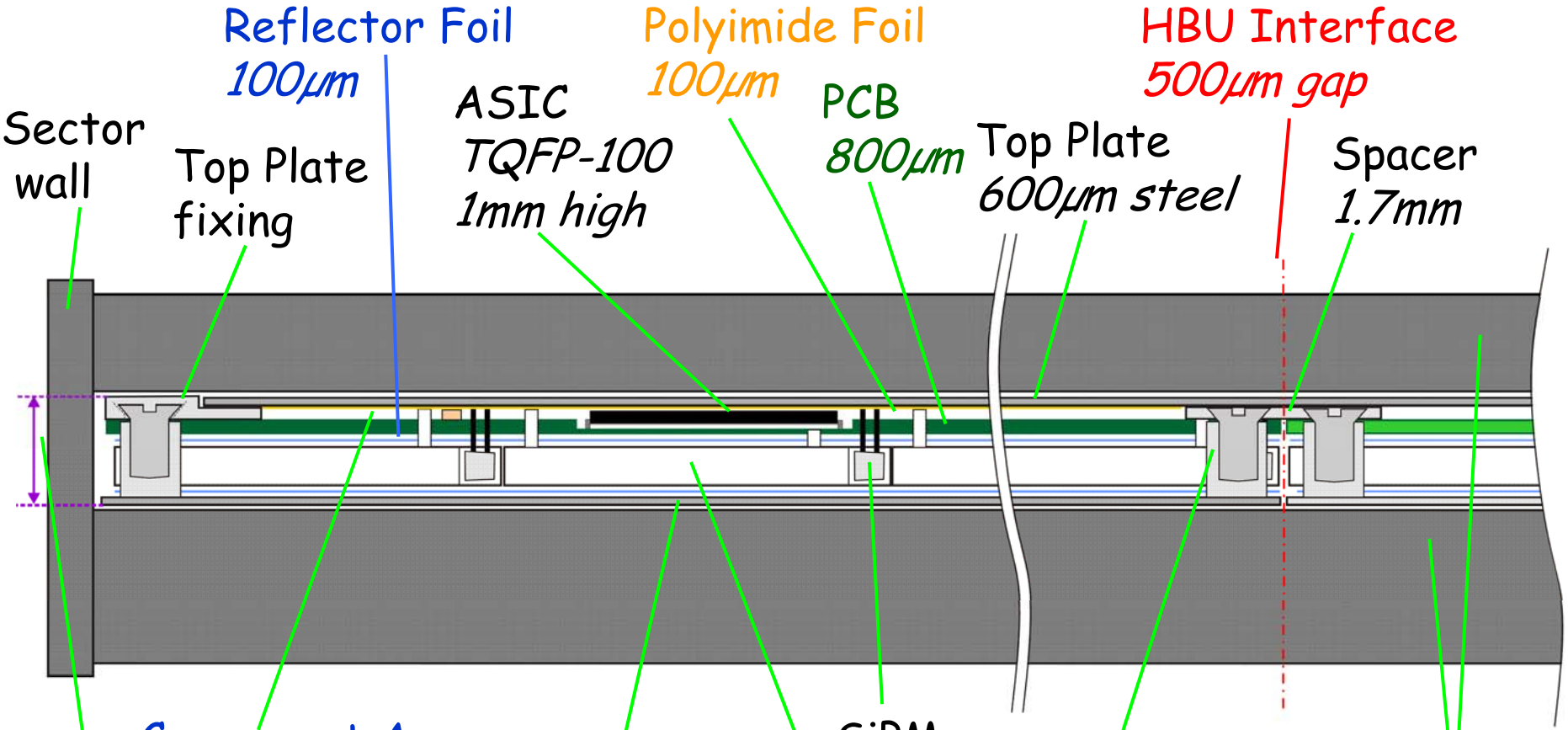

HBU PCB – Layer Structure

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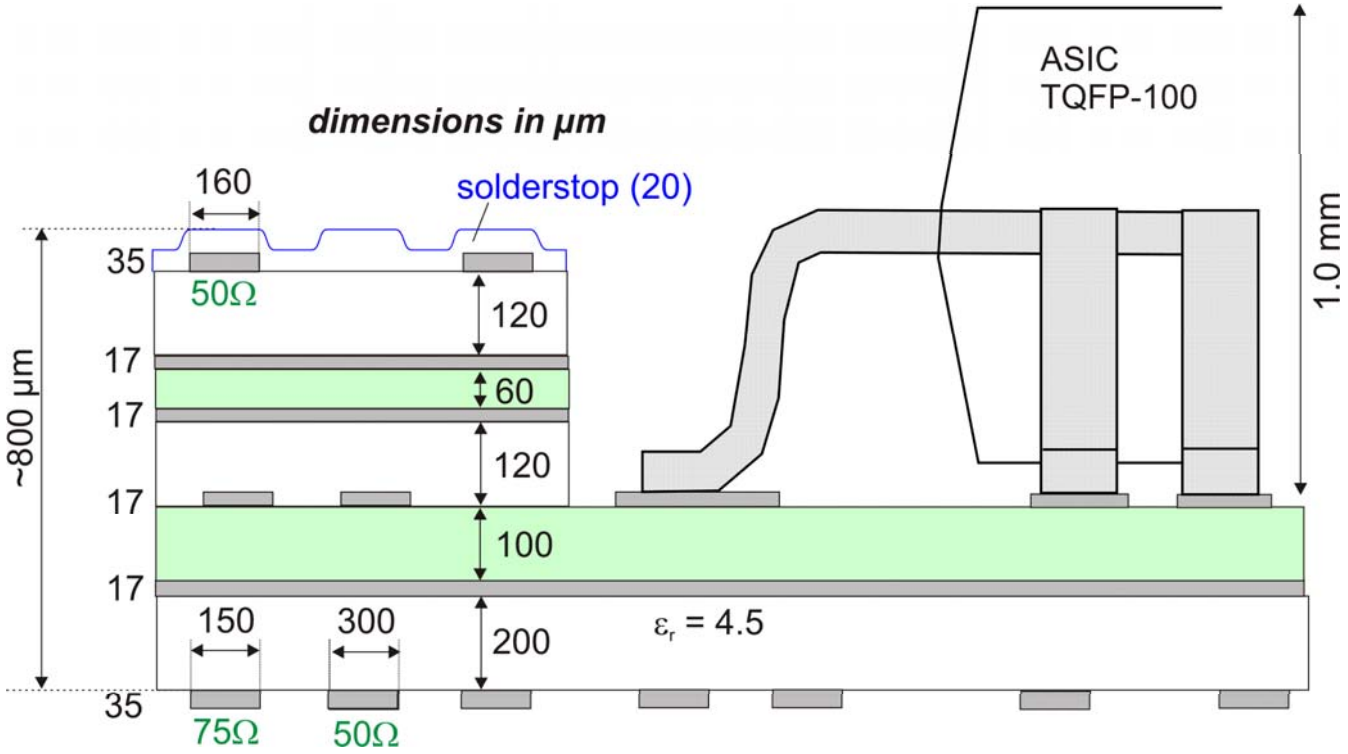
-6 layer design with cut-outs for ASICS and connectors
-75Ω Lines for high-gain SiPM setup
-Two signal layers for impedance-controlled routing
-**Total height (PCB + components): 1.5mm**
-Feasibility / Cost-factor under investigation



SPIROC – SiPM Readout ASIC

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New ASIC, optimized for SiPM readout (L. Raux et al., LAL):

Analog Part:
-36 SiPM input channels with 16-stage analogue memory
-Variable gain (2x), dynamic range 1-2000 photo-electrons
-Variable shaping time, 50-100ns

Digital Part:
-Auto Trigger (threshold 1/2 photo-electrons, adjustable)
-Time measurement (since last bunch crossing): 12-bit TDC
-12-bit ADC and SRAM on-chip

-25μW per channel (power pulsing)

Submission in June 2007

See next talk from Christophe DE LA TAILLE (LAL)

Temperature / Power Dissipation

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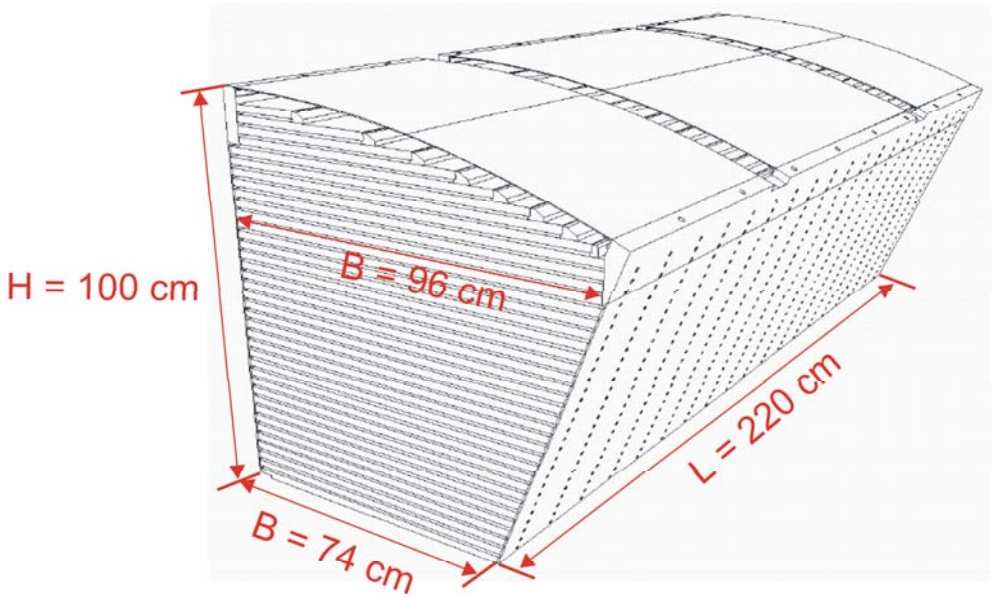
From P. Göttlicher (DESY)



No. channels: 1100 / m^2

Pow. Diss.: 40μW / channel
(25μW ASIC, 15μW HV,
3A / layer during bunch train)

Time constant of heat effects:
α = **6 days**

Temperature at far end (ΔT):
$\Delta T \approx 0.3$ °C

Power pulsing and a good thermal connection (cooling) enables a stable operation!

DAQ - Interface

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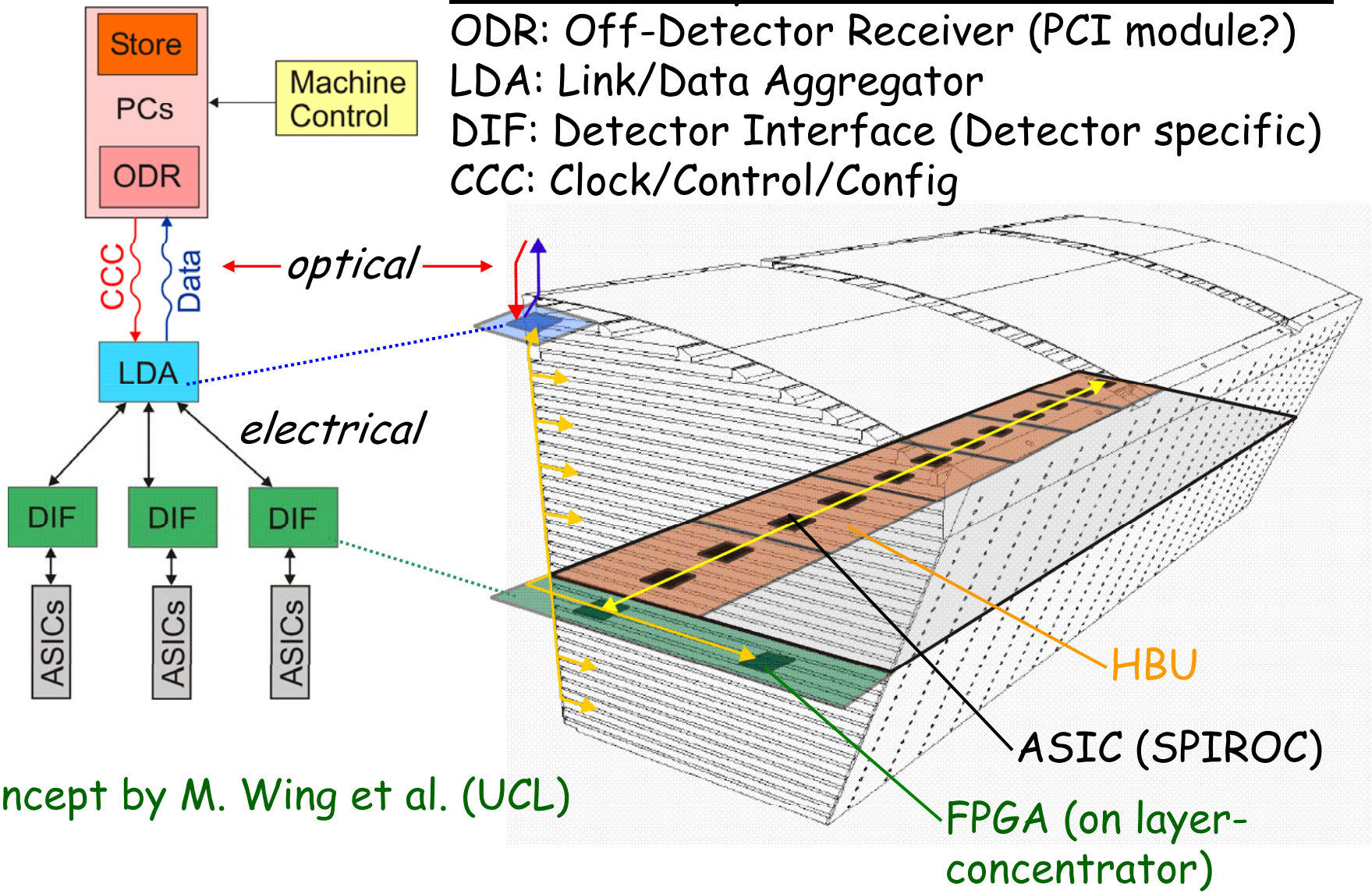
Versatile Setup (similar for ECAL and HCAL):
ODR: Off-Detector Receiver (PCI module?)
LDA: Link/Data Aggregator
DIF: Detector Interface (Detector specific)
CCC: Clock/Control/Config



Concept by M. Wing et al. (UCL)

Light Calibration System (LCS)

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For single photon peaks (incl. losses):

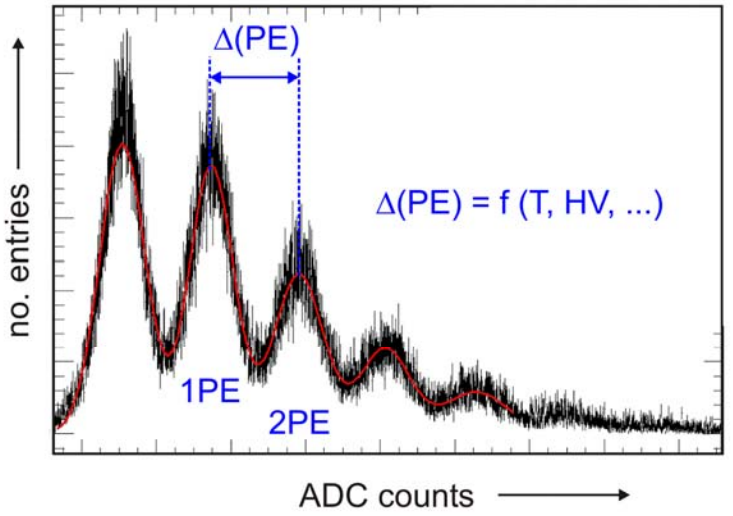
$$P_{opt} \approx 100nW$$

SiPM response strongly depends on temperature and bias voltage.

LCS (based on UV LEDs) needed for:

-Calibration (ADC counts per PE)

-Gain Monitoring



Different options under consideration:

-One LED per tile, integration into HBU => no fibers

-One LED per HBU => no fibers between modules

-LED outside HCAL gap (on DIF) => no electr. crosstalk to SiPM

Concept evaluation together with our colleagues from Prague!

Testboard I : LED

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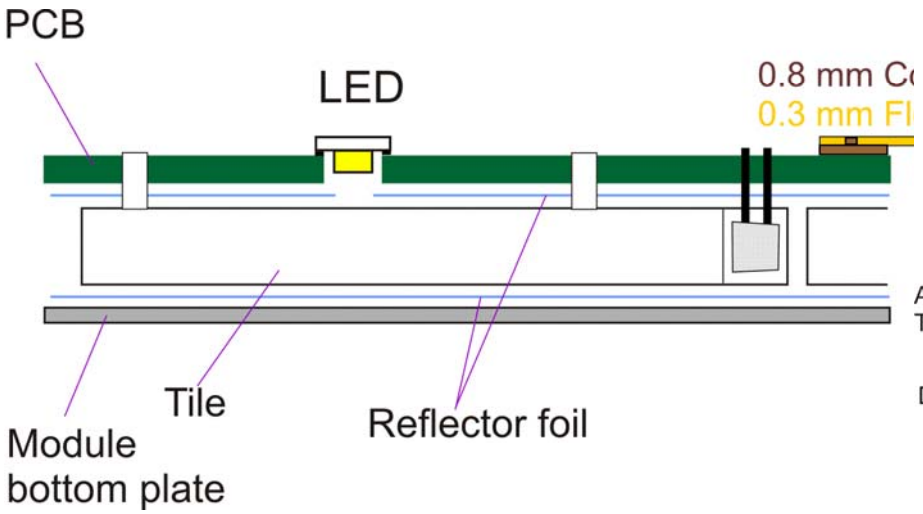
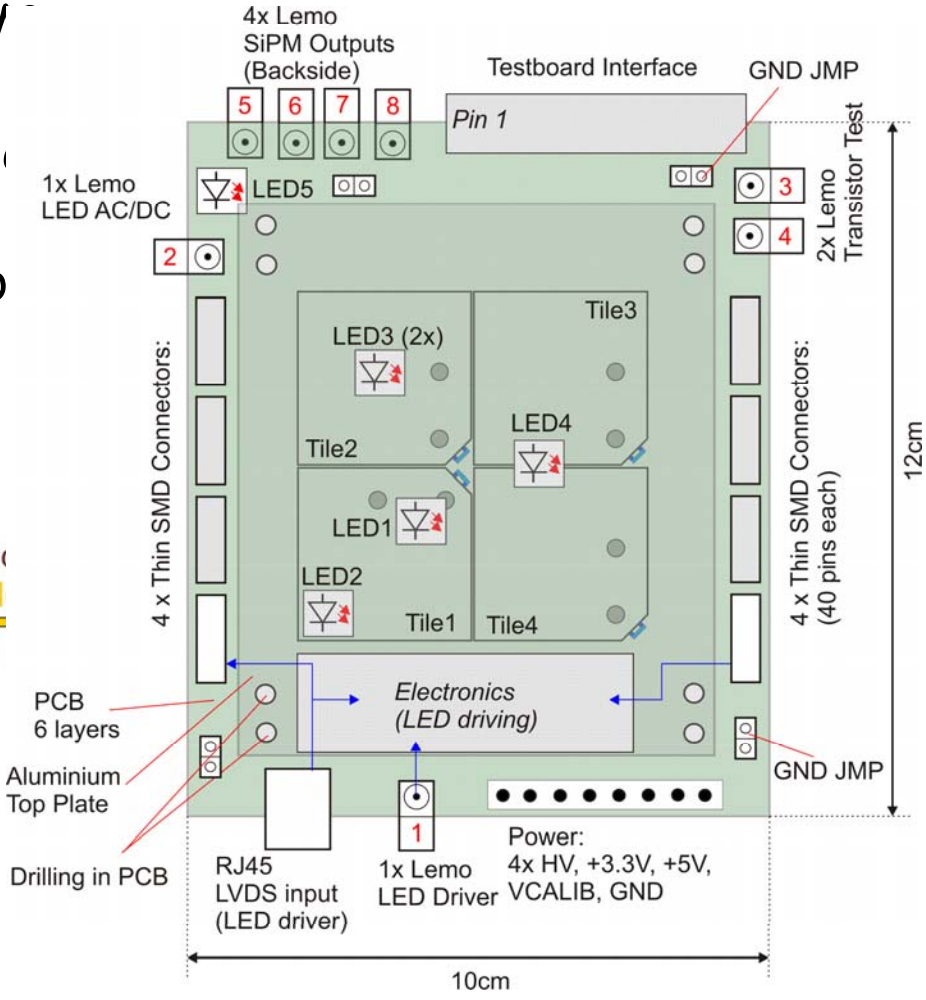
Test LED integration into HBU (LCS):

-Crosstalk of driving circuit to SiPM

-Integration to PCB / coupling to til

-Connector test: stability, number o
connection-cycles?





Testboard II : ASIC + Integration

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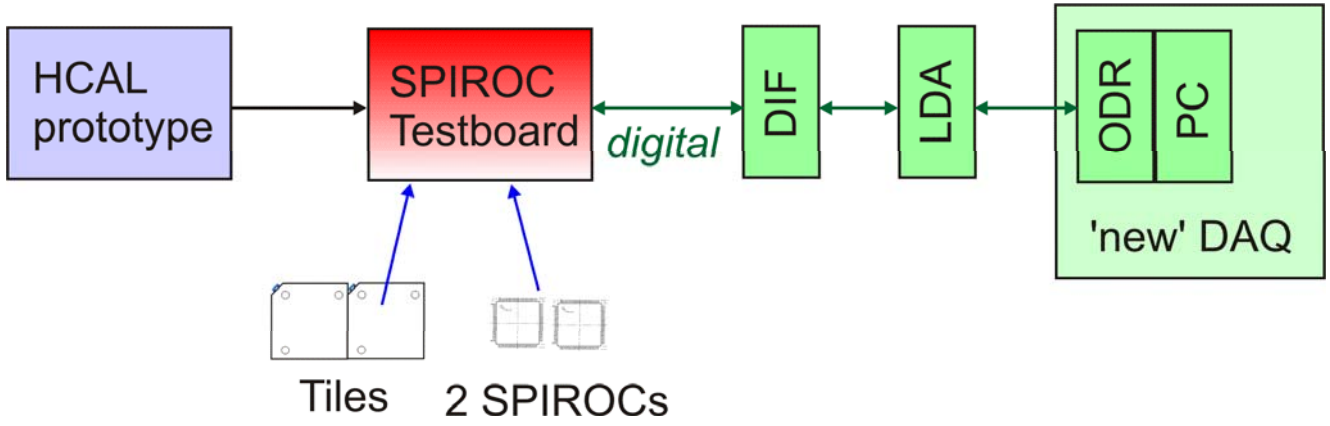
SPIROC Testboard (HBU prototype):

-Assembly (Tiles, PCB, ASICs, LEDs), Cassette Construction
-Performance in the dense HBU setup:
  Noise, gain, crosstalk, power and signal integrity
-DAQ Interface
-LCS with LEDs on board.

Timescale for the first DAQ prototype is under discussion (coupling to the analogue interface of the current DAQ?)



Testboard III : Power-System

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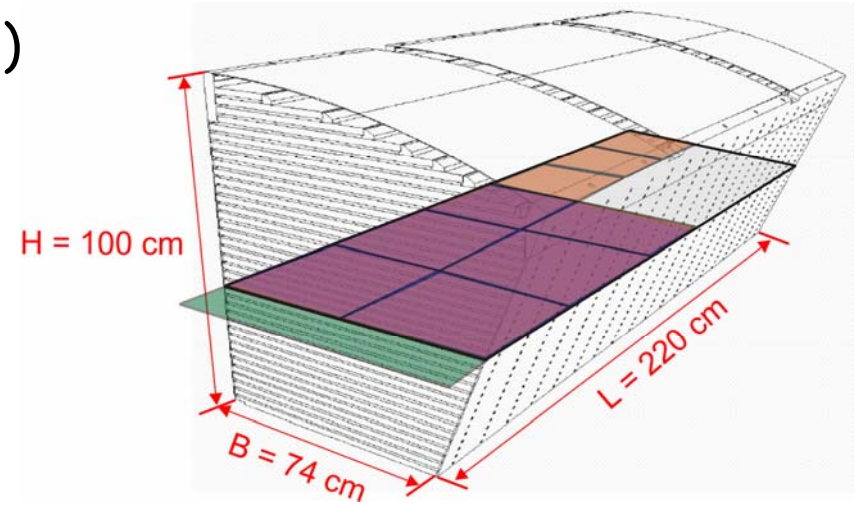
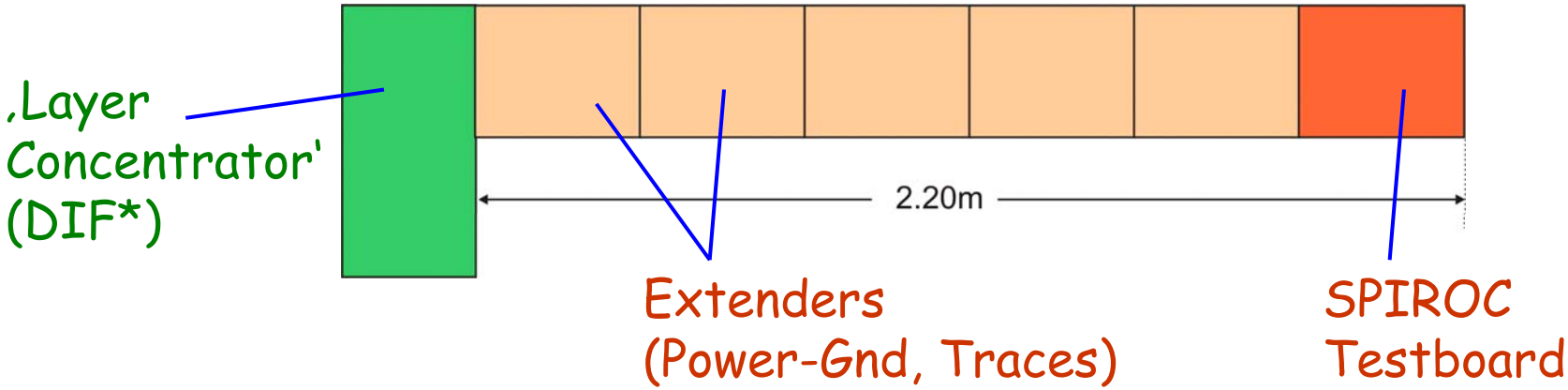
Test Power-Ground System (2.20m)

-Oscillations when switching?

-Voltage drop, signal integrity
(traces, connectors)?

-SPIROC performance @ far end
(blocking caps sufficient)?





Conclusion

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-First ideas about the next generation AHCAL develop to a promising concept.

-Feasibility of many design aspects (e.g. PCB structure) have to be proved.

-Testboard Design I (LCS) under development (PCB order mid June 07).
-Testboard II (HBU prototype) design starts in winter 2007.
-Testboard III (power plane test) runs in parallel (beginning of 2008).