DAQ Summary

Daniel Haas
DPNC Genève

LCWS Hamburg

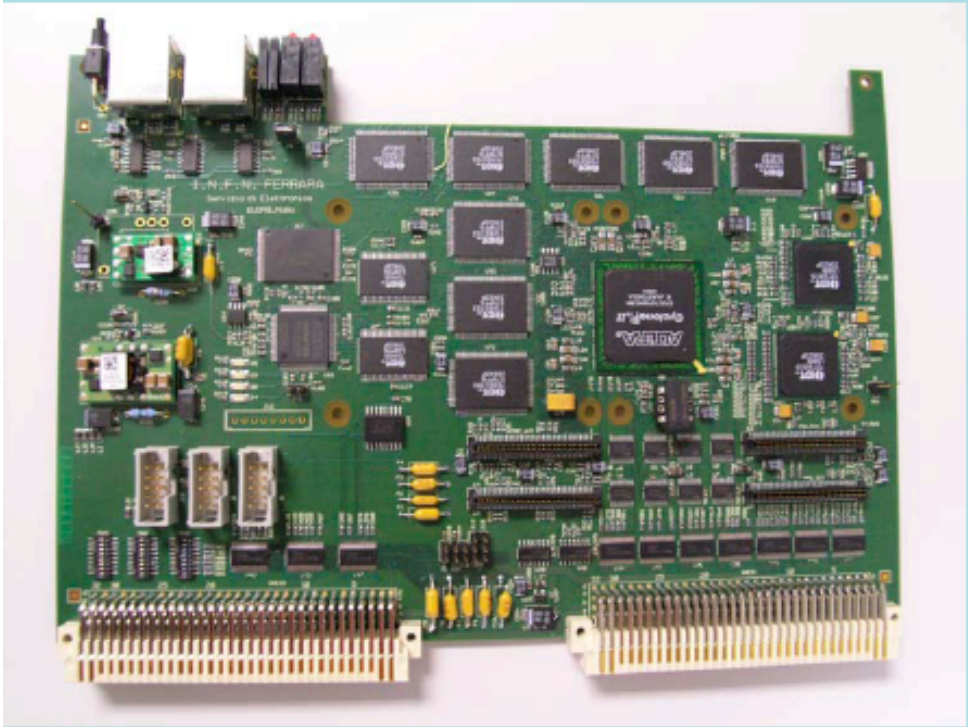
Outline

- Testbeam efforts
- ATCA
- Future needs for the ILC
- Conclusions

Testbeam Efforts

- 3 groups presented ongoing work:
  - Pixel telescope
  - Calorimeters
  - TPC
- All groups will have testbeams this year, so DAQ must first be functional/practical
- Harmonization is on the list, but not (yet) 1st priority

A VME64x/USB2.0-based DAQ card for MAPS sensors



mother board built around an ALTERA CycloneII FPGA (clock rate: 80MHz) and hosting the core resources and Interfaces (VME64X slave, USB2.0, EUDET trigger bus)

NIOS II, 32 bit "soft" microcontroller (clock rate: 40Mz) implemented in the FPGA for

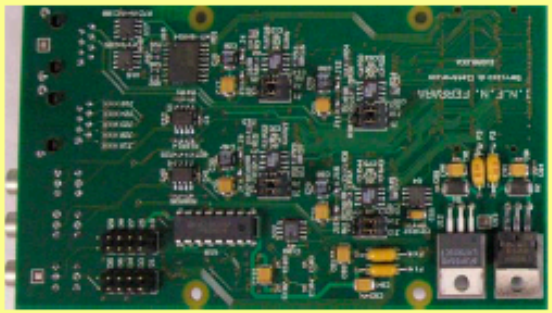
- on board diagnostics
- on-line calculation of pixel pedestal and noise
- remote configuration of the FPGA via RS-232, VME, USB2.0

Two readout modes:

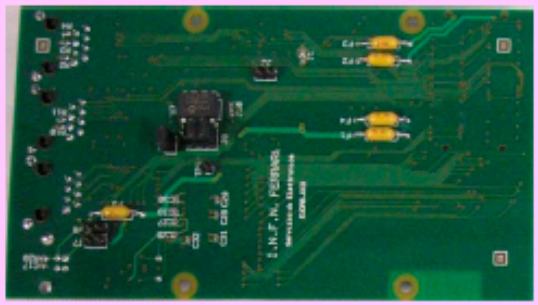
Zero Suppressed readout to minimize the readout dead-time while in normal data taking.

Non Zero Suppressed readout of multiple frames for debugging or off-line pedestal and noise calculations

analog daughter card based on the successful LEPSI and SUCIMA designs clock rate up to 20 MHz

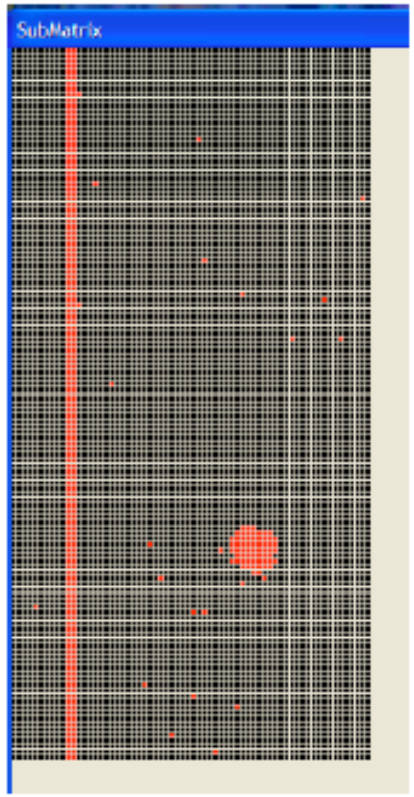


digital daughter card drives/receives control signals for the detectors and features a USB 2.0 link

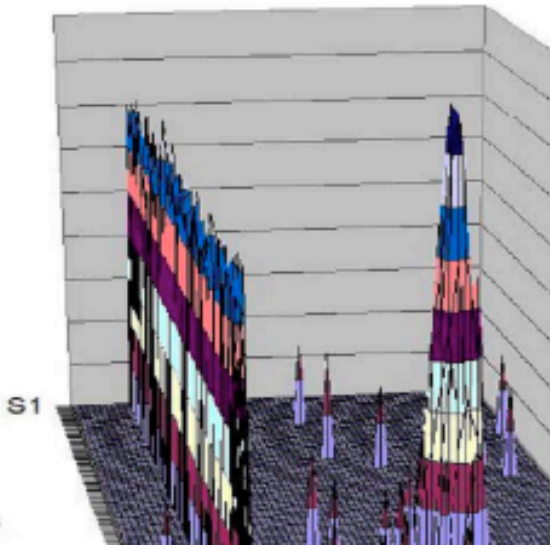


Laser beam results: on board ZS

- The image is obtained by plotting the data from a single laser event captured by the EUDRB in Zero Suppressed mode.
- The EUDRB is configured with ZS threshold=8 for each pixel and ZS pedestal=0 for each pixel except the 10th and 11th of each row (for channel A), for which the ZS pedestal=31.
- Thus in the ZS event captured one can see the “confidence” pattern of pixels 10th and 11th of each row above threshold and then, of course, the signal from the laser pulse.



TestPattern and LaserSpot acquired in Z

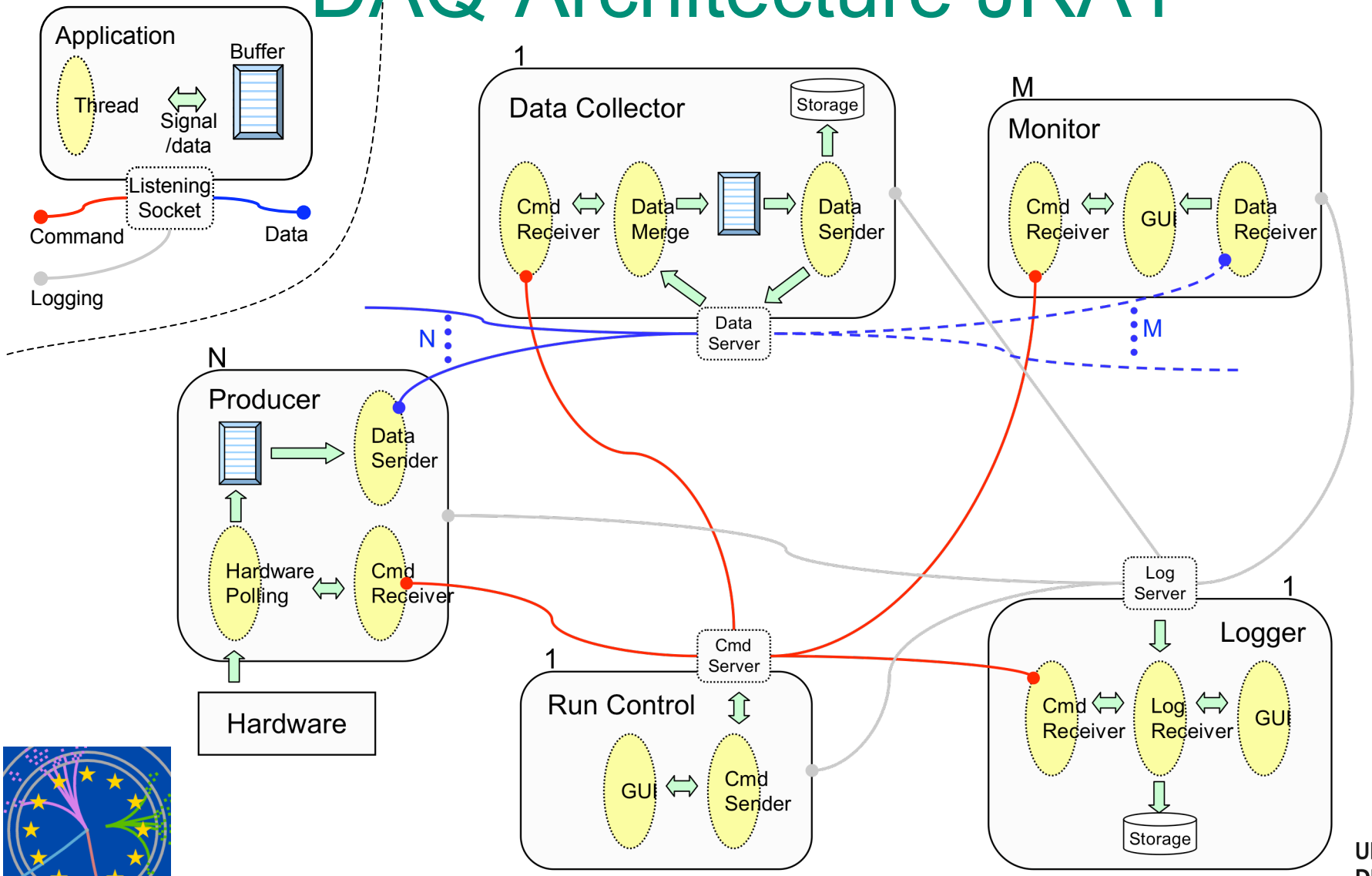


SubFrame A: columns

TLU

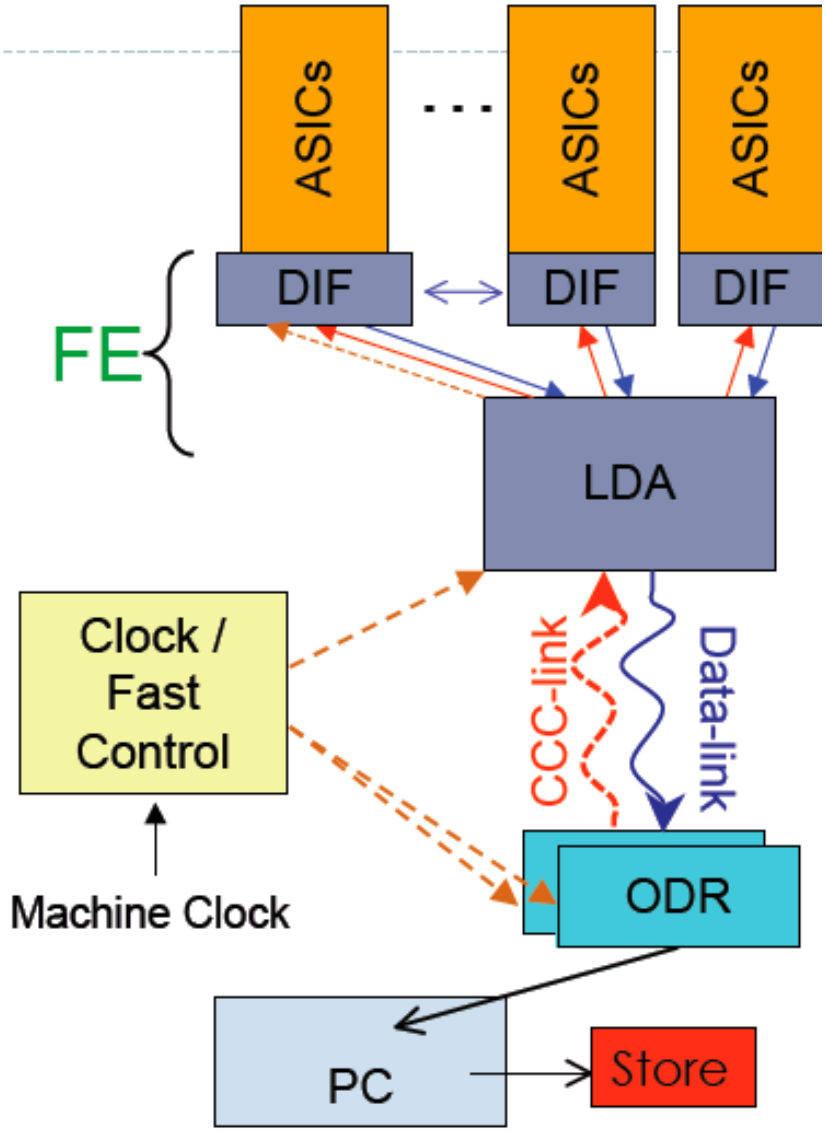
- Simple Handshake via Trigger/Busy/Reset on RJ45 LVDS lines (or TTL-Lemo)
- Discriminator daughter boards
- Timestamp and event-number via USB
- Eventnumber via advanced data handshake on RJ45 available
- Used for Pixel Telescope
- TPC, Calo and SiTra groups interested (some modifications necessary/ongoing)

DAQ-Architecture JRA1



Current Architecture

- DIF
  - Sub-detector specific component (Detector InterFace)
  - Supplied with low jitter clock from first-stage concentrator (LDA)
    - 50MHz with ½ns jitter
    - All detector-specific clocks are derived from input master clock on the DIF
  - Bi-directional serial links to LDA
    - Would like these to be "generic" – driven by highest bandwidth requirement
    - Require fixed latency links if clock and control encoded across them
  - Clock feed through and redundant data links to neighbouring DIF for readout and clock redundancy
  - Standard firmware to talk to DAQ



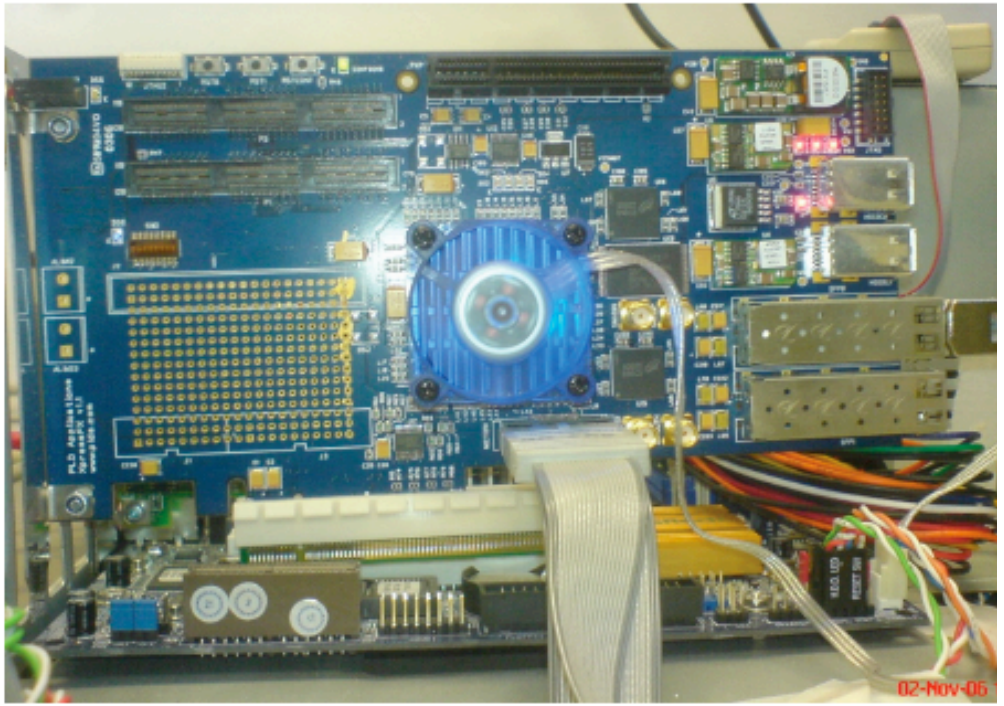
MANCHESTER 1824

The University of Manchester

CALICE Calorimeter for ILC

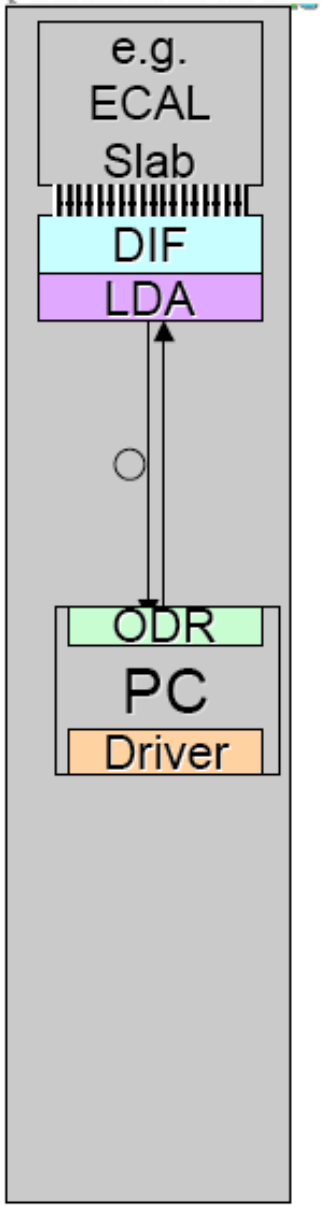
Prototype ODR

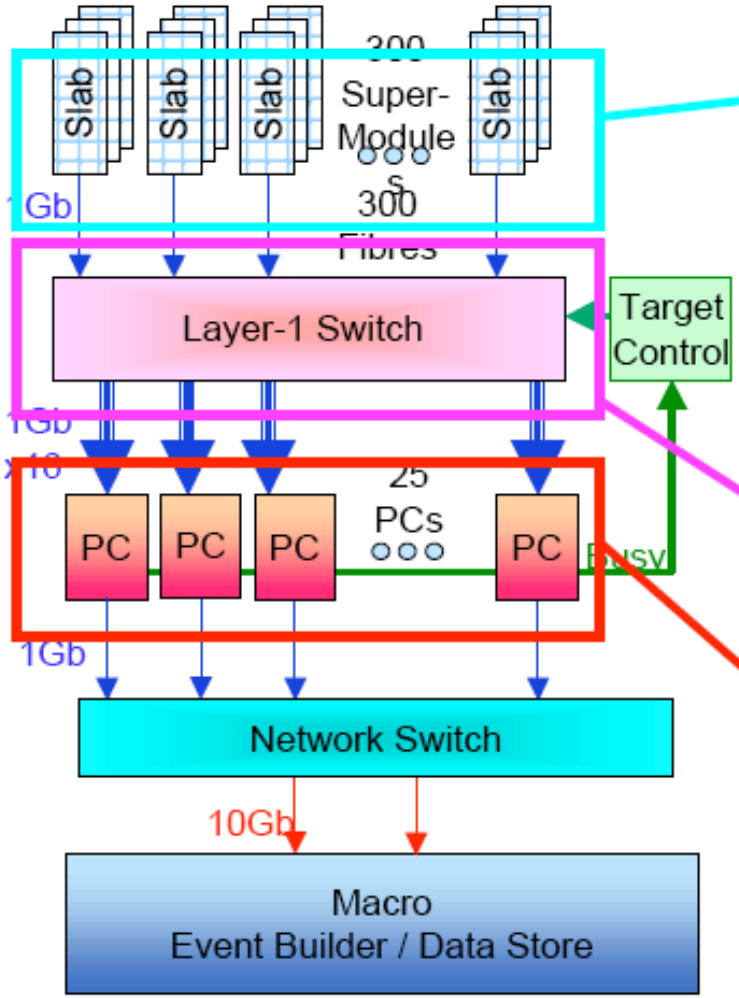
- Development board from PLDApplications
  - 8 lane PCI-e card
  - Xilinx Virtex4FX60 FPGA
  - DDR2 memory
  - 2 SFP cages – 1GigE
  - 2 HSSDC connectors
  - Can drive/receive 1Gbit Ethernet direct to FPGA on the board
  - 10Gbit possible with addition of small daughter card
- Will also be able to test some LDA functionality using on-board LVDS outputs

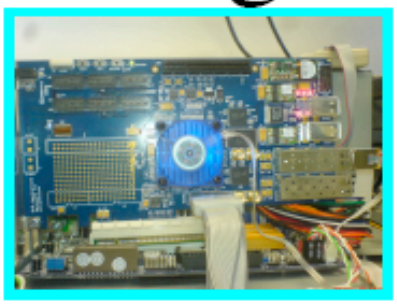


Demonstrated 1Gbit Ethernet operation from this board - See proceedings of IEEE NPSS Real Time Conference 2007 for details

options for network / switching





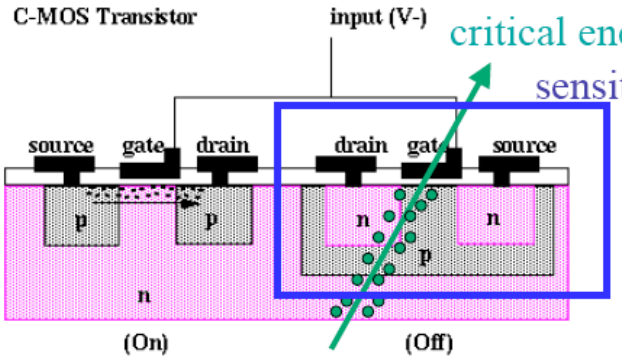


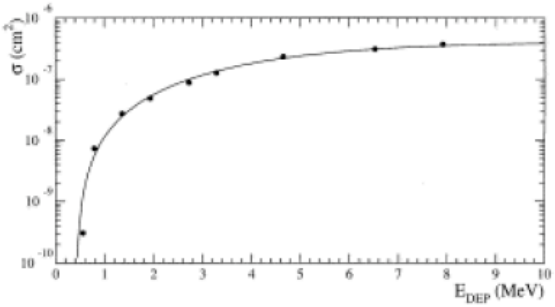
working FPGA based Ethernet system, using RAW frames

optical switch delivered

high (>9GBits) bandwidth usage using PCIe 10Gig cards (from Myricom

SEU principle





from E. Normand, Extensions of the Burst Generation Rate Method for Wider Application to p/n induced SEEs

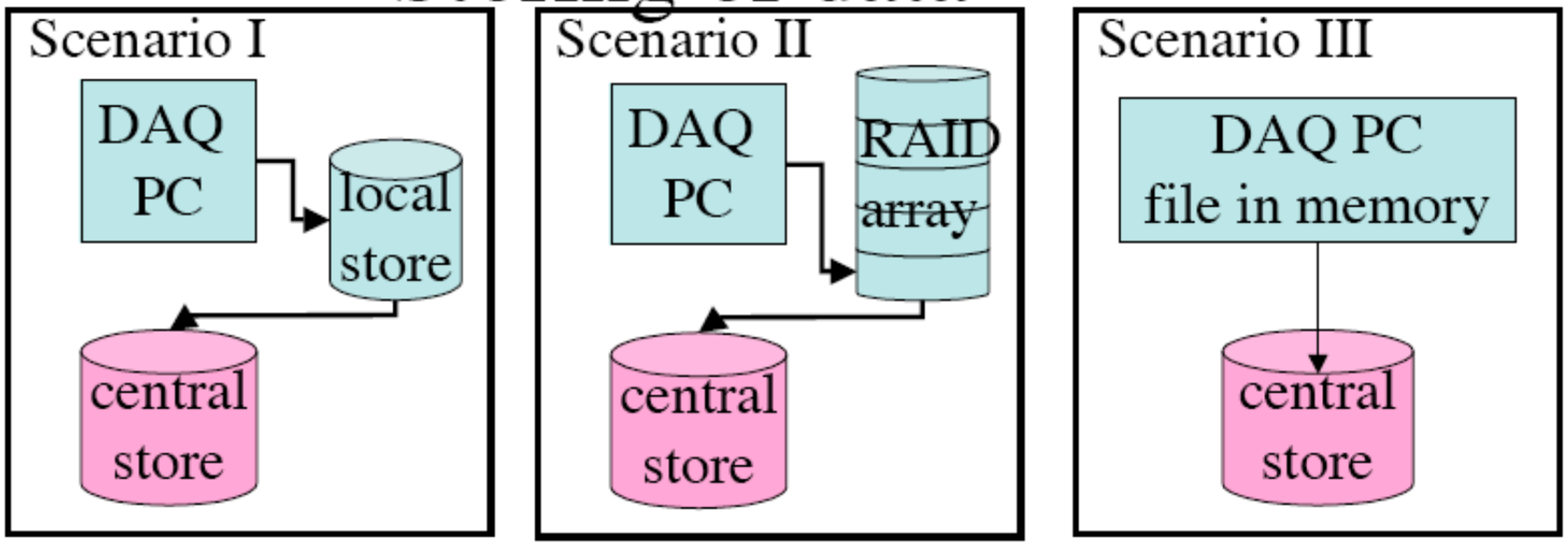
=> look for neutrons, protons and pions depositing energy in the FPGAs

	shold eV]	SEU σ [cm²/device]	SEUs/day
Virtex II X-2V100 & Virtex II X-2V6000	5MeV	$8*10^{-9}$	0.17
Altera Stratix	10MeV	10^{-7}	1.99
Xilinx XC4036XLA	20MeV	$3*10^{-9}$	0.02
Virtex XQVR300	10MeV	$2*10^{-8}$	0.38
9804RP	20MeV	10^{-8}	0.17

all data from literature, references not given in talk

⇒ looks like FPGAs need to be reconfigured once a day
⇒ before operation radiation tests need to be done with FPGAs chosen for experiment

DAQ software for EUDET: Storing of data

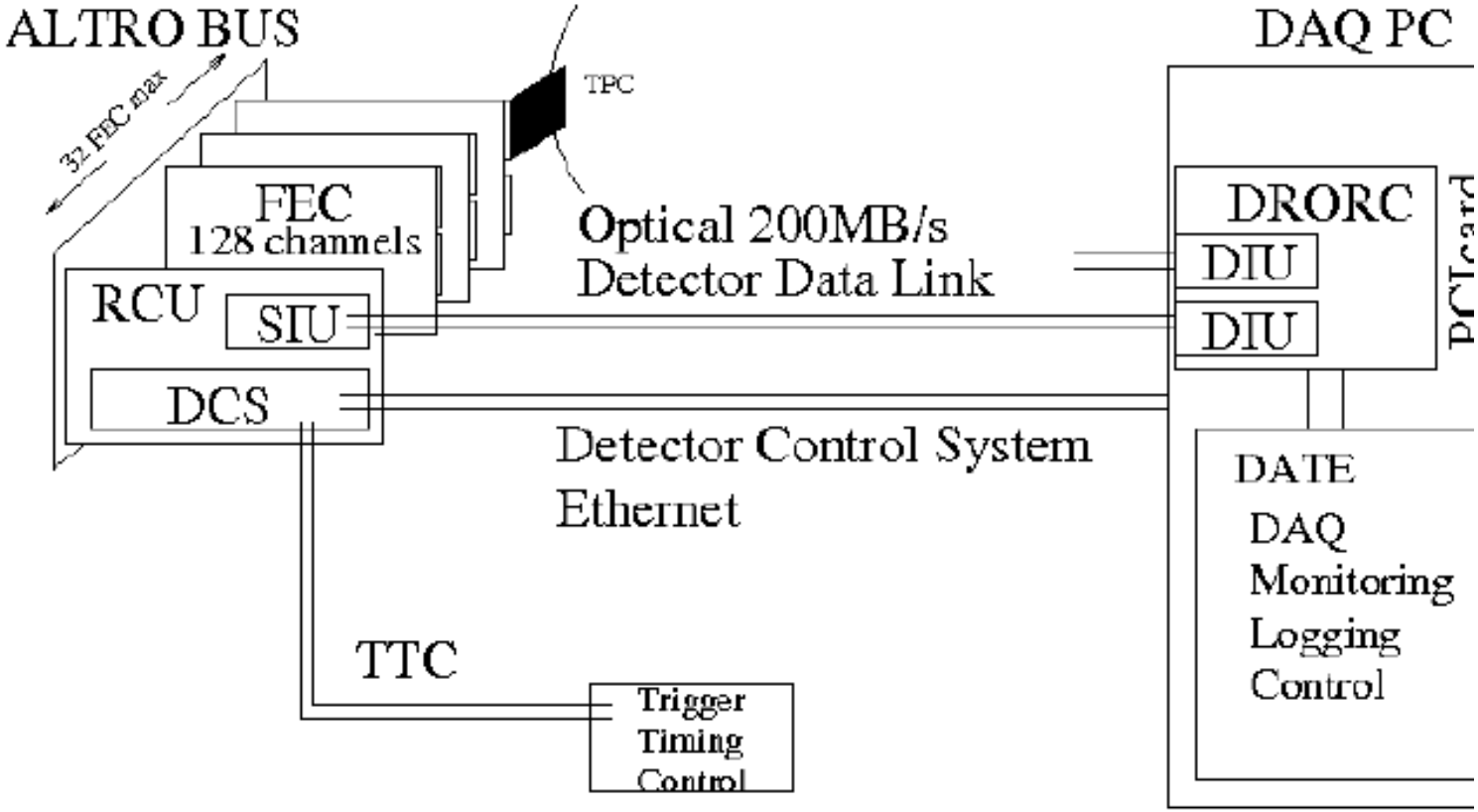


- which scenario to choose depending on the bandwidth with which the data gets produced: (I) up to 200Mbit/sec, (II) up to ~1600Mbit/sec, (III) from there on
- desirable to have files because transfer is easier and in case of timing problems error handling is easier, but keep system flexible for now
- worst case estimate (very rough):

30layers*100cm*100cm*2kB memory @ each ASIC/72 no of channel @ ASICS = 10MB/bunch train = 400Mbit/sec

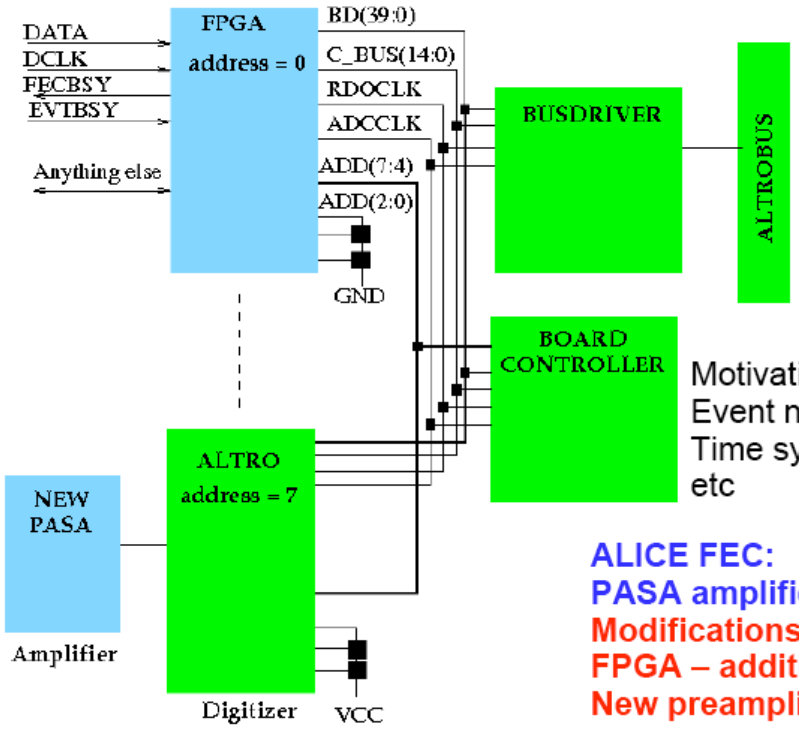
Based on the ALICE TPC readout

Front End Card (FEC), modified for new amplifier
Readout Control Unit (RCU), Source Interface Unit (SIU)
ReadOut Receiver Card (DRORC), Destination Interface Unit (DIU)
ALICE Data Acquisition and Test Environment (DATE)
Trigger Timing Control (TTC)



EUDET: 1 RCU
10000 ch: 4 RCU
possible to distribute 1 RCU system

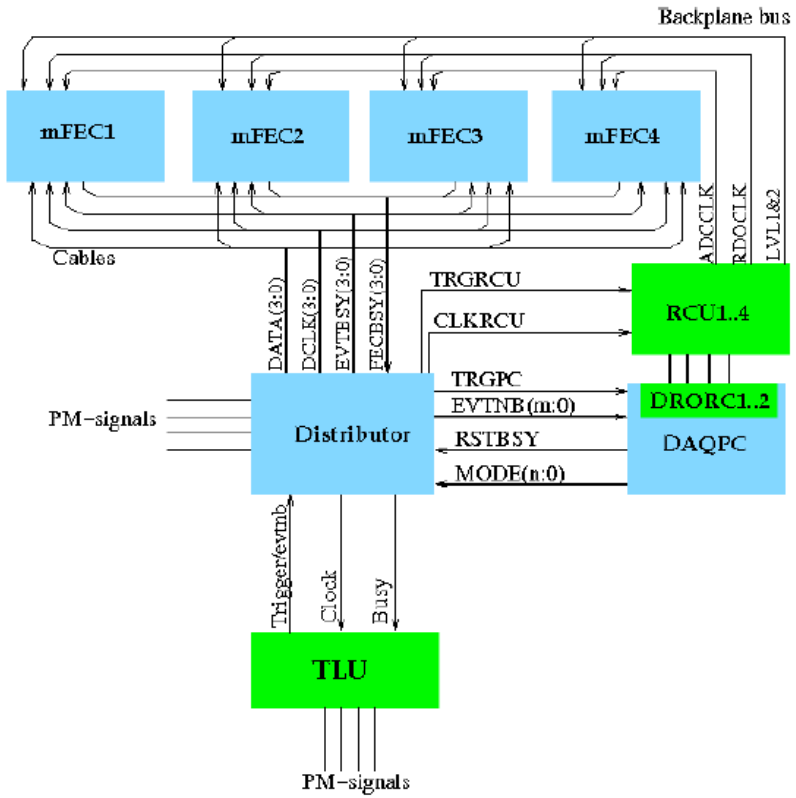
Modified Front End Card (mFEC)



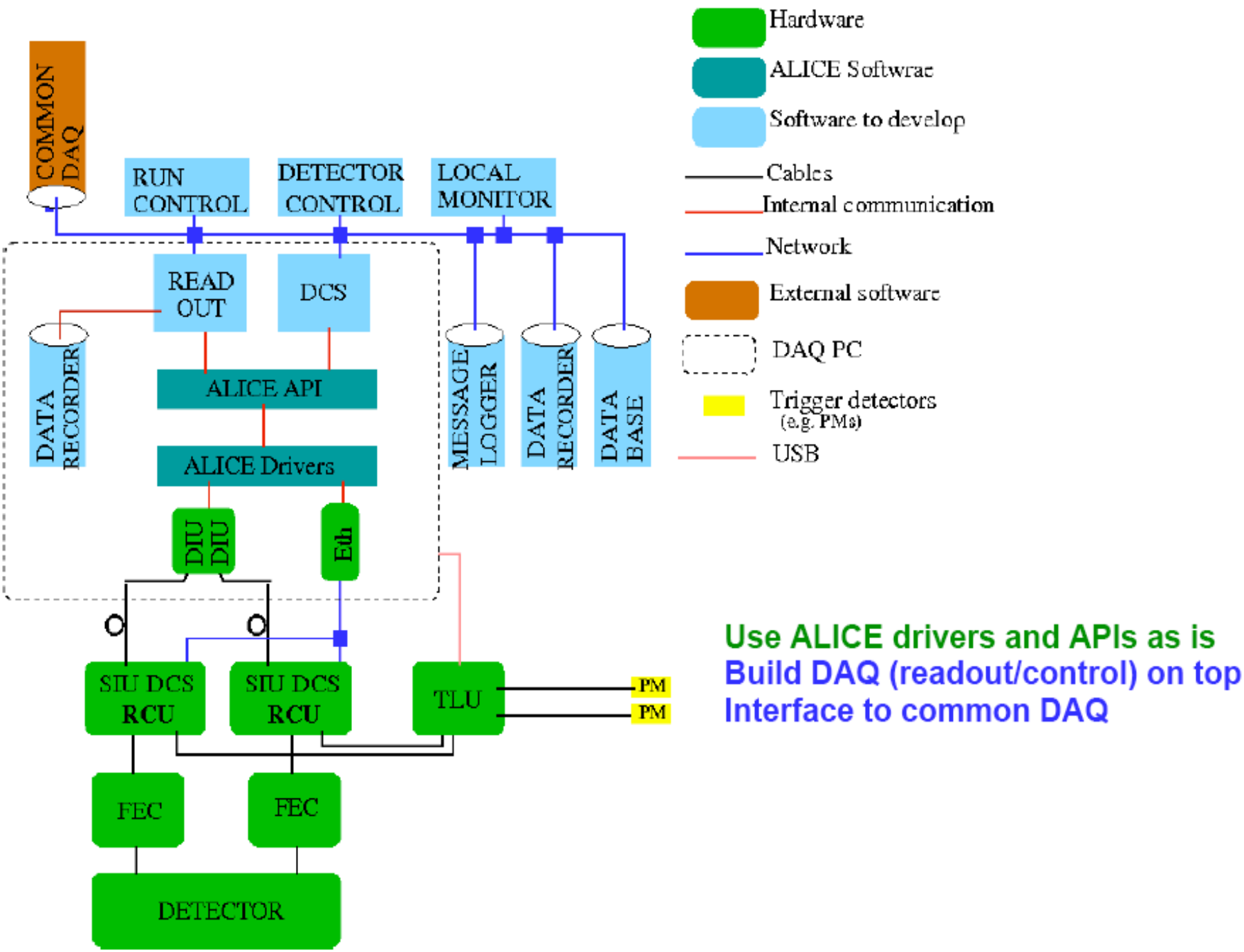
Motivations:
Event number into data stream
Time synchroniztion with other systems
etc

ALICE FEC:
PASA amplifier & ALT
Modifications:
FPGA – additional dat
New preamplifier

Proposed Trigger Timing Control



- Get trigger from central Trigger Logic Unit
- Distribute trigger/data to mFEC & RCUs
- Distribute 40MHZ clock to RCUs
- Require: trigger timing accuracy < 1ns



Use ALICE drivers and APIs as is
Build DAQ (readout/control) on top
Interface to common DAQ

ILC Detector Testbeam Workshop - IDTB 07

- Workshop: 17/1/07 – 19/1/07 at Fermilab

- Aim of the workshop
  Overview on status of the activities of the various R&D groups/collab
  for the ILC
  Overview on tentative sites for testbeam measurements with
  some focus on Fermilab facilities
  Identify the future needs of these activities and outline a Roadmap

- ~120 participants from all areas of detector R&D in
  discussion with maintainers and leaders of
  the potential test facilities

- Starting gun for the write-up of a roadmap document

- Common DAQ hardware and software
- Common online and offline software
  - Reconstruction and analysis software

CALICE Testbeam Data Taking

CALICE collaboration is performing large scale testbeams

Testbeam program poses software "challenges"

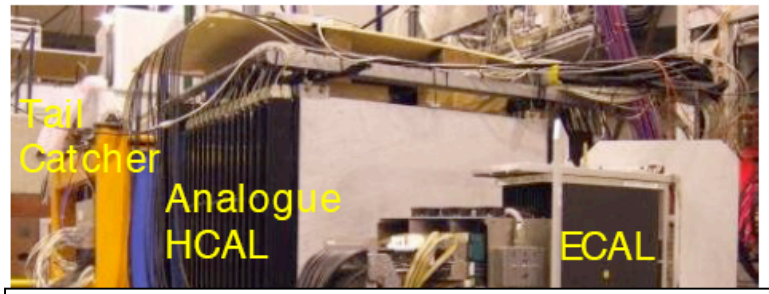
- Data processing from Raw Data to final Clusters in user coherent way

- Handling of Conditions Data Detector Configuration Calibration, Alignment etc.

-Comparison with simulated data
'Physics' Output

O(15000) calorimeter cells readout by Calice DAQ
No Zero Suppression
r/o speed 5 Mbyte/s continously

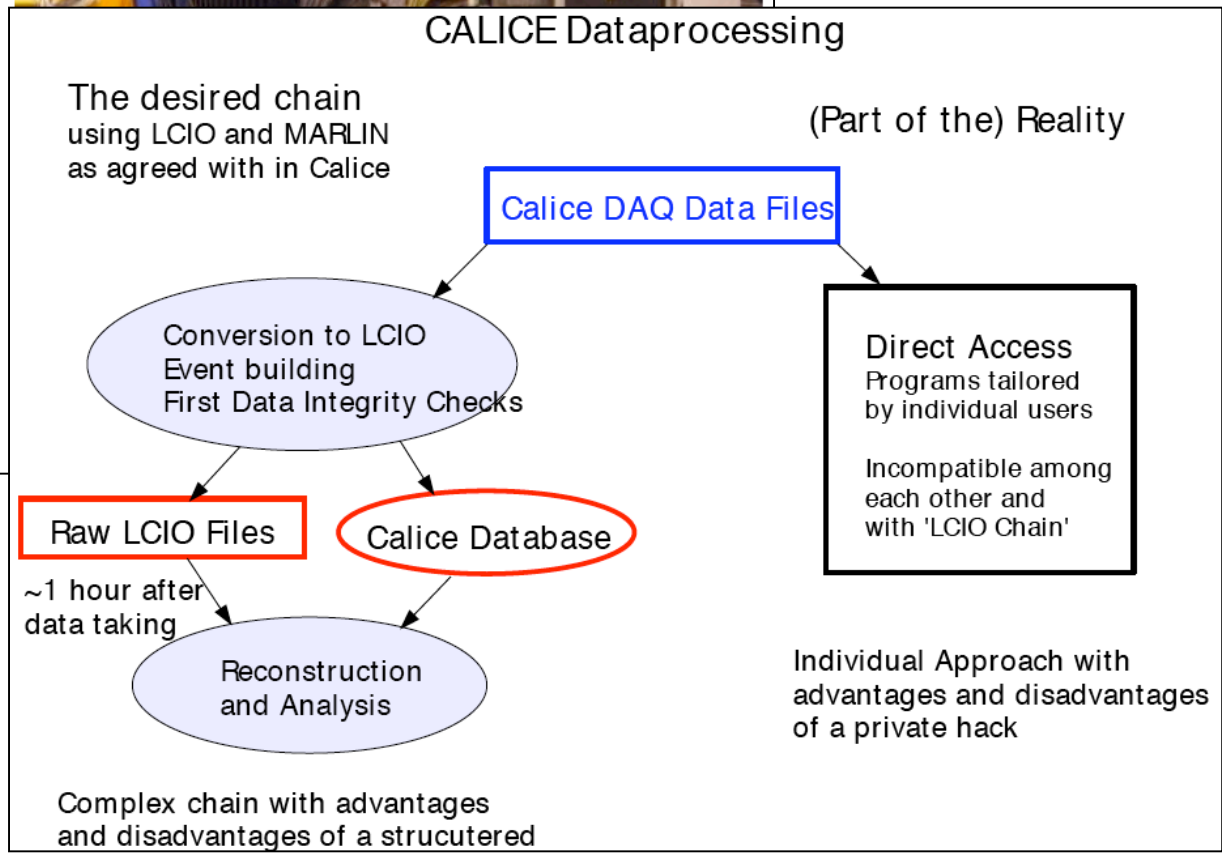
Testbeam Setup at CERN



CALICE Dataprocessing

The desired chain
using LCIO and MARLIN
as agreed with in Calice

(Part of the) Reality



DAQ requirements for LCIO

- in order to further design and develop new features in LCIO it is important that
  - the requirements from the DAQ systems are well known:
    - expected/needed I/O performance
    - data structure – class layout
      - is the data restructered defore written to file is the structure defined by the readout electronics ?
    - will there be an event builder that collects raw data (in non LCIO format?) from the various subdetecto assembles the LCIO event ?
    - if so, will there be an event builder solution all/some DAQ systems ?

LCIO plans

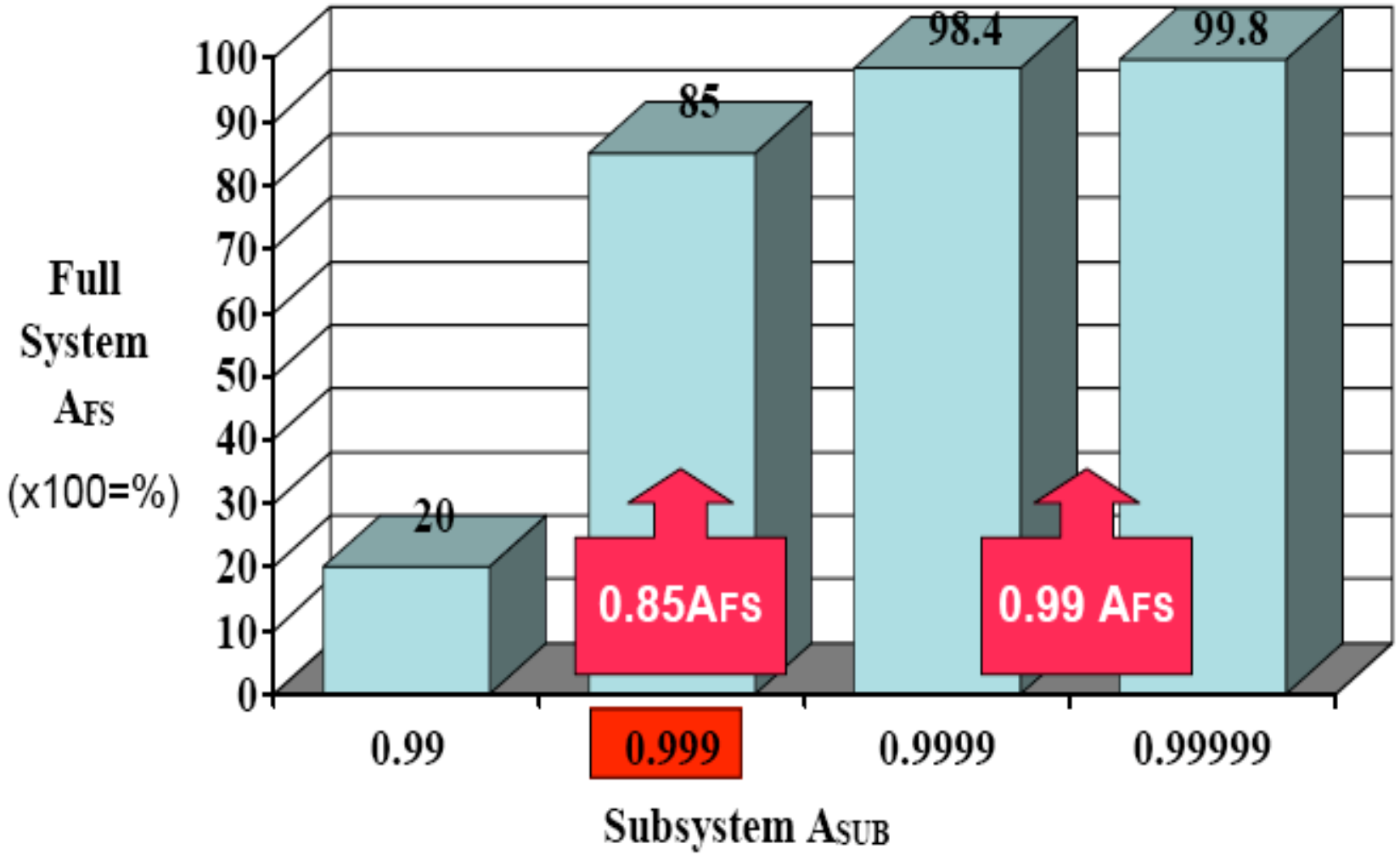
- currently working on a new implementation of the underlying I/O library SIO in C++
- will address these known short comings and provide:
  - direct access
  - split events over several records and files
    - e.g. could write LCIO raw data to one file and processed data (calibrated, zero suppressed,...) to another file
      - users could go back to raw data when needed
  - possibility to read and write user defined classes/records
    - would give DAQ systems flexibility for changes
  - timescale: unclear - depends on manpower situation and needs/requirements of DAQ systems

ATCA

- Ray Larsen presented overview of ATCA (Advanced Telecom Computing Architecture)
- Standards on parallel backplanes are becoming obsolete
- ATCA (currently) only candidate to fullfill our needs
- Interest of ILC, ITER etc for an ATCA-P (Physics) Profile

Required Subsystem Availability A_{SUB} for Full System A_{FS} >0.85 = 0.999 Avg

Comprising 16 Systems, 10 Subsystems each System



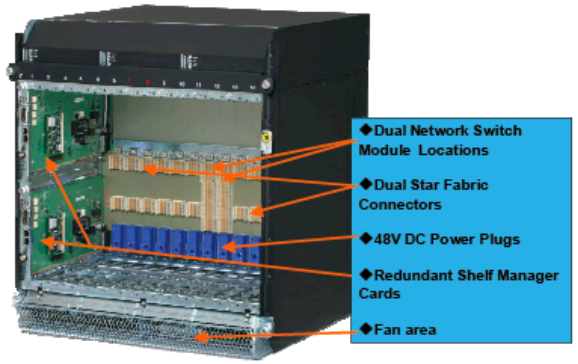
Ref: Larsen & Downing, 2004 IEEE NSS, Rome

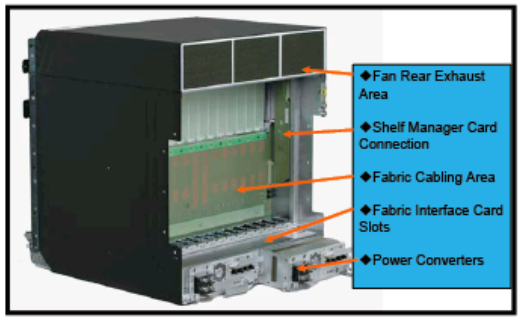
What Can ATCA Provide?

- A system building block of crate (Shelf) and 12-14 modules with vital features:
  - *Dual redundant communications node, processing core w/ auto-failover*
  - *Redundant 48V power supplies, fans*
  - *Serial power feeds to each module, serial I/O, Intelligent Platform Manager (IPM) to diagnose, isolate faulty modules, power or fans*
  - *Once isolated, faulty units can be replaced by technician without interrupt… remaining modules (Hot S…*

2004: Introduction of ATCA*

- Telecom Industry Open Standard
- Driven by $10B/year server and switching market
- *A=0.99999 = Downtime of 5 minutes/year*
- All Gigabit serial Dual Star or Mesh backplane
- Dual controllers, 48V PS, hot swappable,
- 200W/module air cooled, 3+1 Fans hot swappable
- Shelf Manager controls failover, power metering, hot swap





*Advanced Telecom Computing Architecture

ATCA Work In Progress

- Purchased test systems: SLAC, FNAL,ANL, DESY
- Evaluation efforts of core systems underway
- DESY investigating TCA, MicroTCA for XFEL applications
  - *Controls. Protection, Low Level RF*
  - *Must make decisions in ~1y*
- FNAL developing 12 Ch 5(module for BPM's for SRF

Work in Progress 2

- SLAC contracted shelf manager evaluations, development of ATCA VME adapter to University of Illinois (UIUC)
  - *Ability to plug in existing VME instrument cards will make possible configuring test systems much more quickly, gain experience with core systems, software, do real work*
- ANL concentrating on system level 3 tier software, interfacing to EPICS and/or DOOCS
- ILC Controls & instrumentation cost model assumed ATCA as base system; used commercial pricing & applied large quantity learning curves

Future Needs for the ILC

- Data Flow for Pixels (M. Winter)
- Data Flow for Tracking (P. Colas)
- ILC DAQ Issues (P. Le Dû)

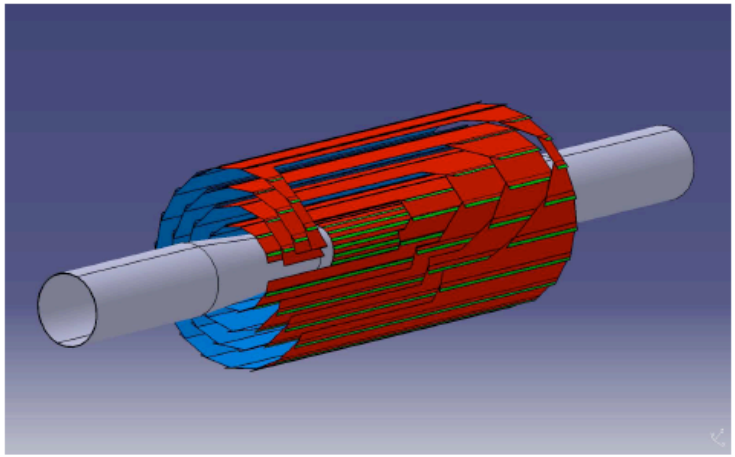
- Dominant source of hits : $e^{\pm}$ from Beamstrahlung

- 1st layer (L0) : $\gtrsim$ 5 hits/cm^2/BX for 4T / 500 GeV / R_0 = 1.5 cm / no safety factor
  $\rightarrowtail \lesssim 1.8 \cdot 10^{12}$ $e^{\pm}$/cm^2/yr (safety factor of 3)
  - 2nd layer: 8 (6 ?) times less
  - 3rd layer: 25 ($<$ 20 ?) times less

Basic Vertex Detector Design features

- Geometry : 5 cylindrical layers (R = 15 – 60 mm), $\|cos\theta\| \leq$ 0.90 – 0.96 (possibly 6 layers)
- L0 and L1 : fast col. // architecture
- L2, L3 and L4 : possibly multi-memory pixel architecture (?)
- Pixel pitch varied from 20 μm (L0) to 40 μm (L4) by 5 μm steps $\rightarrowtail$ minimise P_{diss}

Layer	Radius (mm)	Pitch (μm)	$t_{r.o.}$ (μs)	N_{lad}	N_{pix} (10^6)	P_{diss}^{inst} (W)	P_{diss}^{mean} (W)
L0	15	20	25	20	25	$<$100	$<$5
L1	$\leq$ 25	25	50	$\leq$26	$\leq$ 65	$<$130	$<$7
L2	37	30	$<$200	24	75	$<$100	$<$5
L3	48	35	$<$200	32	70	$<$110	$<$6
L4	60	40	$<$200	40	70	$<$125	$<$6
Total				142	305	$<$565	$<$3–30



- Ultra thin layers: $\lesssim$ 0.2 % X_0/layer (extrapolated from STAR-HFT; 35 μm thick sensors)
- Very low P_{diss}^{mean}: $<<$ 100 W (exact value depends on duty cycle)
- Fake hit rate $\lesssim 10^{-5}$ $\rightarrowtail$ whole detector $\cong$ close to 1 GB/s (mainly from $e^{\pm}_{BS}$)

Vertex Detector Data Flow

- Raw data flow (in absence of any signal):
  - $\triangleq$ L0 : $\sim$ 25 Mpixels read 40 times / train $\cong$ 1 Gpixels / train
  - $\triangleq$ L1 : $\sim$ 50 MPixels read 20 times / train $\cong$ 1 Gpixels / train
  - $\triangleq$ L2 + L3 + L4 : $\lesssim$ 300 Mpixels read $\lesssim$ 10 times /train $\cong$ 3 Gpixels / train

    Total $\cong$ 5 Gpixels / train $\mapsto$ 25 Gpixels / s
  - $\triangleq$ 3 Bytes / pixel ($\leq$ 20 address bits + 5–4 charge bits) $\Rrightarrow$ raw data flow $\cong$ 75 GB / s

Nightmare!

- Signal data size dominated by $e^{\pm}_{BS}$: $\gtrsim 10^3$ hits / BX $\mapsto$ $3 \cdot 10^6$ hits / train
  - $\triangleq$ Assuming 5 pixels / cluster : $15 \cdot 10^6$ pix / train $\mapsto$ 45 MB / train
  - $\triangleq$ Uncertainties on beamstrahlung rate prediction (factor 3 - 5) $\mapsto$ 135–225 MB / train $\Rrightarrow$ 0.7–1.1 GB / s

manageable

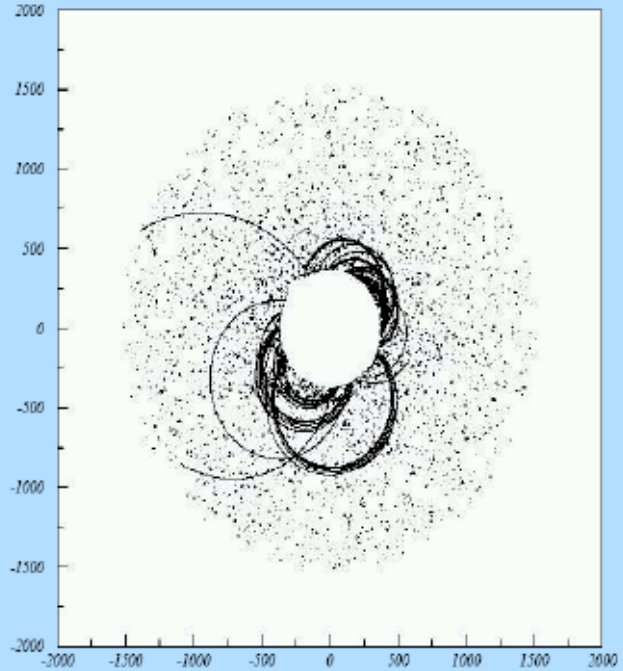
Reminder: Tesla TDR

- Data flow dominated by background
  - O(10^3) photons, few 100 neutrons, 5 electrons from pairs, 0.7 hadrons from minijets, 0.3 halo muons per beam crossing
- Huge uncertainties -> mere order of magnitude possible, or needs detailed case studies : photon and neutron shielding, gas choice, algorithms for data reduction. The Tesla case was a TPC
- 1.2 million channels, 110 Mbytes per train (half of the total detector).

What changed (or should change) since then?

- Machine design (parameters, crossing angle, DID/anti DID)
- At least 3 different technologies for the TPC (GEM with small pads 1x4mm, Micromegas with resistive foil and 2x7mm pads, Digital TPC)
- R&D effort needed to reduce the sensitivity to background (shielding, gas choice). Together with primary ionisation studies starting now.

Mokka hits in the TPC



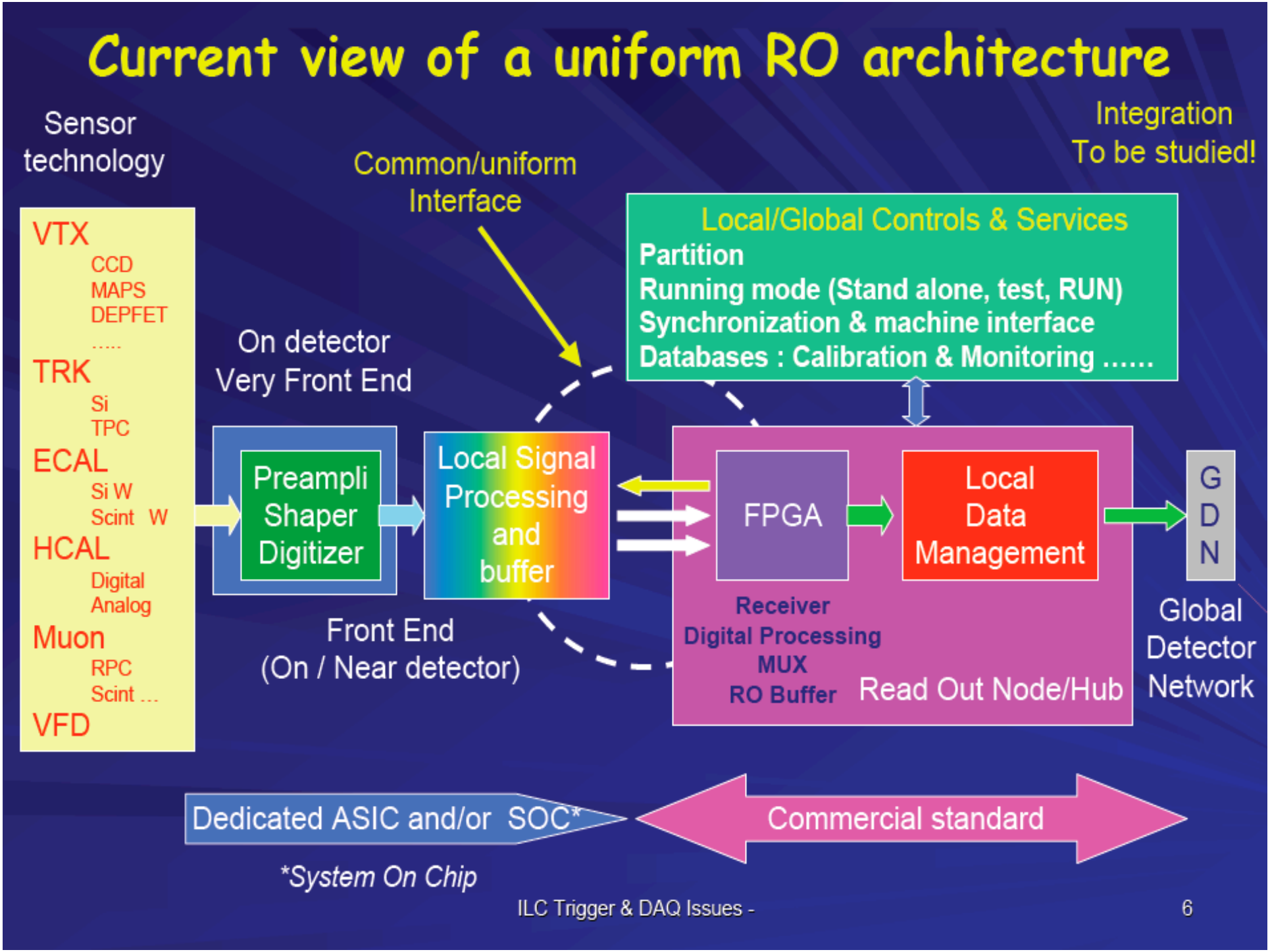
Front view

Necessary upper limit

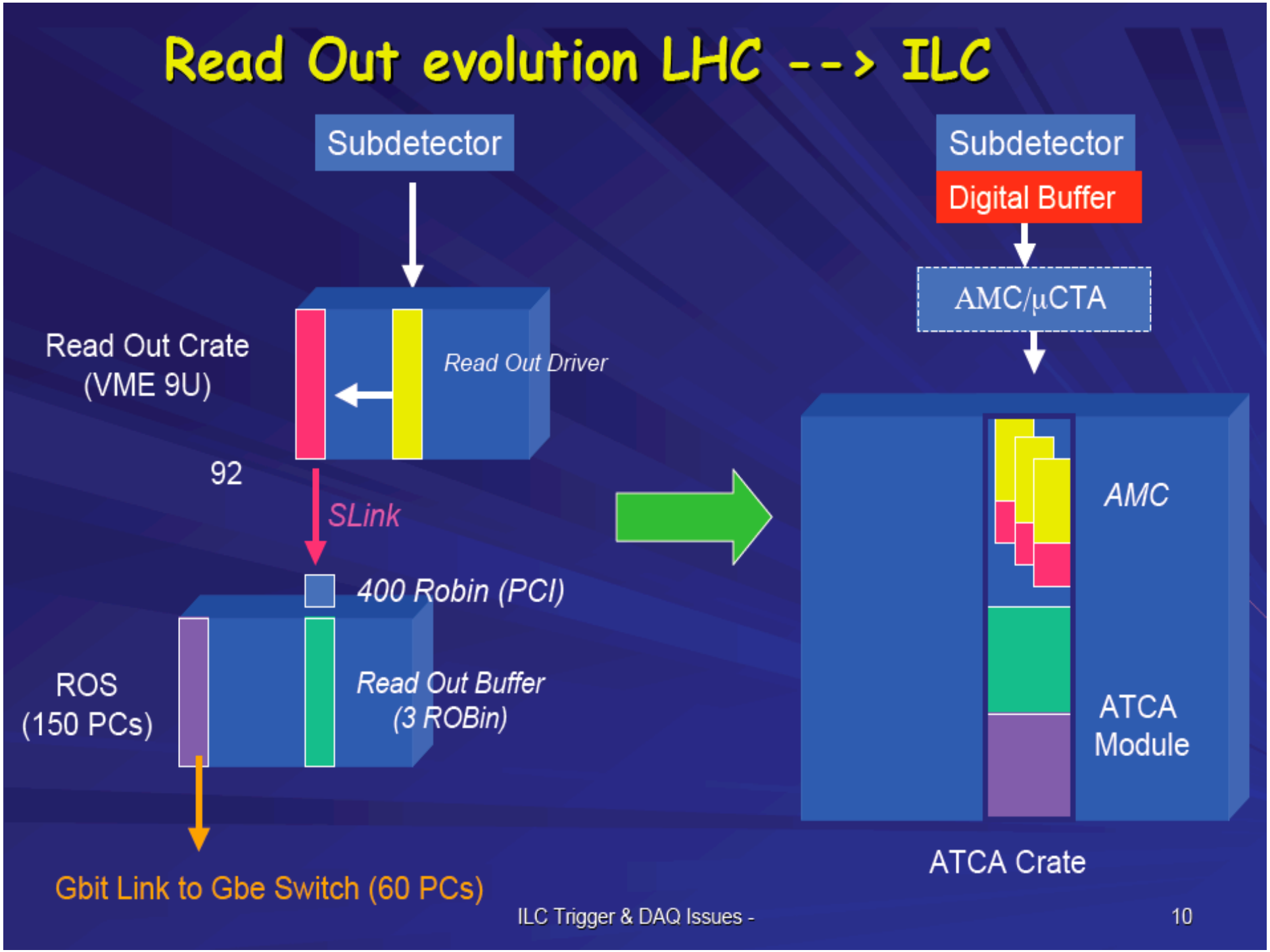
- Before all these studies converge, we can get a "necessary upper limit" from other studies, which say that a 0.2 % pad occupation is to be expected, and that a 1% (see D. Peterson's tracking talk – note that this is for standard pads) is the maximum with no significant damage to the reconstruction.
- In a bunch train, a 1ms time interval is sliced in 50 ns 'pancakes' of 1.5 10^6 pads -> 3 10^8 charge (10 bits) and pad number (21 bits) information, that is 4 bytes : 1200 Mbytes.
- Early zero suppression is mandatory

manageable

Current view of a uniform RO architecture



Read Out evolution LHC --> ILC



Somes Issues

To be discussed in specific meetings

- Cosmic trigger ?????
  - Very useful during installation and debugging
  - Compatibility with power cycling ????
- Clock, machine synchronization and timing distribution
  - with experts from LHC ! (Ph. Farthouat)

Conclusions

- Increasing testbeam activities will push DAQ
  (BUT: demands are different from final ILC DAQ)
- Don't reinvent the wheel!
  (BUT: Are we listening to ourselves?)
- Dedicated Frontends a must, but should use commercial standards whenever possible (ATCA!)
- Reliability becomes an important issue, we should learn e.g. from telecom/aerospace
- Should start to pull on the same rope early (for common hardware AND software)

Contributions

slides from: C. Bozzi, D. Bailey, V. Bartsch, R. Poeschl, R. Larsen, U. Mjornmark, M. Winter, P. Colas, P. Le Dû

Thanks to everybody!

errors, typos and biased opinions from: myself