SiLC: Silicon tracking for the Linear Collider

R&D for the next generation of large Silicon tracking systems for the ILC
presented by:

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Aurore Savoy-Navarro (LPNHE-UPMC/IN2P3-CNRS, France),
Valeri Saveliev (Obninsk State U., Russia) (cancelled),
Bruce Schumm (UC in Santa Cruz, USA),
Marcel Vos (IFIC/CSIC-U. of Valencia, Spain).
Jean Francois Genat (LPNHE-UPMC/IN2P3-CNRS, France)

to the ILC R&D Panel Committee, Tracking Review,
at BILCW07, February 4-8, 2007, Beijing, China

On behalf of the SiLC Collaboration

On behalf of the SiLC R&D Collaboration:

Dept. of Physics, University of Michigan in Ann Arbour, USA
LAPP, IN2P3/CNRS in Annecy, France
University of Barcelona and University Ramon Llull in Barcelona, Spain
Centro Nacional de Microelectronica (IMB-CNM) and CSIC in Bellatera, Spain
Dept. of Physical Sciences and Helsinki Institute of Physics (HIP), University of Helsinki, and VTT Technical Research Center of Finland, in Helsinki, Finland
Inst. für Experimentelle Kernphysik (IEKP), Karlsruhe University in Karlsruhe, Germany
Liverpool University in Liverpool, UK
Moscow State University and SiLab in Moscow, Russia
Dept. of Applied Physics, Obninsk State University of Atomic Energy in Obninsk, Russia
LPNHE, University Pierre and Marie Curie, IN2P3/CNRS in Paris, France
Charles University in Prague, Czech Republic
Santa Cruz Inst. of Particle Physics (SCIPP), University of California in Santa Cruz, USA
Inst. de Fisica de Cantabria (IFCA), University of Cantabria & CSIC in Santander, Spain
Departments of Physics of Yonsei University, Seoul National University and SungKyunKwan University, Chonbuk University, all in Seoul,
and Dept. of Physics of Kyungpook National University in Daegu, Korea
INFN-Torino and University of Torino in Torino, Italy
Inst. de Fisica Corpuscular (IFIC), University of Valencia and CISC in Valencia, Spain
Inst. of High Energy Physics (HEPHY), Austrian Academy of Sciences in Vienna, Austria
Hamamatsu Photonics K.K. in Hamamatsu City, Japan

OUTLINE

- **PART I: The Collaboration and R&D Motivations and Goals**
  - **The SiLC Collaboration**
  - **Why R&D on tracking is needed**
  - **Why Silicon Tracking**

  (A. Savoy-Navarro)

- **PARTII: The R&D objectives**
  - **R&D on Mechanics *(V. Saveliev)***
  - **R&D on Sensors *(M. Lozano and H.J. Kim)***
  - **R&D on Electronics *(B. Schumm and A. Savoy-Navarro)***

- **PART III: The R&D Tools**
  - **Simulations *(M. Vos)***
  - **Lab Test bench and Test beams *(A. Savoy-Navarro)***

Concluding remarks

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The SiLC Collaboration: *PRC-DESY May'03 & status report May'05*

Moscow St.U. &
SiLAB,
Obninsk St.U.

Korean
Universities
Hamamatsu
& KEK
(in progress)

U. of Michigan
SCIPP & UCSC
& close contacts with
FNAL and SLAC
(SiD & beam test)

LAPP/IN2P3-CNRS, Barcelona U.
& U. Ramon Llull, IMB-CNM/CSIC,
HIP-Helsinki & VTT Tech. Res. Center
IEKP Karlsuhe, Liverpool U.,
LNPHE/IN2P3-CNRS, Charles U. Prague,
IFCA-CSIC/ Cantabria U, INFN Torino &Torino U.,
IFIC-CSIC/Valencia U., HEPHY Vienna.
& close contacts with CERN and DESY

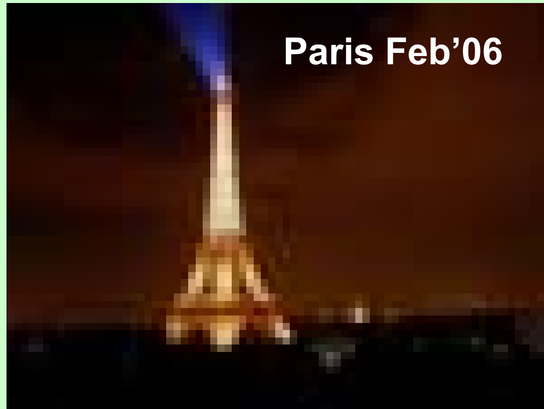
SiIC Collaboration main features:

- Generic R&D: representatives of GLD, LDC & SiD
- Worldwide
- Large expertise on all the R&D facets
- Synergy with LHC and LHC tracking upgrades
- Important R&D infrastructures in several Labs
- Close contacts with international Labs
- Collaboration with industrial firms
- EUDET E.U. Infrastructure project involvement

SiLC R&D collaboration meetings

The SiLC collaboration organizes regular collaboration meetings, talks on: SiLC activities, Other subdetectors & all detector concepts, Industrial firm's, other experiments (especially LHC)

http://www.cnm.es/projectes/SILC_meeting

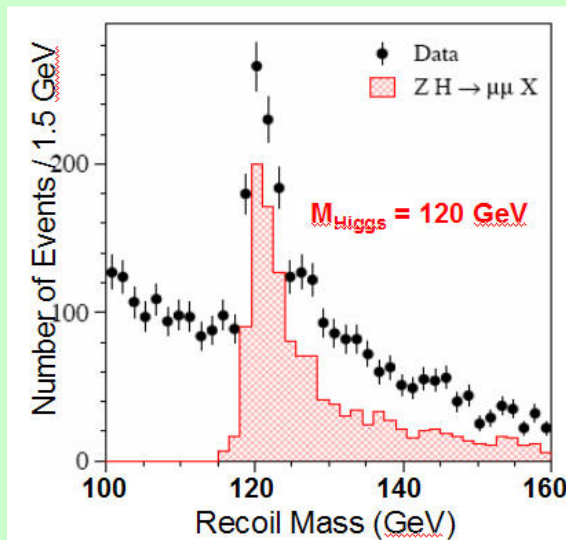


Next ones:
Prague April'07
CERN July'07?
Torino Oct'07
FNAL early 08?

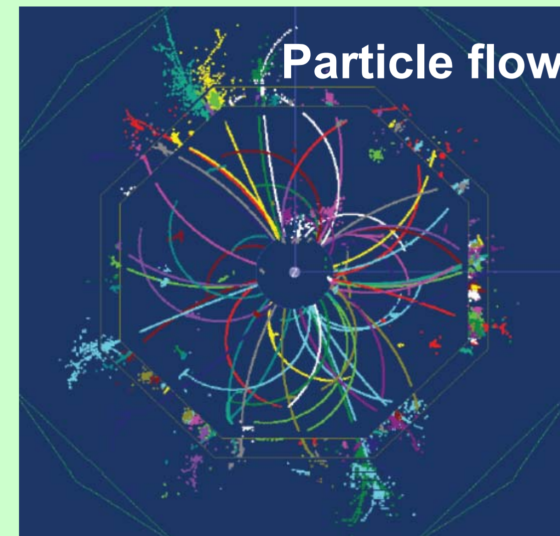
Why R&D on tracking is needed?

Or why present state of the art on trackers is not good enough?

1) PHYSICS AT ILC (& LHC ++):



Long life particles
(standard ones
CHAMPS)
Tau leptons
Multijets etc….

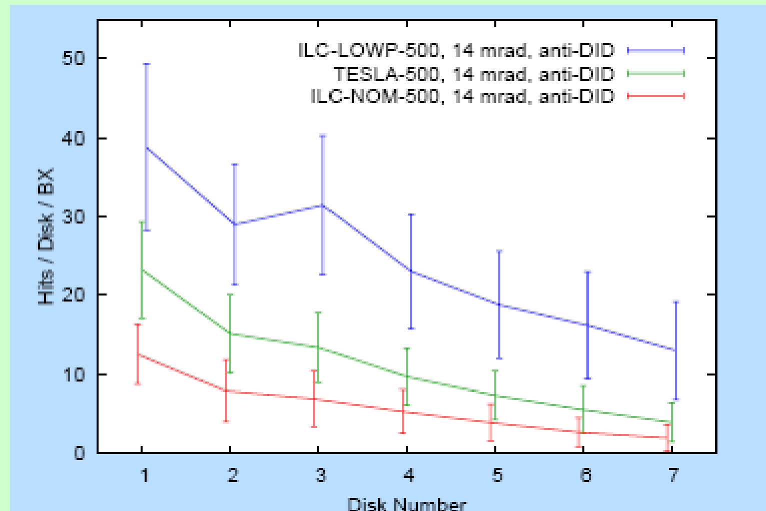


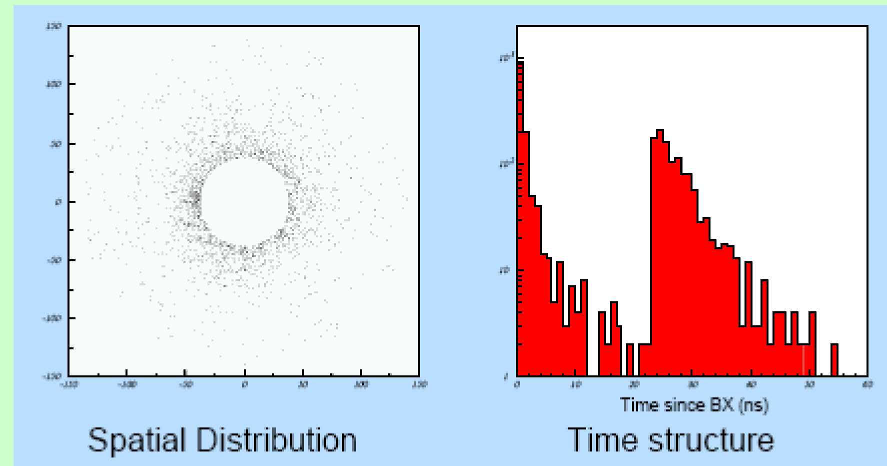
WILL REQUIRE high tracking performances:
(10x Momentum resolution/LEP, better spatial resolution),Full coverage,
Low material Budget, Highly perfoming FE and readout electronics,
Easy to build, calibrate, monitor, align, reliable

Why R&D on tracking is needed?

Or why present state of the art on trackers is not good enough?

2) Machine environmental conditions: harsher





Hits on the innermost FTD (overlay of 100 BX) calculated by MOKKA

Hits per disk per bunch crossing for the FTD, for different parameters set of the ILC with a crossing of 14 mrad.

WILL MAKE LIFE NOT AS EASY in the very forward and innermost central parts:

Impose more stringent conditions on pixel (Forward) on associated FEE & innermost barrel region

SiLC assets: there is a team of people working with MDI (Valencia), identified teams are now tackling the R&D in those regions (see sensors and simus sections)

Why **Si** tracking?

Since 25 years Si sensors have become a must for the tracking devices in HEP

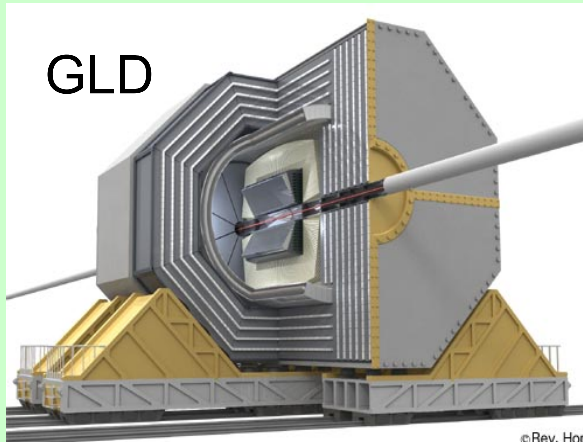
- Condensed medium, thus excellent spatial resolution.
- 1.1eV band gap: low enough to ensure prolific production of charge when particle traverses it,
- But high enough to avoid high dark current Thus confortable operating conditions.
- In ILC environment it provides stable, robust & reliable operation, with no need of continuous calibration (apart for FEE)
- No particular need for handling or environmental conditions (like Pressure or Temp.)
- Low Z element with excellent mechanical & thermal properties; ideal for tracking where multiple scattering (and so it does at ILC)
- Mechanical properties permit building sensors in various shapes and sizes allowing for many different geometries & implementations of the required granularity: pixels, strips etc..
- Use of Si detectors in mass industry products

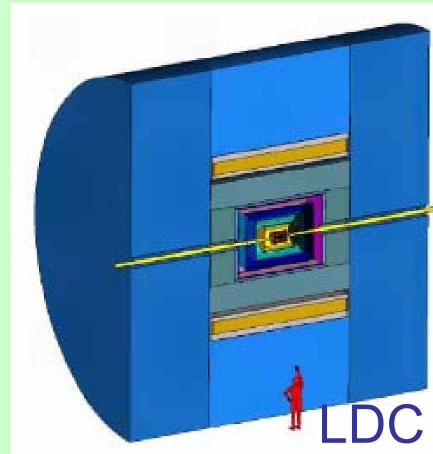
Two main drawbacks:

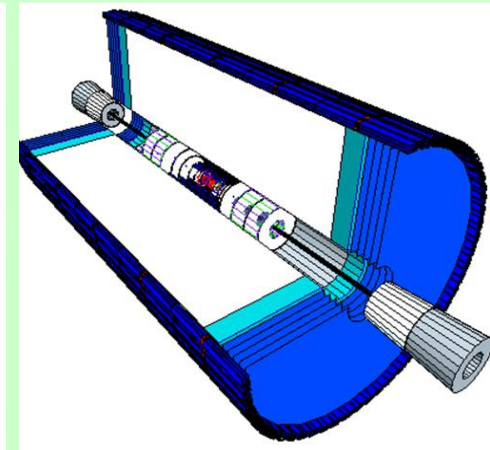
because sensors are small to cover large area: need of support structure that may spoil the material budget,

and huge number of channels thus FEE is challenging in terms of power dissipation and connectivity

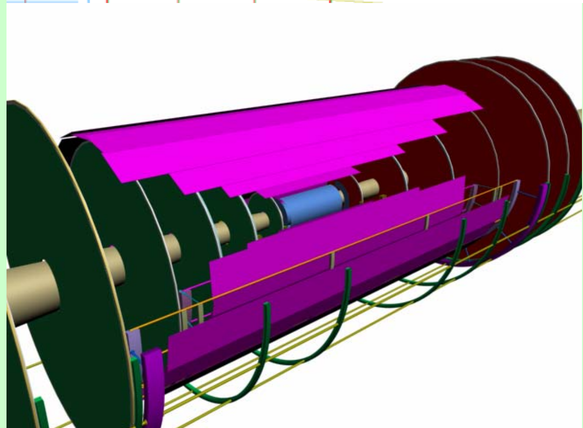
Role of Silicon tracking *or Silicon tracking what for?*

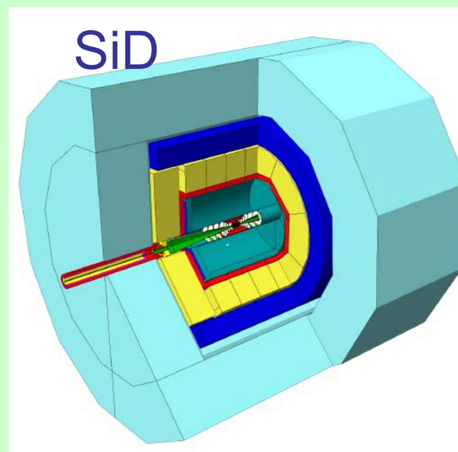


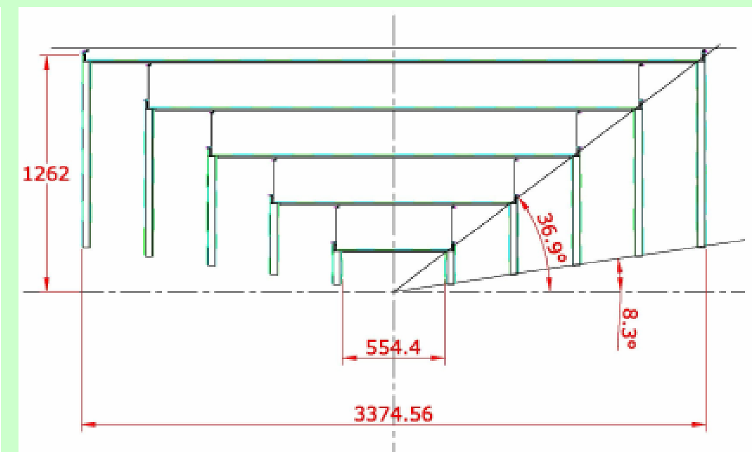




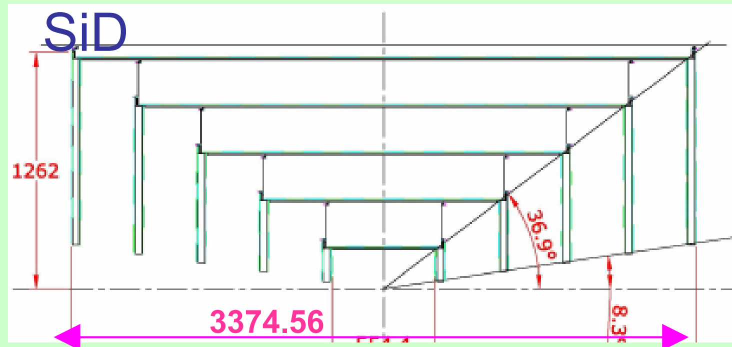
3 detector concepts & main difference:
The tracking strategy=TPC Yes or No



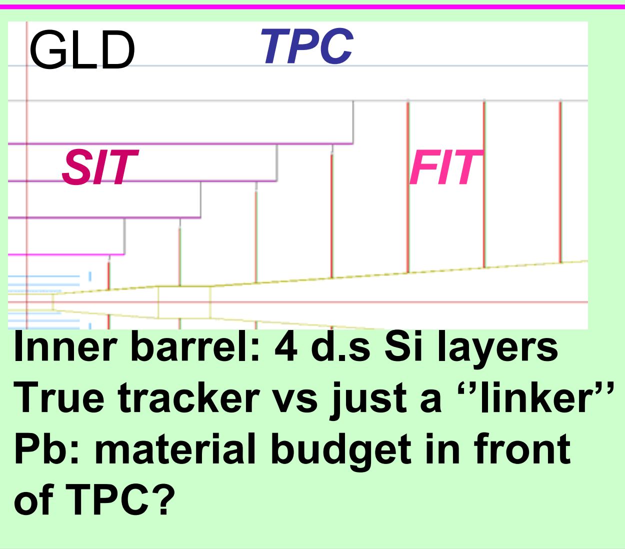




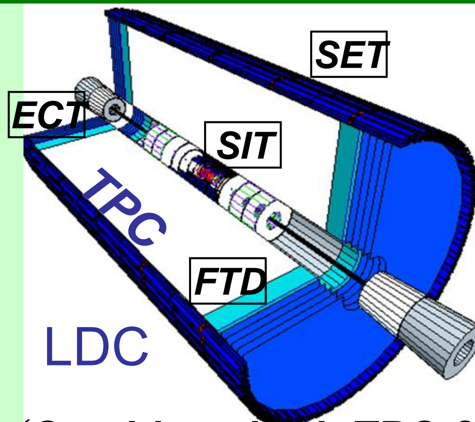
Role of Silicon tracking *or Silicon tracking what for? (cont'd)*

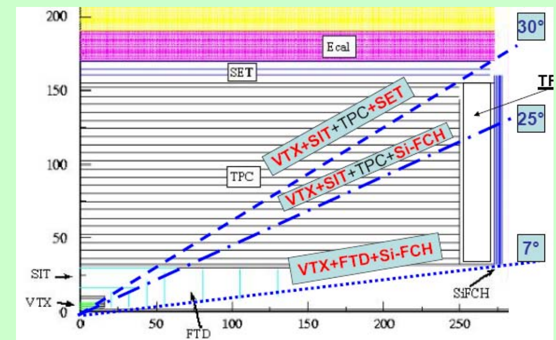


SiD concept: All-Silicon tracking strategy
Integrated Silicon tracker,
Barrel: more a '' sagitter '' than a true tracker?
with fully integrated Forward tracker:
Appealing for hermeticity & large angle Physics.



Inner barrel: 4 d.s Si layers
True tracker vs just a ''linker''
Pb: material budget in front of TPC?





Si Envelope:{SET+(SIT+FTD)+ECT}

- ✓**Combines both TPC & Silicon tracking technologies**
- ✓**Each Si component LINKS 2 subdetectors** (smoother transition)
- ✓**Improves tracking overall performances (see simus)**
- ✓**Calibration of systematics & full coverage**

Si Envelope is like stretching a all Silicon tracking into 2 parts: inner and outer ones and install a TPC in between.

SiLC:UNIQUE place to study/compare these various crucial tracking concepts

Physics and Machine environment at the ILC are both imposing stringent conditions on the tracking system, namely:

- high performance in momentum resolution and spatial resolution
- Low material budget
- Reliability, simplicity and easy to build, monitor and calibrate devices.
- Full coverage (avoid dead regions and importance of End Caps)
- Easy to integrate in the detector and readout/DAQ architecture (part of particle flow)
- System able to handle very high magetic fields (3 to 5 Teslas)

- **This leads to an active R&D for ILC large Silicon trackers, on:**
  - Mechanics R&D
  - Sensors R&D
  - Electronics R&D

  Together with developing the needed tools:
  - Simulations
  - Lab test bench and test beams

With in mind all the issues listed above, for each of these R&D topics

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Concluding remarks

MECHANICS R&D

Teams: IEKP Karlsruhe, IFCA-CSIC/Santander, IFIC-CSIC-Valencia, Korean Group, Liverpool U., LPNHE/IN2P3-CNRS, INFN-Torino & Torino U.

Why R&D on Mechanics?

The requirements on the next generation of large Silicon tracking systems are:

- low material budget,
- simplicity of the design
- easy to construct (automatization or semi-automatization, transfer to industry)
- New materials
- and robustness and stability
- stringent requirements on spatial requirements (alignment & positioning)
- and on hermeticity
- Integration issues (and push pull???)

CAD design studies on Si components

A series of preliminary CAD designs of the various components
of the Silicon tracking system in an ILC experiment with an emphasis on

- simplifying as much as possible the overall design (limiting the number of different fundamental elements of the detector architectures (sensors and elementary modules or ladders))

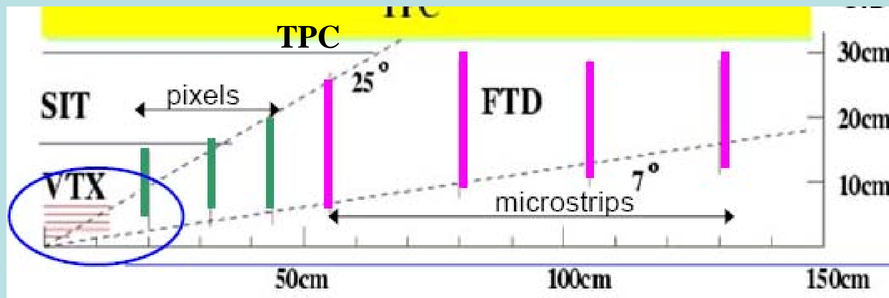
- and the main R&D objectives on Mechanics

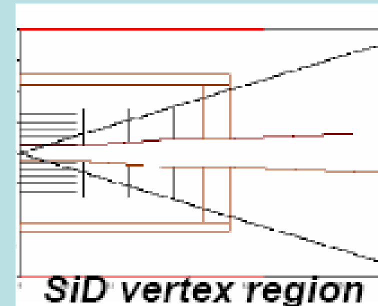
- Developing mechanical prototypes for preliminary mechanical studies and for test beams

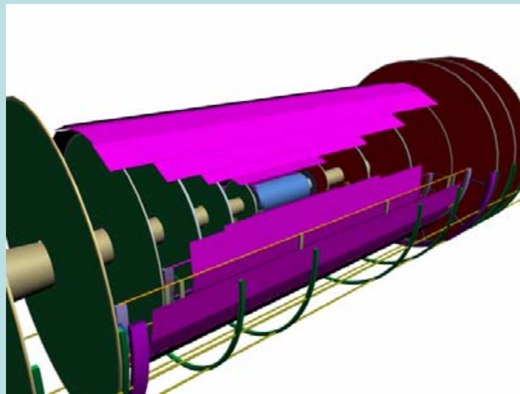
Important input for the detailed simulation (DB Geometry) and for building more realistic prototypes as for instance for thermo mechanical studies.

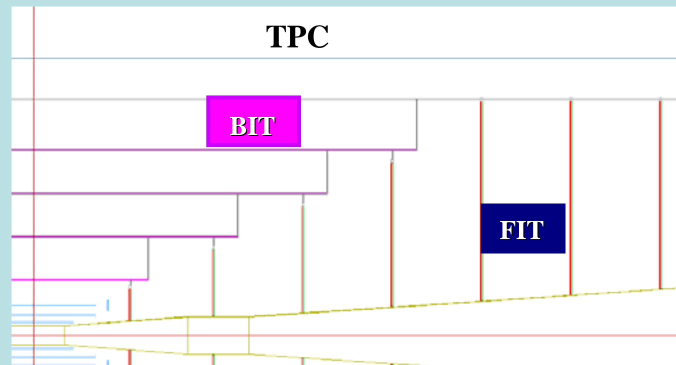
Example 1: The innermost layers

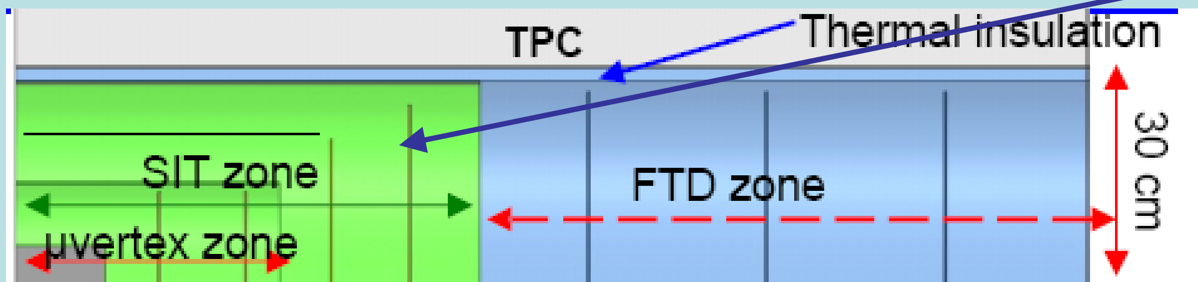
In GLD, LDC and SiD detector concepts the innermost part is done in a rather similar way: Si layers in barrel & disks in the forward/backward regions:





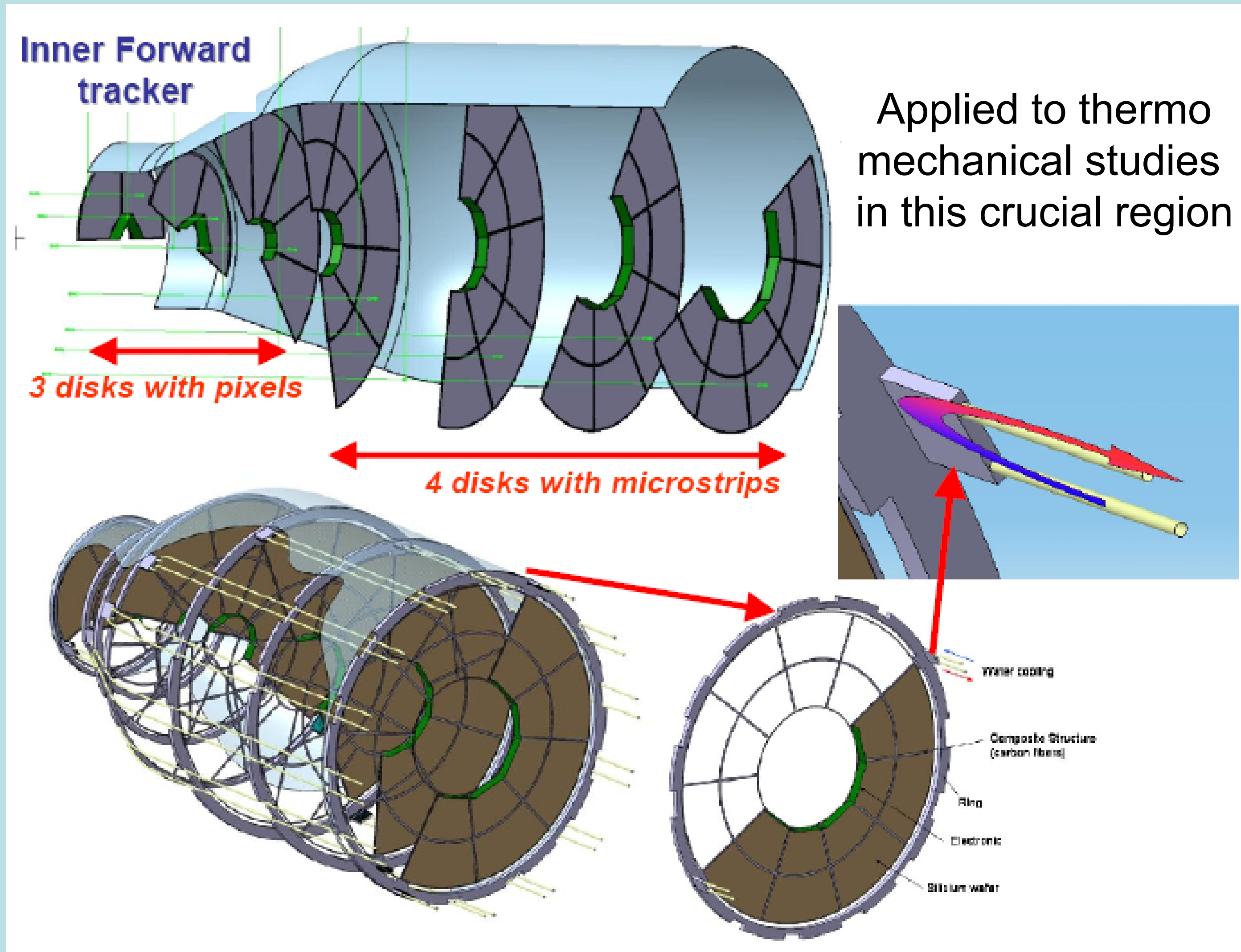






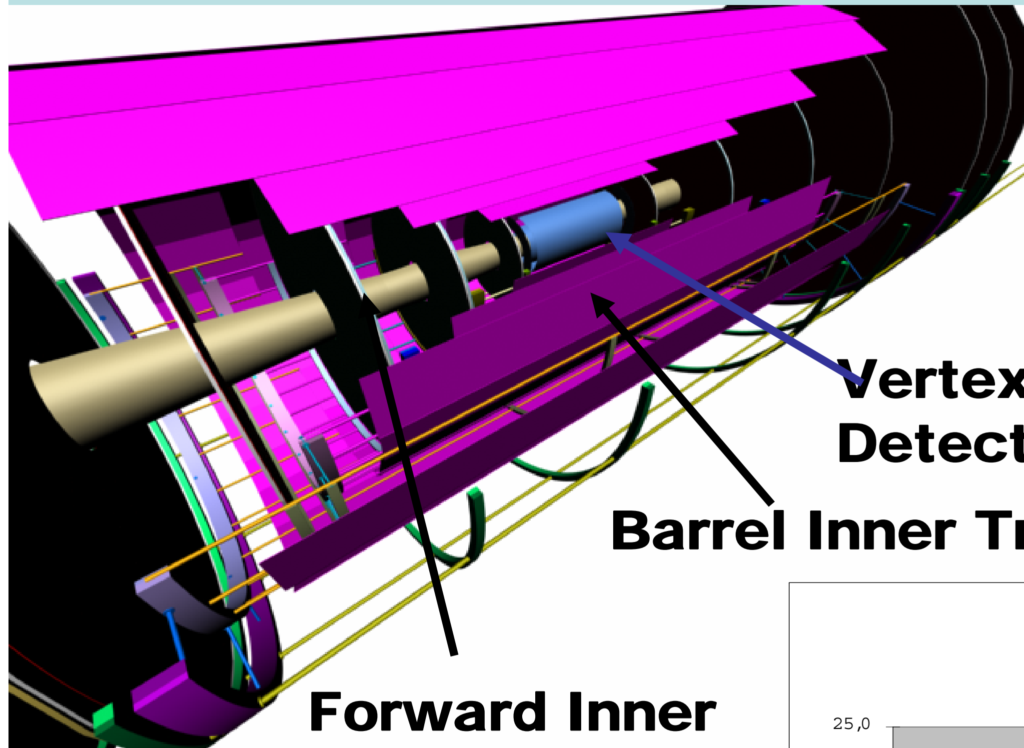
Thus the idea to extend the vertex detector as indicated in green region, borrowing the same sensor technology (pixels). SiLC studies: sensors & simulations

A very preliminary proposed design for the inner Si components

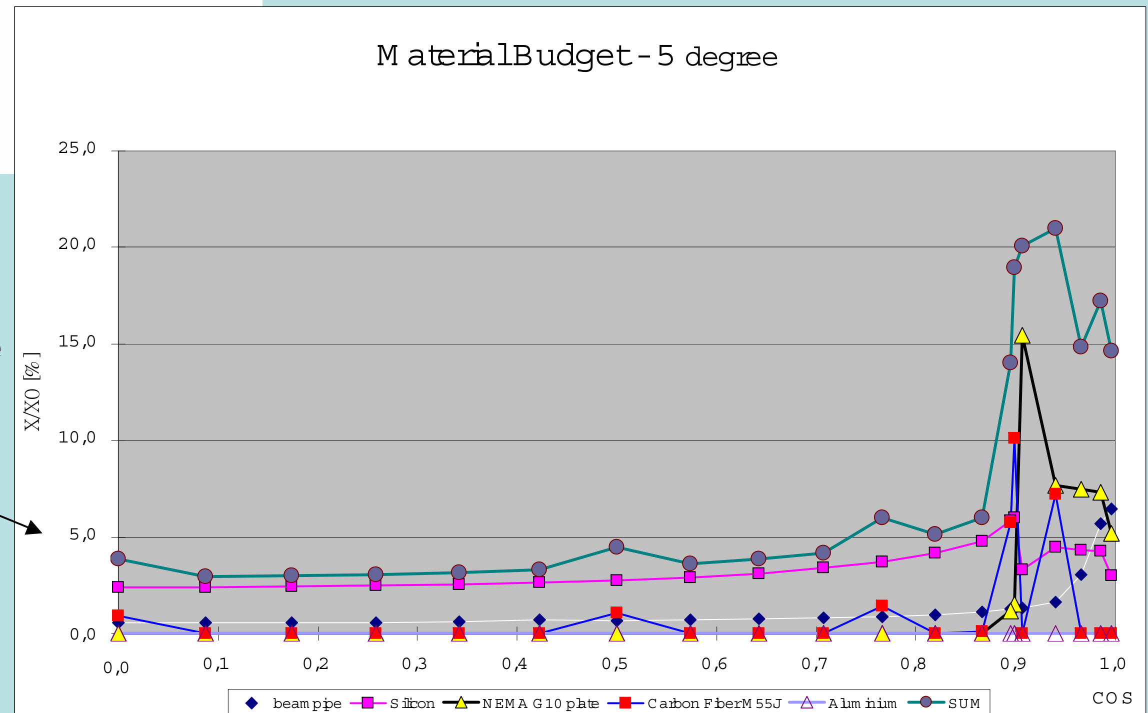


IT Mechanical Structure

Korean Group, H.Kim et al.



Beam pipe+Silicon+NemaG10plate + Carbon support+Al



Example 2:CAD of the EndCap Si layers

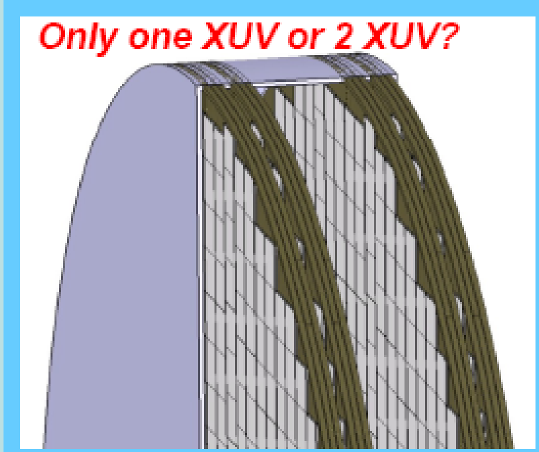
FORWARD SECTOR

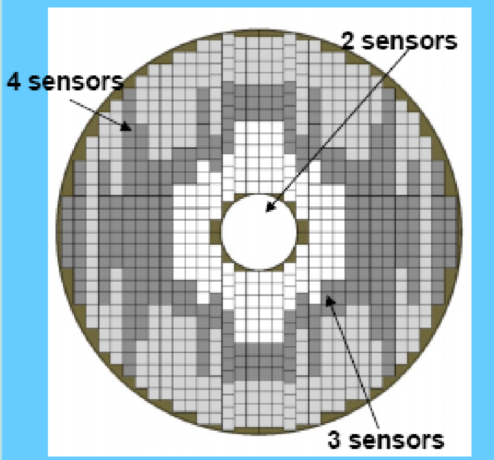
Ø203mm
~157mm
ladder
~117mm
~405mm
~405mm
270mm
104mm
230mm
59mm
sensor
Overlap (hermeticity)
electronics
CF structure
thickness ~ 0.5mm
20mm
0.3mm
0.3mm
4.6mm
Si-FCH - ILC
LPNHE Paris – February 15, 2005

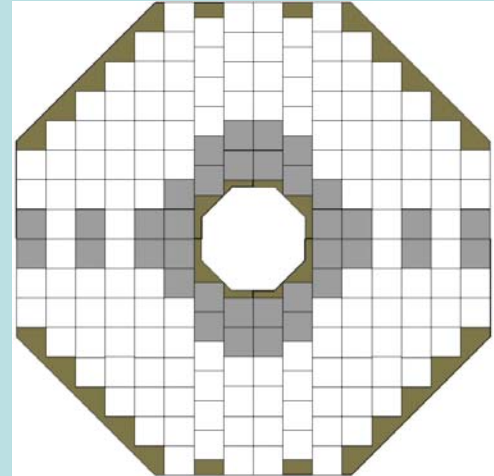
1600mm
300mm

10240 sensors
3840 modules & 2 or 4M channels

Projective geometry as in LHC detectors, adapted both to LDC or SiD case

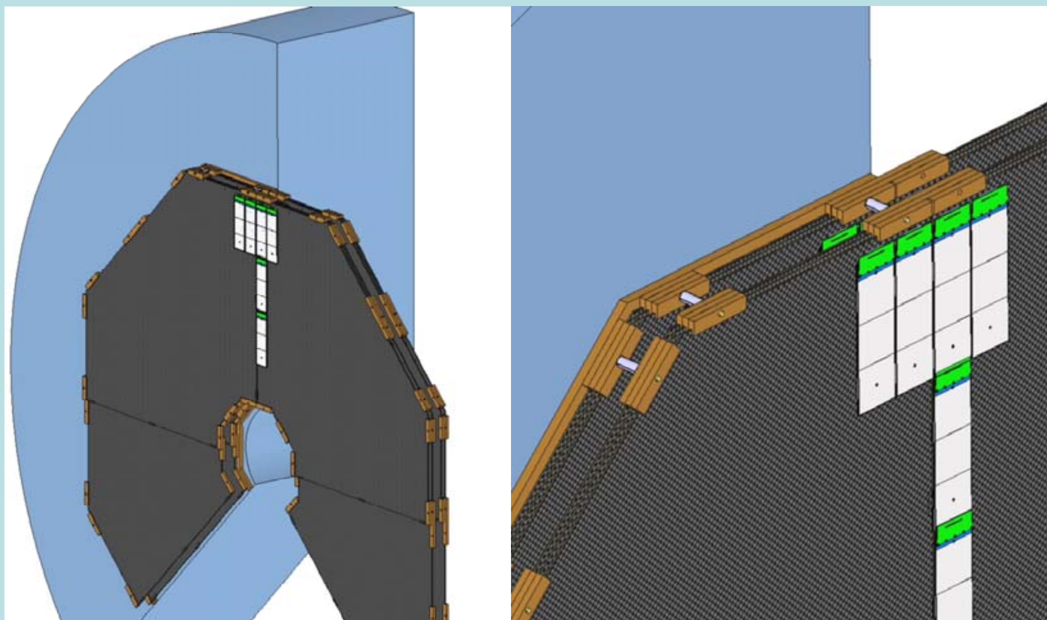




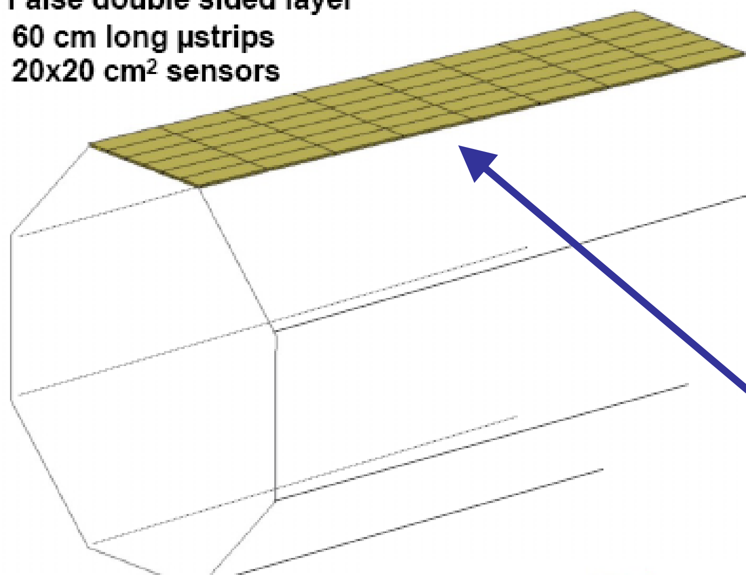


XUV design with different sensor sizes (10x10cm2 or 20x20 cm2)

End CAP CAD design (cont'd)



Integrating one or two XUV Layers in the EndCap e.m. calorimeter



Attractive features of XUV approach

- Simple to design
- Easy to build
- Easy to adapt/integrate to the design of the surrounding detector
- Possible use of a single sensor ''universal'' type
- Possibly the same elementary module (ladder) than external layers in the barrel

A novel approach to construct elementary modules

(Liverpool U., T. Greenshaw & ASN, LPNHE-Paris)

Main quest: transparency & simplicity
Imply working on sensors, FEE,connectivity, mechanical structure, easiness to assemble (automatization issues)

Design & efficacy of Carbon fibre shells as a support structure for the Si tracker Will be investigated. Considerable expertise within SiLC.

Example 1: Liverpool designed & manufactured the supports for the L00 CDF layer (i.e.low mass cylindrical rigid structure of Radius = 1.5 cm and incorporating strips & cooling channels

Example 2: MICE Muon Ionisation Cooling Experiment
This support is at much larger scale: 50 cm diameter Carbon fiber ring

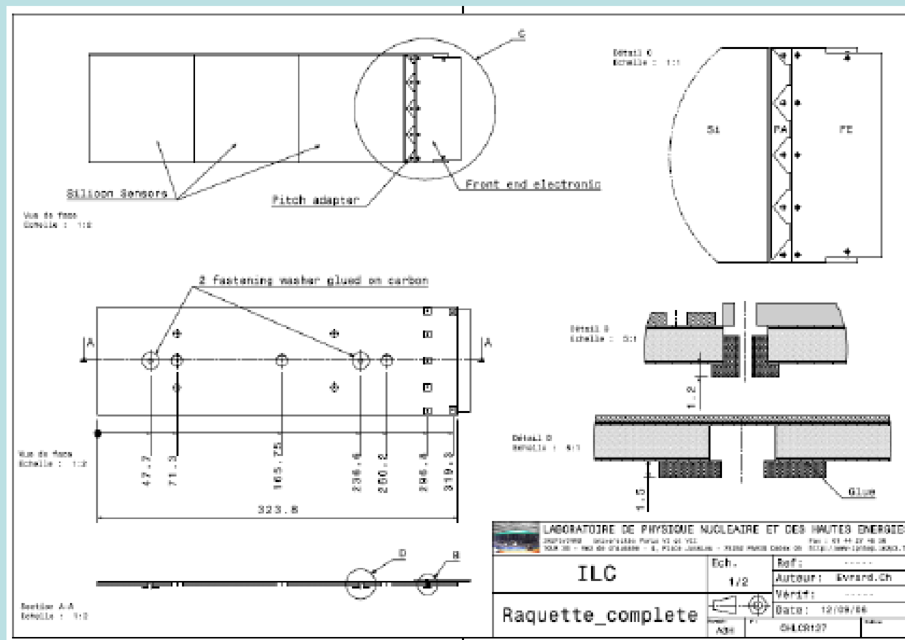
Studies of the support of Si trackers will be studied in 2 ways: sensors directly attached to a fiber shell Or sensors first attached to into ladders and then attached to a support frame

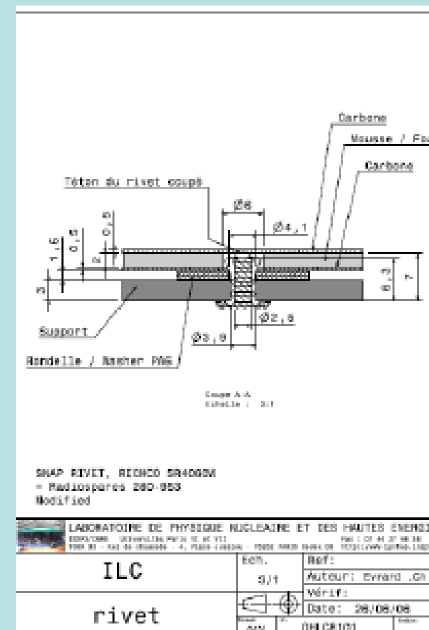
A novel approach to construct elementary modules

The ladder designs which will be investigated by the SiLC Collaboration include foam sandwich structures.

These are being studied for the vertex detector of the ILC by the LCFI group, who have demonstrated that ***both Silicon carbide and reticulated Carbon foams*** can be used to construct stable, extremely low mass ladders

A first step towards this type of ladder support structure is being experienced for the construction of the elementary modules for the forthcoming test beam in 2007.





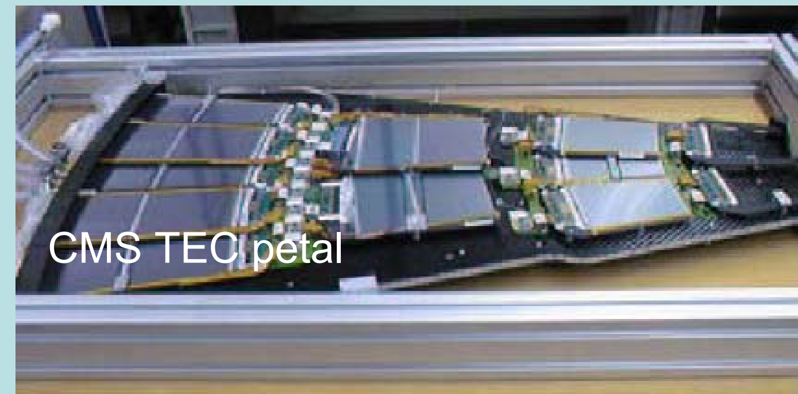
Elementary modules what else?

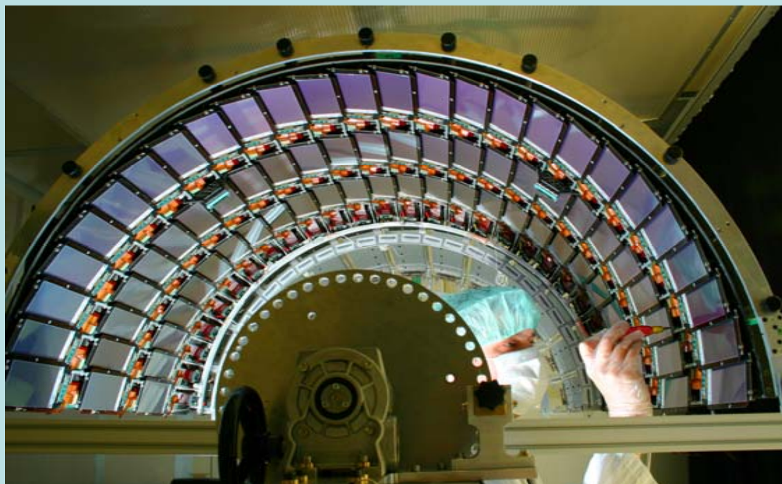
Module can be the basic building block.

Is it the only one?

CMS TEC and TOB introduced an intermediate level of modularity: ladders and petals consist of the order of 10 modules plus local services.

- greatly facilitates the final integration step
- intrinsically robust against component failure





CMS TIB: more classic approach for high-density inner layers

SiLC is making use of a variety of expertise

COOLING *(LPNHE, Torino, IFIC)*

Hypotheses of work

- **At ILC Si tracker will be quite radiation safe**
- **Thus T°C up to 30°C on sensors are allowed and**
- **ΔT°C ~ 10°C**
- **From FEE electronics:**

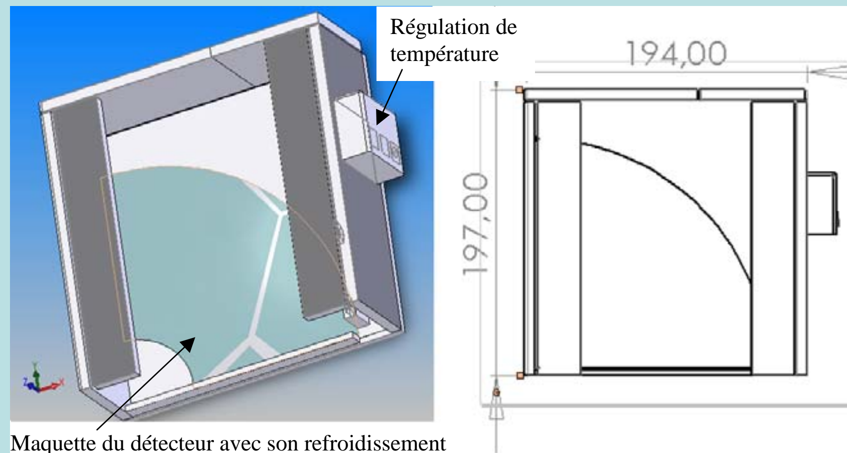
1mWatt per channel (certified by present electronics R&D results)

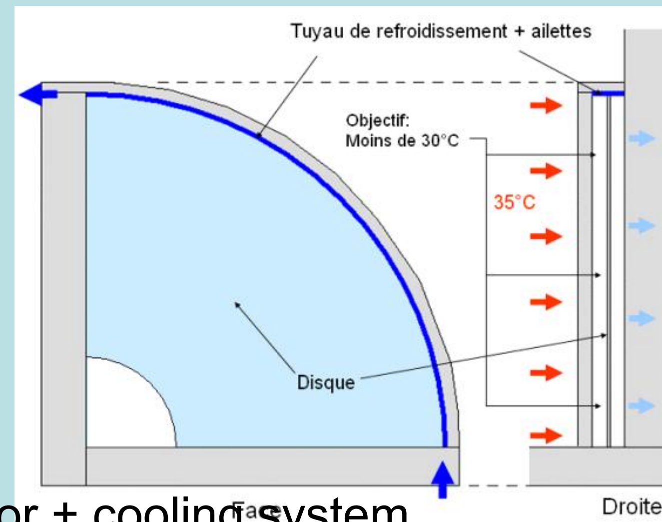
- **Main source of warming up: the neighbours (still unknown??)**

Thus much better conditions than at LHC.

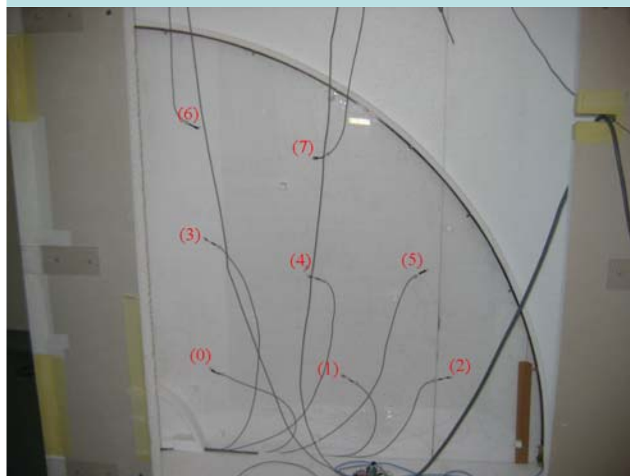
An insulating box will be built in order to protect from the external power dissipation and serving at the same time as Faraday cage for the FEE on detector

Thermo-mechanical studies:endcap case *(LPNHE-Paris)*

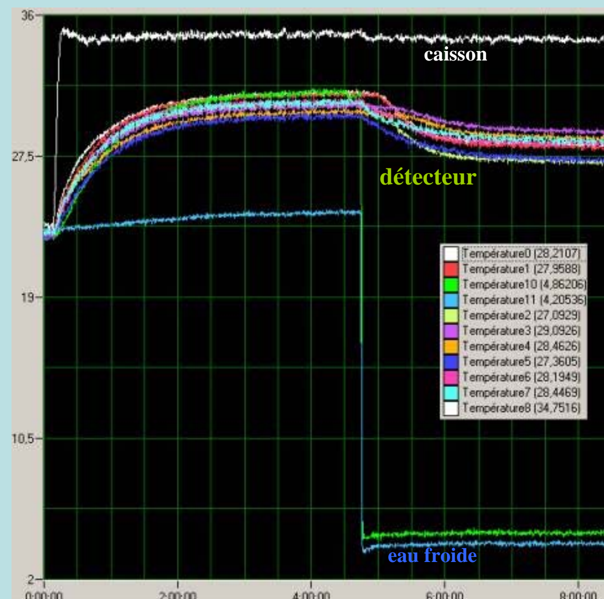




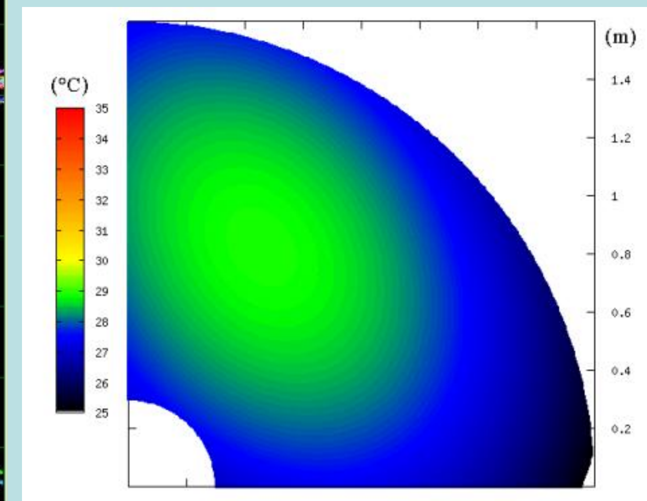
1) Design of the mechanical set-up: detector + cooling system



2) Mechanical proto with thermal resistors as FEE power dissipation simulation



3) Measurements of T°C on detector vs time (cooling)

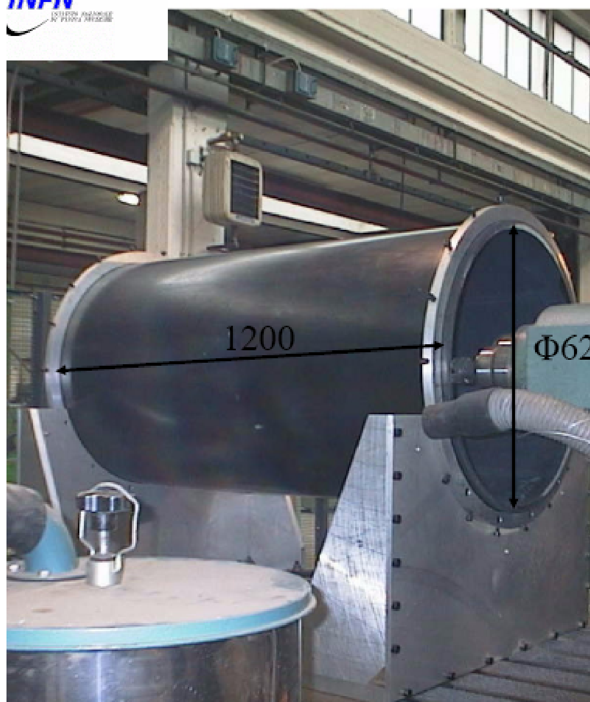


4) Modelling of the simu with obtained results

Examples of thermal enclosure:

THE SSD CYLINDER

Courtesy of Giuseppe Giraudo
INFN-Torino (ALICE)



4+4 PLIES => 1,2 mm
ROHACELL => 5 mm
0,5% X_0
WEIGHT = 10 kg

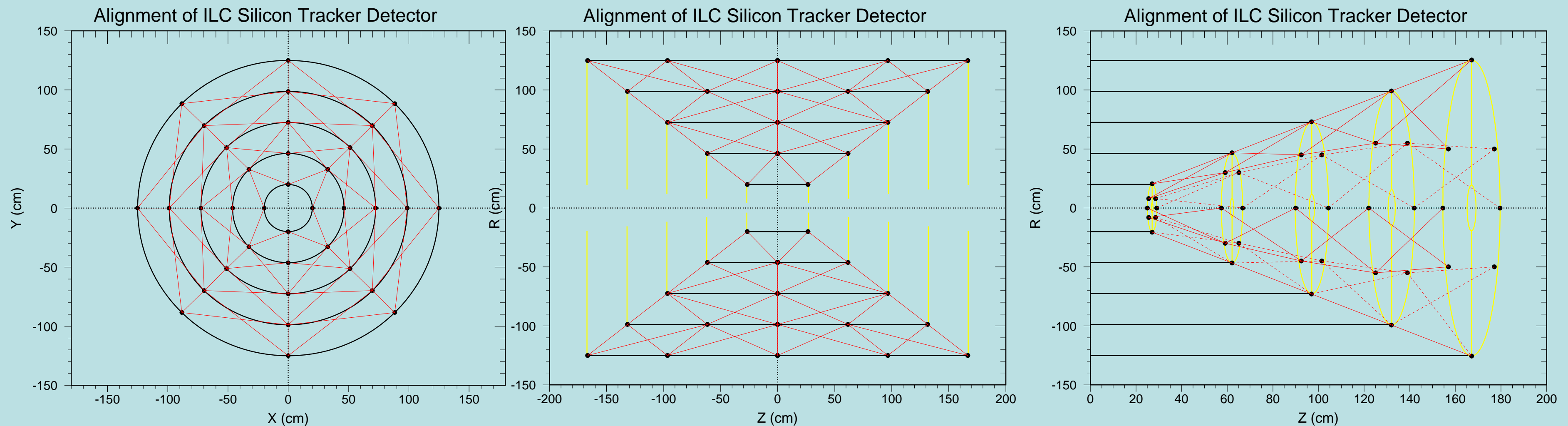
ATLAS SCT thermal enclosure

First cooling system will be built for the November 2007 test beam (SiLC & EUDET)

Alignment – FSI

(H.J. Yang & K. Riles University of Michigan)

- Measure hundreds of absolute point-to-point distances of tracker elements in 3 dimensions; based on development in Oxford University for the ATLAS SCT
- Absolute distances determined using a Frequency Scanning Interferometer ("counting fringes") and an array of optical beam splits from a central laser.
- Grid of reference points overdetermined → Infer tracker distortions

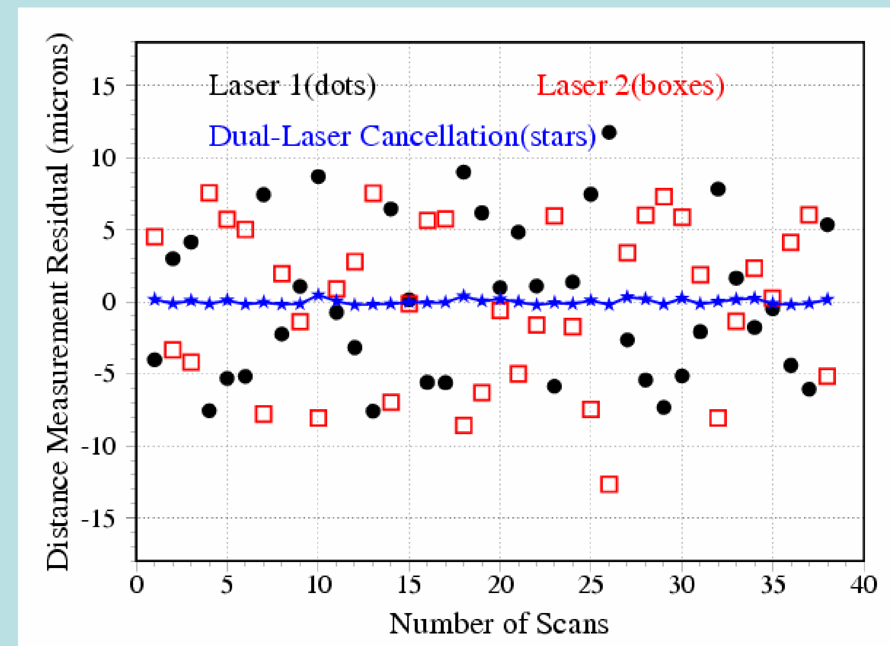


Alignment – FSI (cont'd)

- In well-controlled ambient over distance of 10-60 cm: ~ 50 nm resolution by using multiple-distance measurement technique. Vibration Measurement: 0.1-100 Hz, amplitude as low as few nm. (H.J. Yang, J. Deibel, S. Nyberg, K. Riles, Applied Optics, 44, 3937-44, (2005)

- In real world: temperature fluctuations /drift (refraction index) and vibrations affect distance measurement. Single laser distance resolution degrades to 3-7μm.

Dual-laser technique (Oxford, two independently chopped lasers, scanning over same frequency range in opposite directions) restores precision to 0.2 μm:



(See also SiD presentation)

Alignment – hybrid

(I. Vila, M. Fernandez, C. Rivero, A. Ruiz, M. Lozano, IFCA-CSIC/Cantabria & IMB)

Hybrid approach is born from the AMS-I and CMS development

Key point is the detection of the laser beams using the position sensitive device itself: the silicon sensors. Thus, mechanical transfer of the alignment system measurement to the active area is avoided.

Furthermore, this approach requires no dedicated DAQ system and reconstruction software.

Precision of the order of 2-3 microns expected.

ALIGNMENT HYBRID (cont'd)

Usage of collimated laser beams (IR spectrum) going through silicon detector modules . The laser beams would be detected directly in the Si-modules. This requires:

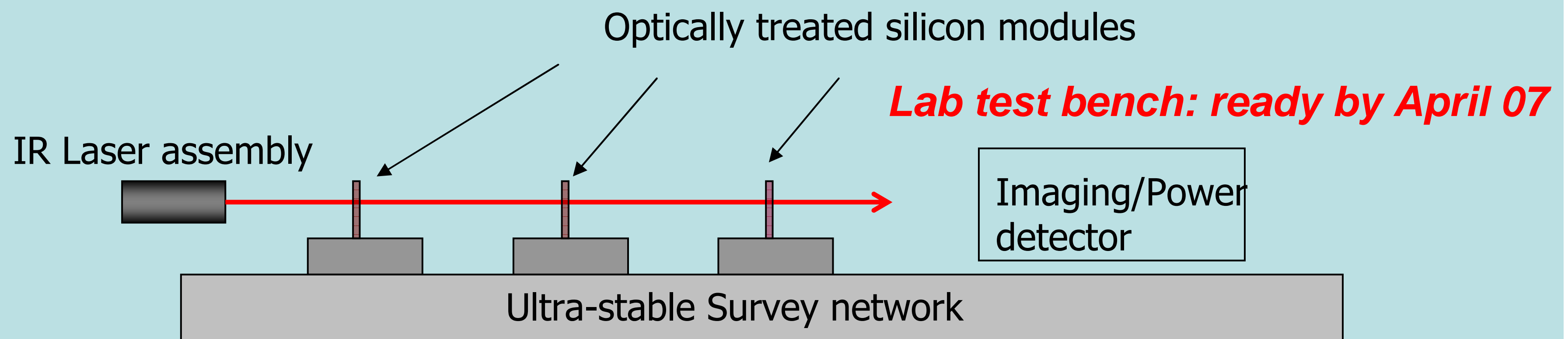
- Silicon module surface requires special treatement to improved its optical quality/transmitance
- Dedicated ultra-stable test stand for "optical" characterization of the modified silicon modules: reflectivity, transmitance, absorption, polarization sensitivity, wedge effect, response uniformity...

Main advantages:

Particle tracks and laser beam share the same sensors removing the need of any mechanical transfer.

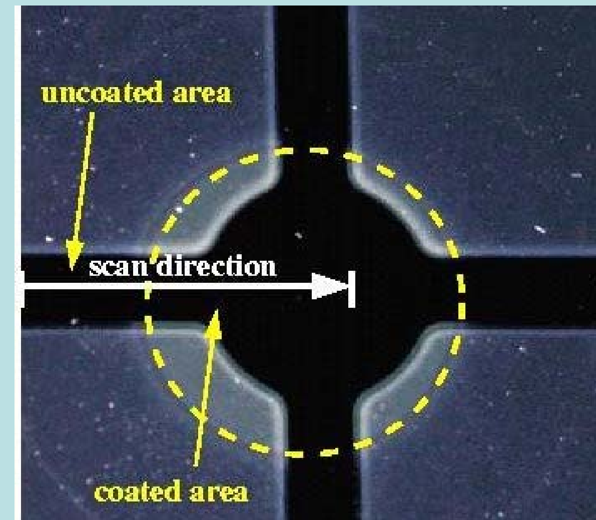
Minimum interference with Silicon support structures

No precise positioning of the aiming of the collimators. The number of measurements has to be redundant enough



Alignment – hybrid approach (cont'd)

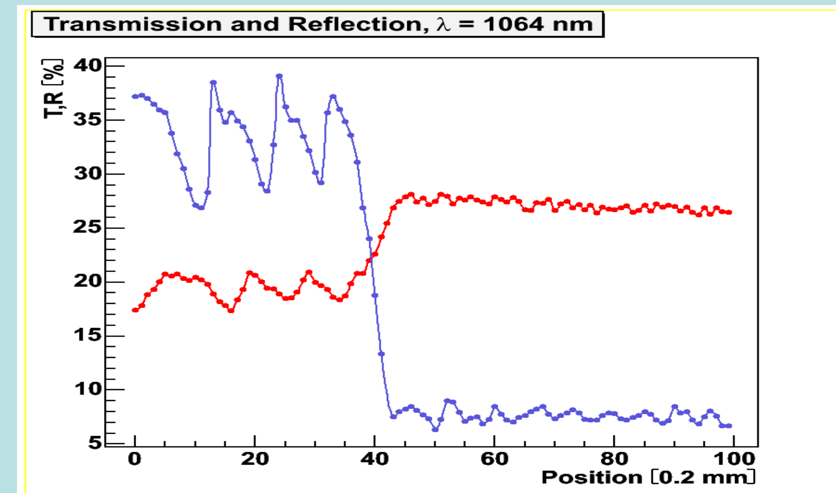
Micro-strip sensor has to operate as a semi-transparent photo-detector.
IFCA Santander and IMB-CNM, within the EUDET are ***performing R&D to optimize the optical properties of silicon sensors*** (transmittance, reflectance, beam deflection, position reconstruction accuracy)



- 10 mm hole in aluminium backside coating
- All sensors with anti-reflective coating

Transmission measured to be 14-20% (at λ=1075 nm)

- Reflectivity <= 6%



Alignment - comparison

Both approaches to the alignment system have complementary (when compared to each other and with respect to the track-based alignment) benefits and challenges.
SiLC is following the two approaches.

CHALLENGES:
- Both: Integration with the system
- The hybrid approach requires the development of sensors with optical properties.
- FSI relies on the mechanical transfer from retro-reflector position to active area.
- FSI is a more complex technique that requires its own DAQ system.

BENEFITS:
- Both: possiblity to resolve “fast” distortions
- FSI: measures arbitrary coordinates, constraints on “weak modes” of the track based alignment.
- hybrid: direct measurement of parameters that couple strongly to the sensor measurement.

SILC intends to test both on test beams in 2007 (1st HYBRID proto) and 2008 (FSI)

Sensors

Microelectronic Research Centers: CNM, ETRI, SILAB, VTT
Characterization Labs: CU Prague, HEPHY-Vienna, HIP-Helsinki, IEKP Karlsruhe, IFIC-Valencia, Korean Group, Liverpool, LPNHE-Paris
and close contact with industries: Hamamatsu, Micron, E2V, Korean firms, WIS-EDGETEK, Canberra, ...

Silicon microstrips detector baseline

- Future Linear Collider Experiment will have a large number of silicon sensors
  - Order of 100-200 m^2 (CMS has 200 m^2)

- SiLC baseline for outer layers
  - 8” high resistivity FZ sensors
  - Thinned by a factor 2 or 3, thickness about 200 μm
  - AC or DC coupled strips
  - 50μm pitch
  - Strip length between 10 and maximum 60 cm
- SilC baseline for inner layers

  - double sided 6” high resistivity FZ sensors
  - AC coupled strips
  - 50μm pitch

Present production baseline

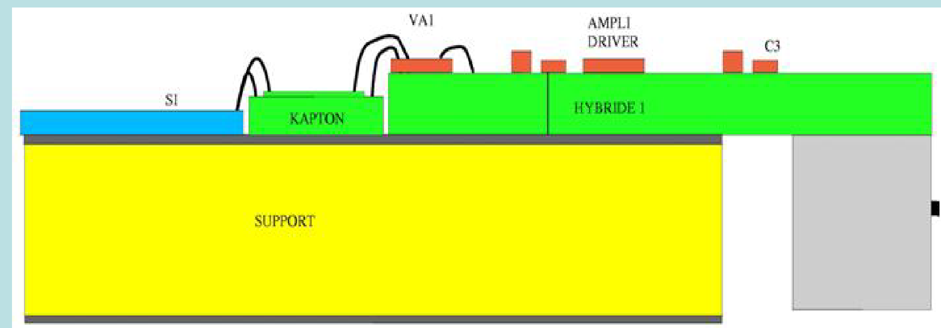
- Thin: 100-300μm
- Low current: Target around O(1nA) per strip
- 6”-8” sensors:
  - 6 inch wafer -> 10×10 cm^2 sensor size
  - 8 inch wafer -> 14×14 cm^2 sensor size
- High resistivity floatzone:
  - 4-10 kΩ·cm resistivity of bulk (n-type)
- Biasing:
  - AC: bias resistor with polysilicon (20 to 50MΩ)

    or
  - DC: FOXFET structure to allow easy testing
- 50 μm readout pitch
  - With no intermediate

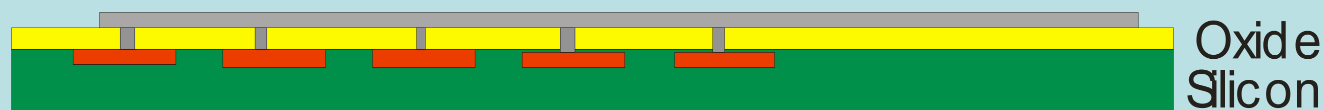
    or
  - With one intermediate strip, resulting in 25μm strip pitch

Future Option:
additional dielectric layer plus 2nd metal layer

- Old fashioned FE Hybrid with wire bonding:



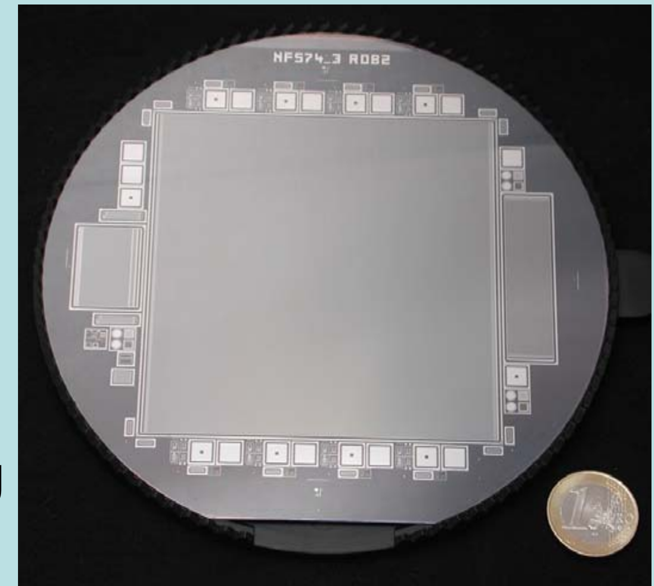
- Future SiLC Option: Avoid FE hybrid for electronics
- Integrate pitch adapter into sensor
  - 2nd metal layer for signal routing:



- Bump-bonding of readout chip directly onto to sensor

Immediate R&D goals

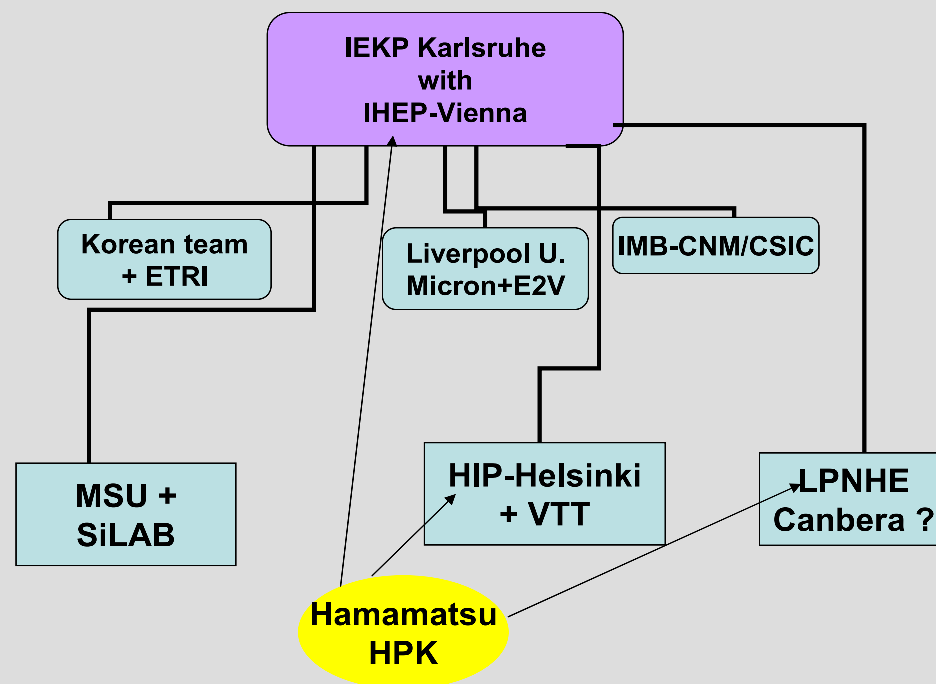
- Identify a 2nd and 3rd vendor with 6" large scale production capability (Presently Hamamatsu)
- Identify a company to produce 8“ sensors and work in close collaboration to bring the technology to HEP maturity.
- Production of 6" thin double sided sensors
- Investigate thin sensors together with the new readout chips for adequate S/N
- Try an alternative connection via bump bonding for silicon strip sensors
- Introduction of standard test structures on ALL wafers to have a real comparison and process monitoring



all this is on the way

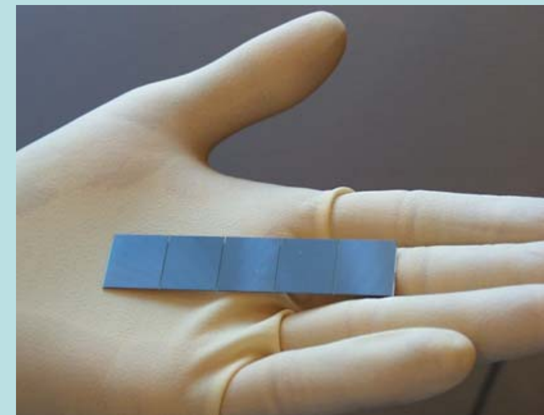
Experience and organization

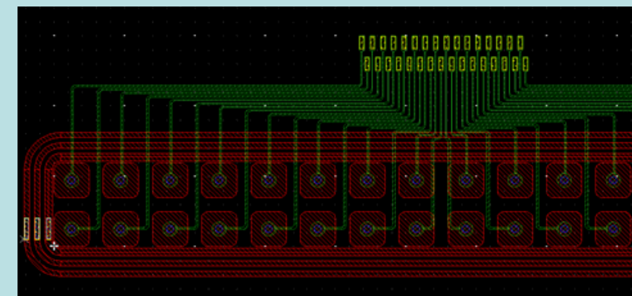
- Most SiLC Institutes have experience in sensor development or testing from previous experiment(s)
- Microelectronics research centers
- Connections with industry
- Several SiLC Institutes have sensor test capacity
- Vienna and Karlsruhe are coordinating the effort



VTT and HIP (Finland) capabilities

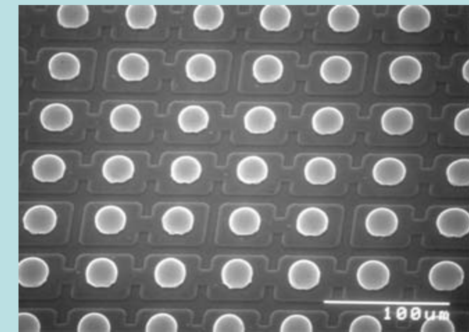
- Micronova: VTT Centre for micro- and nano-technology research
  - 3000 m2 cleanroom (including class 10)
  - Wafer size: 100 mm, 150 mm, 200 mm
  - Activities
    - Active IC and monolithic integration, Micromechanics, Photonics and Optical Communication Devices, Polymer and printable electronics, Advanced Materials and Processing Technologies, Superconducting electronics, Micropackaging
  - Silicon radiation sensors since 1989
    - Since 1989,various activities in early nineties
    - Original initiative from high energy physics (Helsinki University)
    - HEP contribution: LEP/L3 (60 cm ladder), Delphi, Fermilab 2 designs 1992, beamtelescope at CERN 1996
    - Space projects: Sixa, others
    - Spin-off 1992: Detection Technology (www.deetee.com)
    - APD, Strips, pixels, flurorescence, dosimetry, ...
    - Advanced technologies (3D)

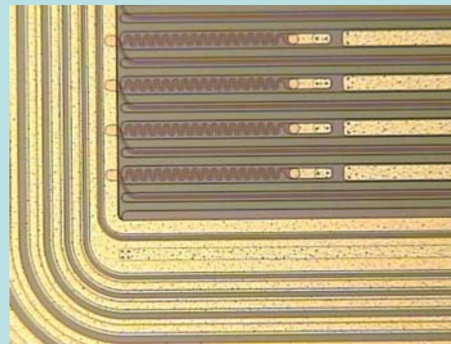


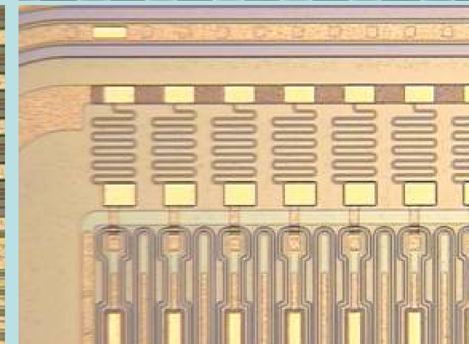


CNM (Barcelona) capabilities

- Spanish Institute for micro- and nano-technology
  - 1000 m² total surface, class 10.000 to 100
  - Wafer size 100 mm (Not for production, but important for technology development)
  - Activities:
    - Micro and nanosystems, silicon sensors, power devices, circuit design, packaging
  - Silicon radiation sensors since 1996
    - Technology development
    - Detector design, simulation, fabrication, and characterization
    - Double side, double metal processing
    - Pad, strips, pixels
    - Radiation effects
    - Worked in ATLAS and RD50
    - Medical imaging





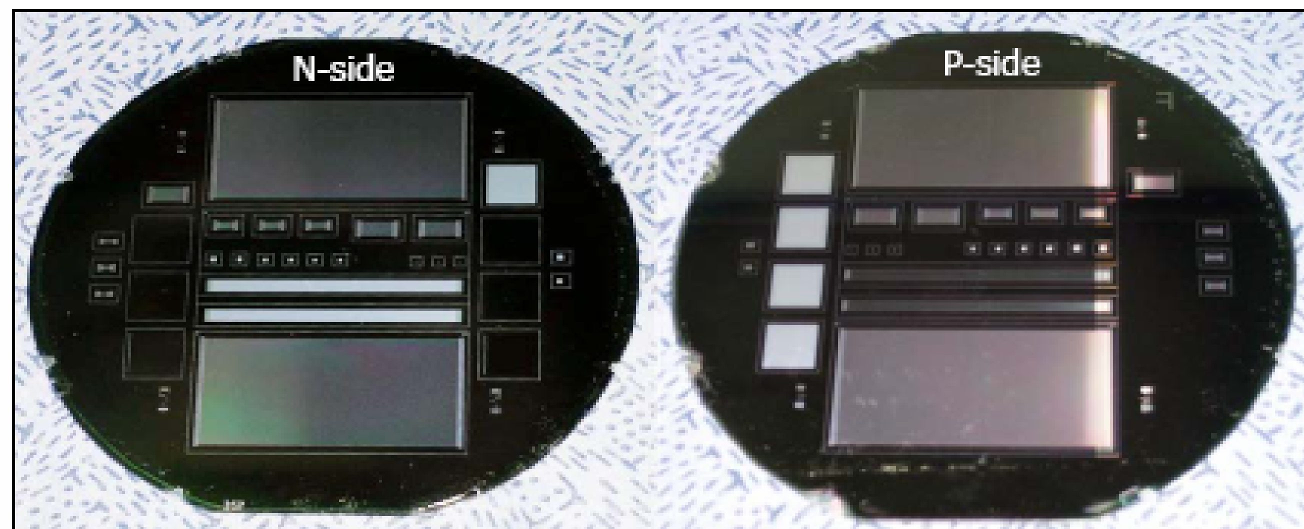


The Korean way

- Example of institute collaborating with research center and industry for developing new microstrip sensors

Sensor R&D:
DC-type DSSD
Development

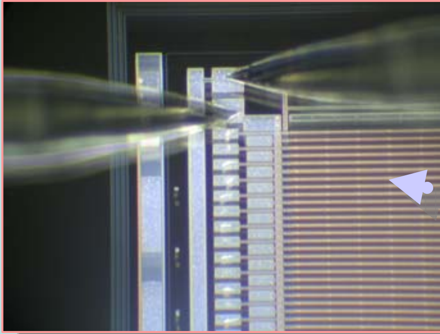
Prototype

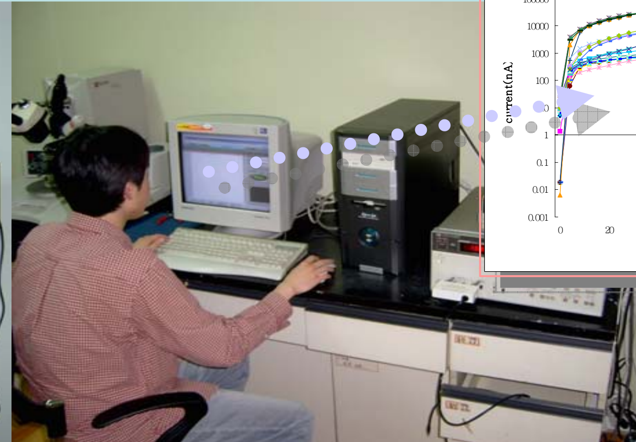


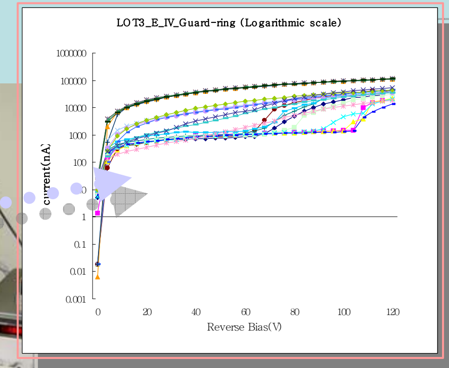
wafer	TOPSIL (5inch, high resistivity, (100), FZ, DSP)	strip width	9 μm
		strip pitch	50(100) μm
thickness	380 μm	readout pitch	50 μm
size	51 x 26 mm^2	readout channel	512(512)

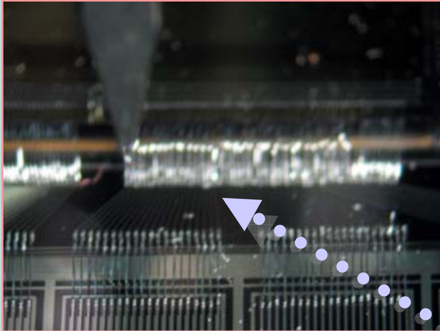
Bangalore

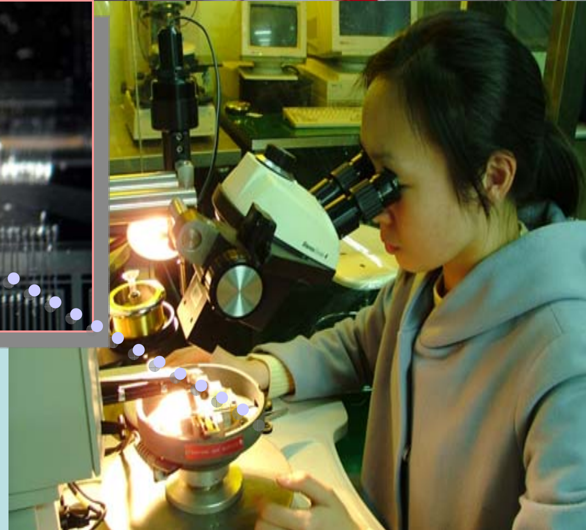
Lab infrastructure

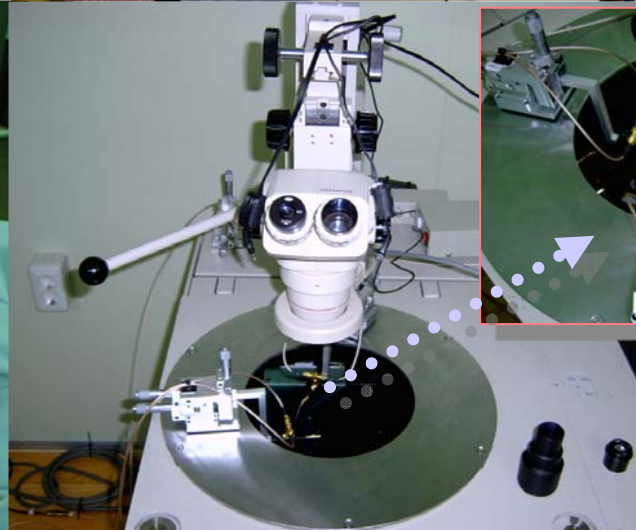


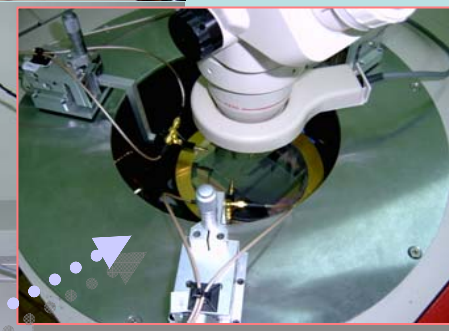




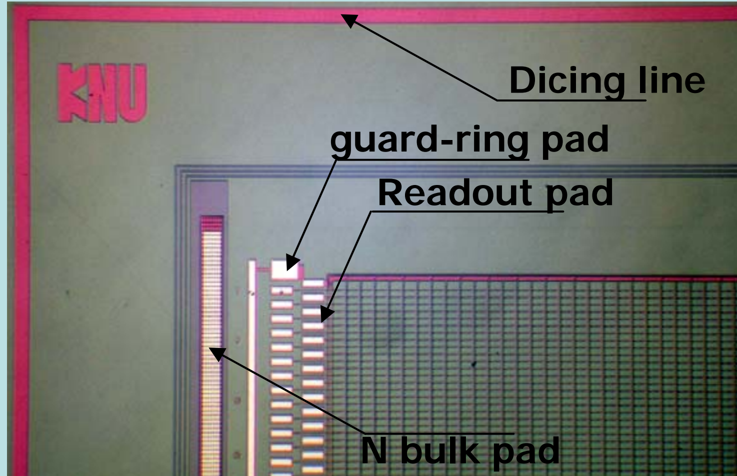


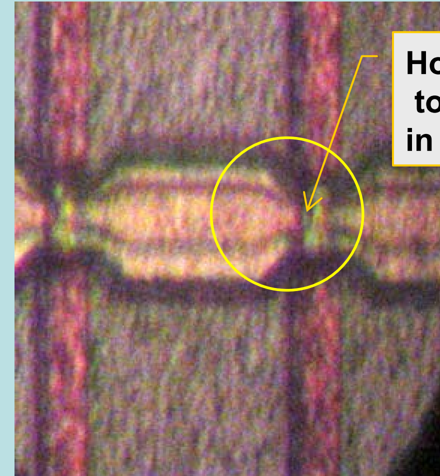






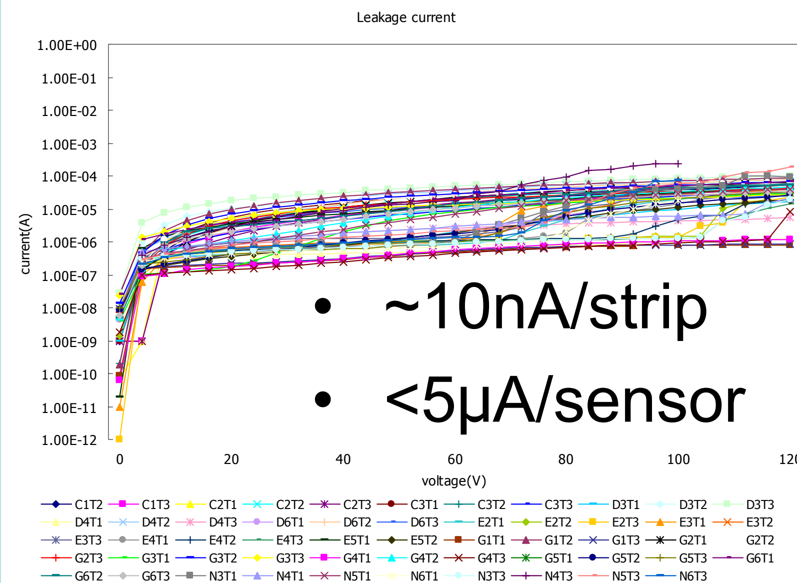
DC Double-sided Silicon Strip Sensor

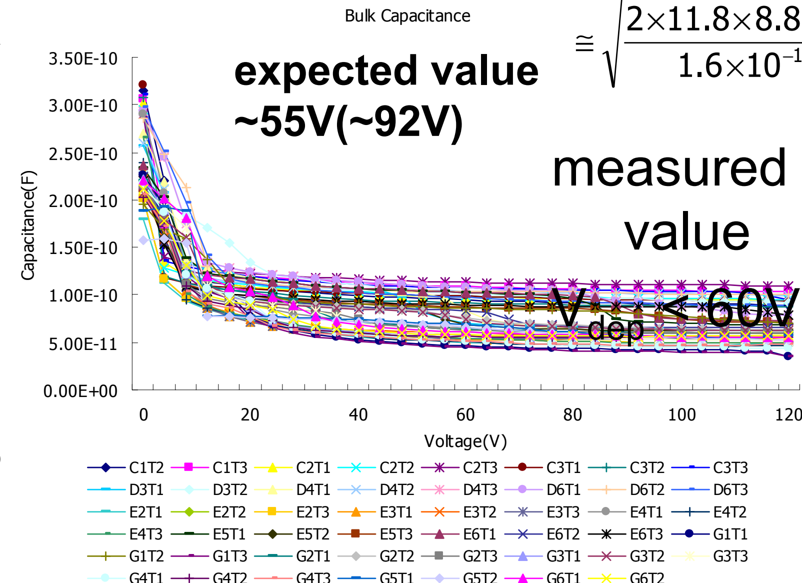




Hour-glass pattern on the p-side to reduce the capacitance in the double metal structure

$$d = \sqrt{\frac{2\varepsilon\varepsilon_0}{qN_D} V_{dep}} \cong \sqrt{\frac{2\times 11.8\times 8.854\times 10^{-14}}{1.6\times 10^{-19}\times N_D} V_{dep}}$$





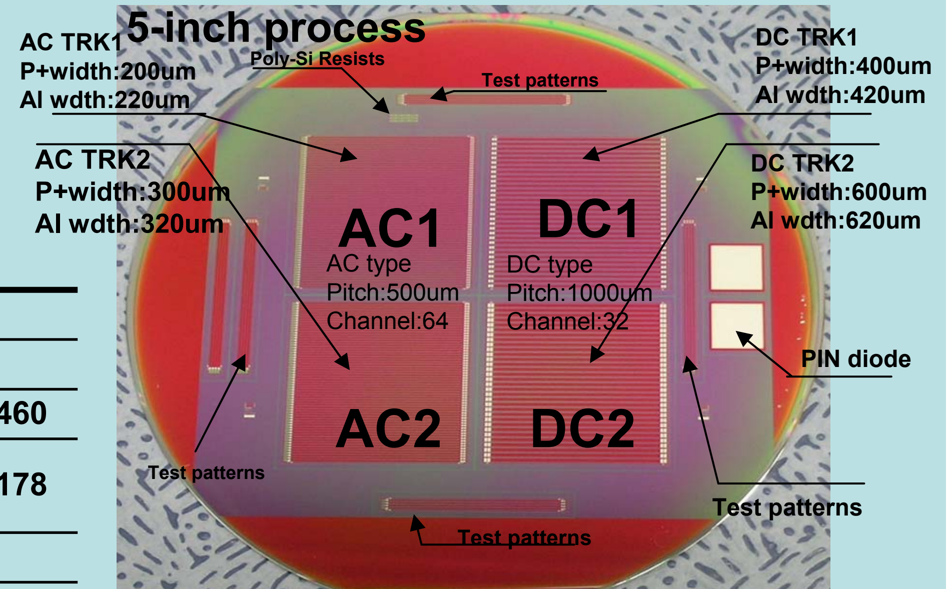
I_d v.s. V

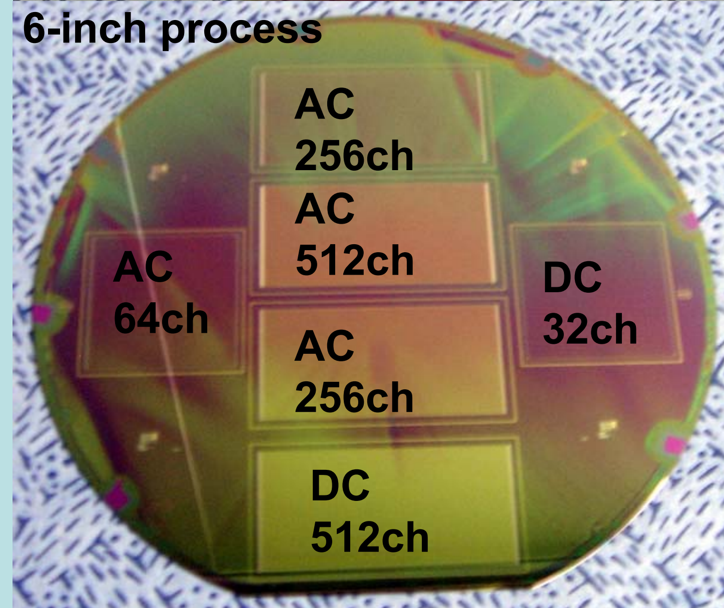
C v.s. V

Fabrication of AC/DC SSD

AC-coupled Single-sided Silicon Strip Detector

	5-inch		6-inch	
thckness(μm)	380		400	
Area (μm²)	35000 × 35000		55610 x 29460	
Effective area (μm²)	31970 × 31970		51264 x 25178	
SiO_2 layer thickness (nm)	1000		250	
Polysilicon length (μm)	10		8	
Polysilicon width (μm)	13500		480	
sheet resistance(kΩ)	~25		~400	
	Type1	Type2	Type1	Type2
Number of strips	64	64	256	512
Strip pitch (μm)	500	500	100	50
Strip width (μm)	200	300	8	8
readout width (μm)	220	320	12	12





Latest R&D developments

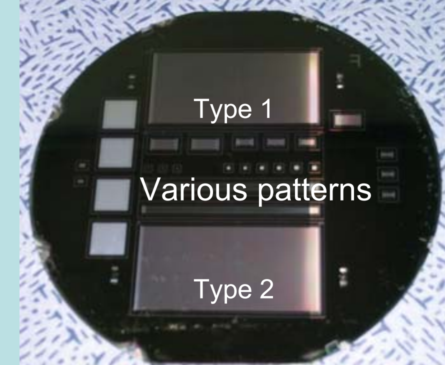
- yield

type	DC-type	AC-type
single-sided	90%	80%
double-sided	< 30%	N/A

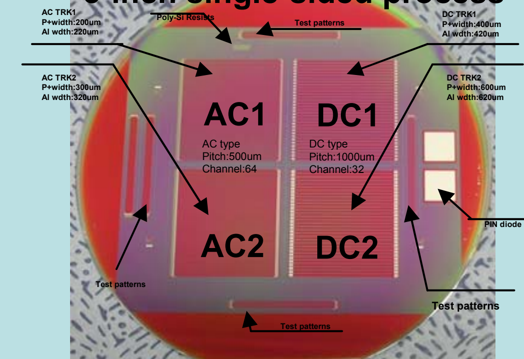
- fabrication line

line	DC-type	AC-type
5 inch	double/single-sided	single-sided
6 inch	single-sided	single-sided (in progress)
8 inch	**thickness (725 um, can be thinned ~500 um)**	

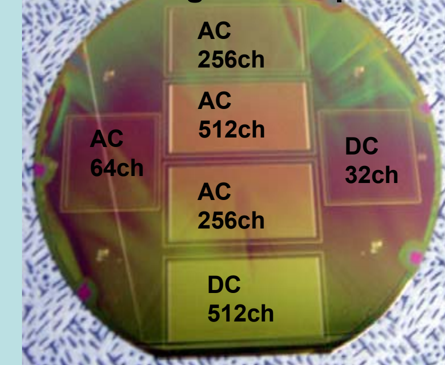
5-inch double-sided process



5-inch single-sided process

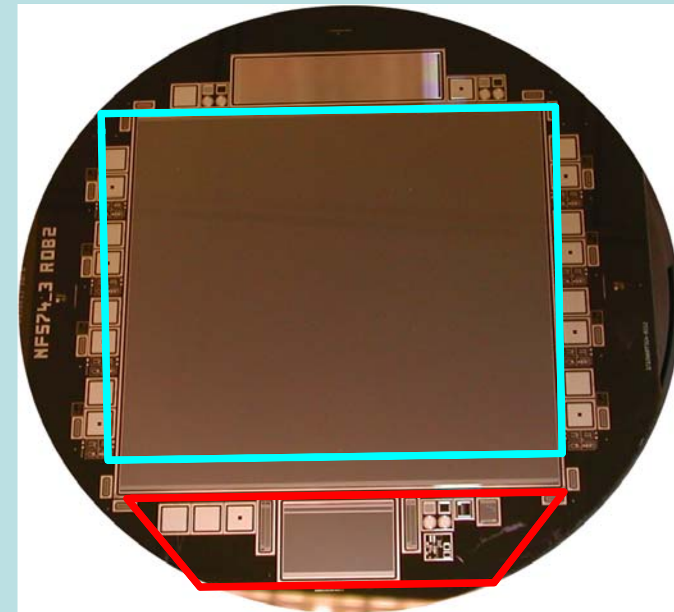


6-inch single-sided process



Coordination by Vienna and Karlsruhe

- Both, Vienna an Karlsruhe worked a long time already with silicon sensors
  - DELPHI @ LEP
  - CDF @ Fermilab
  - CMS @ LHC
- Have experience in
  - Strip-by-strip characterization of Si strip sensor
  - Process monitoring with test structures
  - Proton irradiation facility in Karlsruhe
    - Post irradiation characterization

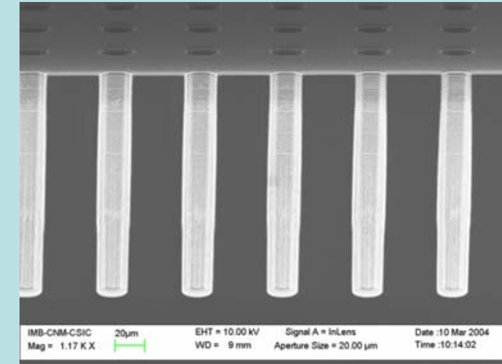


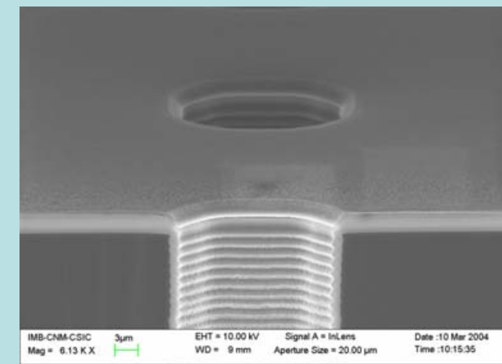
- Examples of experience on QC section

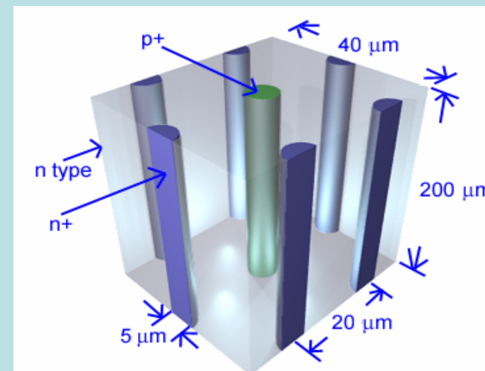
Novel technologies: 3D

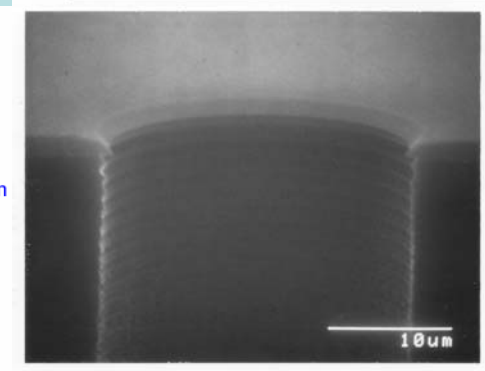
- 3D technologies based on deep Si etching
  - Deep hole or trench etching
  - Aspect ratio 24:1
  - In SiLC developed by VTT, HIP and CNM
- 3D detectors (S. Parker, Hawaii)
  - Electrodes penetrating through the Si
  - Different topologies:
    - semi 3D, true 3D, 2.5D, two side 3D,...
  - Pixels, strips, stripixels
  - Very low depletion voltage (few volts)
  - Very fast (t<3ns)
  - No charge sharing
  - Relevant for high radiation dose

3D detectors not for LC,
but the technology yes



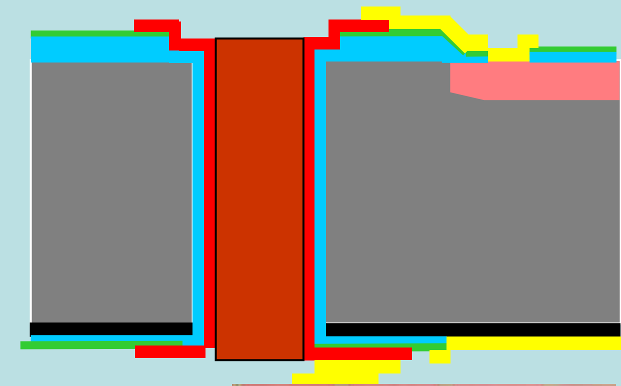


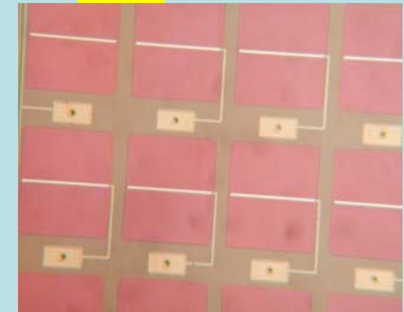


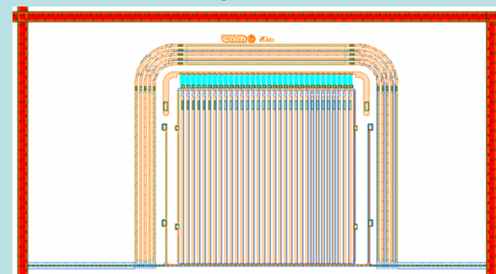


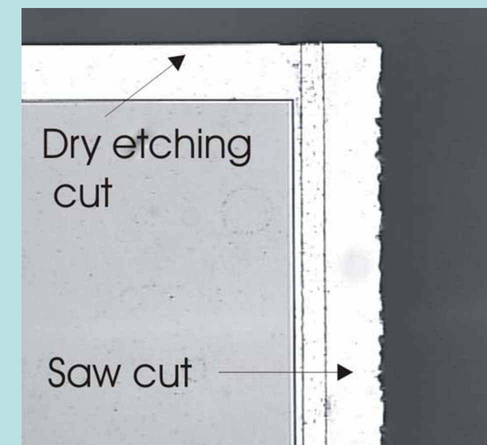
Novel technologies: 3D

- Same deep Si etching technology
- 3D readout
  - reduced area for read-out lines: large area devices
  - constant pixel capacitance
  - mechanical: FC or CSP joining sensors
- Edgeless detectors
  - Deep trench etching
  - Active silicon area very close to beam
  - Edges patterned by deep RIE
  - Minimum distance 25 μm
  - Combined with 3D all side buttable: very large area systems



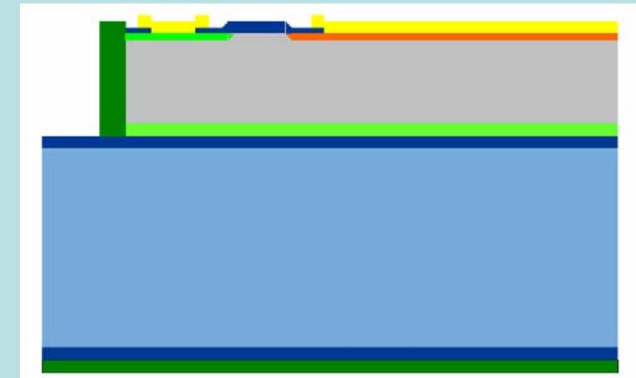


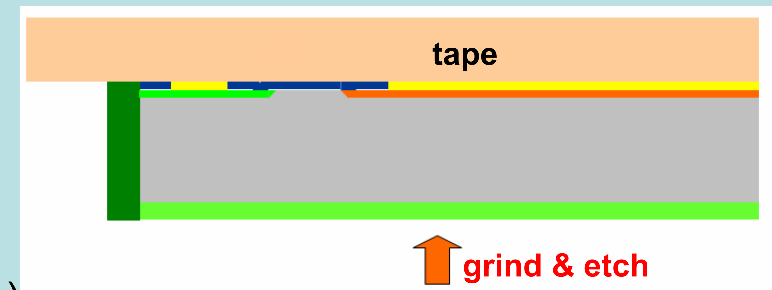




Novel proposal: Edgeless Thin Detector

- Edgless Microstrip Thin Detector (VTT)
  - Starting point: two wafers bonded,
    - one is thinned, acting as sensor
    - the second is only a support structure, released at the end of the fabrication
  - Using DRIE, trenches are made, filled with doped poly
  - Detectors are diced with DRIE again.
  - Finally they are bonded to tape and the support wafer released.
  - End of the process: thin detector
    - Electrically connected without the need of using wire bonding;
    - Backside contact is made from the front through doped poly (dark green in the figure).





- Active edge (dead space≈20 µm) achieved through deep silicon etching & n-type poly fill
- Dicing: the chips are diced using deep Si-ething released from the support substrate

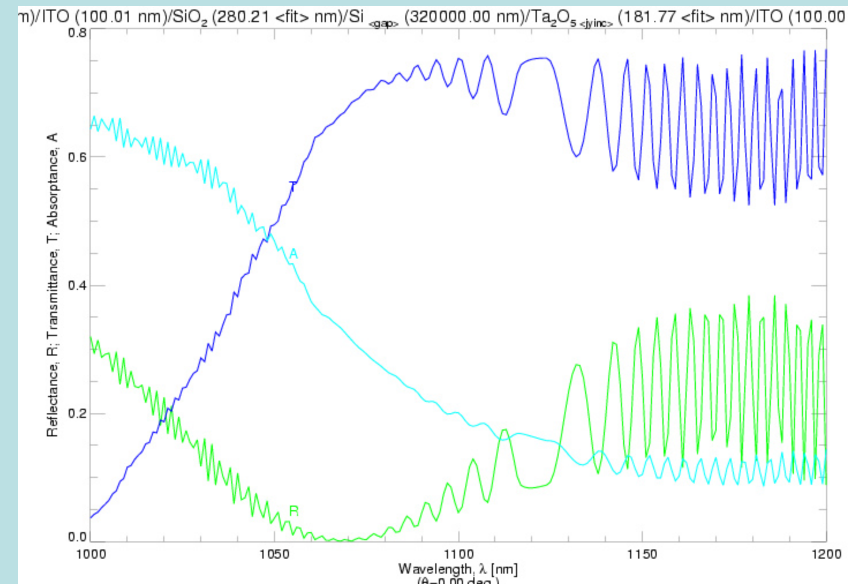
1st prototypes by July '07

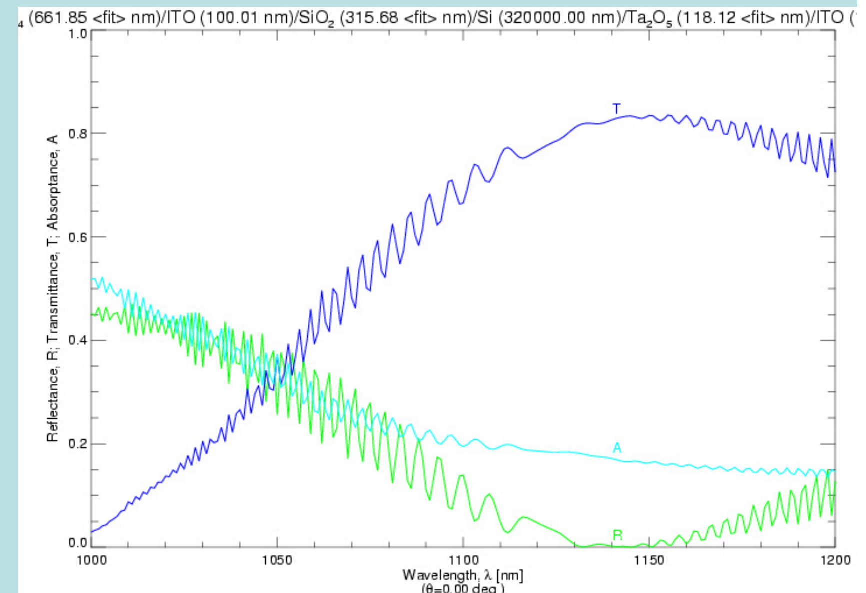
IR transparent detectors

- Alignment strategy with laser beams as straight tracks based on AMS and CMS achievements (as shown previously)
  - InfraRed Laser beams propagate through several silicon modules
  - Signal is readout using module electronics
- Both in AMS and CMS standard sensors modified
  - Transmittance < 50%
- We propose to design from the beginning IR transparent sensors:
  - Substitute Al electrodes (strips and backplane) by transparent electrodes (TCO) as ITO (In doped SnO_2) or AZO (Al doped ZnO)
  - Design proper antireflective coating (ARC) using standard microelectronics layers (SiO_2, Si_3N_4)
  - Take into account all sensor layers
  - Detailed information from manufacturer needed
  - Check if with new technological design there is electrical behavior degradation

IR transparent detectors

- Preliminary simulations
  - Transmittances up to 80% can be achieved
  - Zero reflectances
  - Absorbance > 20%; >5% in Si: good signal
  - Important to simulate changes in %T with layer thickness tolerances
- Multilayer design has to be tolerant to allow small changes in %T for moderate changes of layer thickness
- Complex refraction index of materials is wavelength and process dependent:
  - Measure samples to simulate reliable designs
- Strips structure will be modelled as surface roughness





IR transparent detectors

- R&D Proposal by IFCA and CNM
  - Provide by CNM with suitable samples of different layers and thicknesses for optical characterization at the desired wavelength
  - Assess fabrication tolerances of the different layers
  - Study optical coefficient variation in SiO_2 and Si_3N_4 achievable by deposition condition variation
    - To have room for the ARC optimization
  - Optimization of the vertical layout for maximum %T with reasonable %A
    - Different options are acceptable at this stage
  - Account for process variations
  - Fabricate test samples with suitable mask set
  - Bond to readout electronics
  - Optical and electrical test
- Samples have to be designed and tested both, as photosensors and as charged particle detectors
- If success: transfer technology to companies

Pixels: Introduction

- There (at least) two main questions to be answered before choosing R&D directions:
  - Which should be the macro-pixel (order of magnitude: $50 \times 500\ \mu m^2$?) or mini-strip or strip size? (See simulation section)
  - Which is the amount of material that can be tolerated? (No more that 0.5% X_0 per layer in this region)
- Before knowing the answer there are many potential directions to be investigated:
  - Hybrid technologies with bump bonding or 3D connectivity with direct wafer attachment
  - Import Vertex technologies (agreements required):
    - DEPFET, MAPS, SOI...
    - Determine maximum (allowed by technology) pixel size
    - Possibility to connect various pixels to a single channel building a short strip or macro pixel
- The feasibility of making large pixels is to be investigated as a spin-off and close collaboration with existing R&D for vertex detectors

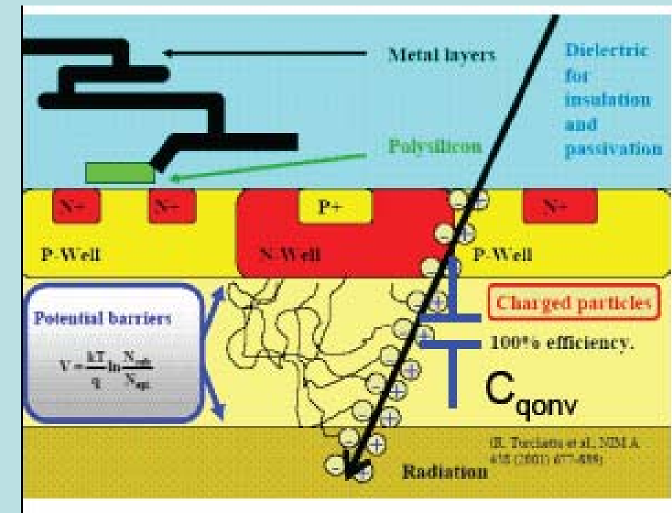
Pixels outside the Vertex

Possible solutions to evaluate:

- Internal barrel:
  - Closest layer to the vertex detector may require finer granularity
    - Very short strips or macro pixels (few microns times few mm up to a cm):
      - Could provide enough resolution in Z (barrel) or R(endcap)
    - Could one import Vertex technologies with larger pixels ?
  - Inner layer(s) further out (r ~ 10/15 - 30/40 cm)
    - 2 Single sided back-to-back strip sensors with stereo angle:
      - Twice as much material
    - 1 double sided strip sensor with stereo angle
- Endcap:
  - Standard size pixels in first disks, but others could have bigger cell size (save in electronics channels)

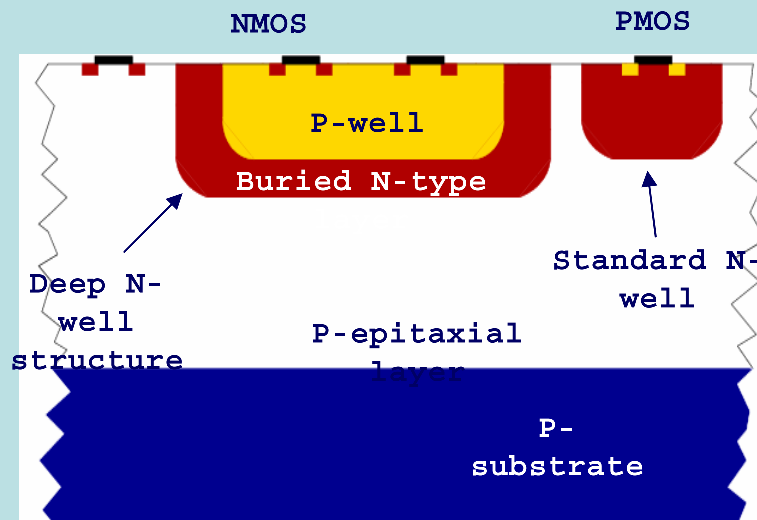
CMOS MAPs epitaxial

- Technologies with epitaxial layer:
  - A possible way to use this scheme for tracking with large pixels (but not too large) is to add the signal of several pixels. Problems:
    - Noise increases as sqrt(2). Possible solution: to discriminate pixels with charge >3σnoise...
    - Uniformity.
  - There are some proposals to create an electric field in the pixel increasing charge collection efficiency and allowing to use both kind of MOS transistors: these could make possible complex electronics (CSP) in-pixel, thus making larger pixels.
    - P. Rehak, NIMA, vol. 568, 1, pp 167-175, 2006



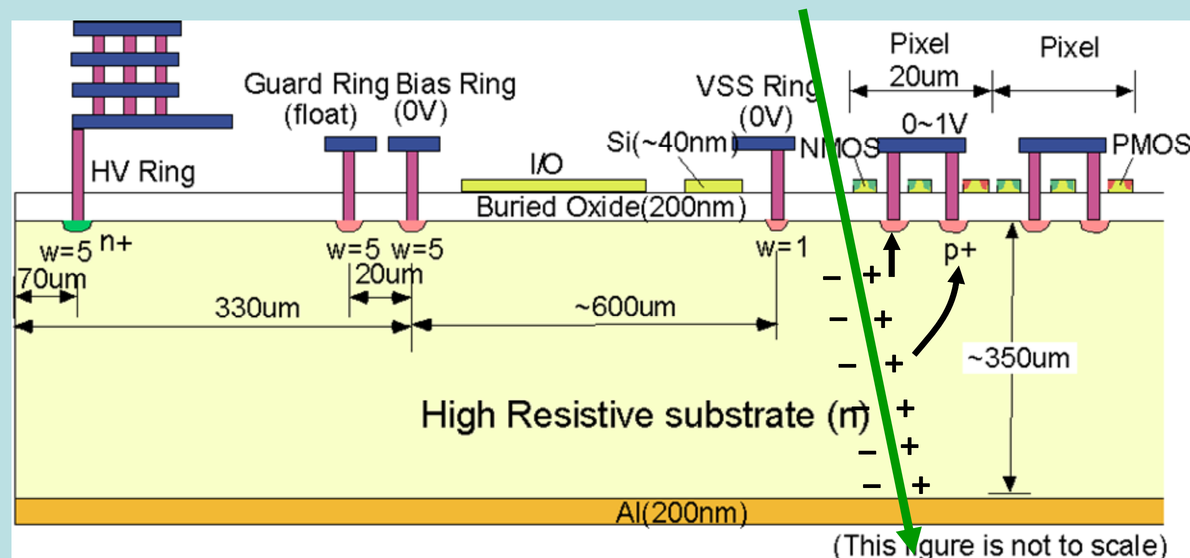
CMOS MAPs epitaxial and triple well

- Technologies with epitaxial layer and triple well
  - Possible to build large pixels: not rely on small parasitic capacitance of pixel to convert charge to voltage.
  - Problems:
    - Effect of N-well for PMOS (charge sharing)
    - Uniformity
    - Cost: all the technos are DSM, in contrast MAPS without triple well can be implemented in more “accessible” technos (AMS,...)



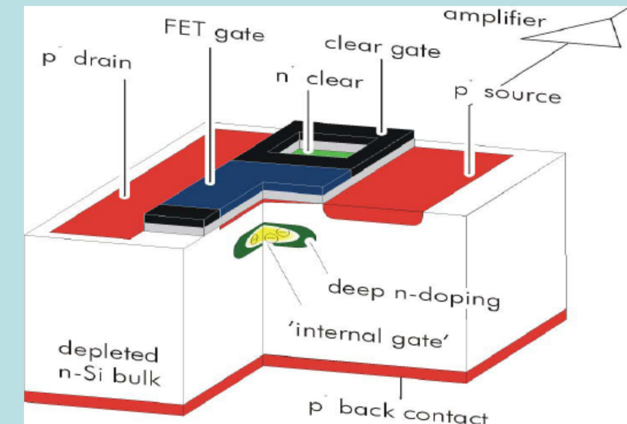
SOI

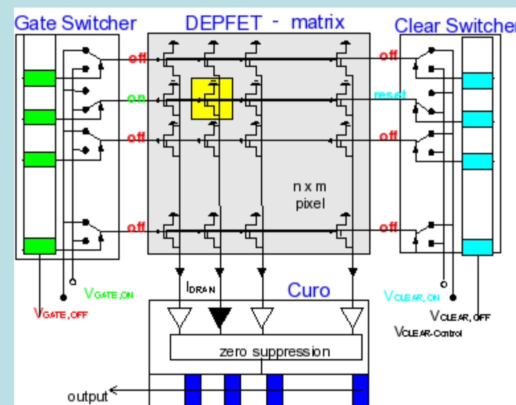
- Possible to build large pixels: not rely on small parasitic capacitance of pixel to convert charge to voltage.
- Large and fast signal!
- Problems: Access to the technology (not yet standard technologies)

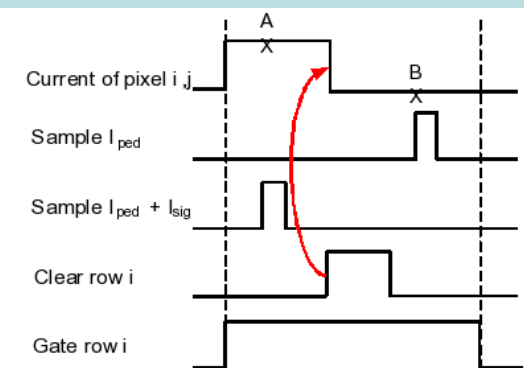


DEPFETS

- DEPFETS:
  - Ideally very good candidates:
    - Low power consumption:
      - Sensor: 0.5 mW/active device
      - ASICs: SWITCHER 6.3mW/active channel
        CURO: 5mW/channel
    - Depleted: higher signal
    - What is the maximum cell size providing adequate signal uniformity?
    - If various pixels connected: noise increases only as sqrt(L) instead of L
  - Issues:
    - Price...
    - Could we do timing? If not we can still rely on external layers.



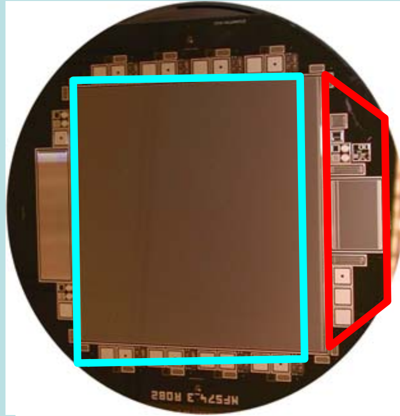


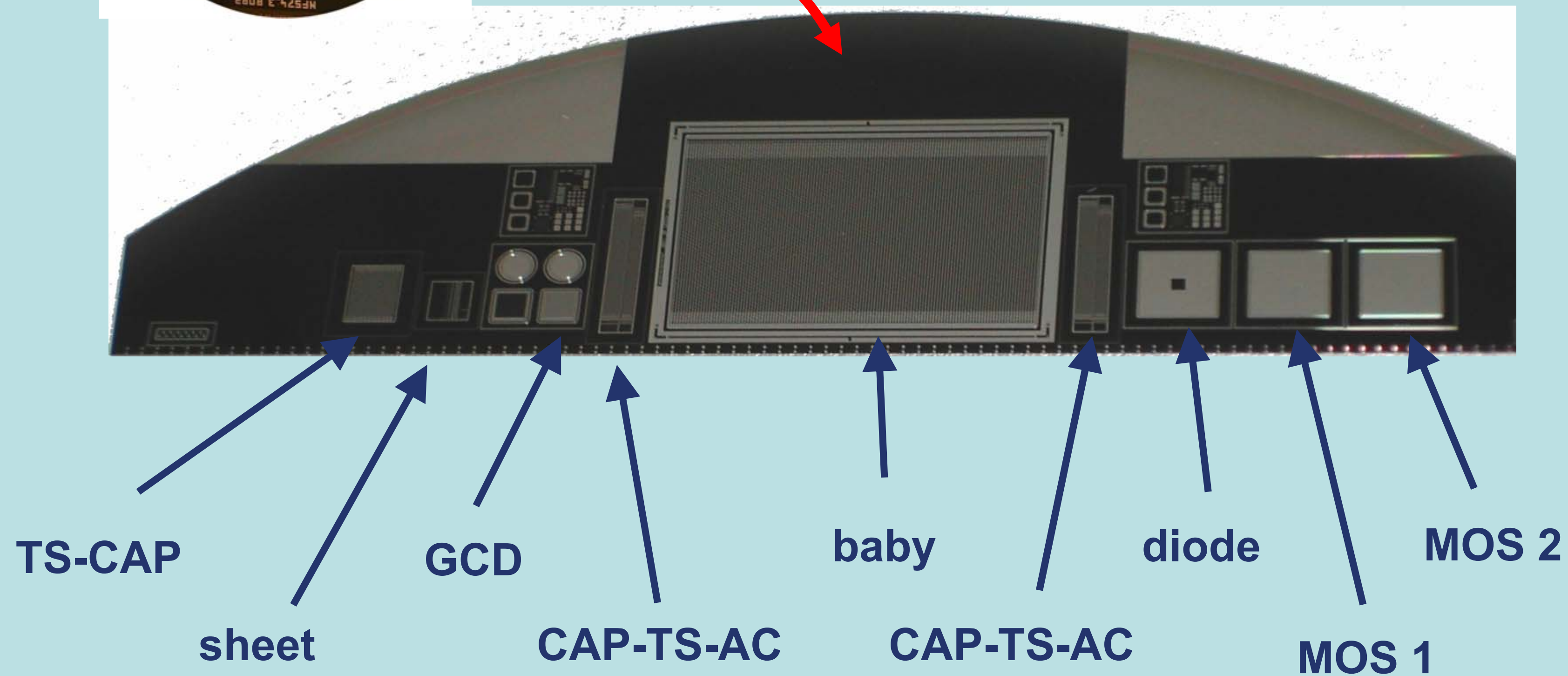


Process Monitoring on Test Structures

HEPHY Vienna

“Standard Half moon”
9 different structures
Use to determine one parameter per structure

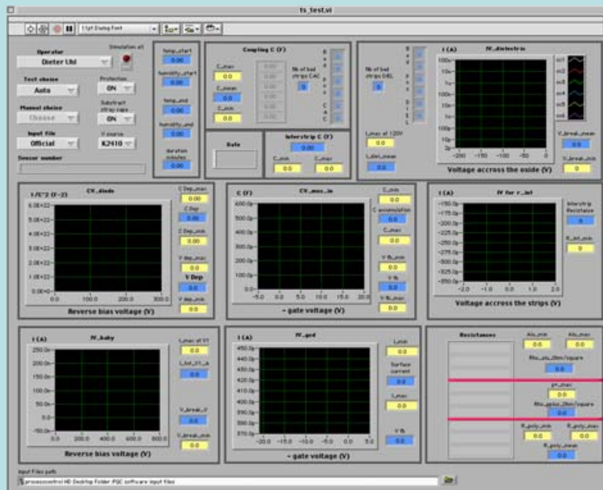




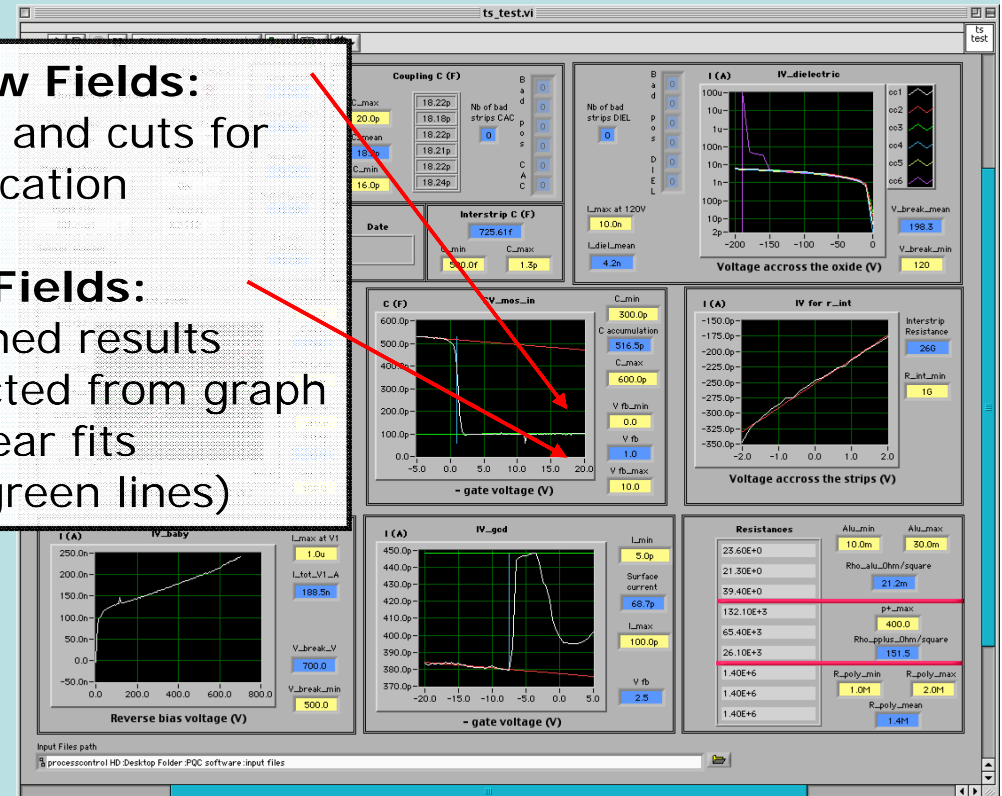
Test structures Measurement Software

HEPHY Vienna

Before run:



After run:



Yellow Fields:
Limits and cuts for qualification

Blue Fields:
Obtained results extracted from graph by linear fits (red/green lines)

- LabVIEW program
- Fully automatic measurement procedure (~30 minutes)
  - Except alignment of Half moon and placement of probecard
- Automatic extraction of parameters

Thinning

- SiLC is interested, since its beginning, in the possibility of thinning the substrate of larger dimension sensors by a factor 2 or 3.
- This is under investigation and contacts with industrial firms are under exploration or being established, with several possibilities, for instance in France, UK or Russia (SILAB)