SiLC
ELECTRONICS R&D
currently concentrating on the FEE

Two approaches

The TOT approach

The DSM FE and readout electronics

SCIPP R&D on Time-Over-Threshold Electronics and Long-Ladder Readout

Beijing Linear Collider Workshop

Beijing, China

February 4-8 2007

Bruce Schumm

The SCIPP/UCSC SiLC/SiD GROUP (Harwdare R&D Participants)

Faculty/Senior	Post-Docs	Undergrads
Vitaliy Fadeyev	Jurgen Kroseberg	Greg Horn
Alex Grillo	Lei Wang	Luke Kelley
Bruce Schumm		Patrick Au

Lead Engineer: Ned Spencer

Technical Staff: Max Wilder, Forest Martinez-McKinney

All participants are mostly working on other things (BaBar, ATLAS, biophysics…)

Students are undergraduates from physics and engineering

FOCUS AND MILESTONES

Goal: To develop readout generically suited to any ILC application (long or short strips, central or forward layers)

Current work focused on long ladders (more challenging!):

- Front-end electronics for long (>1 meter) ladders
- Exploration of sensor requirements for long ladders
- Demonstration (test-beam) of < 10 μm resolution mid-2008

After long-ladder proof-of-principle, will re-optimize (modest changes) for short-strip, fast-rate application

We also hope to play an increasing role in overall system development (grounding/shielding, data transmission, module design and testing) as we have on ATLAS and GLAST

BRIEF SUMMARY OF STATUS

Testing of 8-channel (LSTFE-1) prototype fairly advanced:

- Reproducible operation (4 operating boards)
- Most features working, with needed refinements understood
- A number of "subtleties" (e.g. channel matching, environmental sensitivity) under control
- Starting to make progress on fundamental issues confronting long-ladder/high-resolution limit.

Design of 128-channel prototype (LSTFE-2) well underway (April submission)

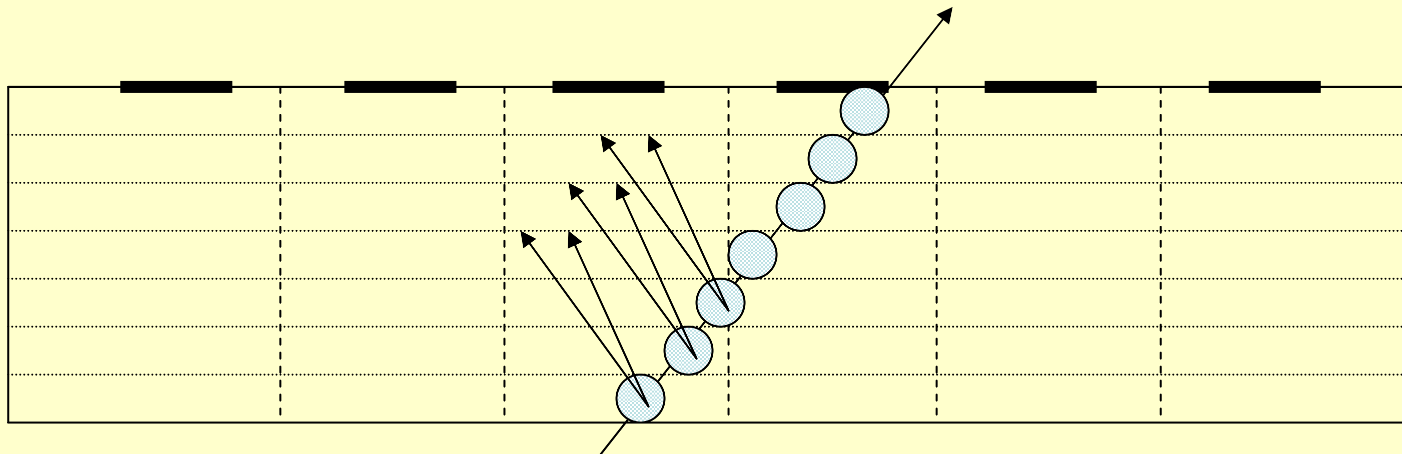
Now for the details…

Pulse Development Simulation

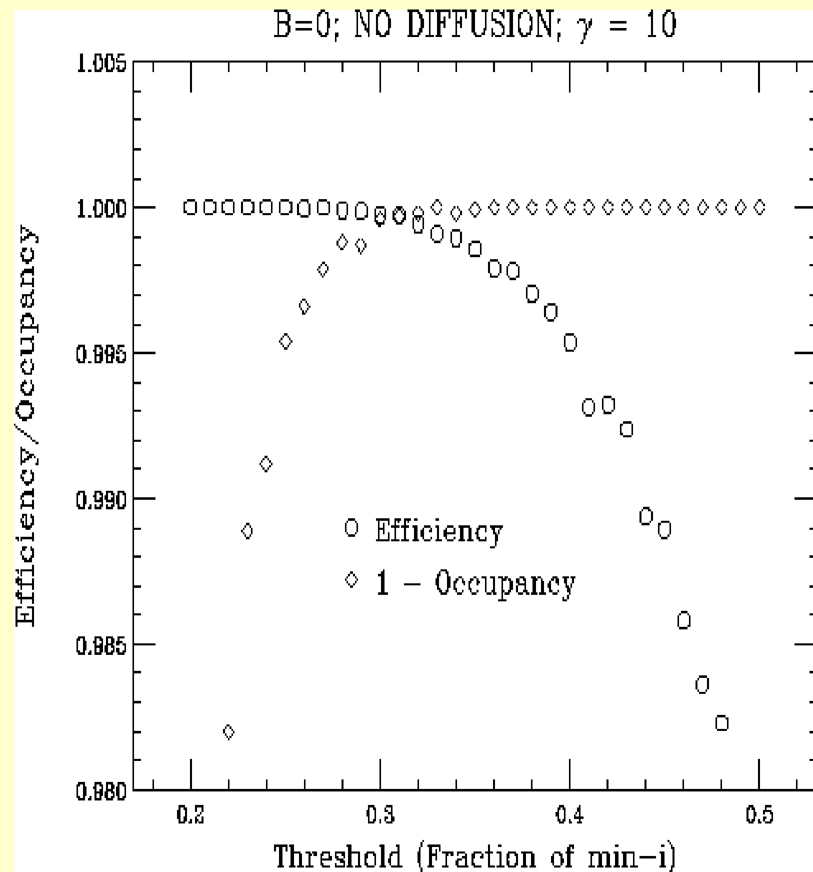
Christian Flacco & Michael Young (Grads); John Mikelich (Undergrad)

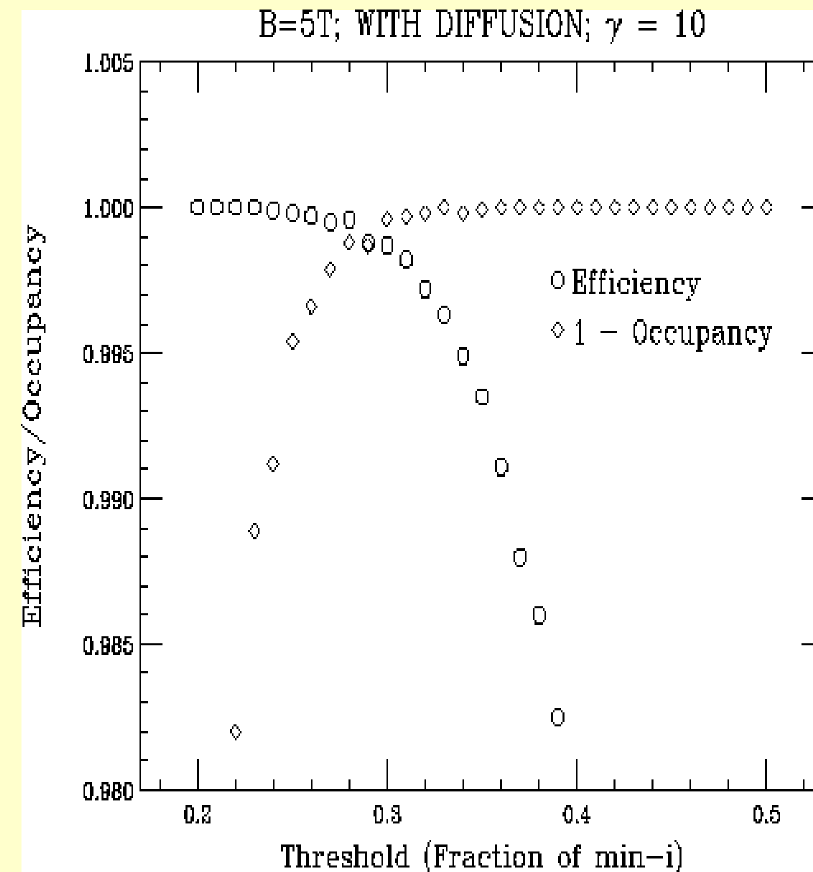
Long Shaping-Time Limit: strip sees signal if and only if hole is collected onto strip (no electrostatic coupling to neighboring strips)

Include: Landau deposition (SSSimSide; Gerry Lynch LBNL), variable geometry, Lorentz angle, carrier diffusion, electronic noise and digitization effects

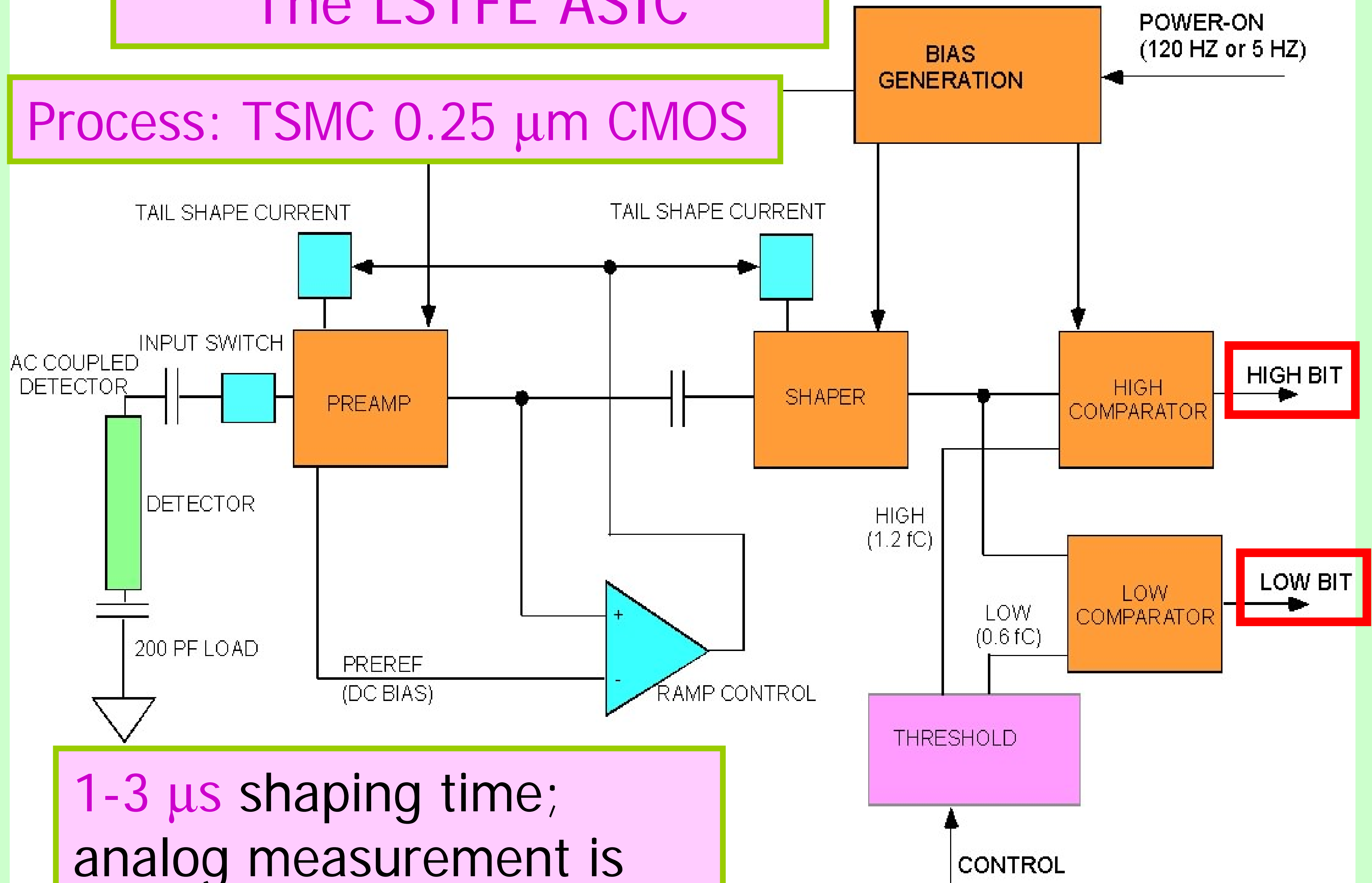


Simulation Result: S/N for 167 cm Ladder (capacitive noise only)

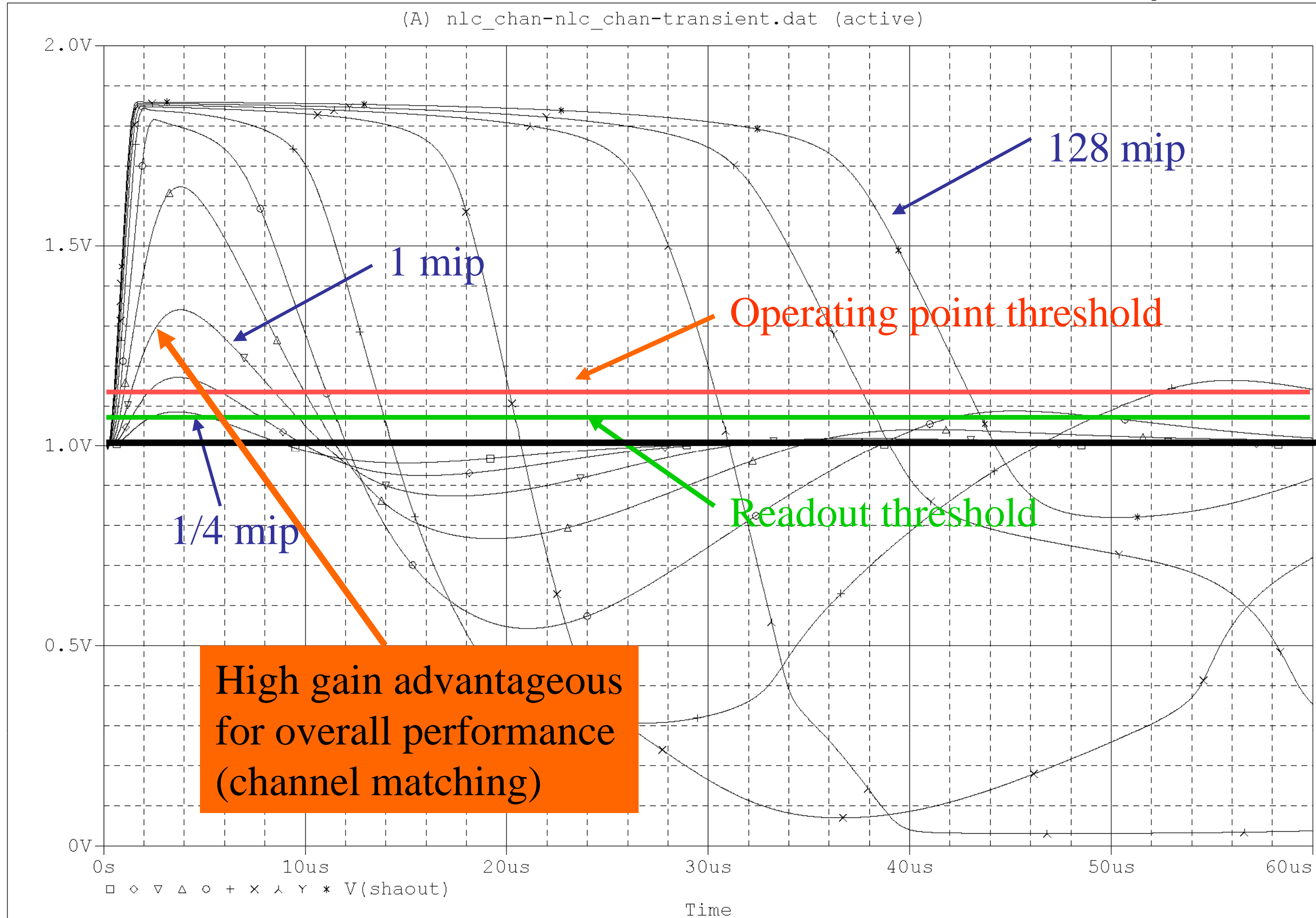




Simulation suggests that long-ladder operation is feasible



The LSTFE ASIC
Process: TSMC 0.25 μm CMOS
BIAS GENERATION
POWER-ON (120 HZ or 5 HZ)
TAIL SHAPE CURRENT
TAIL SHAPE CURRENT
INPUT SWITCH
AC COUPLED DETECTOR
PREAMP
SHAPER
HIGH COMPARATOR
HIGH BIT
DETECTOR
HIGH (1.2 fC)
LOW COMPARATOR
LOW BIT
LOW (0.6 fC)
200 PF LOAD
PREREF (DC BIAS)
RAMP CONTROL
THRESHOLD
CONTROL
1-3 μs shaping time; analog measurement is Time-Over-Threshold


** Profile: "nlc_chan-transient" [C:\Projects\NLC\preampTSMCmodels\nlc_chan-nlc_chan-transient.sim]
Date/Time run: 01/02/04 14:15:19
Temperature: 27.0
(A) nlc_chan-nlc_chan-transient.dat (active)
2.0V
1.5V
1.0V
0.5V
0V
0s
10us
20us
30us
40us
50us
60us
V(shaout)
Time
Date: January 02, 2004
Page 1
Time: 14:18:43
128 mip
1 mip
Operating point threshold
Readout threshold
1/4 mip
High gain advantageous
for overall performance
(channel matching)

Electronics Simulation: Resolution

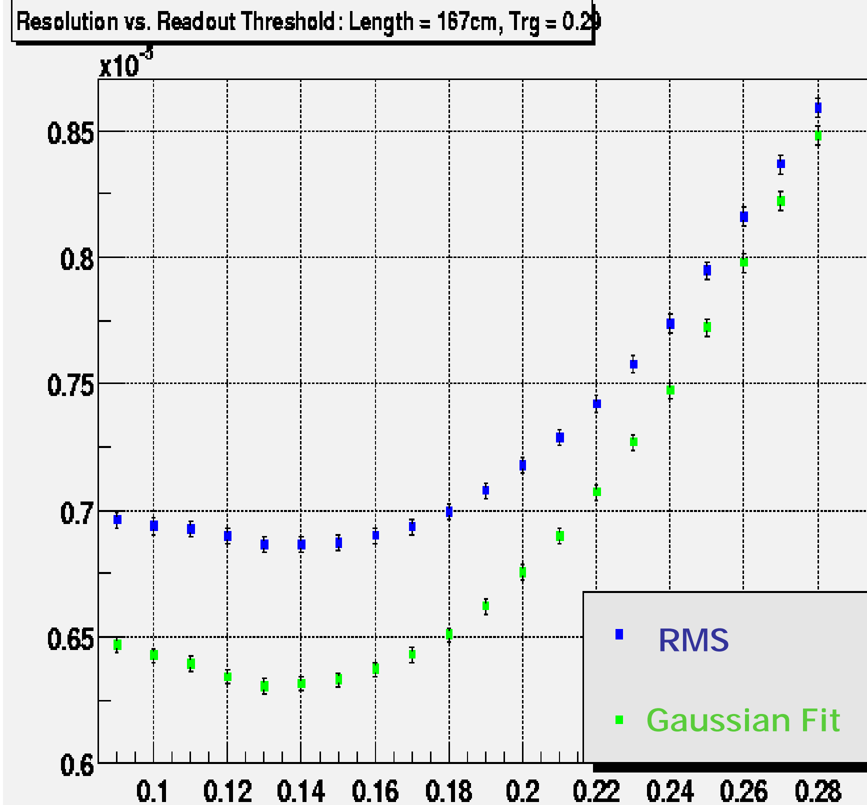
Detector Noise:

Capacitive contribution; from SPICE simulation normalized to bench tests with GLAST electronics

Analog Measurement:

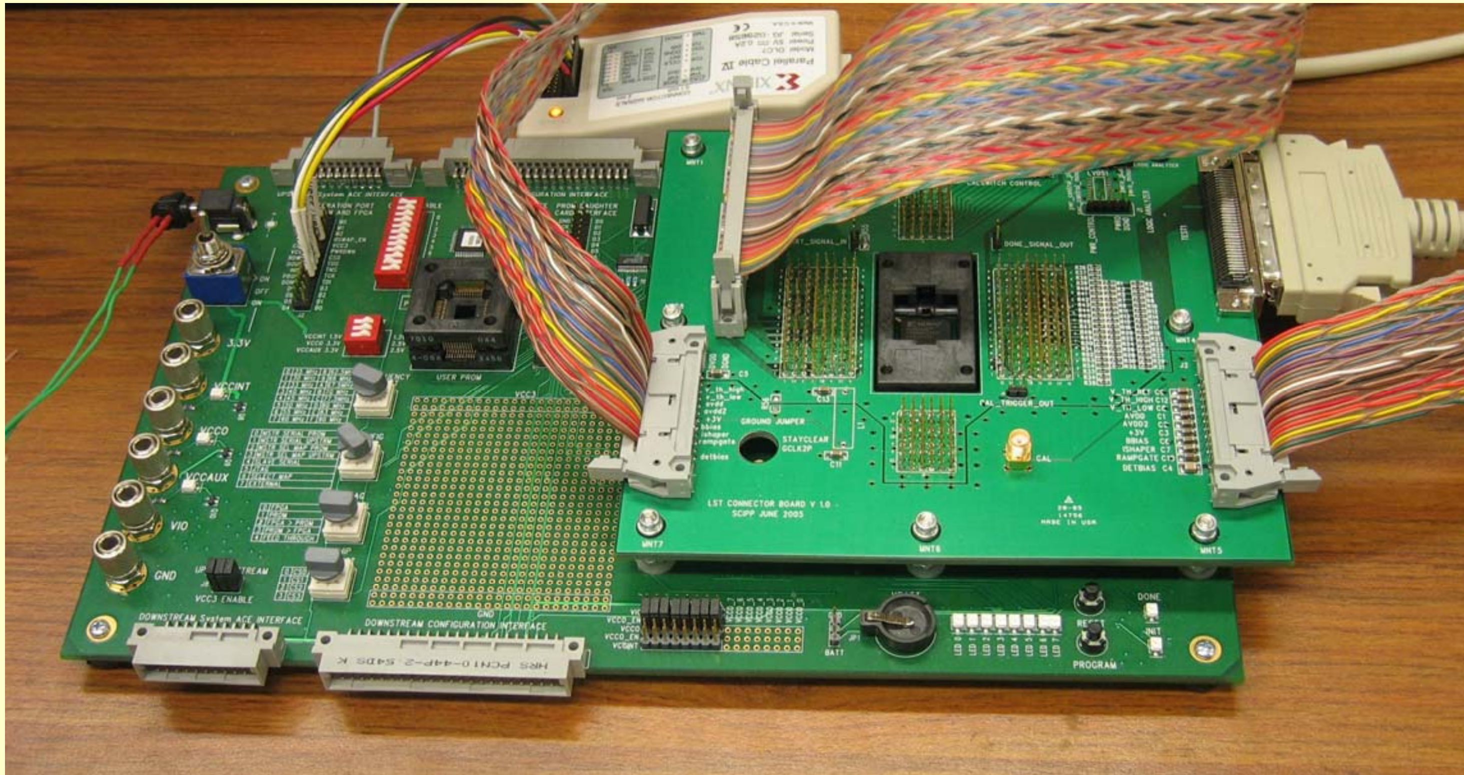
Provided by time-over-threshold; lookup table provides conversions back into analog pulse height (as for actual data)

Detector Resolution (units of 10μm)



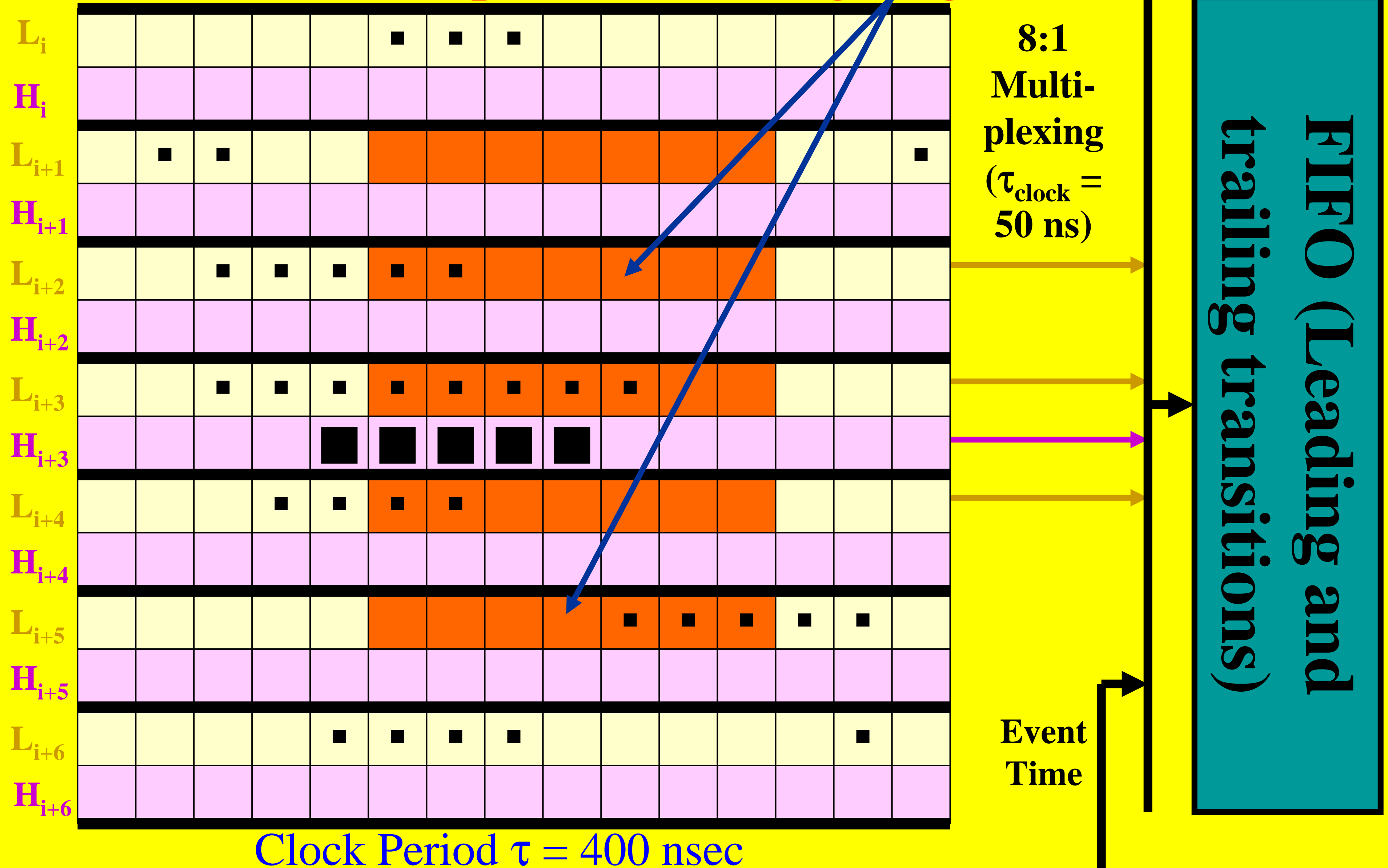
Lower (read) threshold in fraction of min-i
(High threshold is at 0.29 times min-i)

DIGITAL ARCHITECTURE: FPGA DEVELOPMENT



Digital logic under development on FPGA (Wang, Kroseberg), will be included on front-end ASIC after performance verified on test bench and in test beam.

Proposed LSTFE Back-End Architecture



Note on LSTFE Digital Architecture

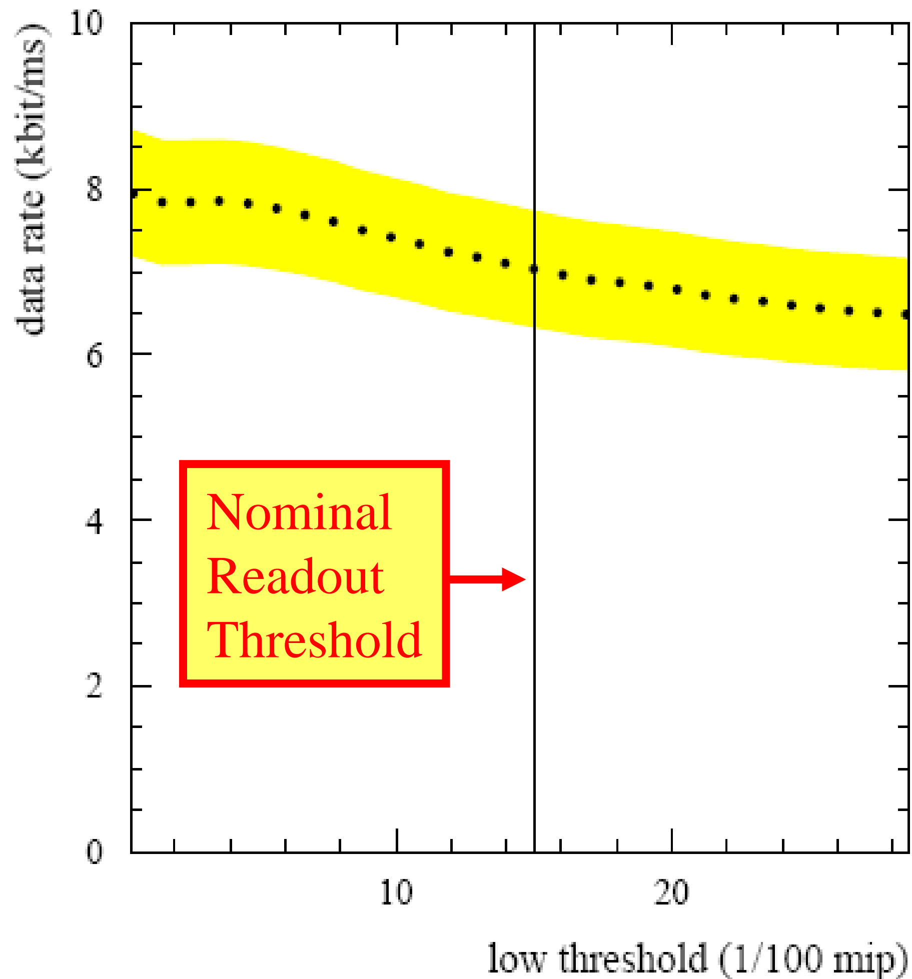
Use of time-over-threshold (vs. analog-to-digital conversion) permits real-time storage of pulse-height information.

➔ No concern about buffering

➔ LSTFE system can operate in arbitrarily high-rate environment; is ideal for (short ladder) forward tracking systems as well as long-ladder central tracking applications.

DIGITAL ARCHITECTURE SIMULATION

ModelSim package permits realistic simulation of FPGA code (signal propagation not yet simulated)

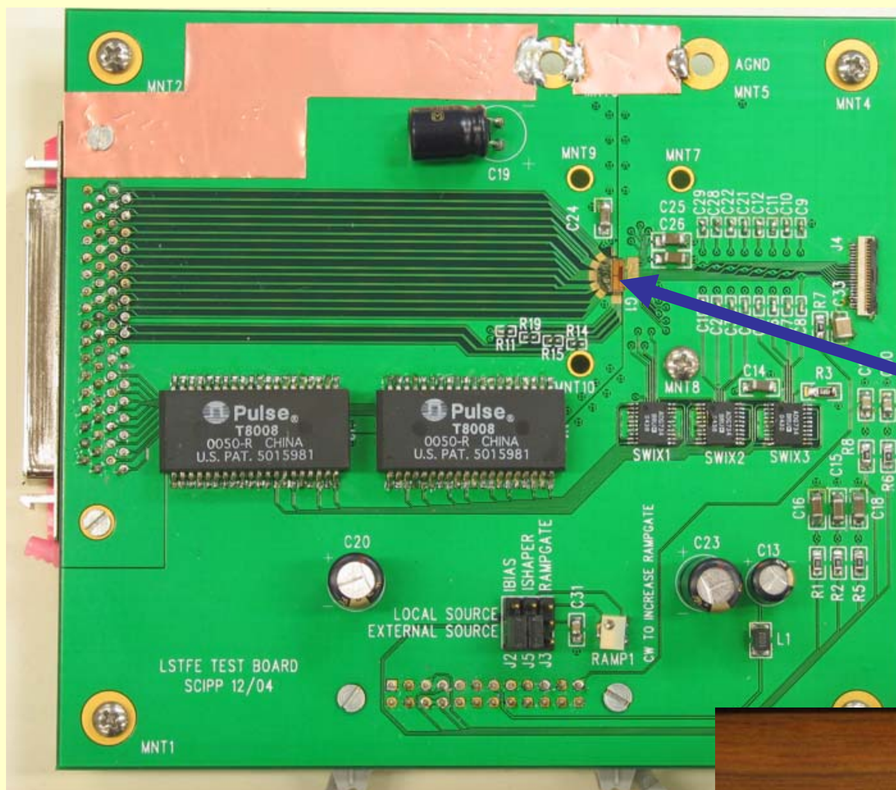


Simulate detector background (innermost SiD layer) and noise rates for 500 GeV running, as a function of read-out threshold.

Per 128 channel chip ~ 7 kbit per spill ➔ 35 kbit/second

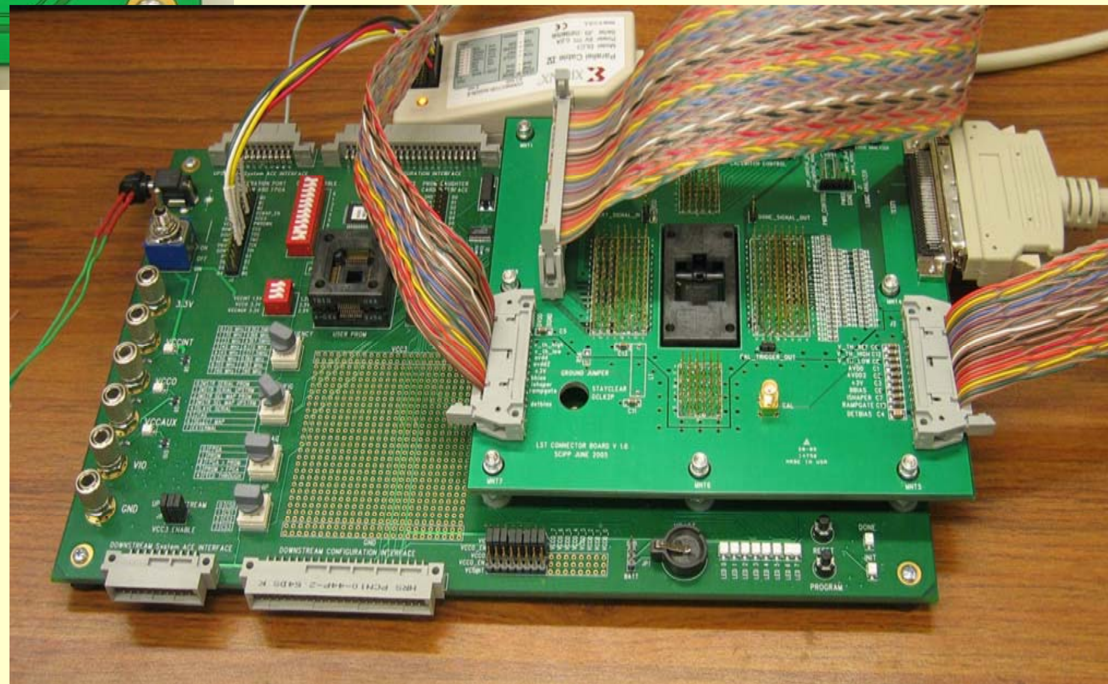
For entire SiD tracker ~ 0.5-5 GHz data rate, dep-ending on ladder length (x100 data rate suppression)

INITIAL RESULTS



LSTFE chip mounted on readout board

FPGA-based control and data-acquisition system



Note About LSTFE Shaping Time

Original target: τ_{shape} = 3 μsec, with some controlled variability ("ISHAPR")
➔Appropriate for long (2m) ladders

In actuality, τ_{shape} ~ 1.5 μsec; tests are done at 1.2 μsec, closer to optimum for SLAC short-ladder approach

Difference between target and actual shaping time understood in terms of simulation (full layout)

LSTFE-2 will have 3 μsec shaping time

Comparator S Curves

Vary threshold for given input charge

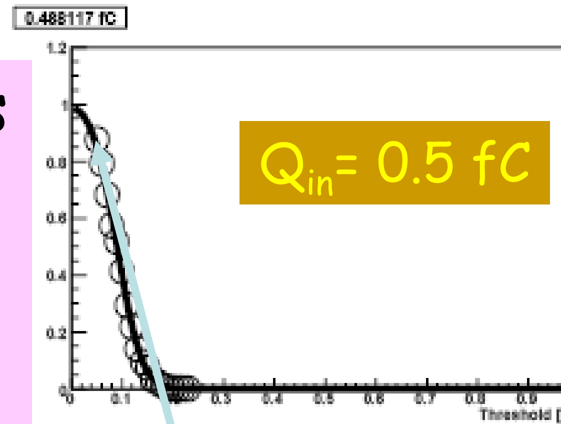
Read out system with FPG-based DAQ

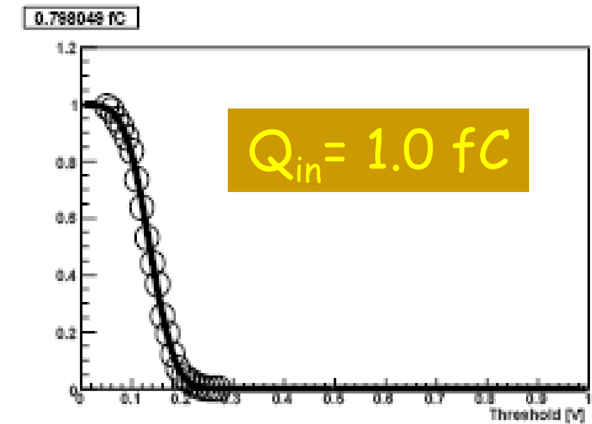
Get

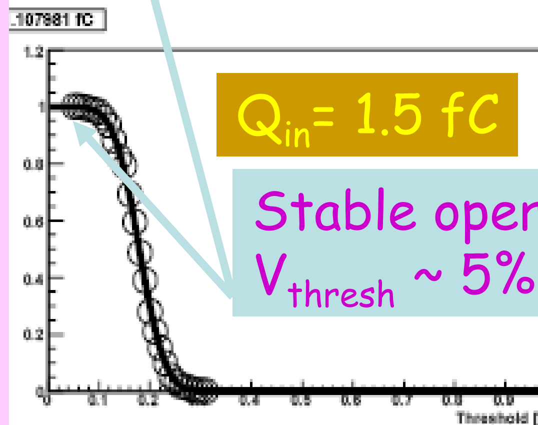
```
1-erf(threshold)
```

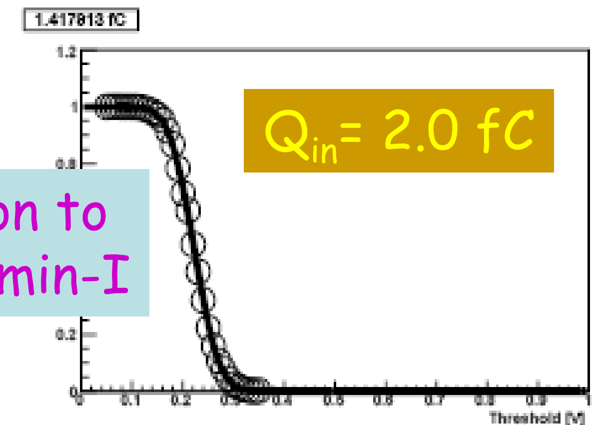
with 50% point giving response, and width giving noise

Hi/Lo comparators function independently

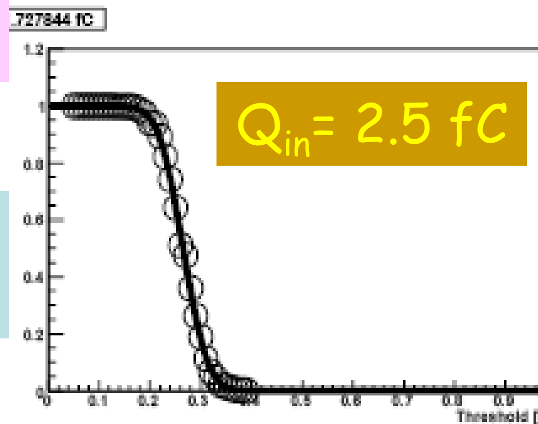


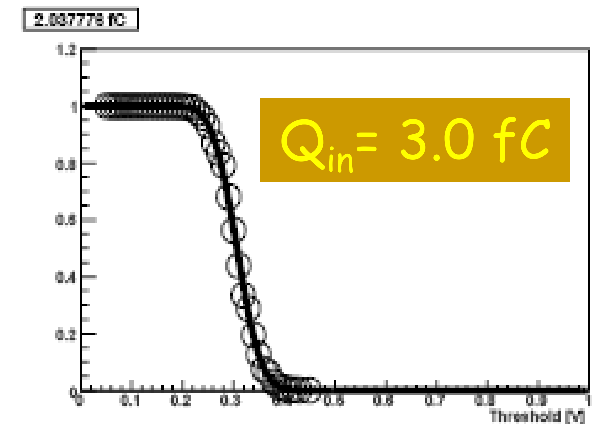






Stable operation to V_{thresh} ~ 5% of min-I





EQUIVALENT CAPACITANCE STUDY

Noise vs. Capacitance (at τ_{shape} = 1.2 μs)

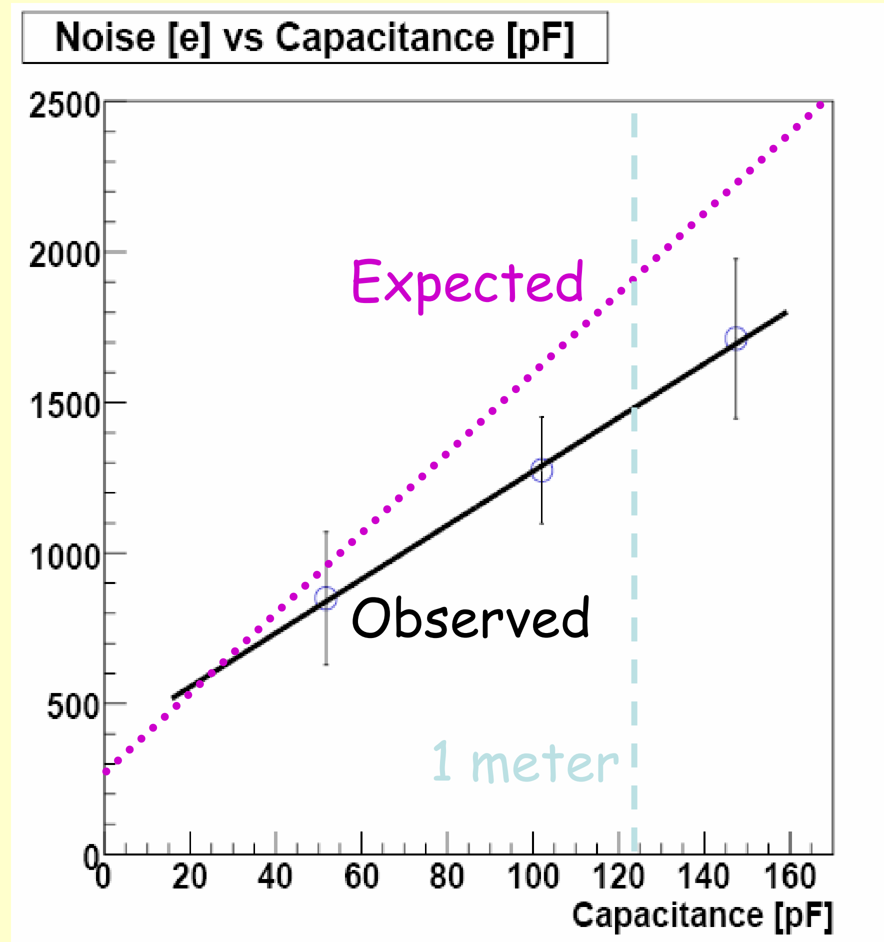
Measured dependence is roughly (noise in equivalent electrons)

$$\sigma_{noise} = 375 + 8.9*C$$

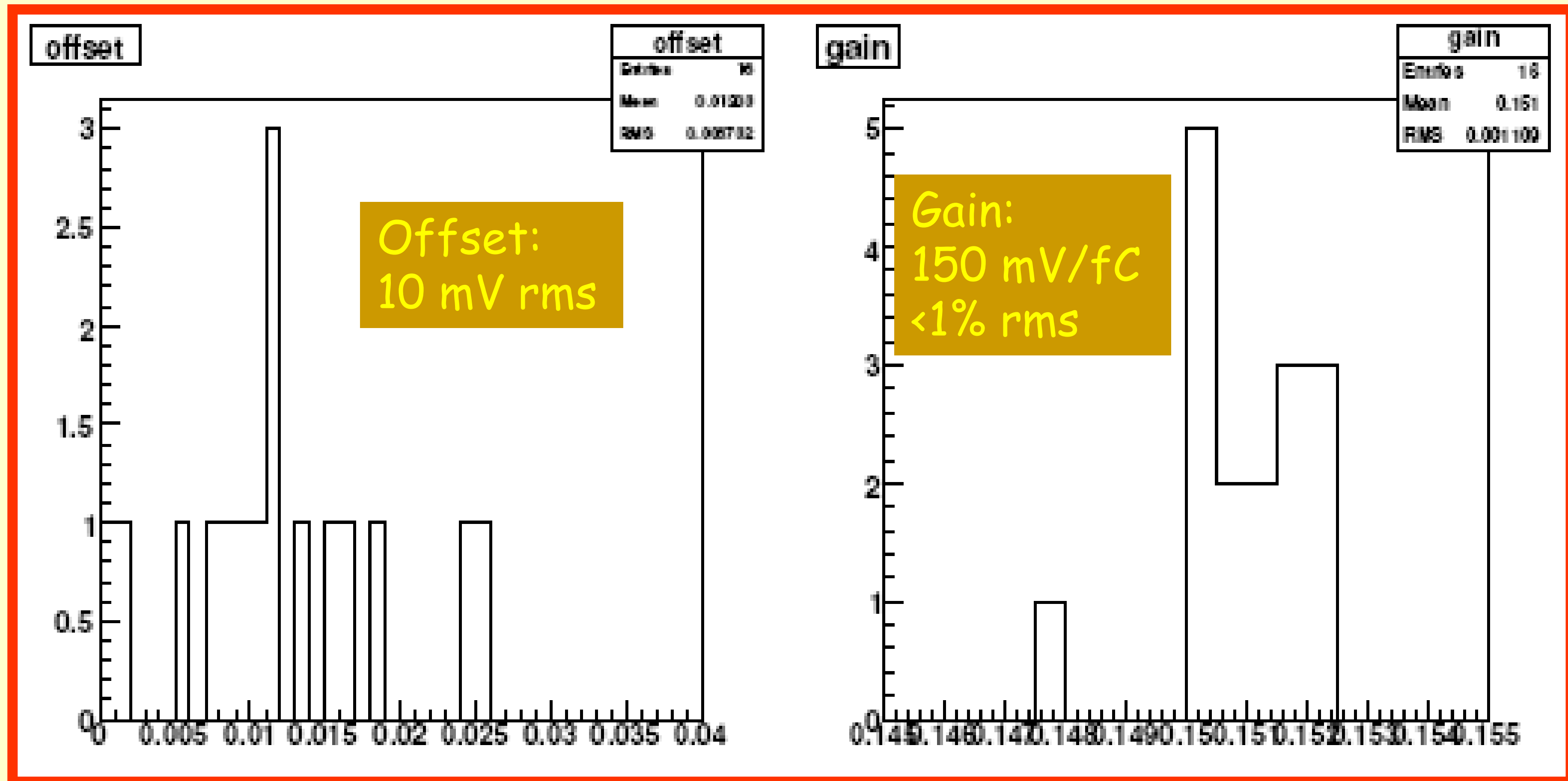
with C in pF.

Experience at 0.5 μm had suggested that model noise parameters needed to be boosted by 20% or so; these results suggest 0.25 μm model parameters are accurate

➔ Noise performance somewhat better than anticipated.



Channel-to-Channel Matching



Occupancy threshold of 1.2 fC (1875 e^-) ➔ 180 mV

± 2 mV (20 e^-) from gain variation

± 10 mV (100 e^-) from offset variation

Power Cycling

Idea: Latch operating bias points and isolate chip from outside world.

- Per-channel power consumption reduces from ~1 mW to ~1 μW.
- Restoration to operating point should take ~ 1 msec.

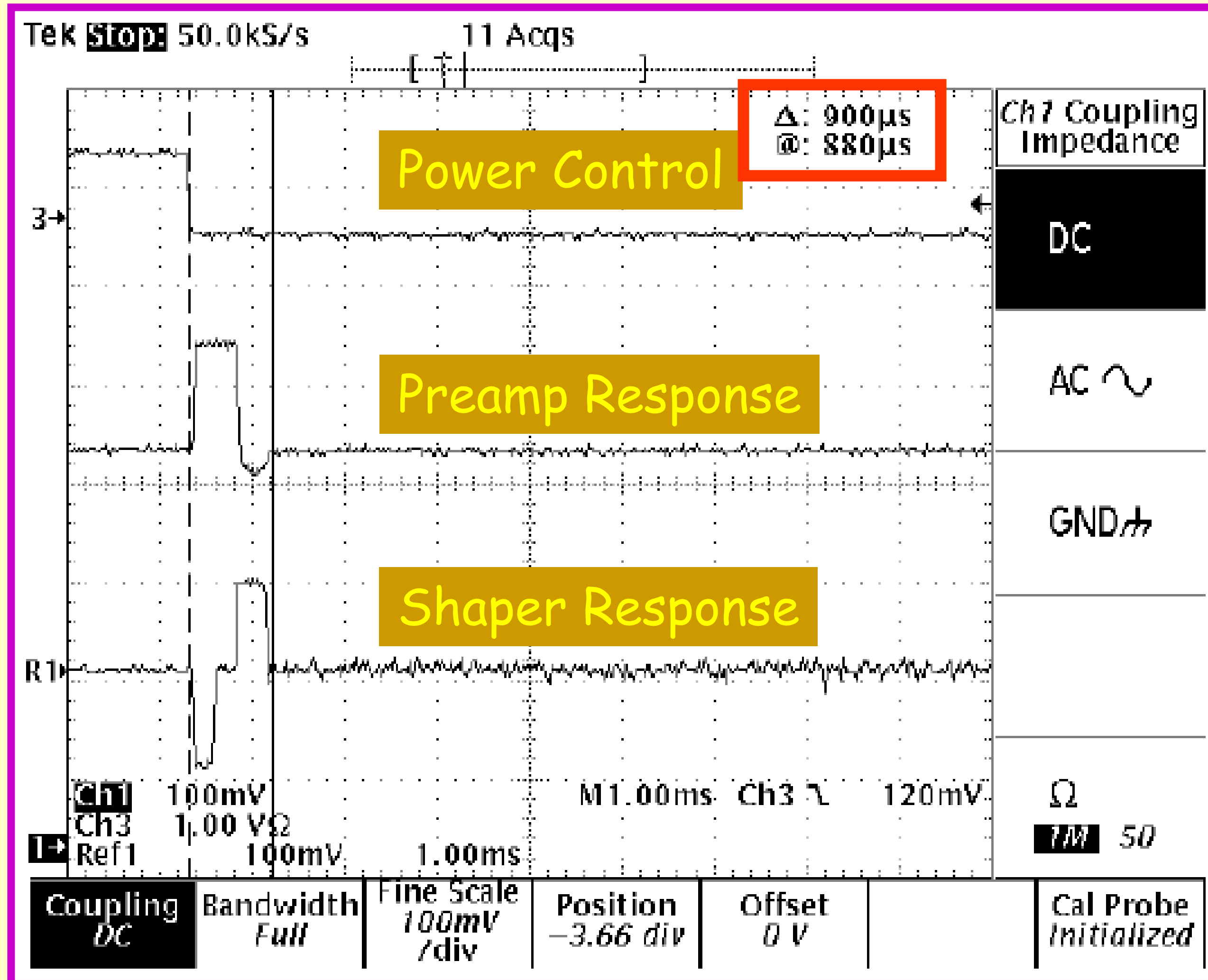
Current status:

- Internal leakage (protection diodes + ?) degrades latched operating point
- Restoration takes ~40 msec (x5 power savings)
- Injection of small current (< 1 nA) to counter leakage allows for 1 msec restoration.

Future (LSTFE-2)

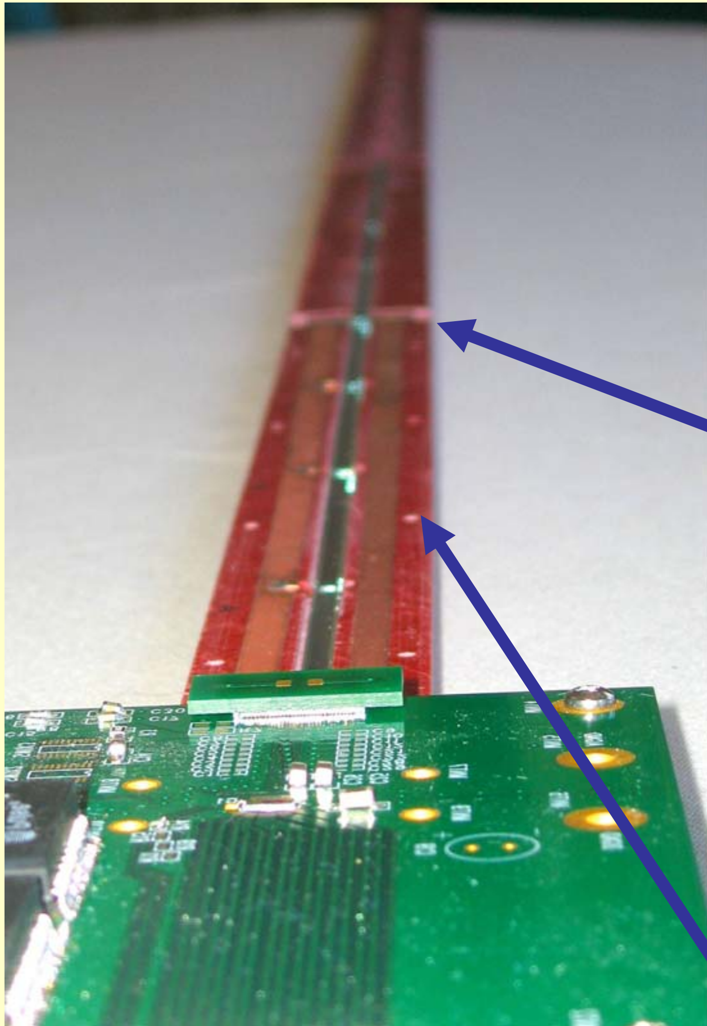
- Low-current feedback will maintain bias points; solution already incorporated in LSTFE-2 design

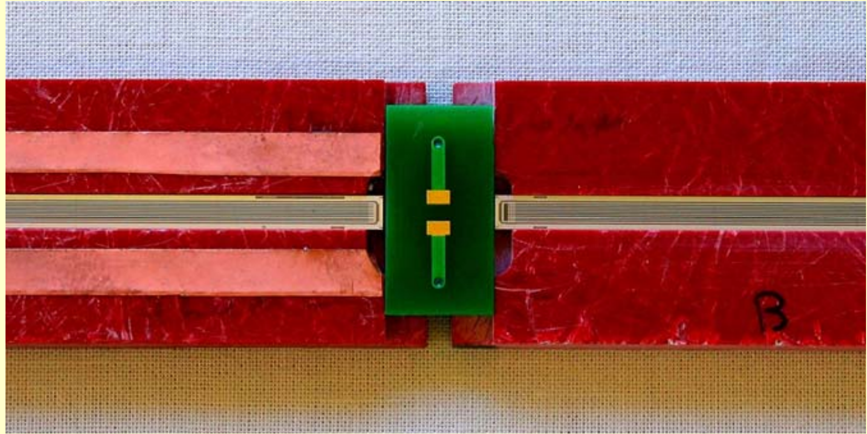
Power Cycling with Small Injected Current

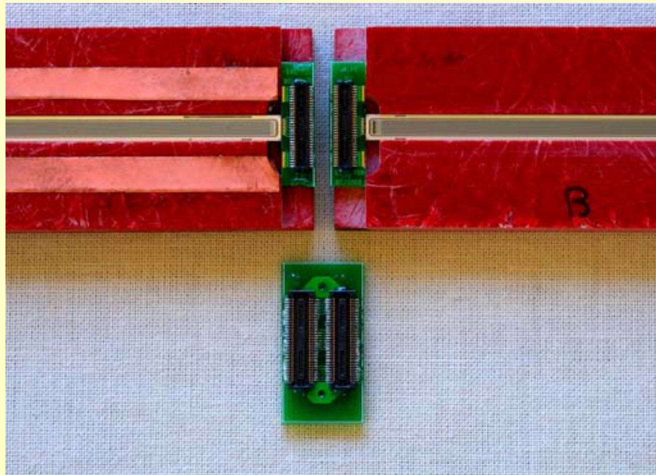


Solution in hand to maintain bias levels in "off" state with low-power feedback; will eliminate need for external trickle current

LONG LADDER CONSTRUCTION







LONG LADDER EXPERIENCE

A current focus of SCIPP activity

Using GLAST "cut-off" (8 channel) sensors; 237 μm pitch with 65 μm strip width

Have now studied modules of varying length, between 9cm and 72cm. [2/1/07: Now have up to 143 cm…]

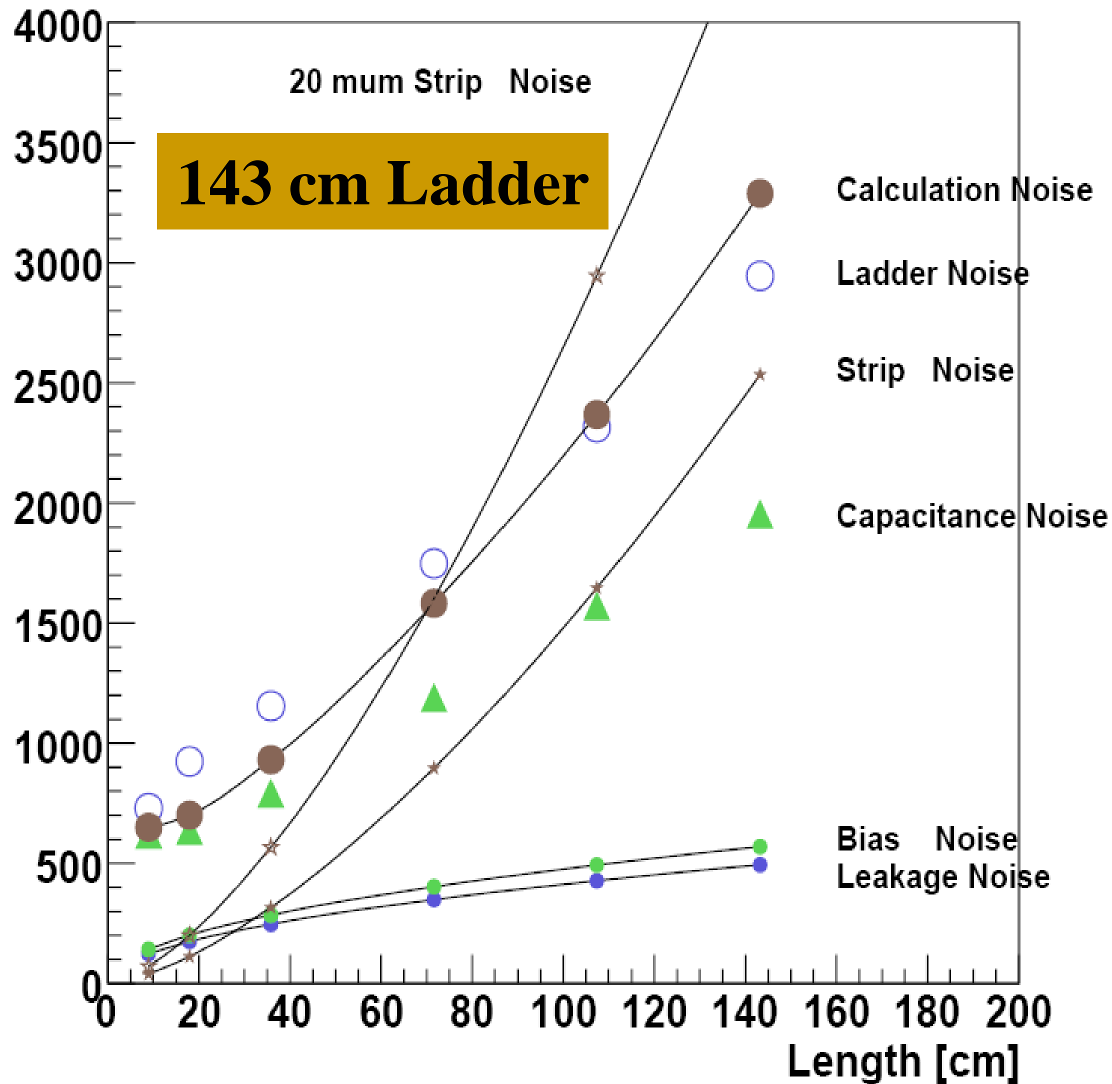
Measure inputs to estimate noise sources other than detector capacitance:

• Leakage current	1.0 nA/cm
• Strip resistance	3.1 Ω/cm
• Bias resistance	35 MΩ per sensor

All of these should be considered in module design!

Strip resistance for fine pitch could be an issue ➔ are starting careful study and considering options ➔ feedback to detector/module design.

Measured Noise vs. Sum of Estimated Contributions



Measured noise

Sum of estimates

Projected Johnson noise for 20 μm strip (not part of estimate)

Estimated Johnson noise for actual 65 μm strip (part of estimate)

TIME-OVER-THRESHOLD READOUT SUMMARY

The LSTFE readout system is:

- Universally applicable (long strips, short strips, central, forward, SiD, LDC, GLD, 4th…)
- Rigorously optimized for ILC tracking
- Relative simple (reliability, yield)
- In a relatively advanced stage of development
- Is now being used as an instrument to understand fundamental principles of long ladder operation, particularly for narrow strips (CDF Layer00 sensors available, being qualified)

Front-End Digitized Readout using Deep Sub-Micron Technologies: SiTR-XXX chips

[2] J. David, [2] M. Dellhot, D. Fougeron, [1] **J.F. Genat** [2], R. Hermel [1],
H. Lebbolo[2] , **T.H. Pham** [2], F. Rossel [2], A. Savoy-Navarro [2],
R. Sefri [2] , S. Vilalte [1]

[1] LAPP Annecy, [2] LPNHE Paris

And also the collaboration of IMEC-Leuven (Europractice)
E. Deumens, P Malisse

Presently joining Institutes: University of Barcelona & University Ramon Llull
IFCA-CSIC/University of Cantabria
Increasing collaborative contacts with CERN

SiTR chips data processing

- Pulse height: Cluster centroid to get a few μm position resolution
  Detector pulse analog sampling

- Time: Two scales:
  - Coarse : 150-300 ns for BC identification, 80ns sampling

    Shaping time of the order of the microsecond

  - Fine: nanosecond timing for the coordinate along the strip
    10ns sampling

    Not to replace another layer or double sided
    Position estimation to a few cm using pulse reconstruction from samples

    Shaping time: 20-50 ns

Technologies

Silicon detector and VLSI technologies allow to improve detector and front-end electronics integration

Front-end chips:

- Thinner CMOS processes 250, **180**, **130**, 90 nm now available
- SiGe, less 1/f noise, faster
- Chip thinning down to 50 μm

More channels on a chip, more functionalities, less power

Connectivity:

- On detector bump-bonding (flip-chip)
- 3D

Smaller pitch detectors, better position and time resolution. Less material

SiTR chips integrated functionalities

- Full readout chain integration in a single chip

  - Preamp-shaper
  - Trigger decision (sparsification with analog sums) : → compact data
  - Sampling: Analog pipe-lines
  - On-chip digitization (highly multiplexed)
  - Buffering
  - Digital Processing: Centroids and Least Squares time/amplitude estimation
  - Calibration and calibration management
  - Power switching

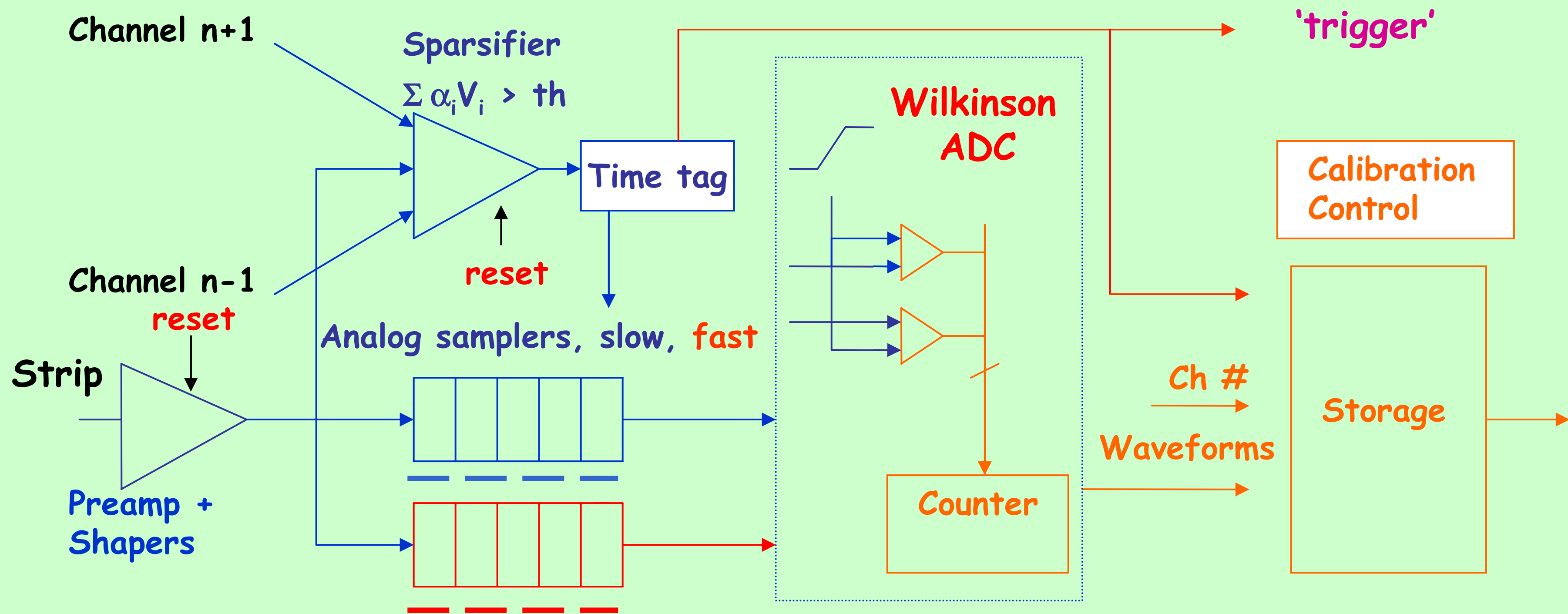
- First production series will be based on 128 channels/chip; the goal is to go to 1024 (or at least 512) channels.

SiTR Front-End readout Chip goals:

- Integrate 512-1024 channels in 90nm CMOS:
  - ➢ Charge Amplifiers: 20-30 mV/MIP over 30 MIP
  - ➢ Shapers:
    - slow 500 ns – 2 μs
    - fast 20-50 ns
  - ➢ Zero-suppression: threshold the sum of adjacent channels
  - ➢ 2D analog memory:
    - 8-16 samples
80 ns and 10 ns sampling clocks
    - Event buffer 16-deep
  - ➢ ADC: 10 bits
  - ➢ Buffering
  - ➢ Calibration
  - ➢ Power switching saves a factor 100-200

- **ILC timing:** 1 ms: ~ 3-6000 trains @150-300ns / BC
200ms in between

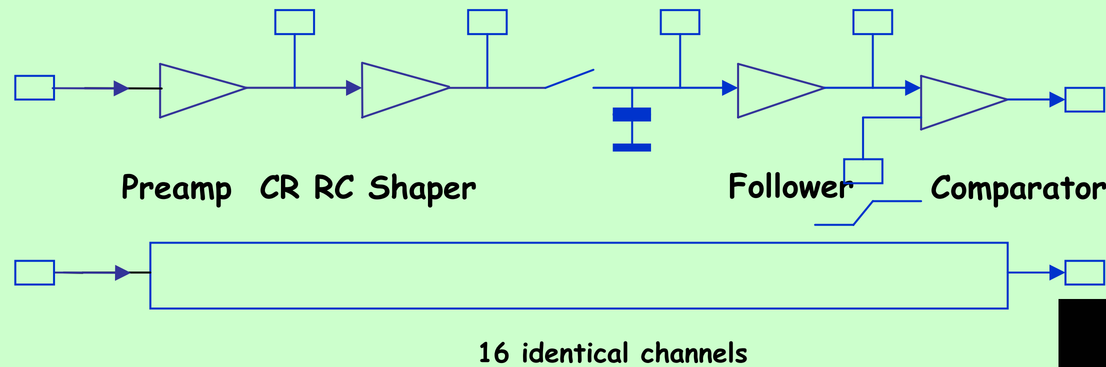
SiTR chips Front-End architecture



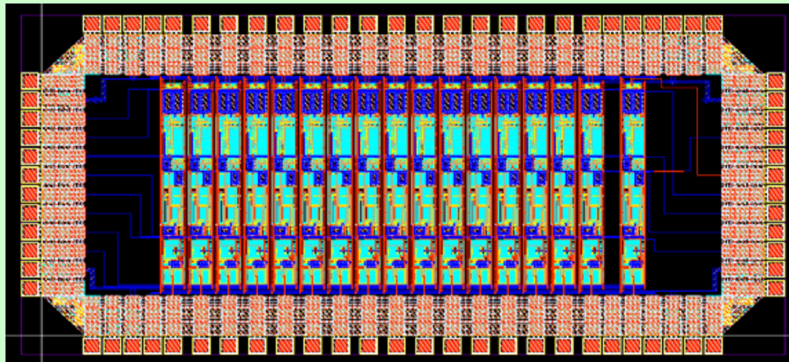
Charge 1-40 MIP, Time resolution: BC tagging 150-300ns, fine: ~ 1ns

Technologies: Deep Sub-Micron CMOS 180-130nm
Future: SiGe &/or deeper DSM

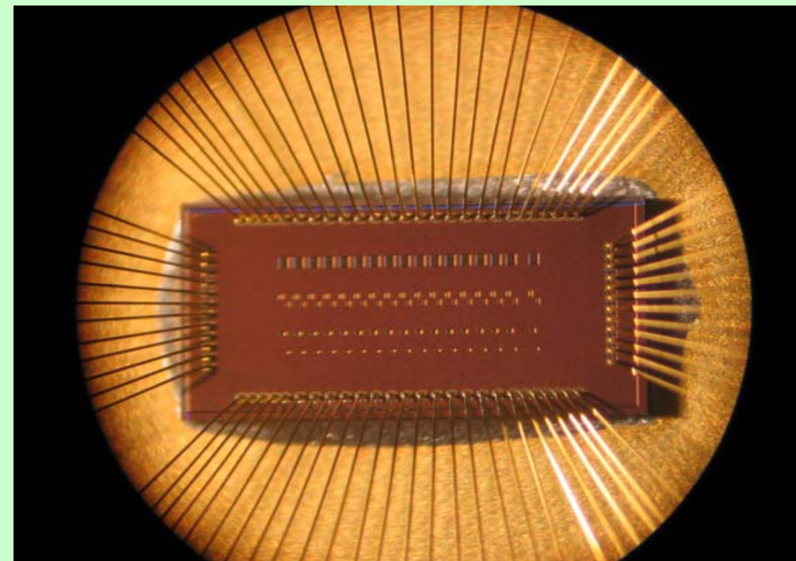
First prototype in CMOS UMC 180nm (2005):SiTR-180



Analogue part only



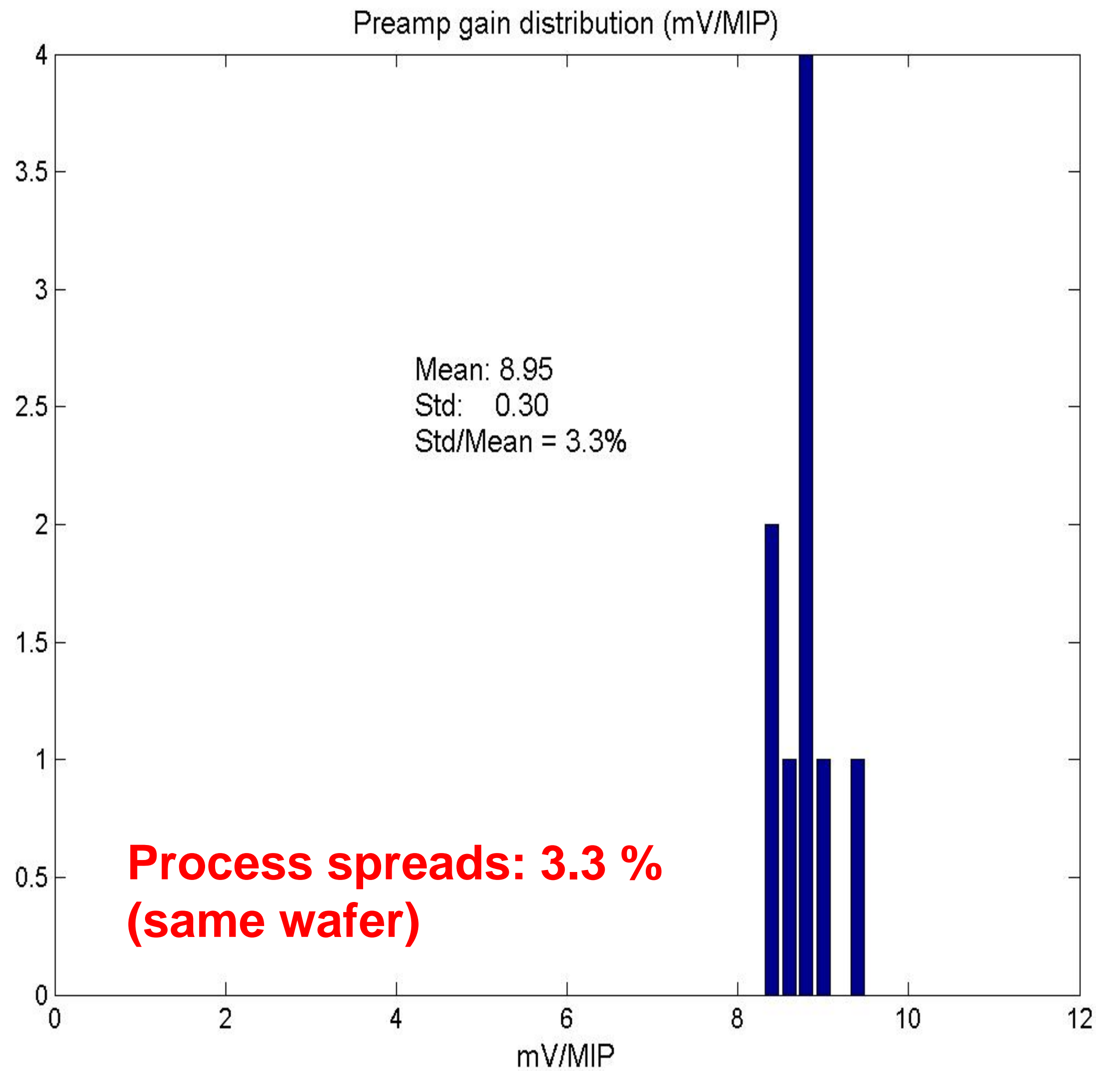
- Preamp
- Shaper
- Sample & Hold
- Comparator



3mm

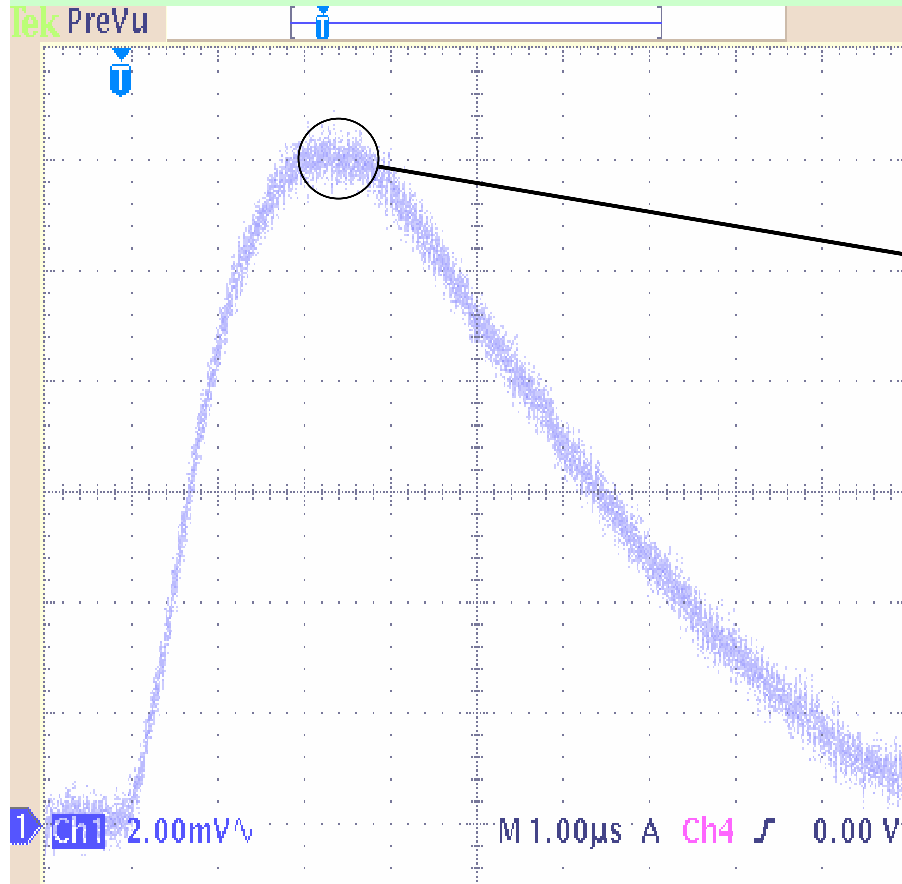
16 + 1 channel UMC 180nm chip: SiTR-180 (layout and picture)

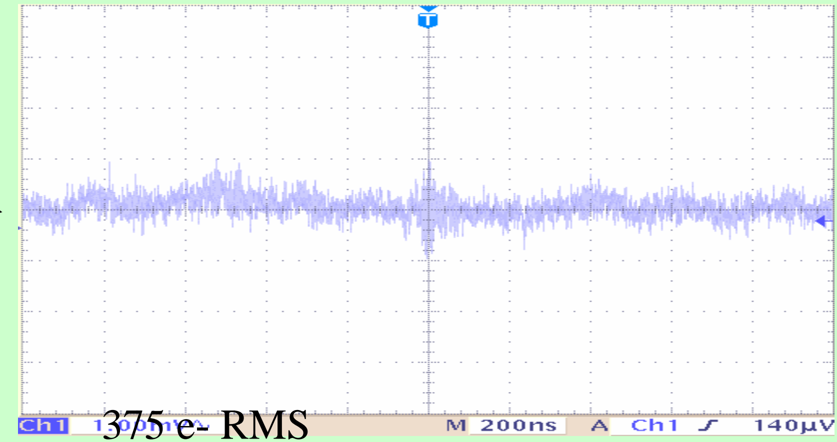
SiTR-180: Process spreads



Preamp gains statistics (same wafer)

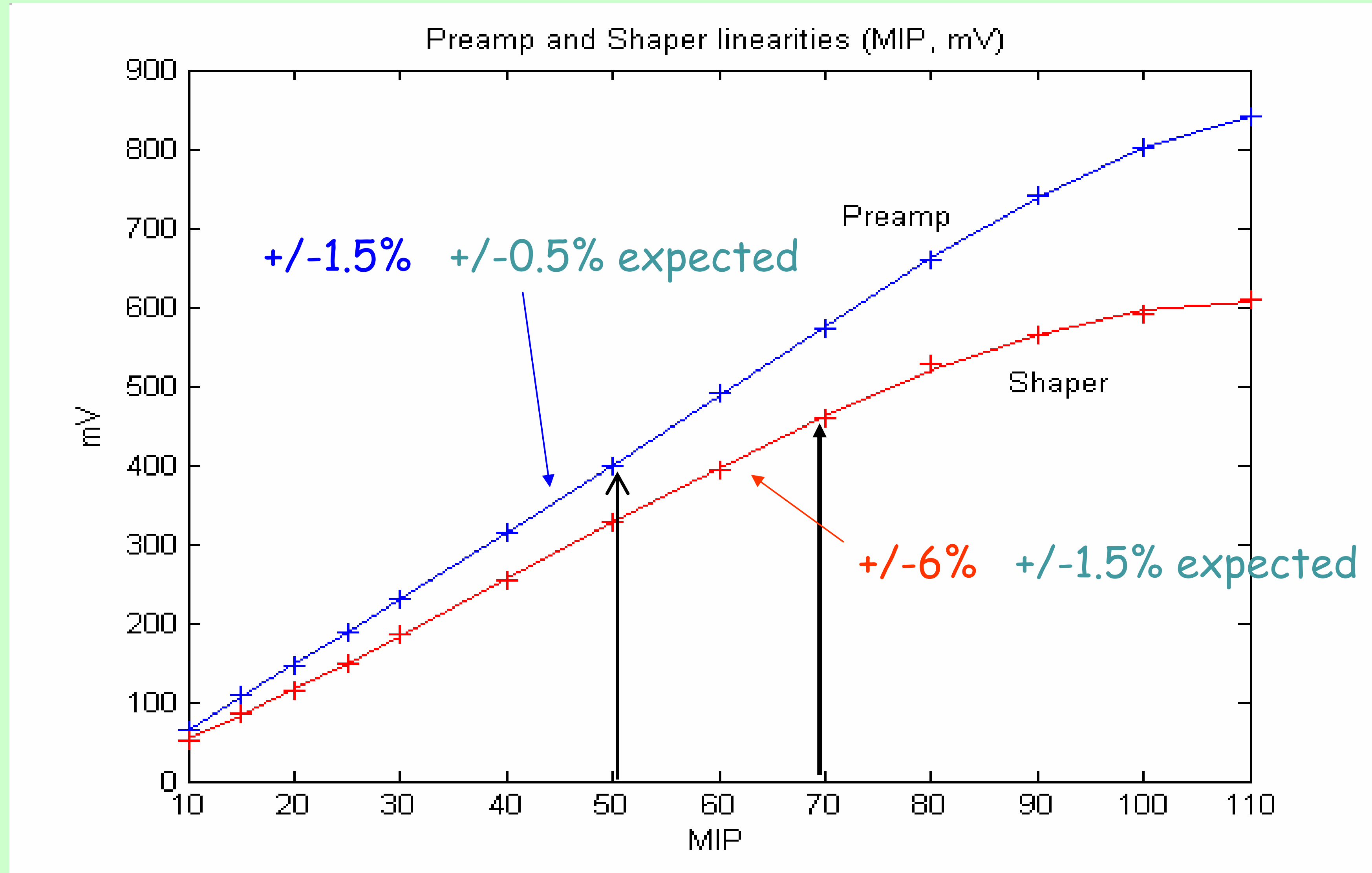
SiTR-180: Shaper output noise





375 e- +10.4 e-/pF input noise with chip-on-board wiring
275 + 8.9/pFsimulated

Linearities (SiTR-180 chip)



Functionality tests conclusions on SiTR-180 chips

12 chips tested (end 2005)

The UMC CMOS 180nm process is mature and reliable:

- Models mainly OK
- Only one transistor failure over 12 chips
- Process spreads of a few %

Very encouraging results regarding CMOS DSM

→ go to 130nm

90Sr Source tests with SiTR-180 connected to a Si detector and comparison with VA1 chip from Ideas (see test bench section)

Front-end in CMOS 130nm

130nm CMOS motivations:

- Smaller
- Faster
- More radiation tolerant (not a real issur at ILC)
- Less power
- Presently dominant in the IC industry

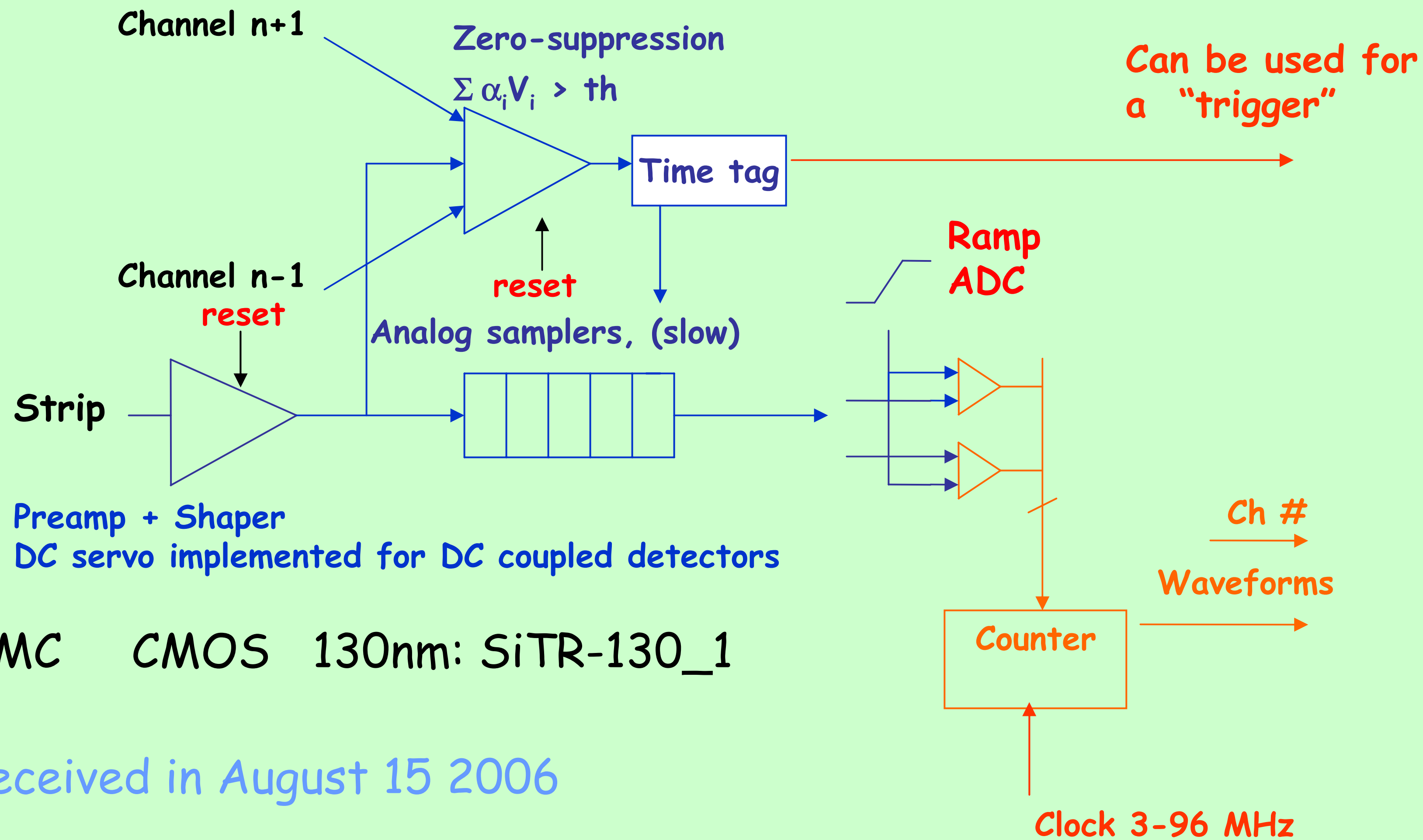
Features:

- Design more constraining (Design rules)
- Reduced voltage swing (Electric field constant)
- Leaks (gate/subthreshold channel)
- Models more complex, sometimes still not accurate

UMC Technology parameters

	180 nm	130nm
• 3.3V transistors	yes	yes
• Logic supply	1.8V	1.2V
• Metals layers	6 Al	8 Cu
• MIM capacitors	1fF/mm^2	1.5 fF/mm^2
• Transistors	Three Vt options	Low leakage option

130nm 4-channel test chip: SiTR-130

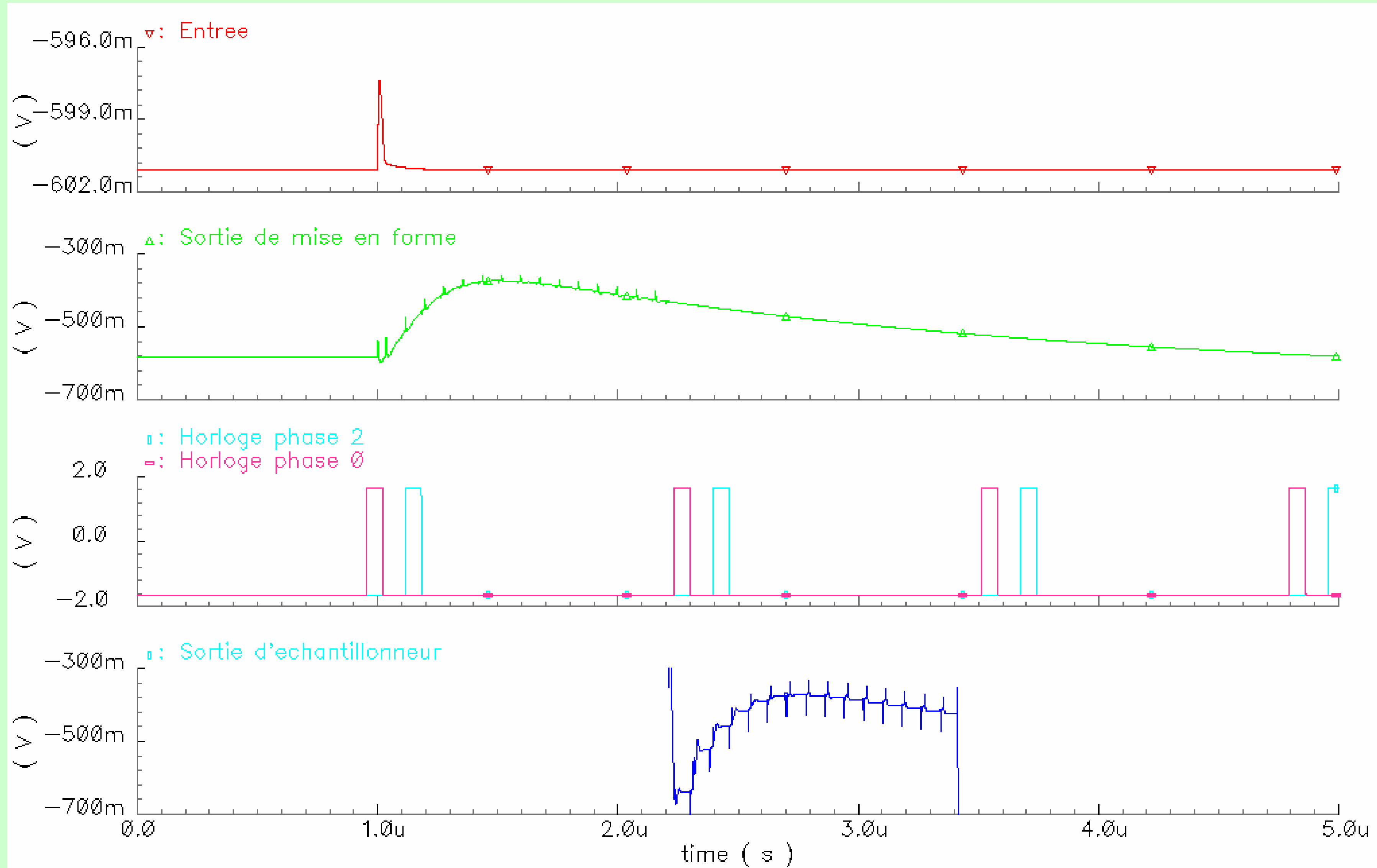


UMC CMOS 130nm: SiTR-130_1

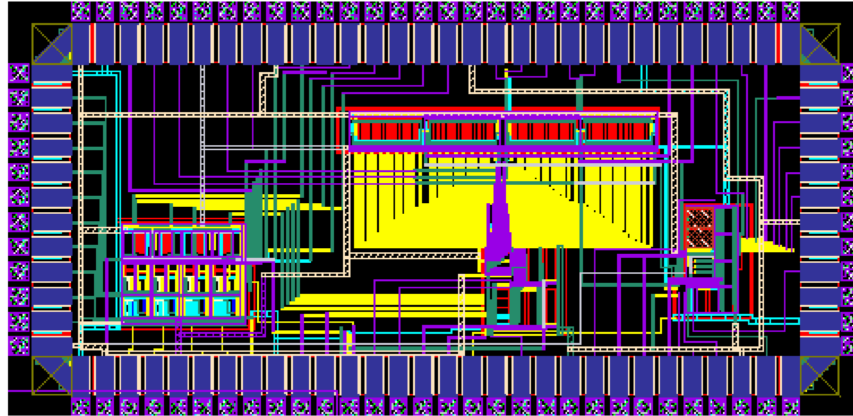
Received in August 15 2006

Being tested: Analog OK, Digital under tests

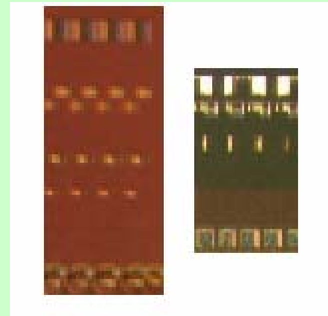
Analog pipeline simulation



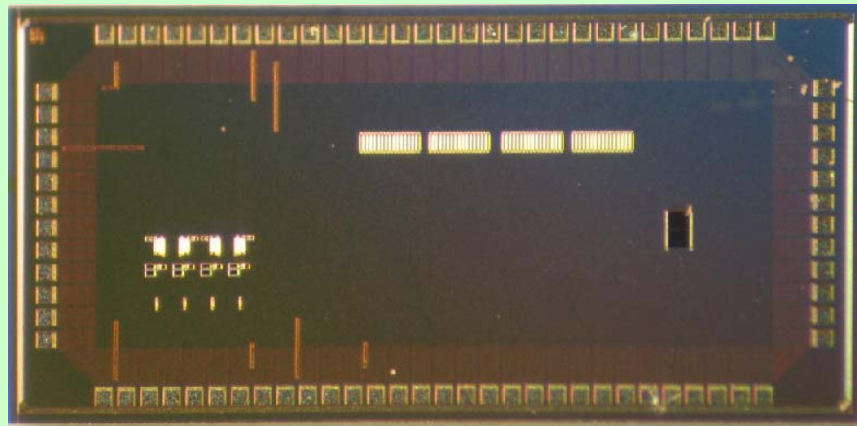
The SiTR-130_1 chip



Layout of the 130nm chip including sampling and A/D conversion

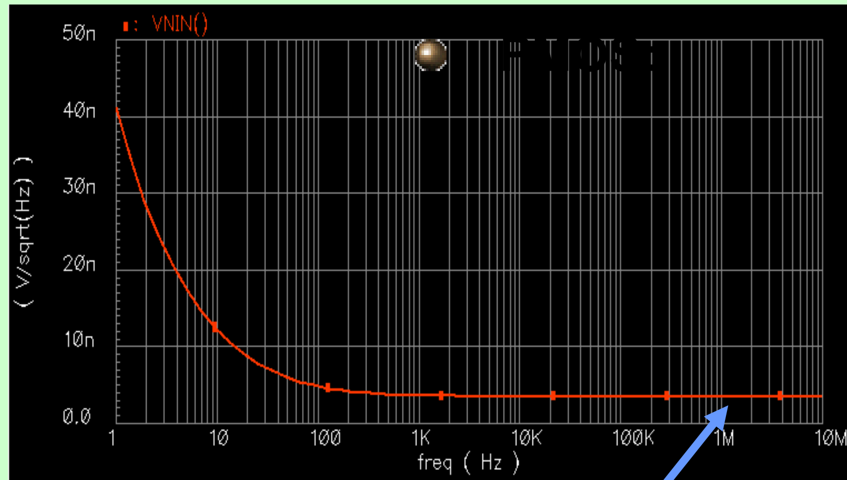


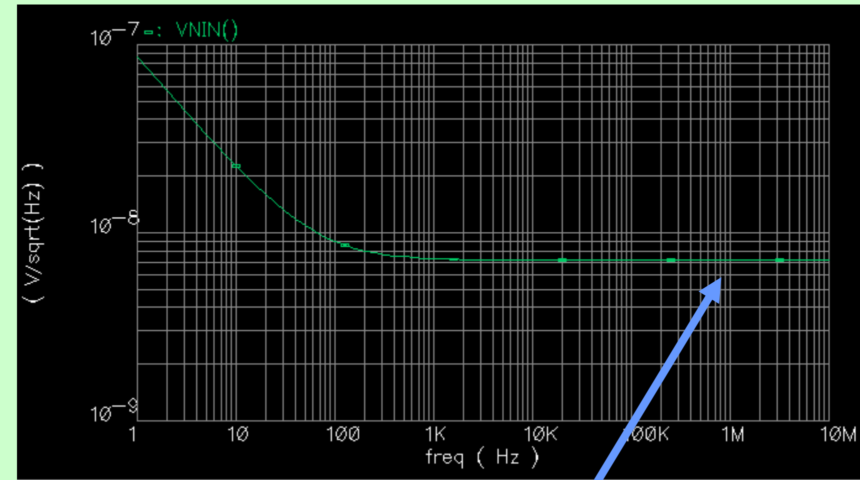
180nm 130nm



Picture

Possible issues: noise: 130nm vs 180nm (simulation)





180nm

gm=944.4uS

1MHz → 3.508nV/sqrt(Hz)

Thermal noise hand calculation = 3.42nV/sqrt(Hz)

130nm

gm=815.245uS

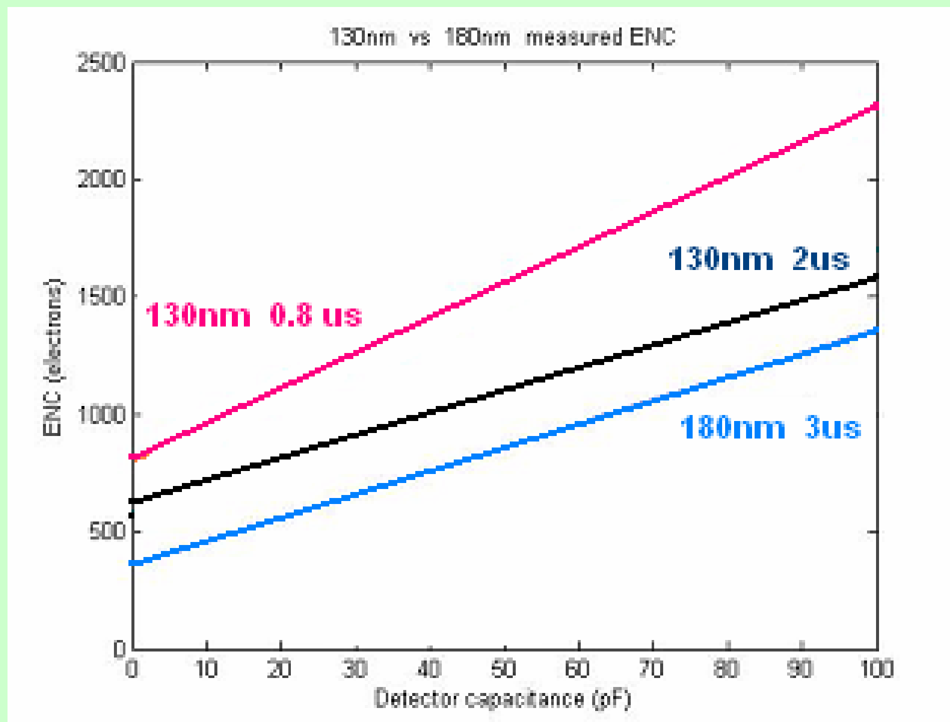
1MHz → 7.16nV/sqrt(Hz)

Thermal noise hand calculation = 3.68nV/sqrt(Hz)

Measurements show 2 times better results

SiTR-130_1 tests results

Gain OK:	30 mV/MIP	OK
Dynamics:	30 MIPs @ 5%	OK
Peaking time:	0.8 – 2µs	0.7 - 3 µs



Power (Preamp+ Shaper) = 300 µW

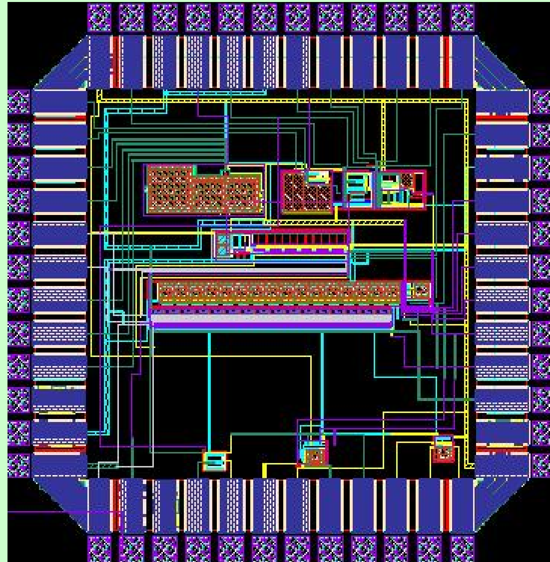
Noise comparative		
	130nm @ 0.8 µs :	850 + 14e-/pF
	130nm @ 2 µs :	625 + 9e-/pF
	180nm @ 3 µs :	360 + 10.5 e-/pF

Some issues with 130nm design

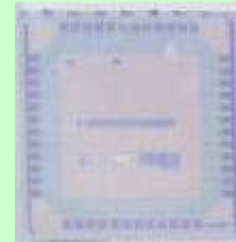
- Noise models pessimistic, Silicon actually much better !
- Design rules more constraining
- Some design kits are not fully developed and thus additional effort needed

SiTR-130_2

One channel version with the SiTR-130_1 analogue part only,but:
- **ServoDC**
- **Improved pipe-line**
- **DAC**



Layout

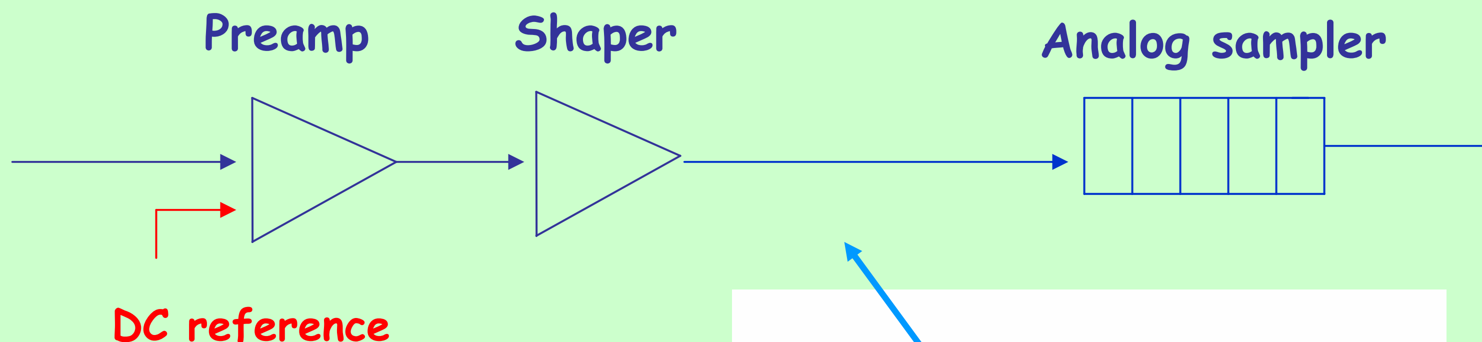


Picture

One channel 1.5 x 1.5 mm^2

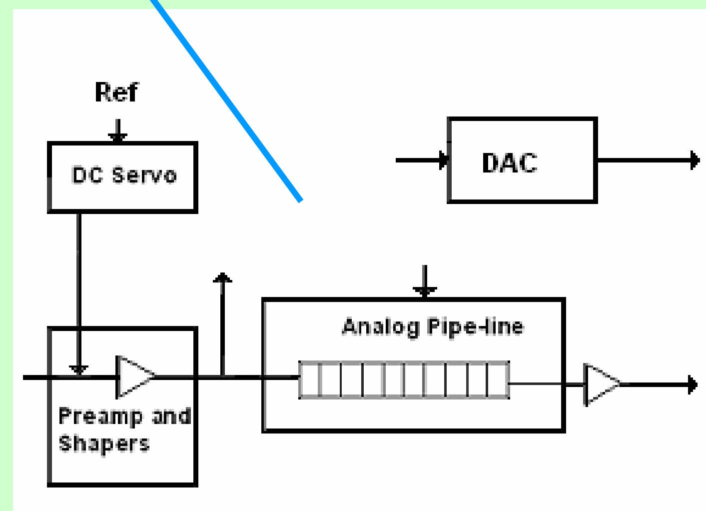
SiTR-130_2 architecture

DC servo to accommodate DC coupled detectors,
DAC,
Improved pipe-line



Received January 5th 2007

Test card under wiring
Test stand under work



SiTR-130_1 present conclusions

Good matching wrt simulation

Except noise which is…

much better !

- **Still lot of work to test pipe-line & digital**
- **Statistics from two wafers (70 chips)**

→ **Very encouraging results**

→ *Pursue on 130nm (techno choice?)*

→ *And we will start exploring90 nm*

Technology comparisons

The questions are:

1) At what DSM level to go?

2) What founder to choose

Following the presently achieved results and the increasing expertise in the SiLC collaboration (new Institutes joining), there are at disposal within SiLC:

UMC, STMicroelectronics and IBM (via CERN collaboration in EUDET).

It is foreseen to have before the end of 2007, a review of 130nm techno in these 3 foundries to compare the performances especially in terms of noise (analogue part)

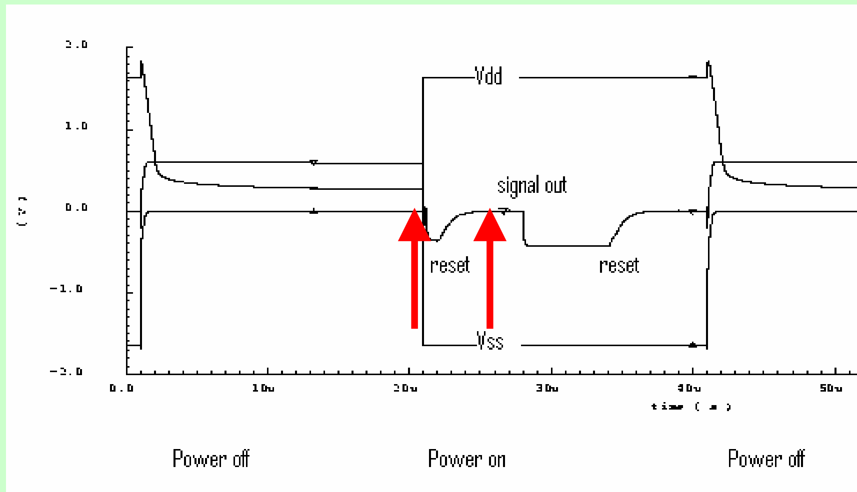
Power dissipation budget
(measured)

	Preamp	Shaper	Zero suppr.	Pipe-line	Total Analog	ADC	Logic	Total Digital
180nm/ch	90	180			270			
130nm/ch	148	148	198	10	575	66		
Common				100		5	96	101

Final goal: ≤ 1 mWatt/channel all included (looks achievable)

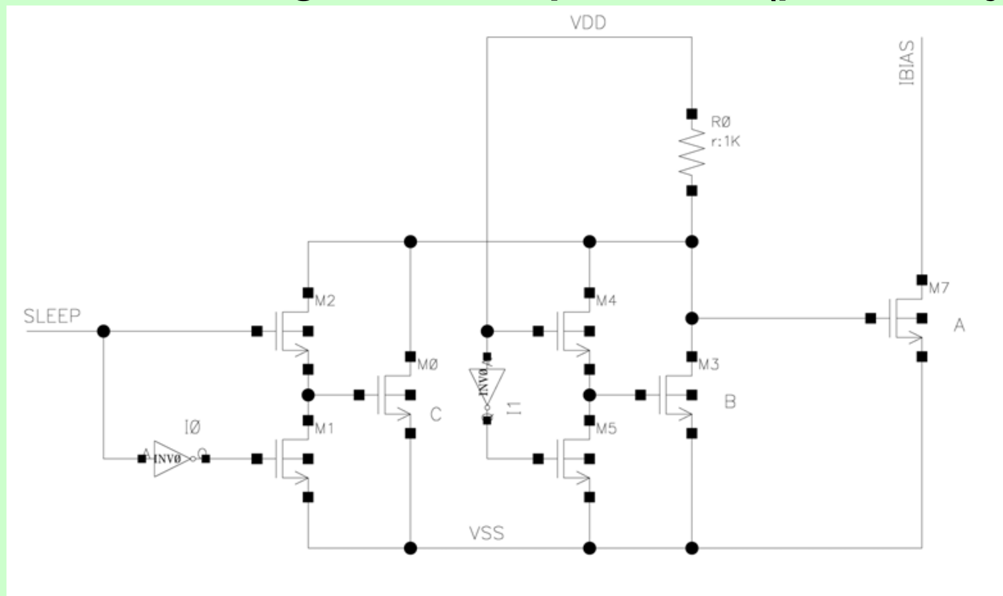
Power cycling: to be implemented next

Power switching at zero power-off: SPICE SIMULATION only



This option switches the currents to zero. The simulation shows that, provided the integrating capacitor of the charge amplifier is reset before power-off and after power-on, the whole procedure should take ~ 5 µs.

Power switching with some power left (preliminary schema only)



This option switches the current source feeding both the preamplifier & shaper between 2 values to be determined by simulation.

A very small fraction (order 0.1% - 1%), to be determined by simulation studies, of biasing current is held during « power off ».This can be done in a very simple way by switching one more transistor in the current mirror.

Next developments

- Implement the fast (20-50ns shaping) version in Silicon-Germanium including:

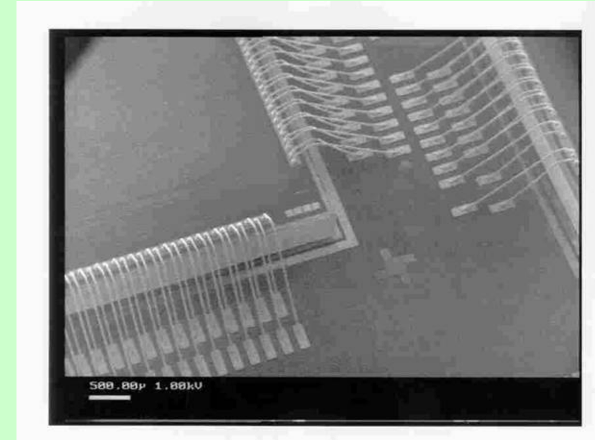
  - Preamp + Shaper (20-100ns)
  - Fast sampling

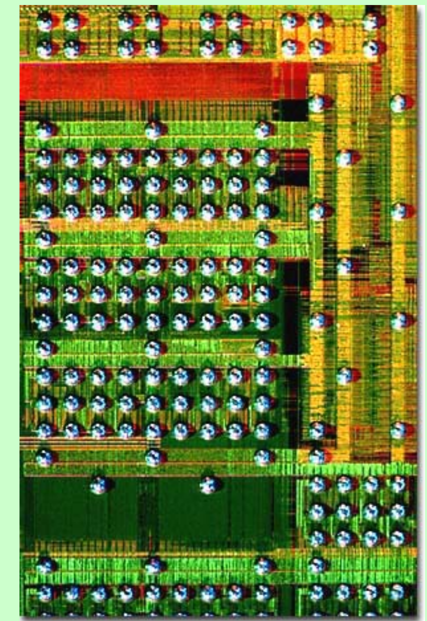
- Submit a full 128 channel version in 130nm CMOS including slow and fast analog processing, power cycling, calibration and digital (e.g:amplitude, time and centroid)

Chip connection on µstrips

Presently available:

- Wire bonding (µstrips)
  - Only periphery of chip available for IO connections
  - Mechanical bonding of one pin at a time (sequential)
  - Cooling from back of chip
  - High inductance (~nH)
  - Mechanical breakage risk



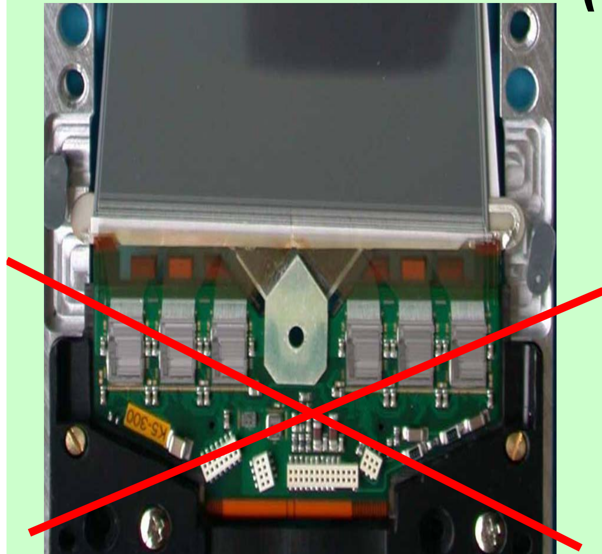


- Flip-chip (pixels)
  - Whole chip area available for IO connections
  - Automatic alignment
  - One step process (parallel)
  - Cooling via balls (front) and back if required
  - Thermal matching between chip and substrate required
  - Low inductance (~0.1nH)

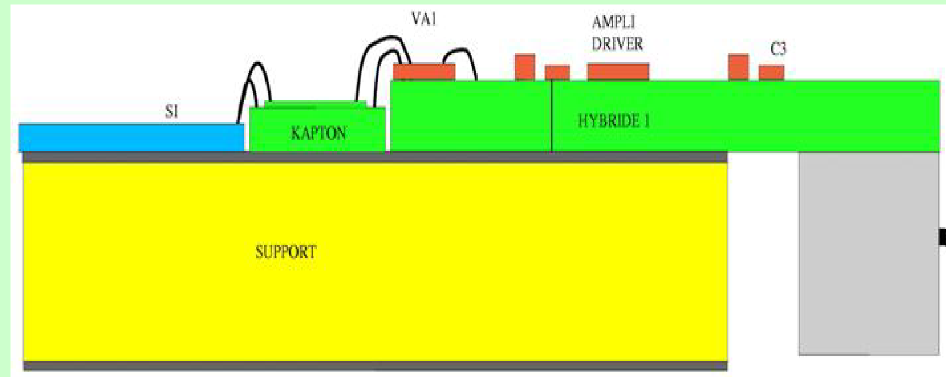
  Is this adaptable to µstrips?

Towards the novel elementary module

(the electronics side of it)

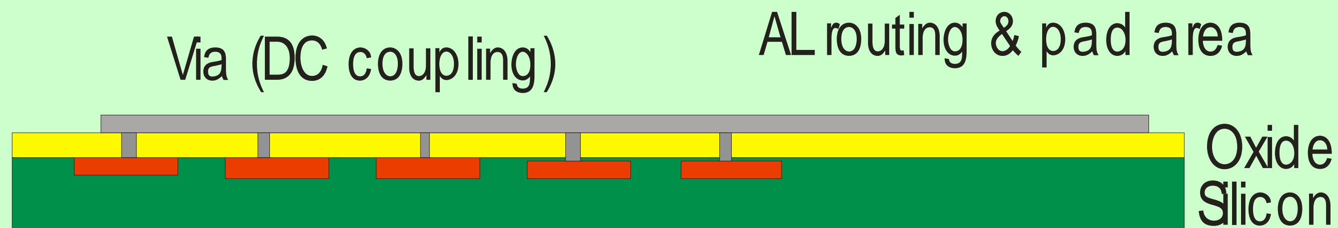


Old fashioned FE Hybrid with wire bonding



Important issue in developing a novel elementary module is the **direct connection of the FEE on board.**

- Integrate pitch adapter into sensor, 2nd metal layer for signal routing (see sensor section)



- Bump-bonding of readout chip directly onto to sensor

Bump bonding FEE on detector

IMB-CNM, VTT, HIP, LPNHE, Liverpool (firms)

- Design of the fan-in fan-out on the µstrip sensor:

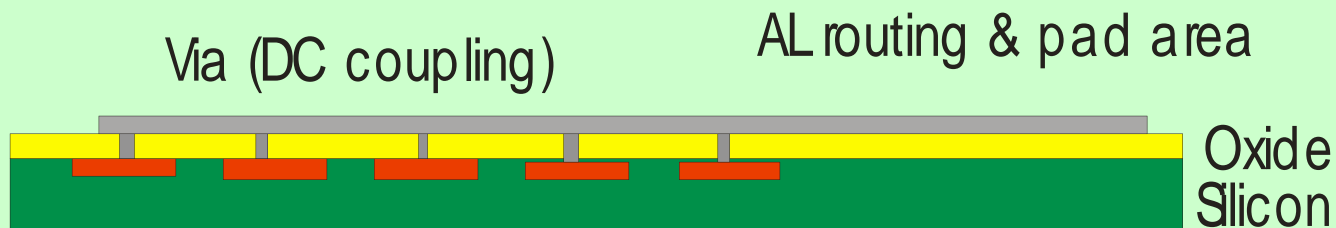
The design is starting in LPNHE based on 50µm single sided 6''sensors, considering 2 cases:

1st case: 128 ch (chips available by end 2007)

2nd case: 1024 channel (chips available later)

Fanin/Fanout design should be ready in 2 months from now.

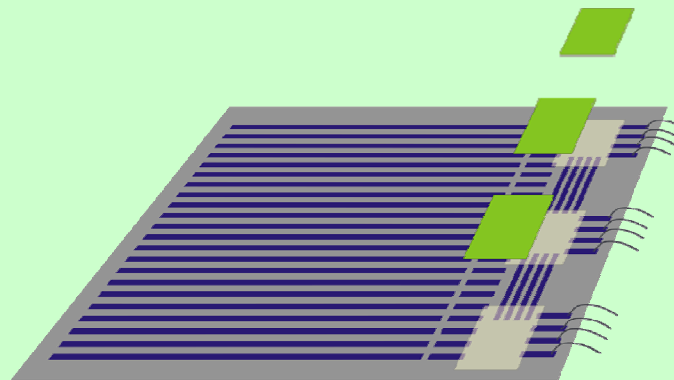
- Have a foundry or a indutrial firm ready to implement it on the sensor (underway: see sensor section)



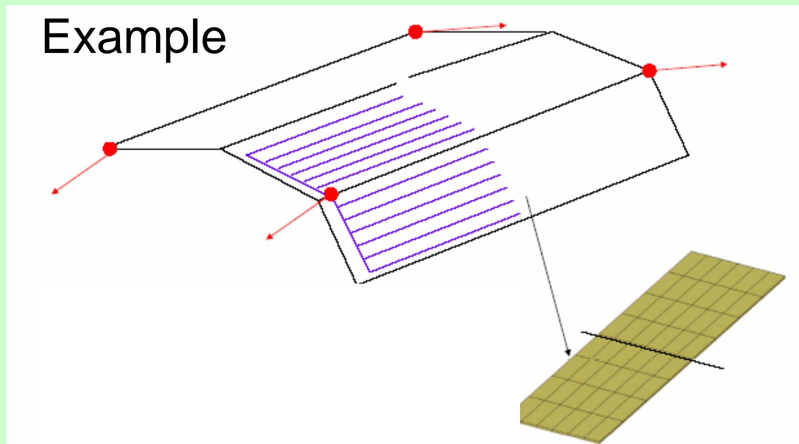
- Bump bonding of the FEE chip:
  crucial point: have a working chip with the required nb of channels

  (SiTR-130_128 by end 2007)

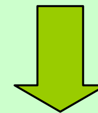
- Cabling => use: Tape Automated Bonding (TAB) or ??????
  Don't forget auxiliary electronics that degrades any fancy solution on paper
  ex: decoupling capacitors



Cabling, Data Flow and Data transmission:
preliminary thoughts



Present idea: daisy chaining several adjacent front-end chips (e.g.4) on the two corresponding single-sided layers, of the same octagonal plane, with micro coax cabling. This would make 6 micro coax cables per octagonal plane read out in parallel by digital fibers in the considered example.
One fiber could serve 2 half octagonal plane.



Using **micro-coax cables** of typically one inch diameter, 300 mW power dissipation at 1 GHz and that can be power cycled. **Kapton cables** are also under consideration. At a later stage in the cabling scheme, i.e. to transmit the information from the edge of the detector to the outside, 6GHz **SCM fiber optic** links are presently considered.

This is under serious investigation because the following main issues /or concerns:
✓Cabling versus and/or fibres: micro coax are making a real comeback
✓ High multiplexing rate versus redundancy
✓Technological field that evolves very rapidly (telecom etc..)

OUTLINE

- **PART I: The Collaboration and R&D Motivations and Goals**
  - **The SiLC Collaboration**
  - **Why R&D on tracking is needed**
  - **Why Silicon Tracking**

  (A. Savoy-Navarro)

- **PARTII: The R&D objectives**
  - **R&D on Mechanics *(V. Saveliev)***
  - **R&D on Sensors *(M. Lozano and H.J. Kim)***
  - **R&D on Electronics *(B. Schumm and A. Savoy-Navarro)***

- **PART III: The R&D Tools**
  - **Simulations *(M. Vos)***
  - **Lab Test bench and Test beams *(A. Savoy-Navarro)***

Concluding remarks

SiLC simulation task force

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Korean Group collaborators

Outline

- what simulations and why?
- microscopic simulations
- macroscopic simulations (fast and full)
  - status of available tools
  - glossary of results
- outlook

Introduction

In this phase, simulations plays a major role in guiding the R&D.

“Microscopic” simulations, representing in detail the signal formation in the sensors and how it is processed in the Front End electronics, lead to enhanced understanding of the basic process of (new) technologies, allow to validate and optimize designs.

“Macroscopic” detector *simulations* allow to relate the detector design parameters (layout, technology) to the overall physics performance of the experiment. The *simulation* package should be accompanied by a sophisticated *reconstruction* framework. Monte Carlo production (GRID) infrastructure is required.

Needless to say, the whole system will be thoroughly validated (against beam and system tests) and meticulously kept up-to-date.

A flexible simulation and reconstruction framework, provides invaluable guidance to the detector design:

- studies of physics topologies will be used to draw up detector requirements
- the impact of design variations can reliably be predicted

Microscopic simulation

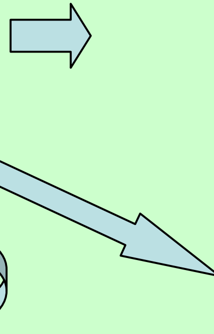
Read-out electronics design:

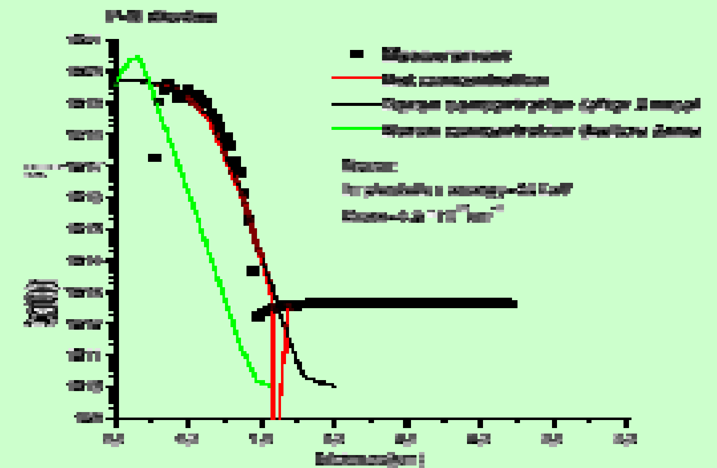
Behavioral models:	Simulink, ADS
Functional and system:	Level System Verilog, System C
Logical and RTL:	VHDL, Verilog
Electrical circuits:	SPICE, Spectre

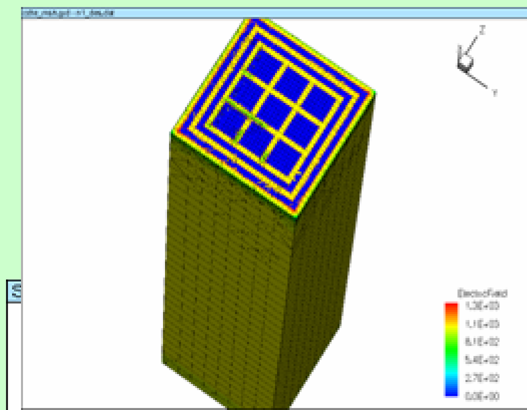
Several SiLC institutes have access to electronics design software
and experienced engineers

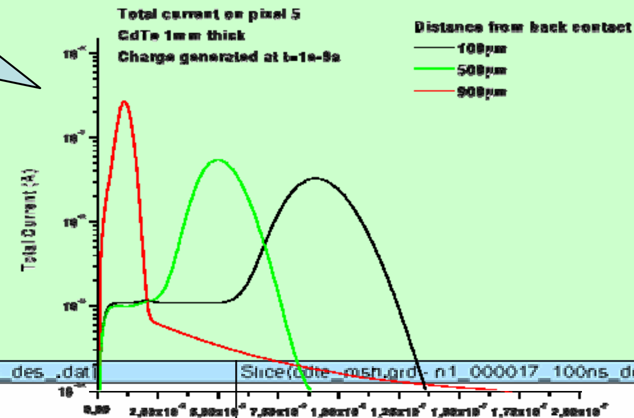
Detector simulation

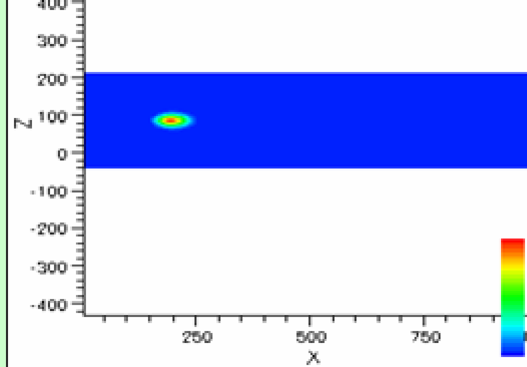
- ISE-TCAD, TMA, Silvaco
- Technology simulation
- Electrical simulation
  - Static and dynamic
  - Charge collection in 3D

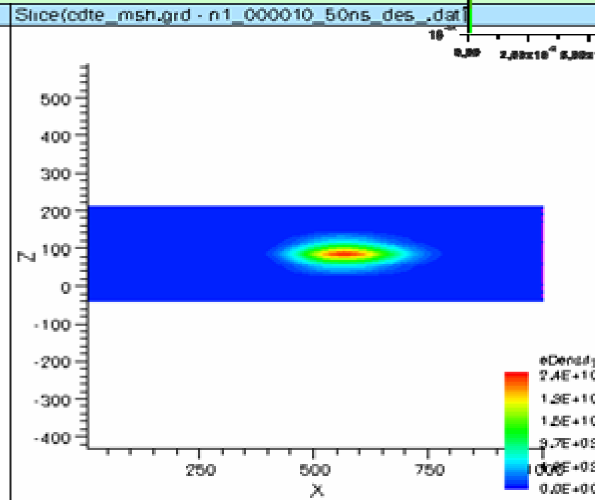


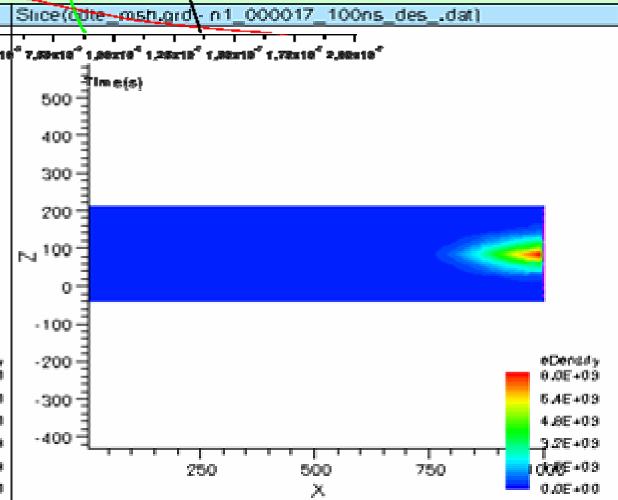










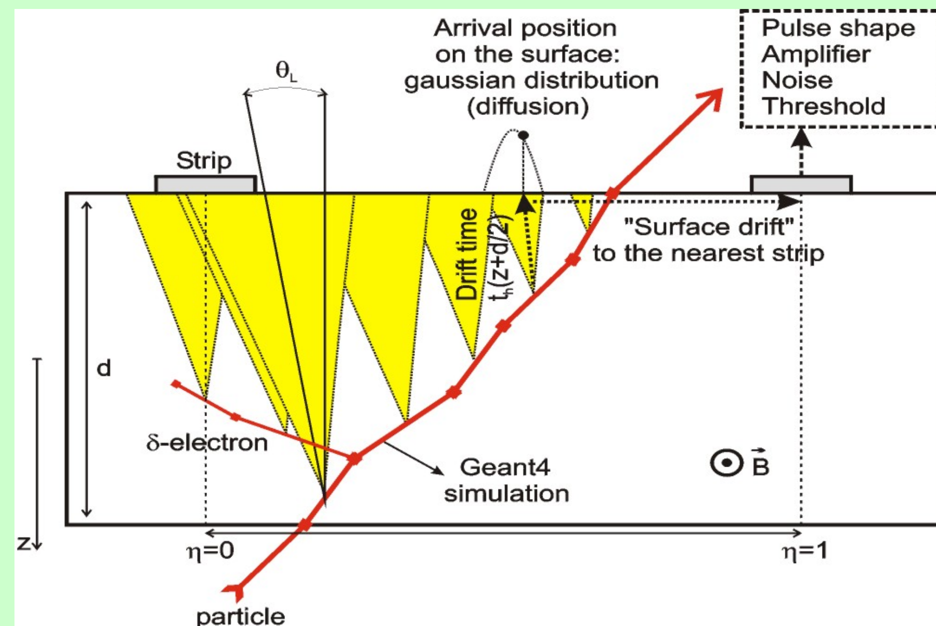


Thermal model of
ATLAS – SCT barrel
mstrip module

Digitization

The bridge between microscopic and macroscopic worlds.

Digitization step in the “full” simulation should represent our best understanding of the detector response. As the Front End and sensor design emerges, and results from (beam) tests of prototypes become available, this information is going to find its way into the simulation software.



Geant4 simulation in http://www-ucjf.troja.mff.cuni.cz/diploma_theses/reznicek _dipl.pdf

Macroscopic simulation

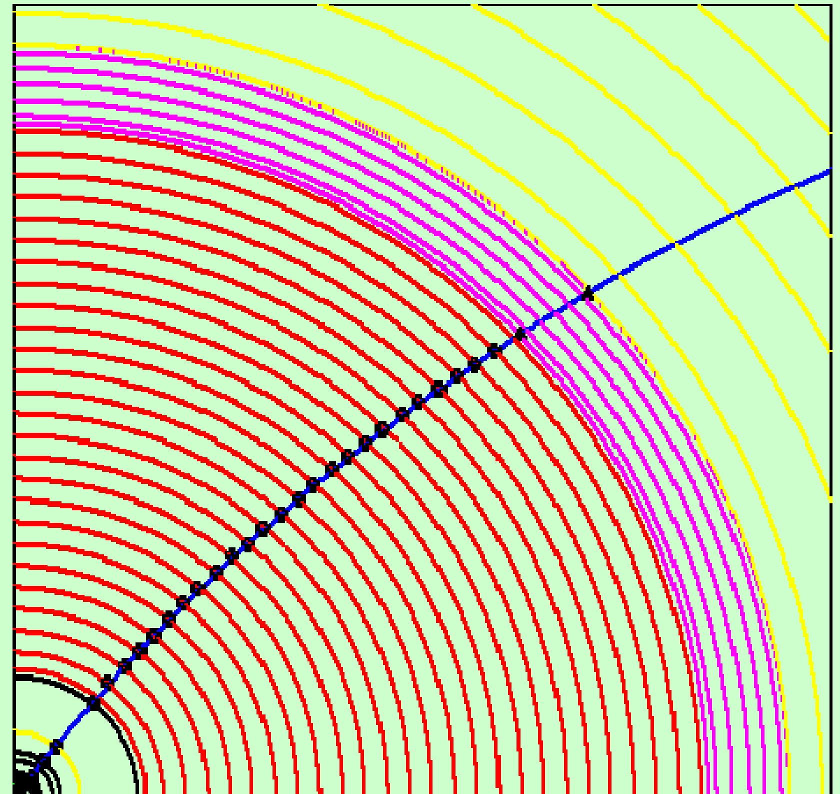
Fast simulation:

Provides a reliable estimate of “ideal” parameter resolutions for a given layout.

Macroscopic simulation: SGV

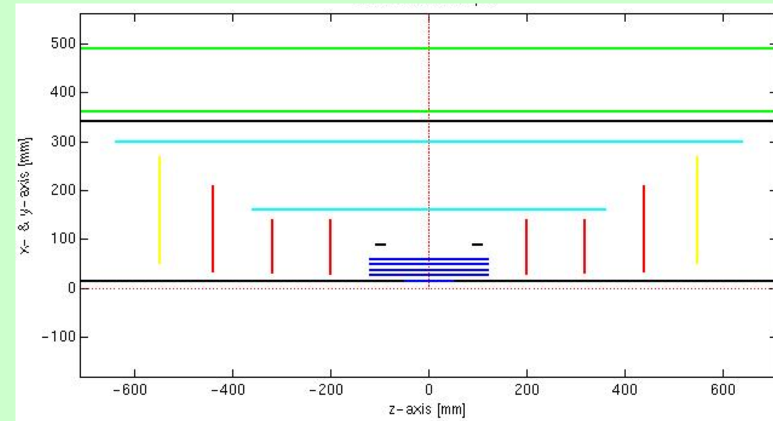
Simulation a grande vitesse, M. Berggren, LPHNE, Paris

Analytical calculation of track parameter resolution from geometry LCIO output module (B. Jefferey, Oxford) allows to compare full and fast simulation outcome on the same footing.
The program has a long history, and has been thoroughly validated against a running experiment (DELPHI).



Macroscopic simulation: LiCToy

LiCToy, M. Regler, M. Valentan, R. Fruehwirth, LPHNE, HEPHY, Vienna



Fast simulation tool for detector design.

Position measurements are simulated at the intersections of an ideal helix trajectory and a simplified geometry.

Sophisticated Kalman filter track fit, including material effects, yields the parameter covariance matrix.

Validation against experiment and other simulators ongoing.

http://wwwhephy.oeaw.ac.at/p3w/ilc/talks/06_SiLC_Barcel/MK_LiCToy.ppt

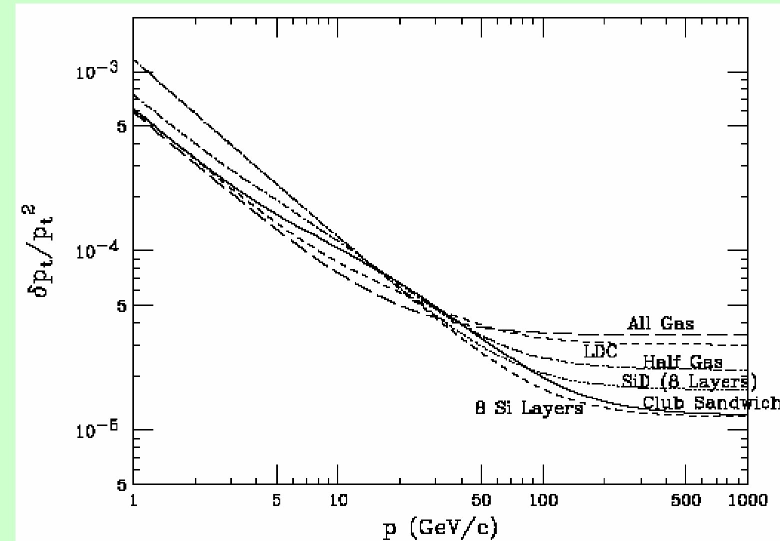
http://wwwhephy.oeaw.ac.at/p3w/ilc/reports/LiC_Det_Toy/UserGuide.pdf

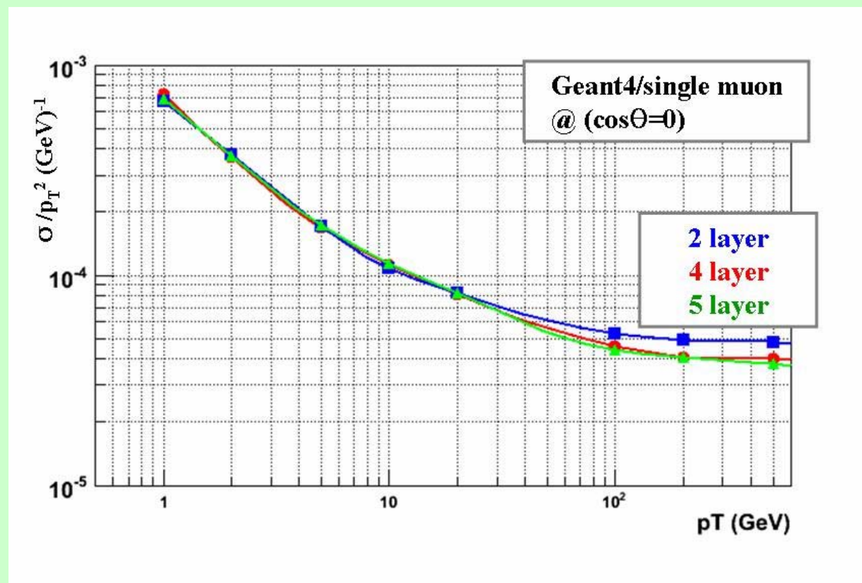
Macroscopic simulation: fast

LCDTRK (Bruce Schumm, SCIPP): analytical determination of momentum resolution for a given layout, space point resolution, material burden

http://ww.slac.stanford.edu/~schumm/lcdtrk20011204.tar.gz

excellent example: hep-phys-0511038





GLD fast simulation (Korea): Kalman filter fit of space points from fast simulation

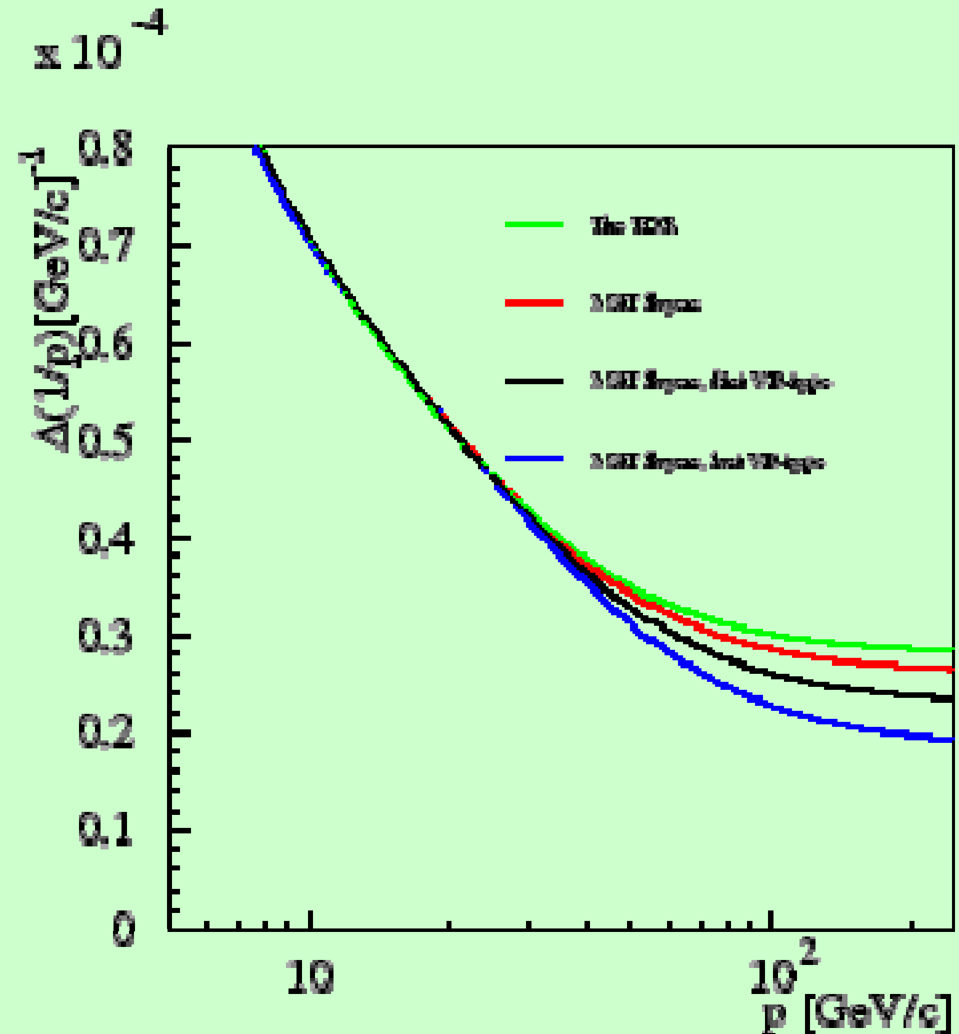
Macroscopic simulation: fast

Fast simulation provides important feed-back to layout optimization:

SGV simulation (M. Berggren) of the LDC tracker central region

Momentum resolution for 4 different SIT scenarios.

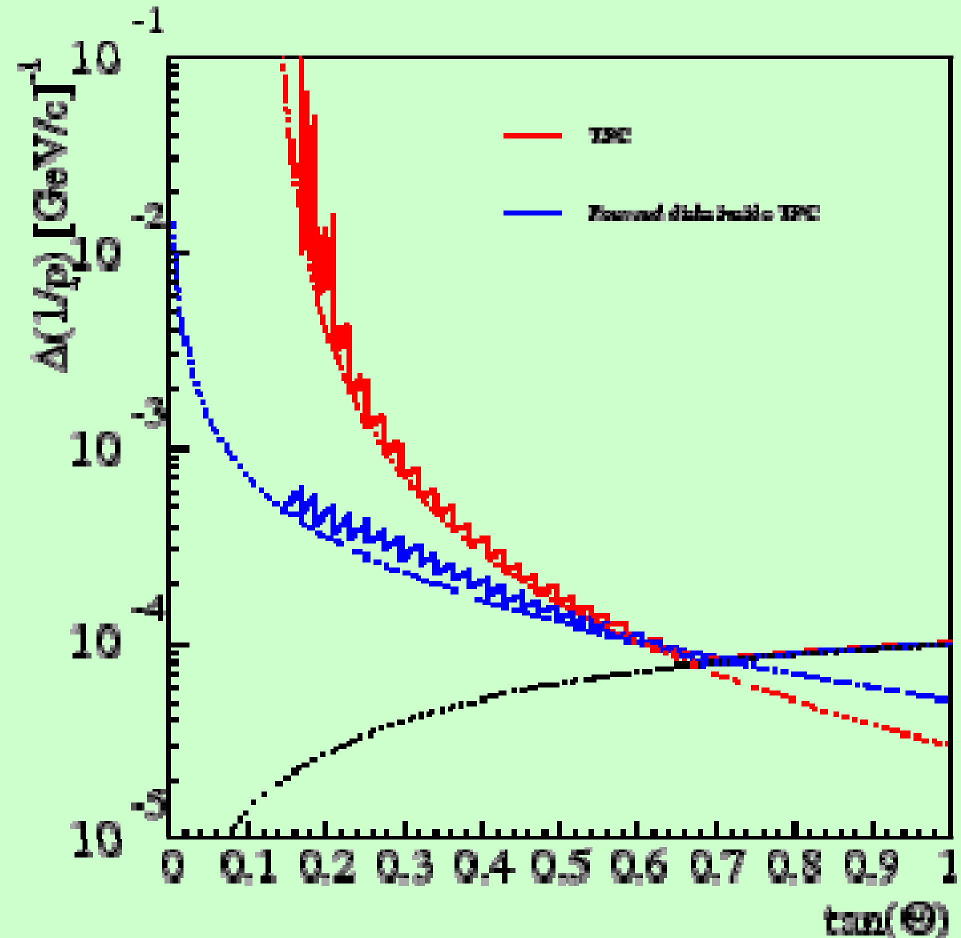
2-3 layers -> marginal differnce
improved space point resolution yields substantial gain (especially for outer SIT layer)



Macroscopic simulation: fast

SGV simulation (M. Berggren) of the LDC tracker central region

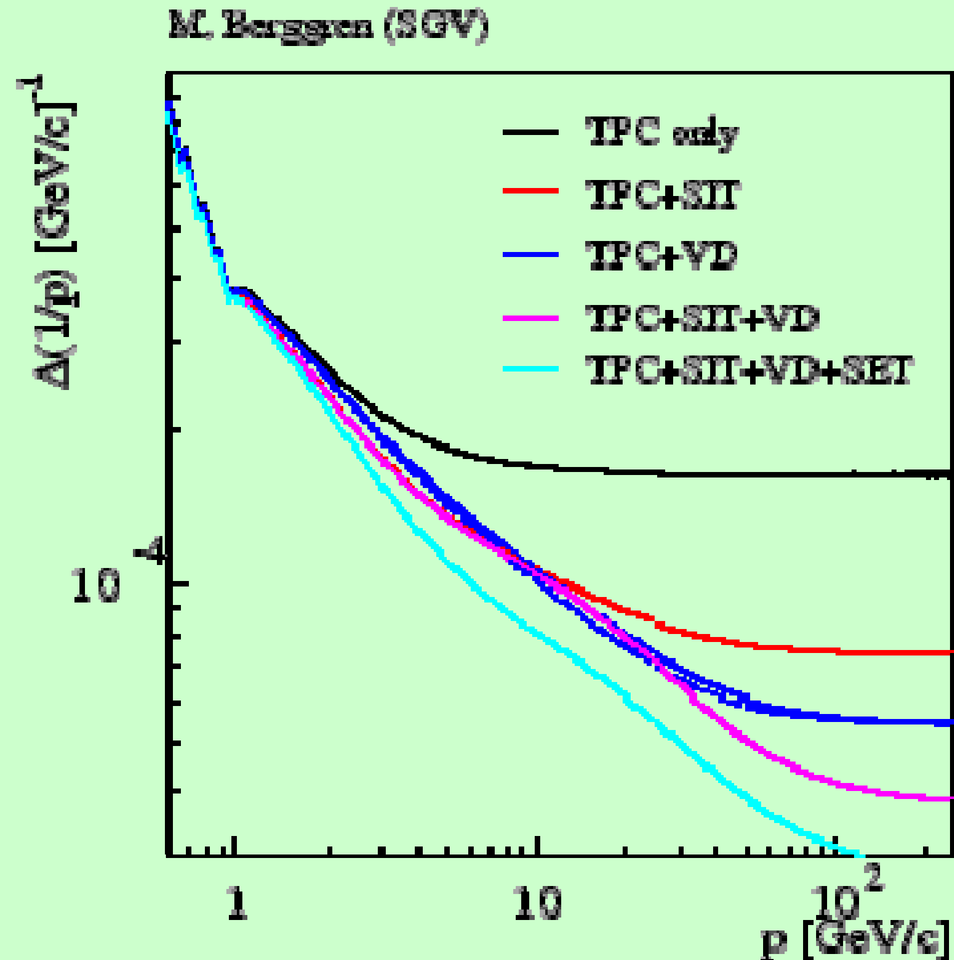
Impact of silicon (FTD) disks on momentum resolution on forward tracking.
To maintain an adequate performance in the forward region, the TPC must be complemented by silicon.



Macroscopic simulation: fast

SGV simulation (M. Berggren) of the LDC tracker central region

Silicon envelope for the TPC: a precise measurement extending the lever arm improves resolution for large momentum.



Macroscopic simulation: full

Full simulation:

Full detail in detector geometry.

GEANT4 description of particle interactions with detector.

Detector response ("digitization").

Full simulation only provides guidance if complemented by a sophisticated reconstruction framework, with realistic implementations of central algorithms.

Macroscopic simulation: full

Several (regional) frameworks exist:

Europe: Mokka (http://www-flc.des.de/ilcsoft/ilcsoftware/Mokka/), MySQL geometry description, GEAR

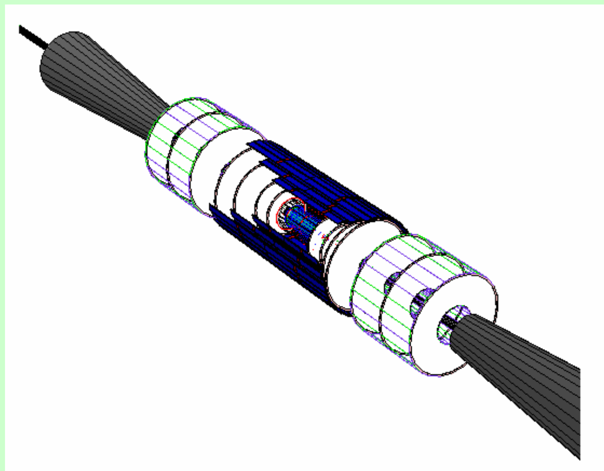
America: SLIC (http://www.lcsim.org/software/slic), XML-based GDML

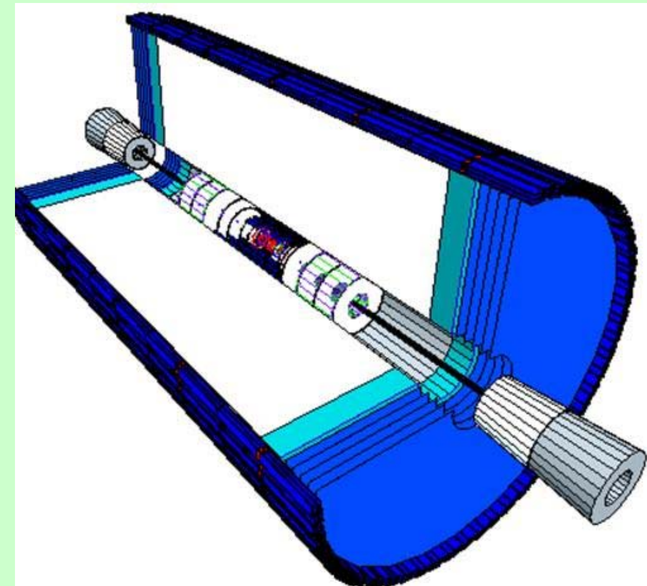
Asia: Jupiter

Geometry implementation: LDC in Mokka, SiD in SLIC and Mokka, GLD in Jupiter

SiLC is closely following the unified geometry description effort

Digitization: in progress



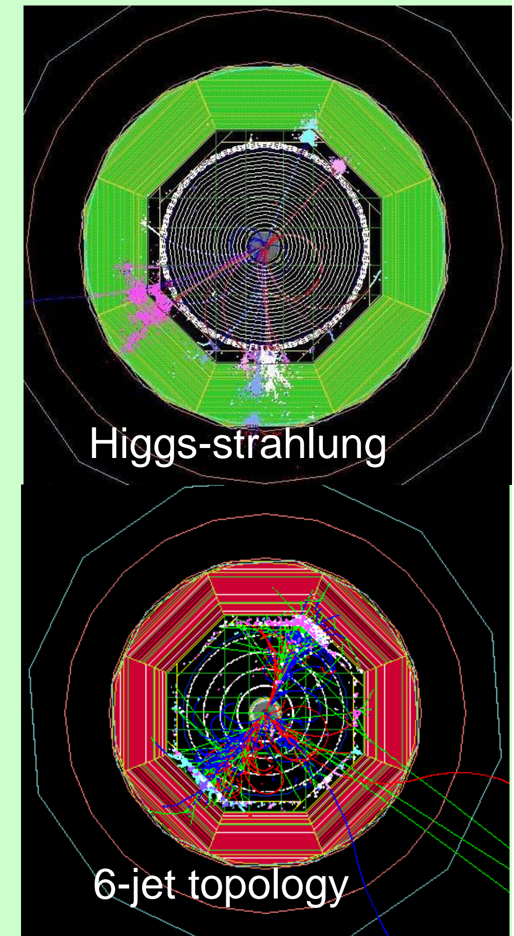


Macroscopic simulation: full

Using GRID and LCIO several data samples are accessible:

- For various relevant signal topologies
- For pair-background due to beamstrahlung (*)
- For the main detector concepts

(*) generated using GUINEA-PIG, simulated for LDC geometry, nominal machine parameters, anti-DID field, Adrian Vogel, Desy



Pattern recognition

Tracking environment: the challenge to pattern recognition should be studied in detail following the ILC physics benchmarks, in particular and for example:

- jet topologies:
  - Highest possible total multiplicity: tt
  - Highest possible collimation: tau jets
  - Highest energy jets: light quark antiquark

- for Non-prompt tracks (long-lived particles, photon conversions) pose a special challenge which will be studied by SiLC:
  - SIT or FTD in LDC
  - SIT and FIT in GLD
  - first SiD layers

issue: resolve ambiguities without the VXD

-Forward physics: comparison between two tracking strategies (gas+Si vs Si)

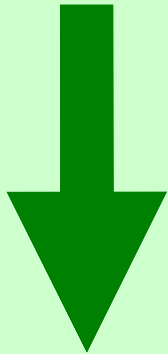
--Background rejection through precise BCO tagging

Pattern recognition

Occupancy: # hits/mm2/BX

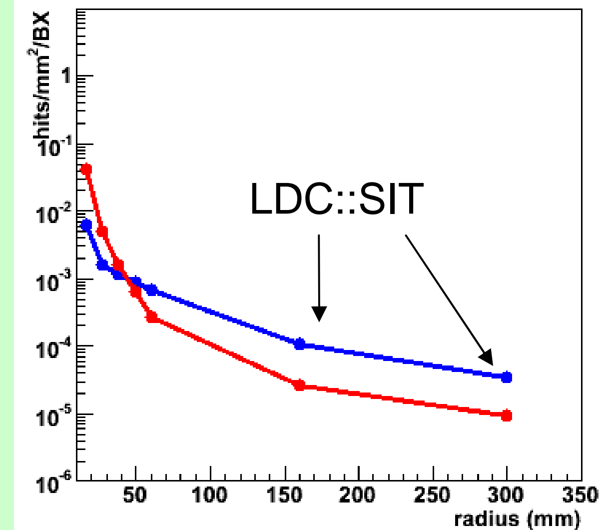
red: contribution from pair background

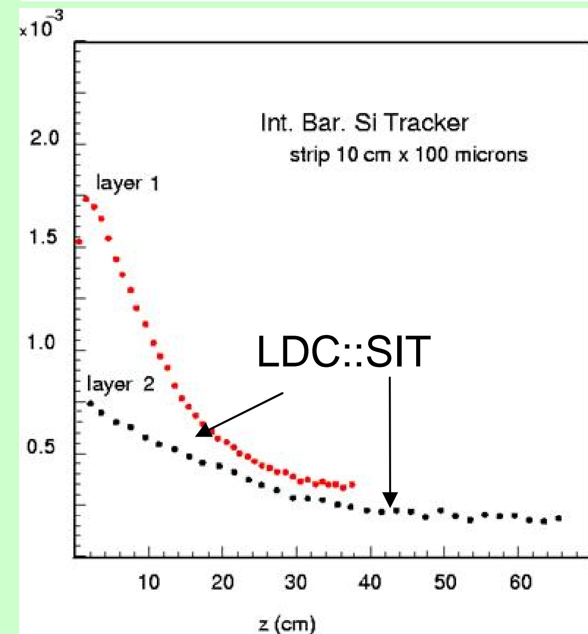
blue: dense signal topology (tt)



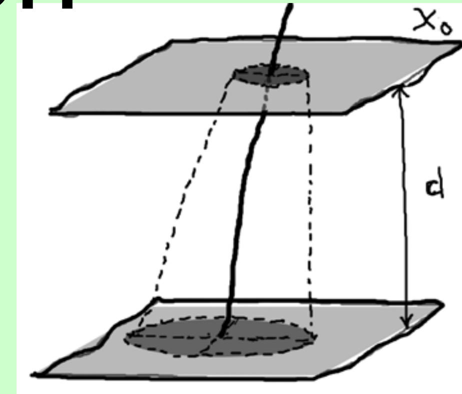
Convolute with detector design
(cell size, bunch crossing ID)

Occupancy: # hits/channel
(ZH -> mumu bb)





Pattern recognition

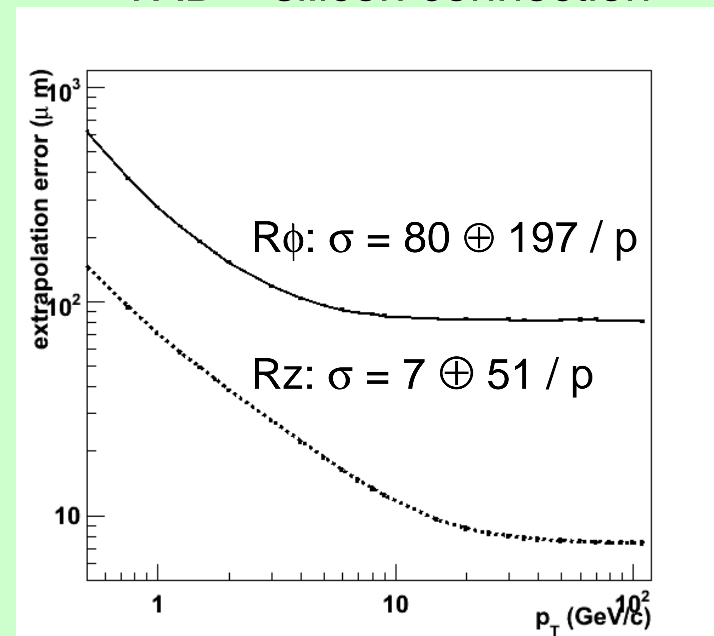


Convolution of search window with occupancy yields contamination or confusion.

Crucial layout parameters: distance VXD – silicon and VXD lever arm (for all concepts), distance TPC-silicon and material

Use a Kalman filter to predict the search window

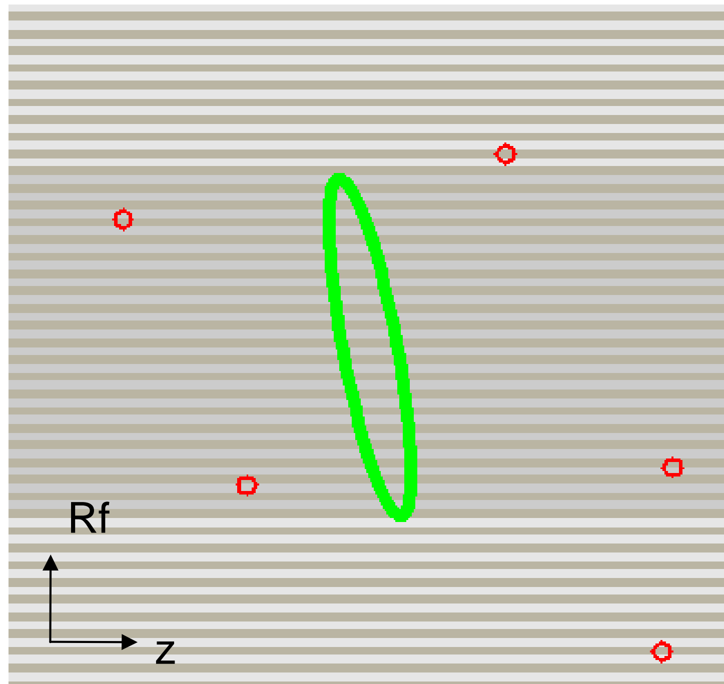
Typical result of a "toy" VXD – silicon connection

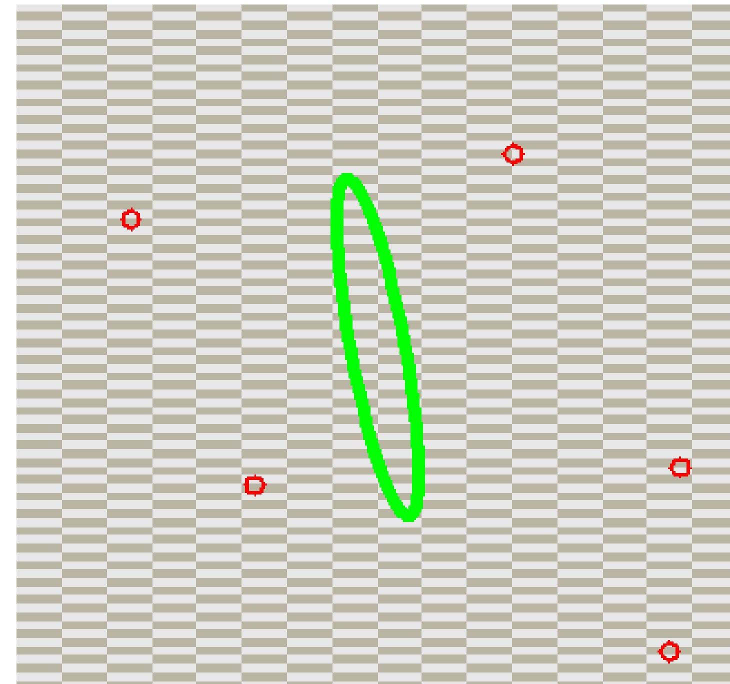


Search window

Example of interplay between search window and technology:

compatible hits in single sided silicon mstrip detector vs pixel detector.

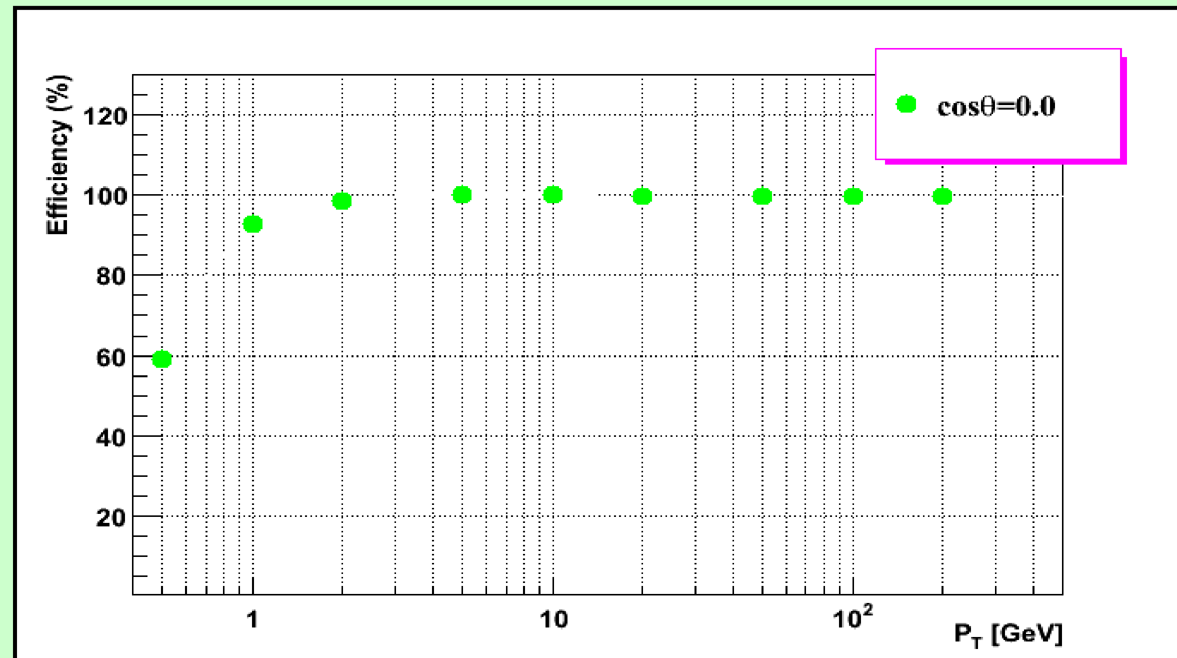




Reconstruction

Low p_T tracks clearly present a challenge to reconstruction software and detector.

Single-muon study of the GLD concept (Korean Group).



Outlook

The SiLC simulation taskforce is taking shape

Microscopic, and fast and full simulation tools in place

Effort needed on:

- understand background levels and its uncertainties and dependence on machine/detector parameters
- digitization
- pattern recognition:
- feedback to technology (cell size optimization for innermost layers)
- feedback to layout (disks with radial strips vs. XUV)
- embed SiLC effort in global ILC simulation & reconstruction framework

Lab test bench & test beams for Si trackers R&D

Needed tools because:

Lab test benches of different types are a first approach towards experiencing in more realistic ways various real life conditions. The test beams are their indispensable continuation and extension to ensure that the device will satisfy the requirements and/or verify how much it satifies them.

Test beams allow identifying new problems, not yet anticipated even at Lab test bench.

Test beams allow combining several sub detectors.

Lab test bench and test beams give feedback to the simulations (refining them).

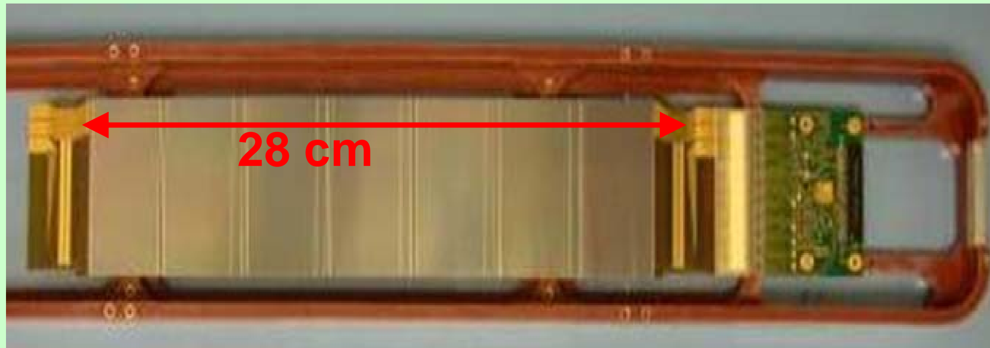
o Most (if not all) the Institutes participating to SiLC have Lab test bench facilities. All intend joining the SiLC test beam programme.

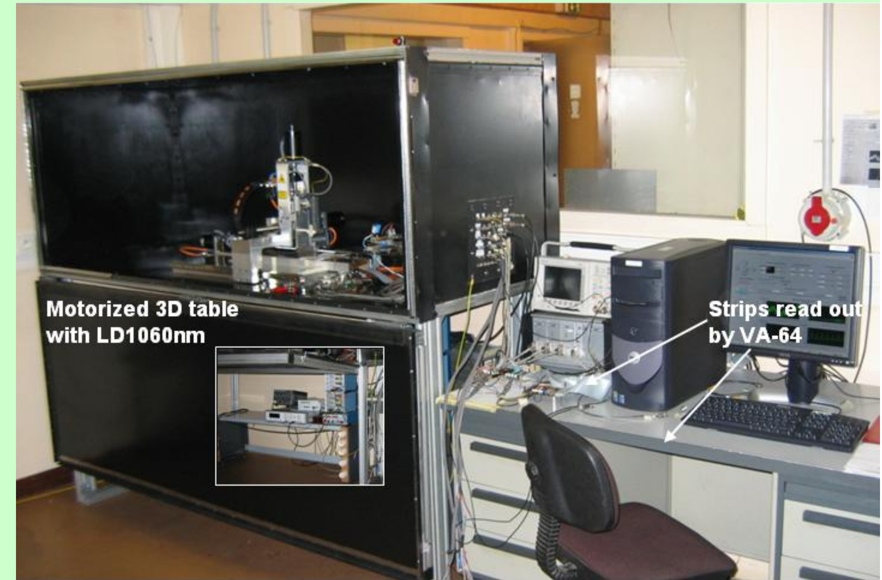
o Both the continuous needed evolution of the Lab test bench and the construction and running of the test beams are requesting lot of efforts (FTE) and of financial support.

LAB TEST BENCH: results

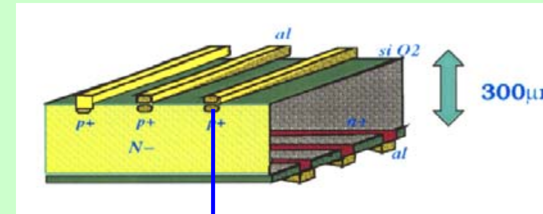
(LPNHE + U. Geneva, CU Prague)

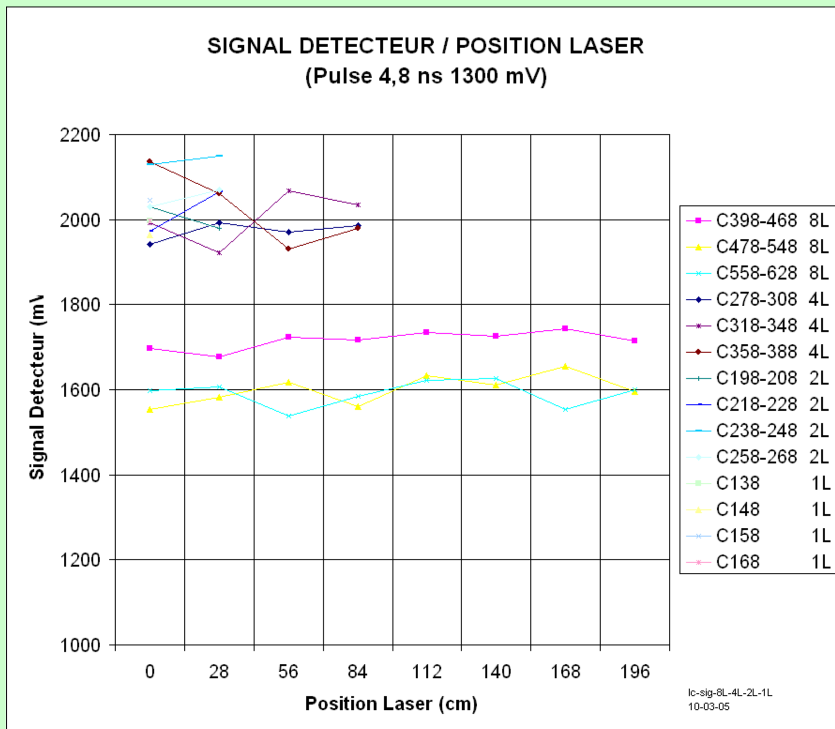
Detector with µstrips of L= 28 cm x (N=1,4)
VA_64hdr readout chips from IDEAS.

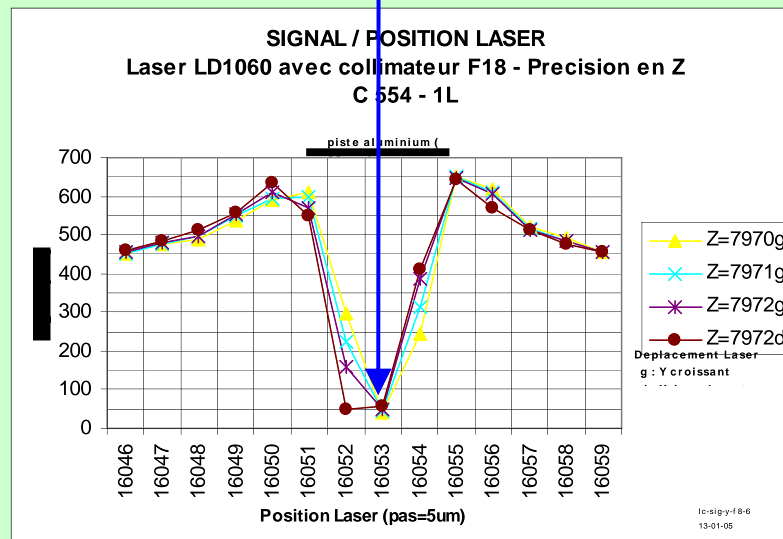




➢ **Characterization with LD1060**

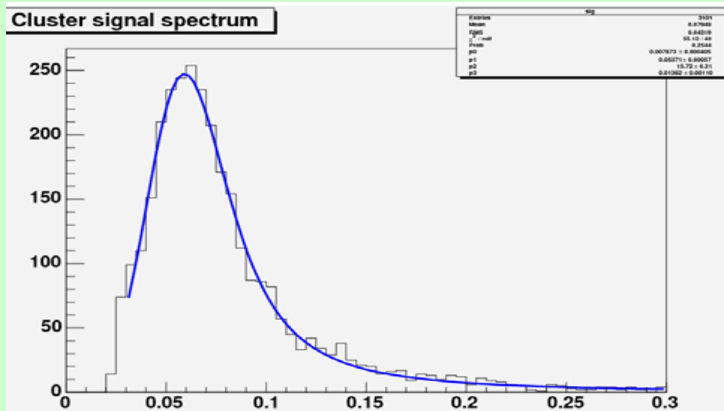




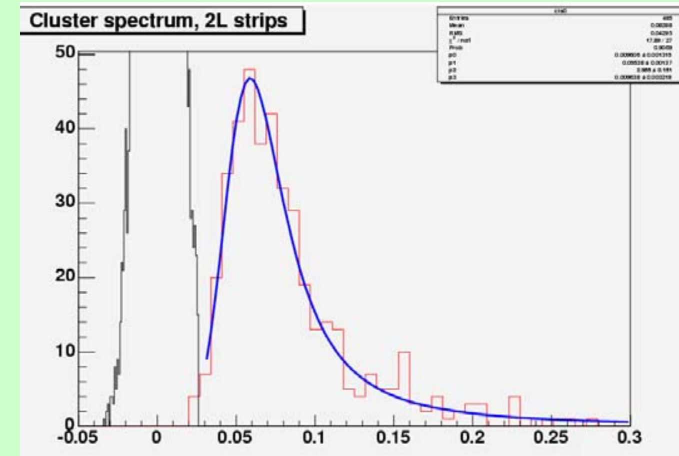


Signal-to-noise ratio vs µstrip length

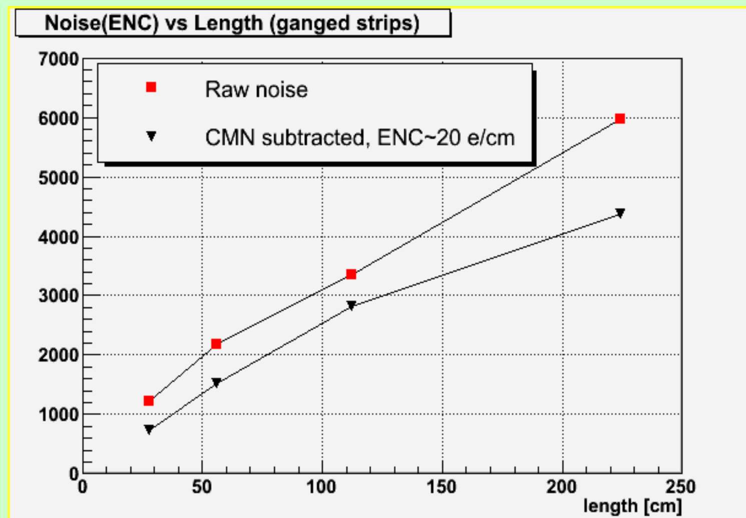
- ***Characterization S/N with a radioactive source***

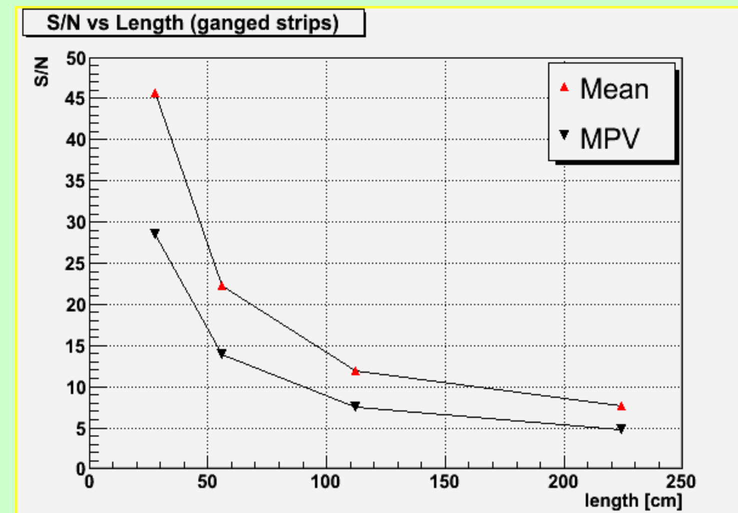


S/N for 28cm strip long: **20 (MPV) or 30 (Mean)**

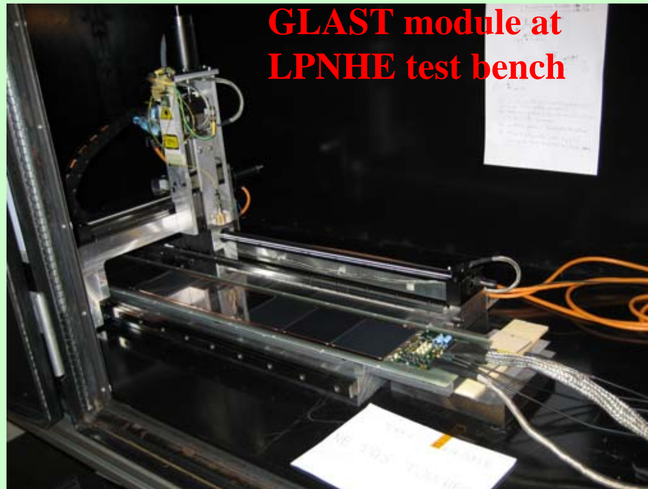


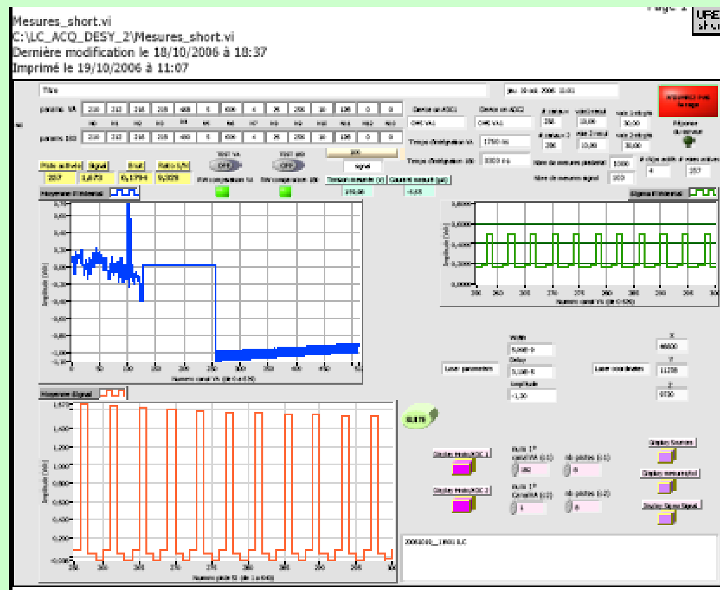
S/N for 56 cm strip long: **12(MPV) or 18(Mean)**

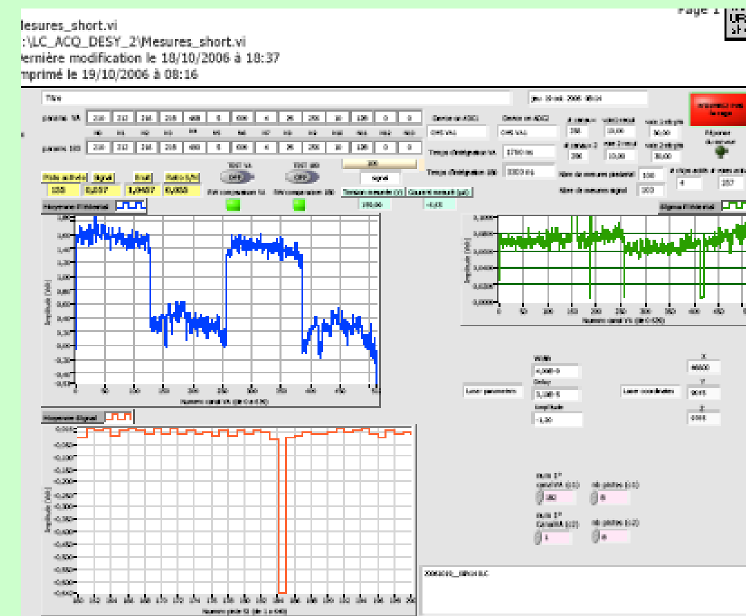




Before leaving for the test beam in DESY: tests the functioning of the modules & associated FEE

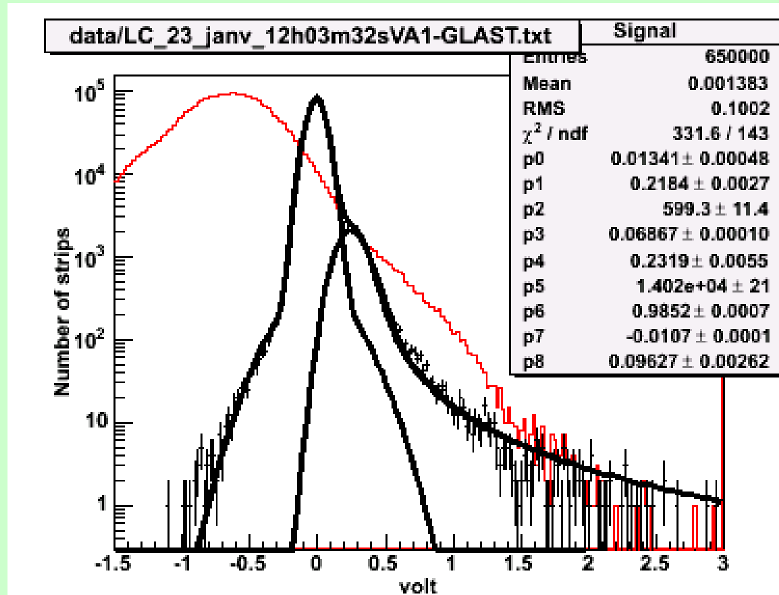


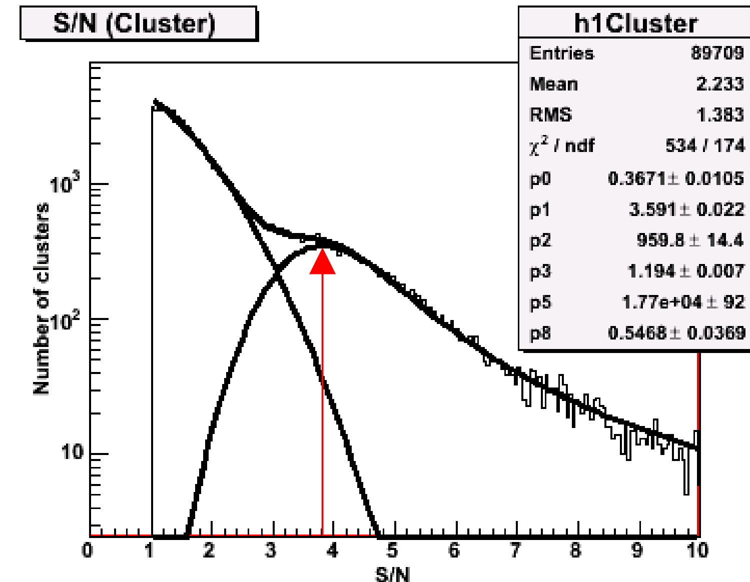




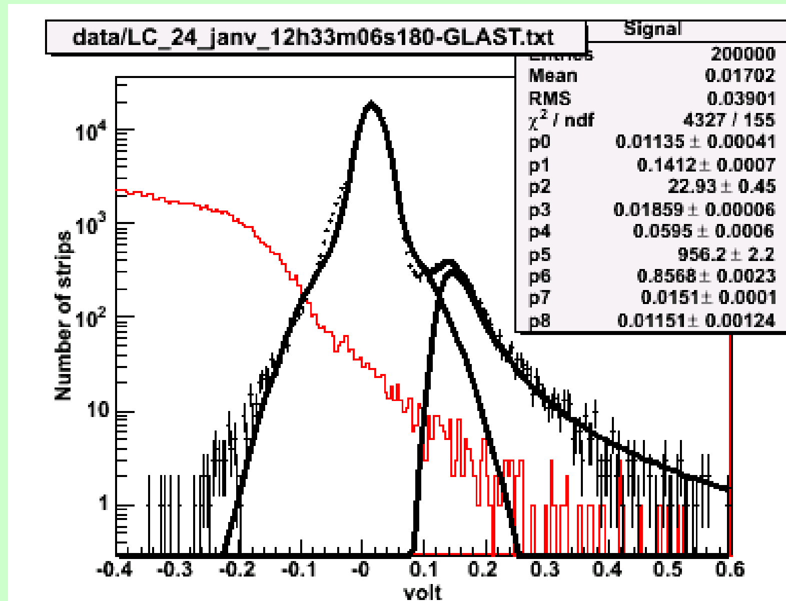
S/N measured with SiTR-180 *(after t.b.)*

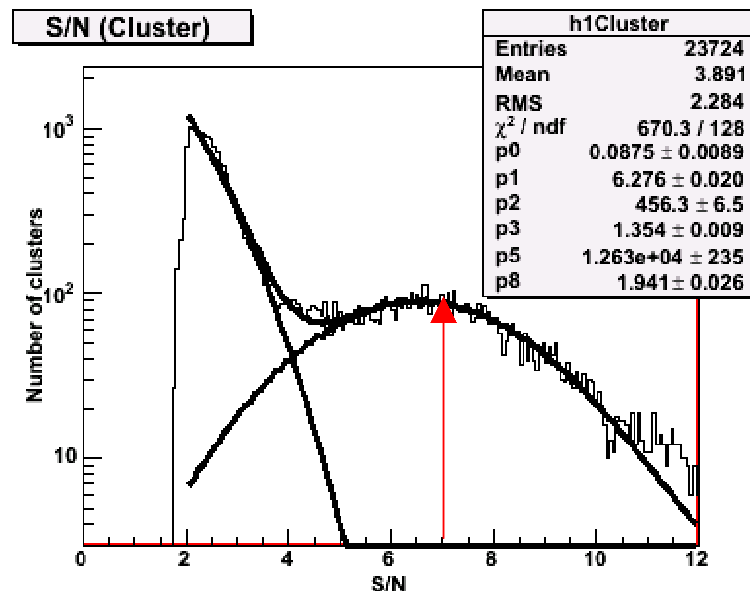
W. Da Silva, J. David, F. Kapusta, F. Rossel (LPNHE)





GLAST module channels read by VA1 (top) or 180 (bottom)



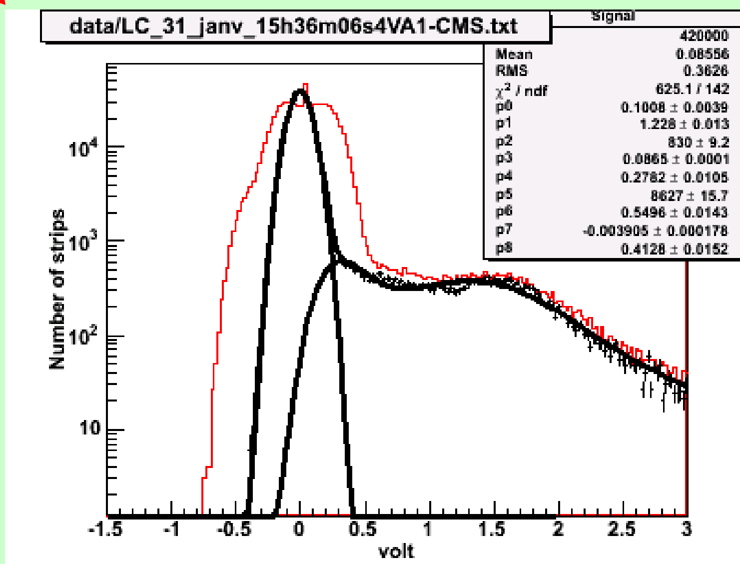


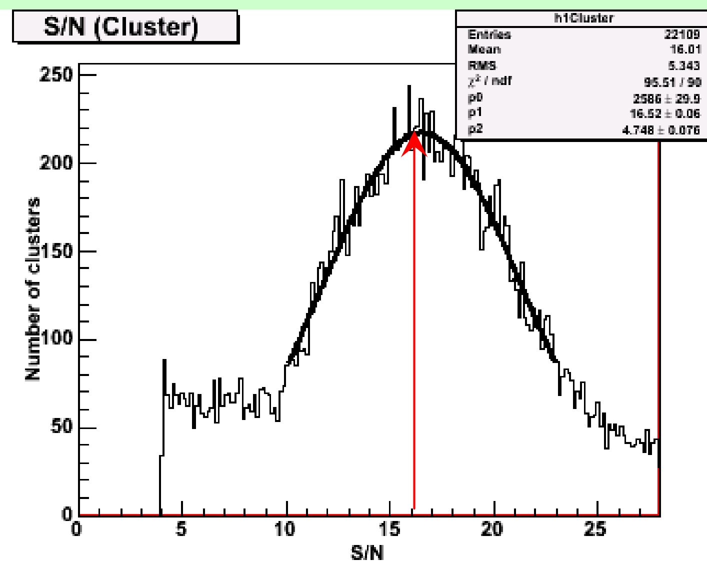
VERY VERY PRELIMINARY

S/N measured with SiTR-180

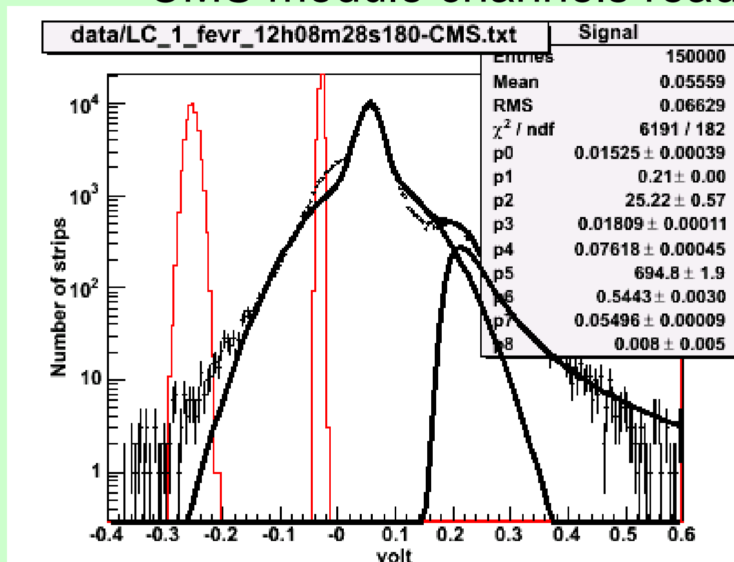
W. Da Silva, J. David, F. Kapusta, F. Rossel (LPNHE)

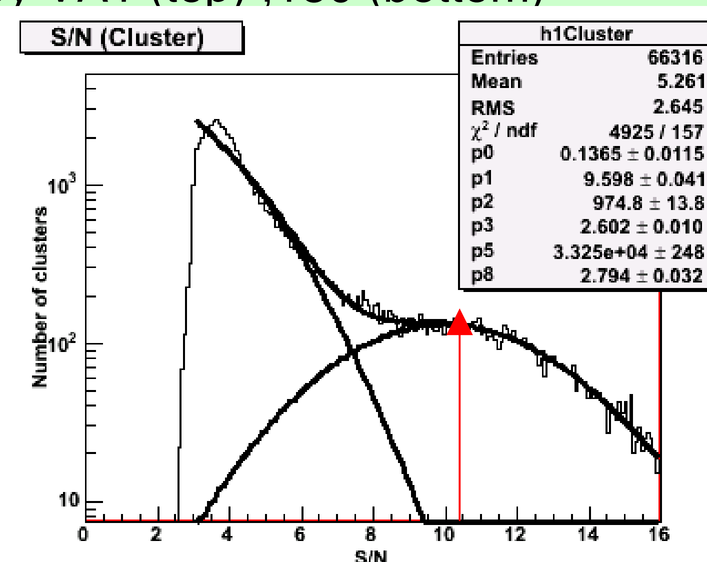
VERY VERY PRELIMINARY





CMS module channels read by VA1 (top) ,180 (bottom)

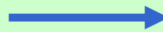


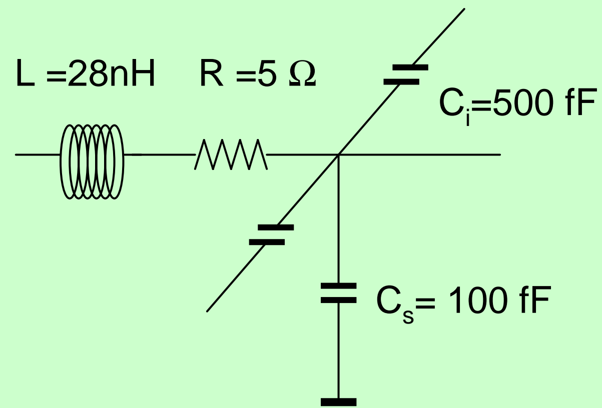


N.B. Not the same module tested (CMS+4VA1 vs CMSVA1+180)

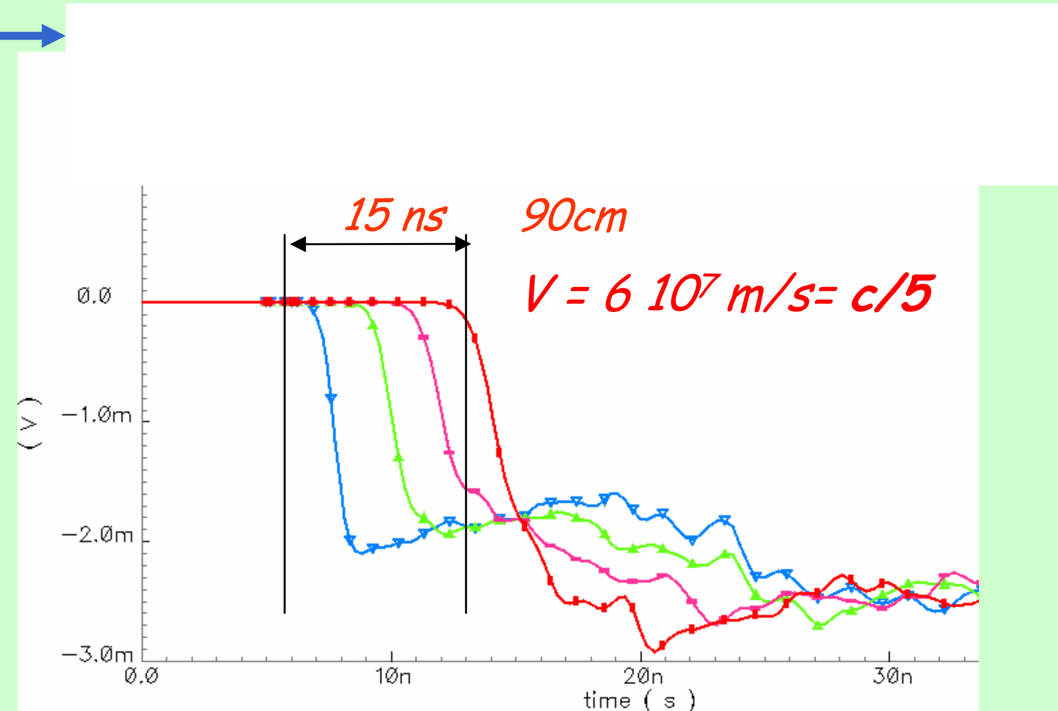
Coordinate along the strip

J.F. Genat (LPNHE)





$$V = 1/\sqrt{LC}$$

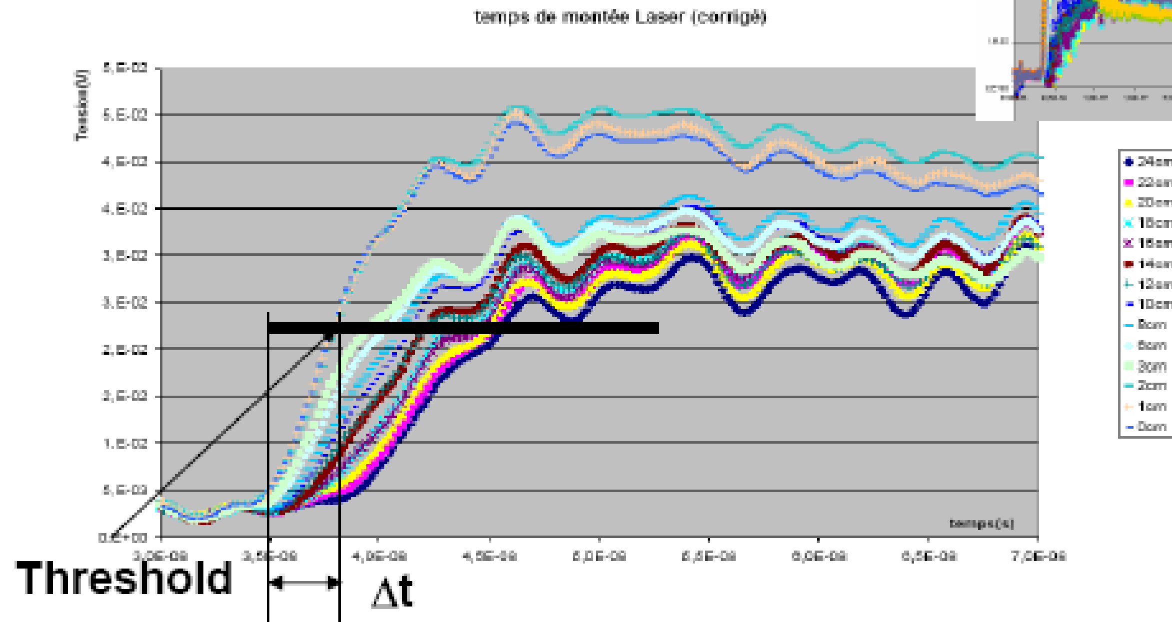


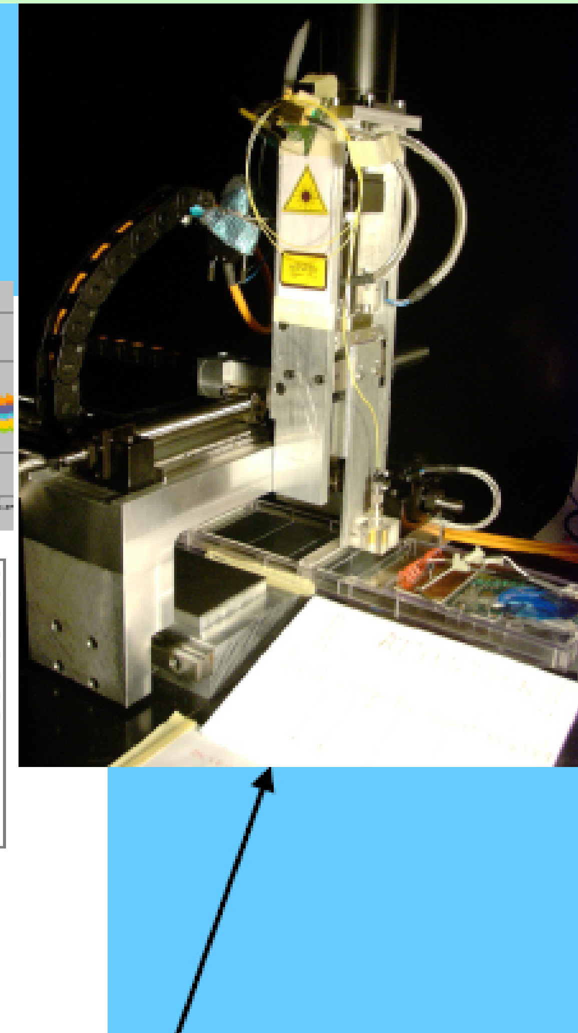
1 ns time resolution is 6 cm

Jacques David et Francois Rossel (LPNHE)

Measured Pulse Velocity on Lab test bench: reality

Measured velocity: 22ns/m



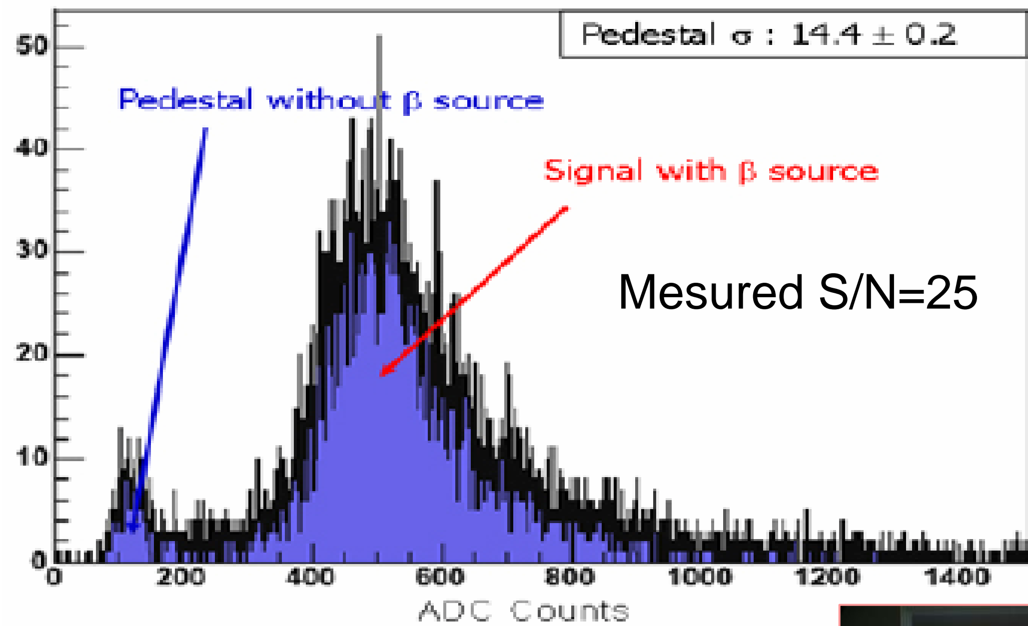


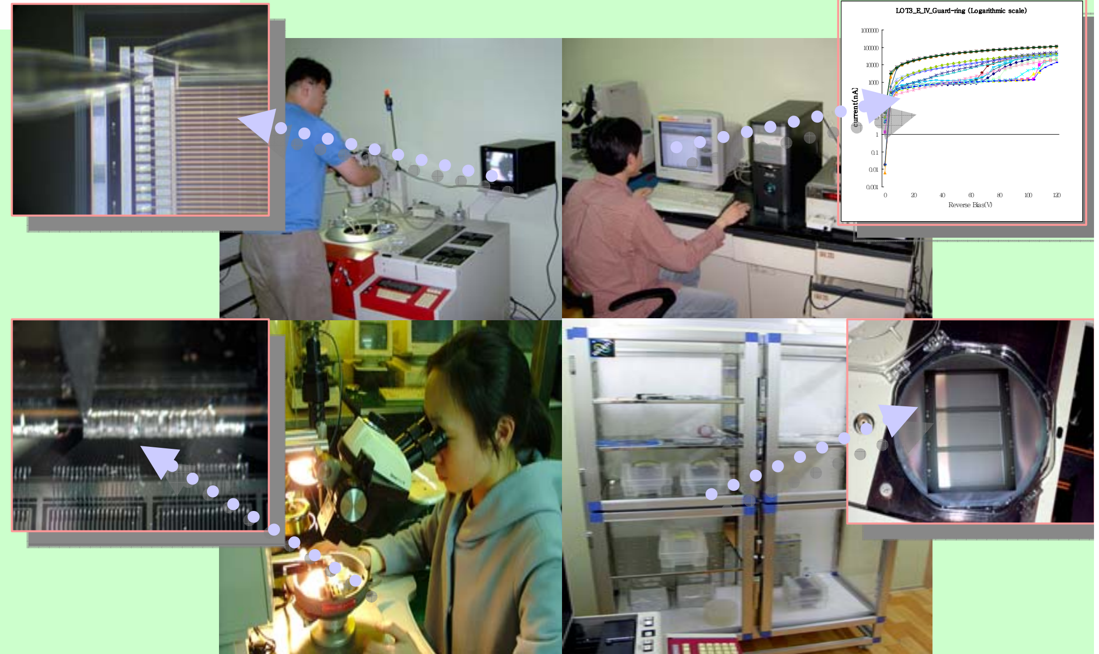
Measured velocity: 5.5cm/ns Measured moving a laser diode along 24 cm at LPNHE Lab test bench with first module prototype

Now: Improving the Lab test bench measurement using Radioactive Source

Will start design of the fast FEE in one of the next chips.

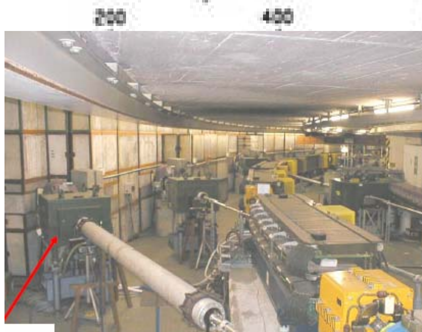
Characterization of new sensors *(Korean group)*





Silicon Main Tracker R&D:

Test beam present status and perspectives



SiLC Roadmap & Scientific Objectives

23/10-3/11/2006
DESY 1-6 GeV e-
S/N: 180nm/ VA1,
two 30cm strip
modules & one
90cm strip module

-April 07: DESY 130nm
-July 07: CERN 2 mod.
new sensors+VA1-130nm
-Nov. 07: CERN cont'd
-2008: Full size Si detector
pro.; combined tests(small
calo, F.C. +TPC,B field)
with various Si prototypes
and 128 ch chips

2009: FNAL(CERN)
Combined tests with
final protos of Si
tracker, calo and TPC
new foundry FE chips,
cooling and alignment
protos and new chips

2006 | 2007 | 2008 | 2009

Preparation test beam 07:
130nm chips & detector protos

Prepa test beam 09:new chips & new
detector protos, cooling & alignment

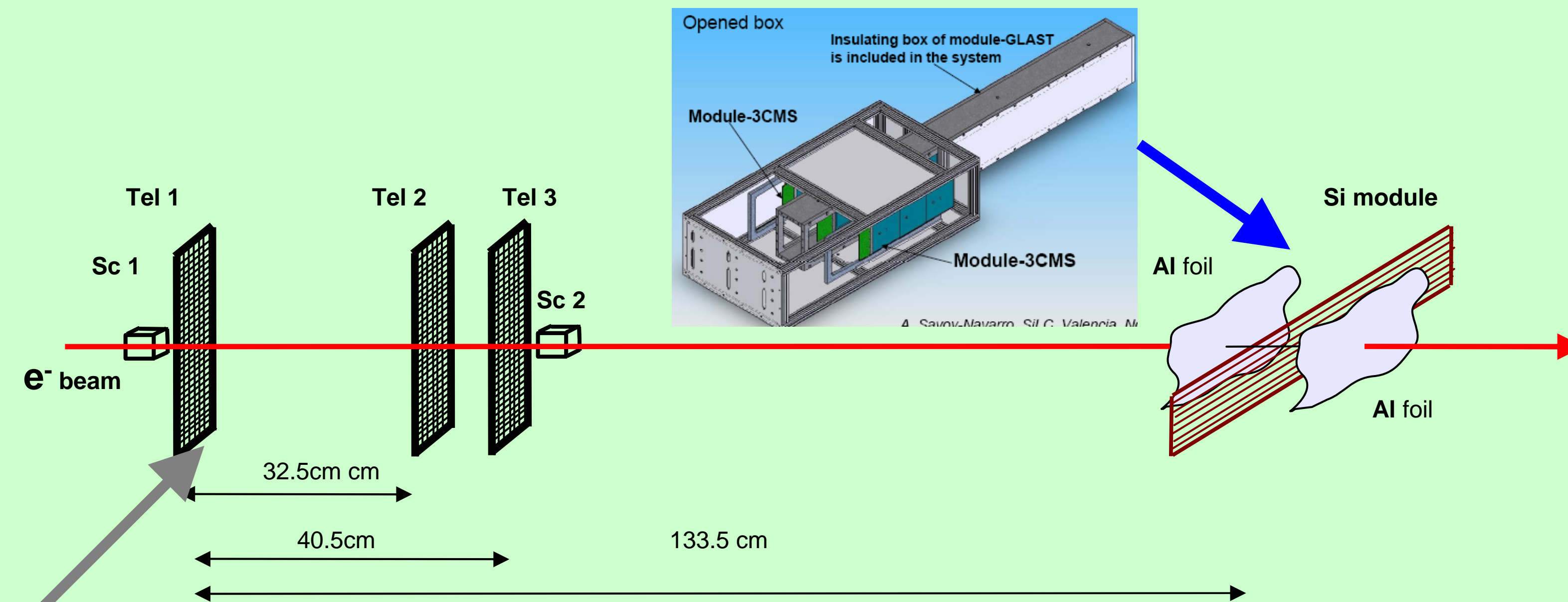
To be delivered: **VDM FE readout chips to equip test beam prototypes**

Large area SIlicon tracking structure prototypes
Cooling & alignment systems
Series of testbeams Si alone or combined (see Roadmap)

SiLC Test beams @DESY in 2006

1-6 GeV e- beam, no B, from Oct. 23 to Nov. 3; this will be pursued April 07; goals:

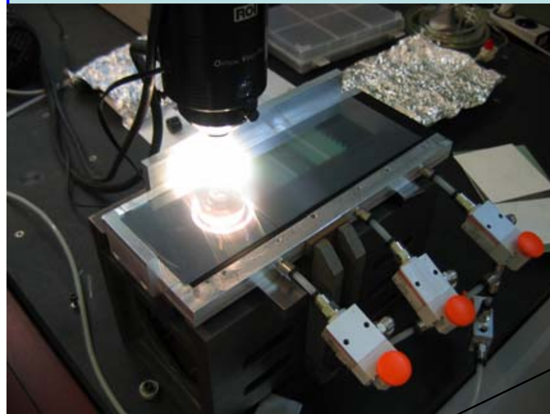
- Test the complete new test set-up (modules, read out electronics, DAQ)
- Compare new first FEE prototypes (SiTR-180/130,wrt to reference: VA1)
- Measure S/N



sensor	pitch [μm]	total length [mm]	FE electronics
GLAST	228	900	180 nm + VA1
CMS	183	283.5	180 nm + VA1
CMS	183	283.5	VA1 (reference)

Detector prototypes

CERN(A.Honma), IEKP-Karlsruhe, LPNHE-Paris, IEHP-Vienna, Hamamatsu



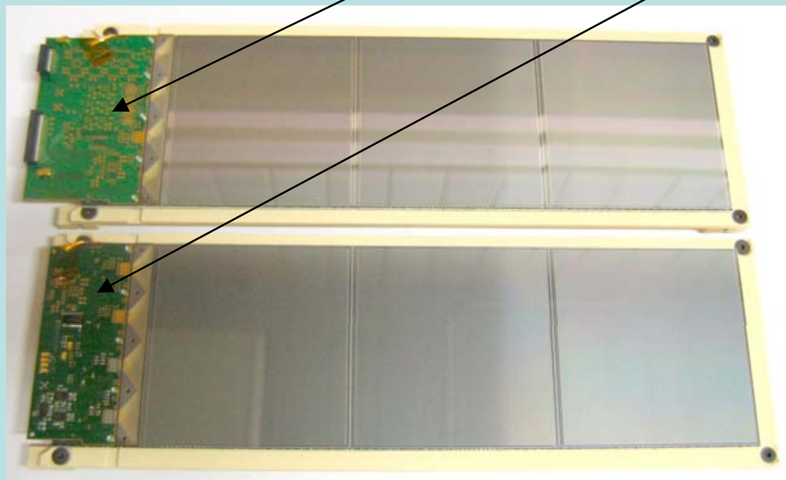
Assembly

3 CMS sensors 28 cm strip long

Read out:

VA1+180UMC r.o

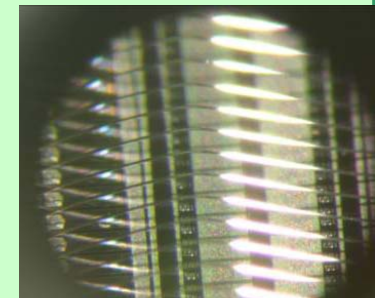
and all VA1 r.o.



2 modules fabricated in Paris,
bonding CERN on automated CMS system
(Collab CERN-LPNHE)

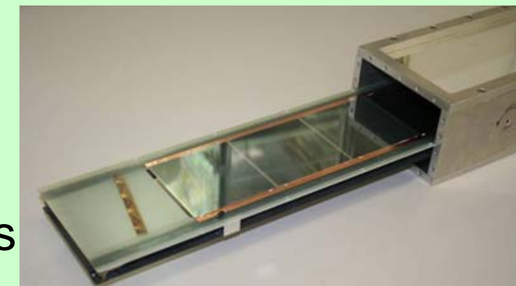
Assembly:
Module = 10 GLAST sensors
90 cm strip long

Bonding

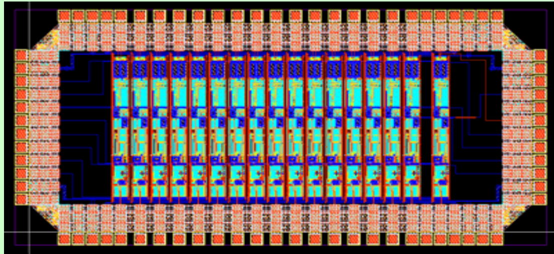


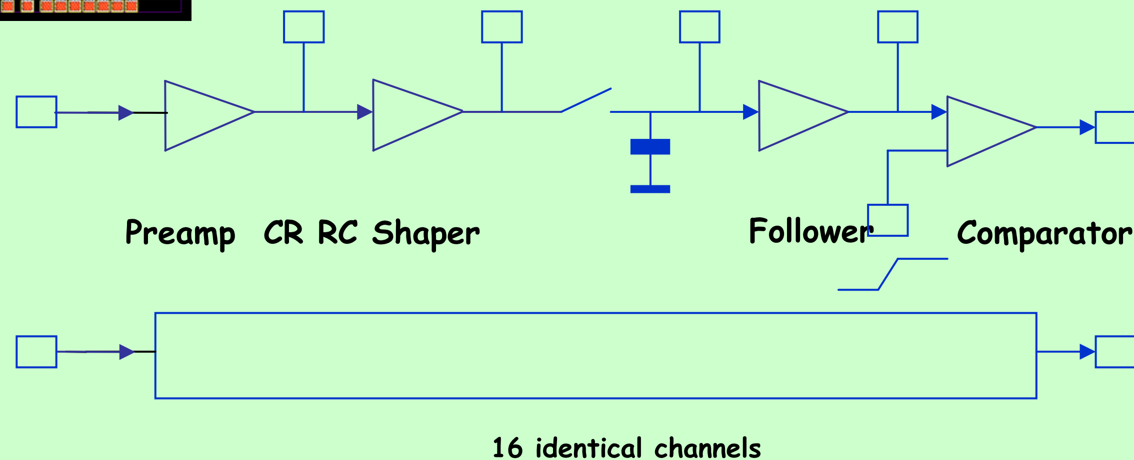
The full construction done at IEKP

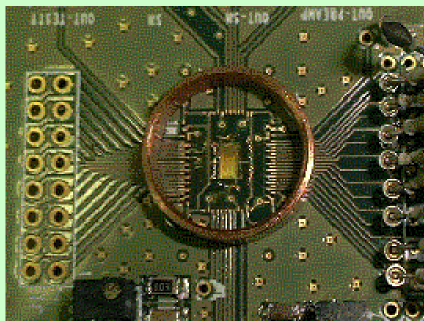
R.O.
Pitch adapter +
VA1 + 180UMC
provided by Paris



Front-end chip: SiTR-180 first prototype







- Low noise amplification + pulse shaping
- Sample & hold
- Comparator
- No power cycling yet

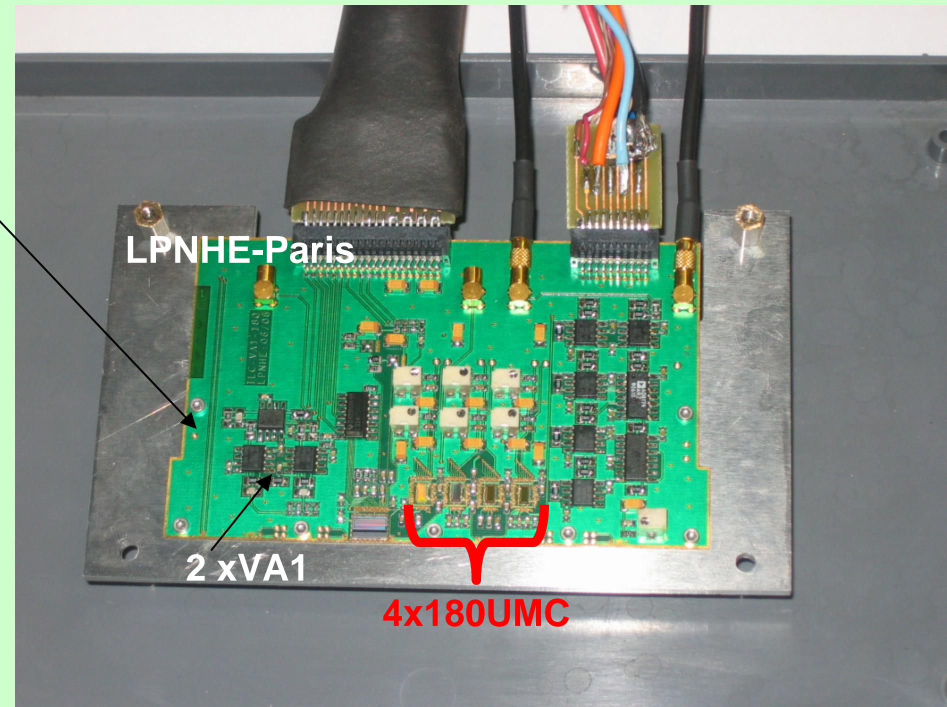
Readout Electronics: LPNHE Paris

2 VA1 + 4x 180UMC channels: hybrid R.O. card under test

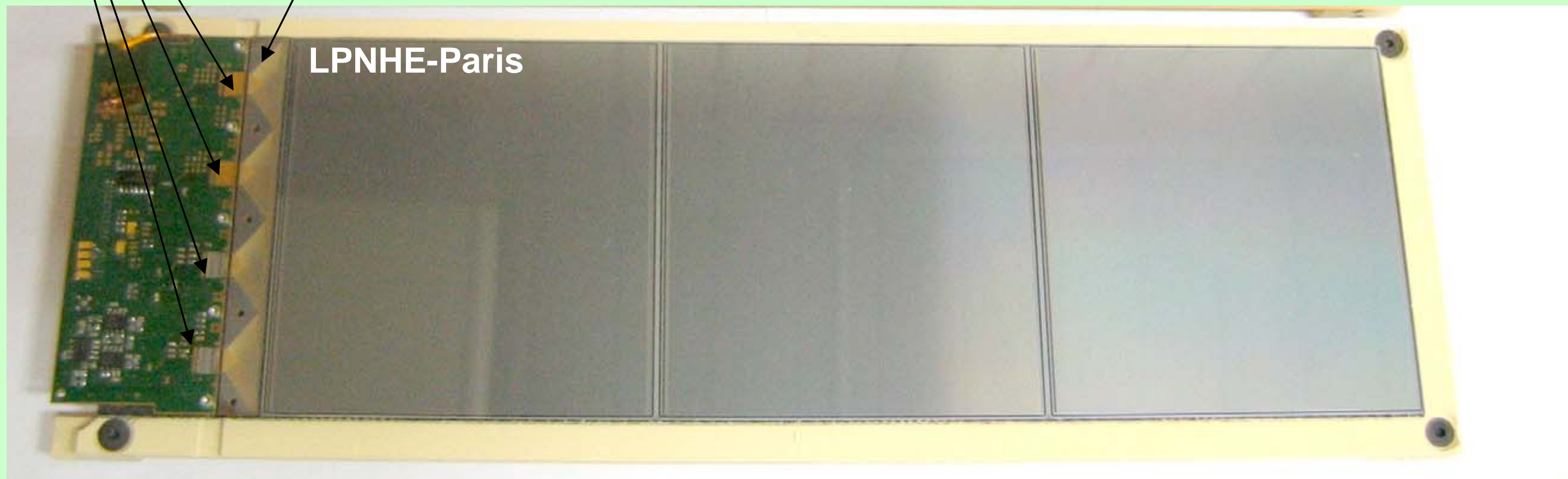
- VA1 r.o. card ready
- 2 hybrid r.o. cards: VA1+180UMC ready

Both being tested at Paris Lab test bench

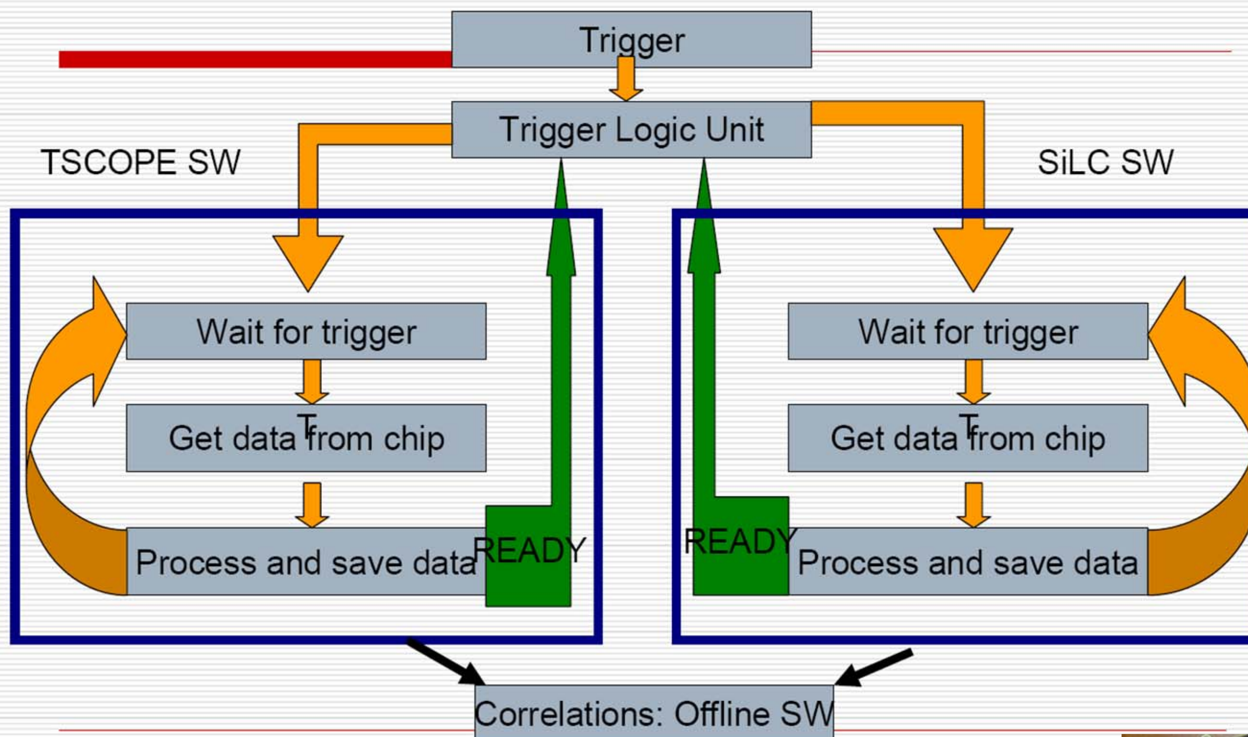
4 VA1 r.o card



Pitch adapter



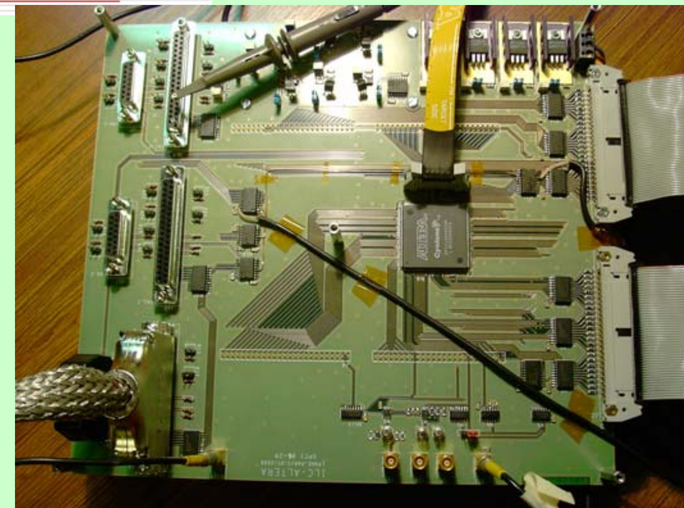
DAQ: hardware & software



LPNHE-Paris:
Rebuilt its DAQ test bench
To be used both for
- Tests @ Lab t.b. before
- Tests @DESY t.b.

Adapted to
- new R.O. electronics
- and to be linked to DAQ of the beam telescopes.

DESY and CU-Prague:
Use of the existing hardware and software developed by DESY for the beam telescopes implementing a very basic trigger logic for connecting the two DAQ systems.



Tests at the Lab Test bench before DESY

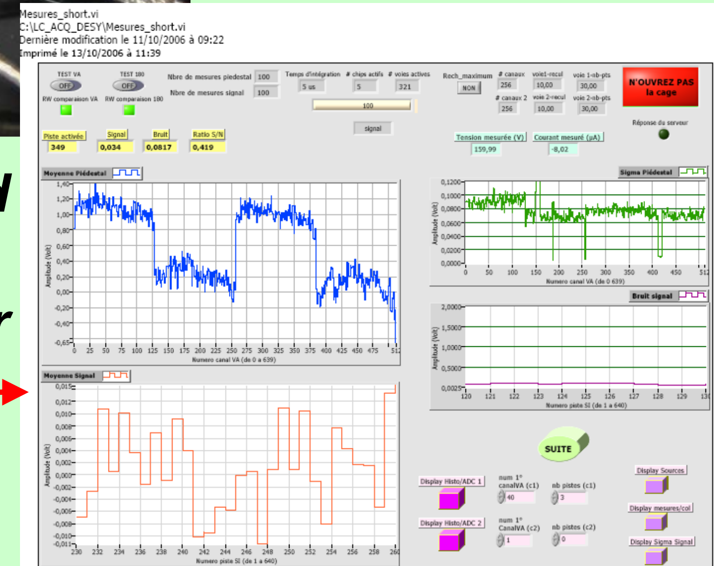
- Complete upgrade of the Paris Lab test bench
- Characterization of the new readout chips (VA1 and 180UMC)
- Characterization of the new Si modules:
  - → 2 x 3CMSmodule
  - → One long strip module
- Test of the functioning of the new DAQ hardware
  - → New command card
  - → New Altera card
  - → Effect of 15 m long cable between Altera & detector R.O.
- Test 2 DAQ's running in parallel (beam telescope and Si detector R.O.)
- Test analysis packages with Lab test bench runs

All these tests were performed at the Paris Lab test bench since end of September till October 20.

Tests were pursued at the Lab test bench after the first round at DESY for further investigations and completion of the measurements.

GLAST module sitting on the Lab test bench

Modules and readout electronics were tested on Lab test bench in Paris, before going to DESY., as for example, the GLAST module or the CMS-4VA1 module



Preparation for the DESY test beam

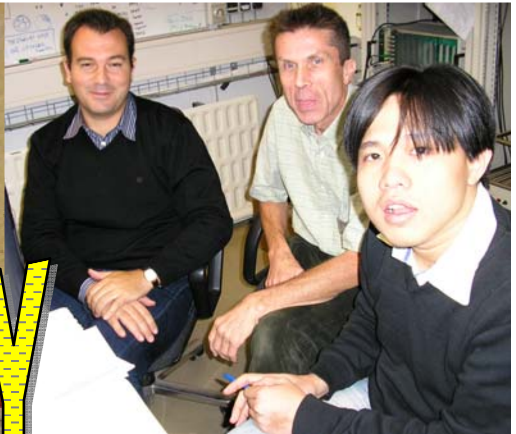
October 23 to Nov 5, 2006

Sharing of tasks

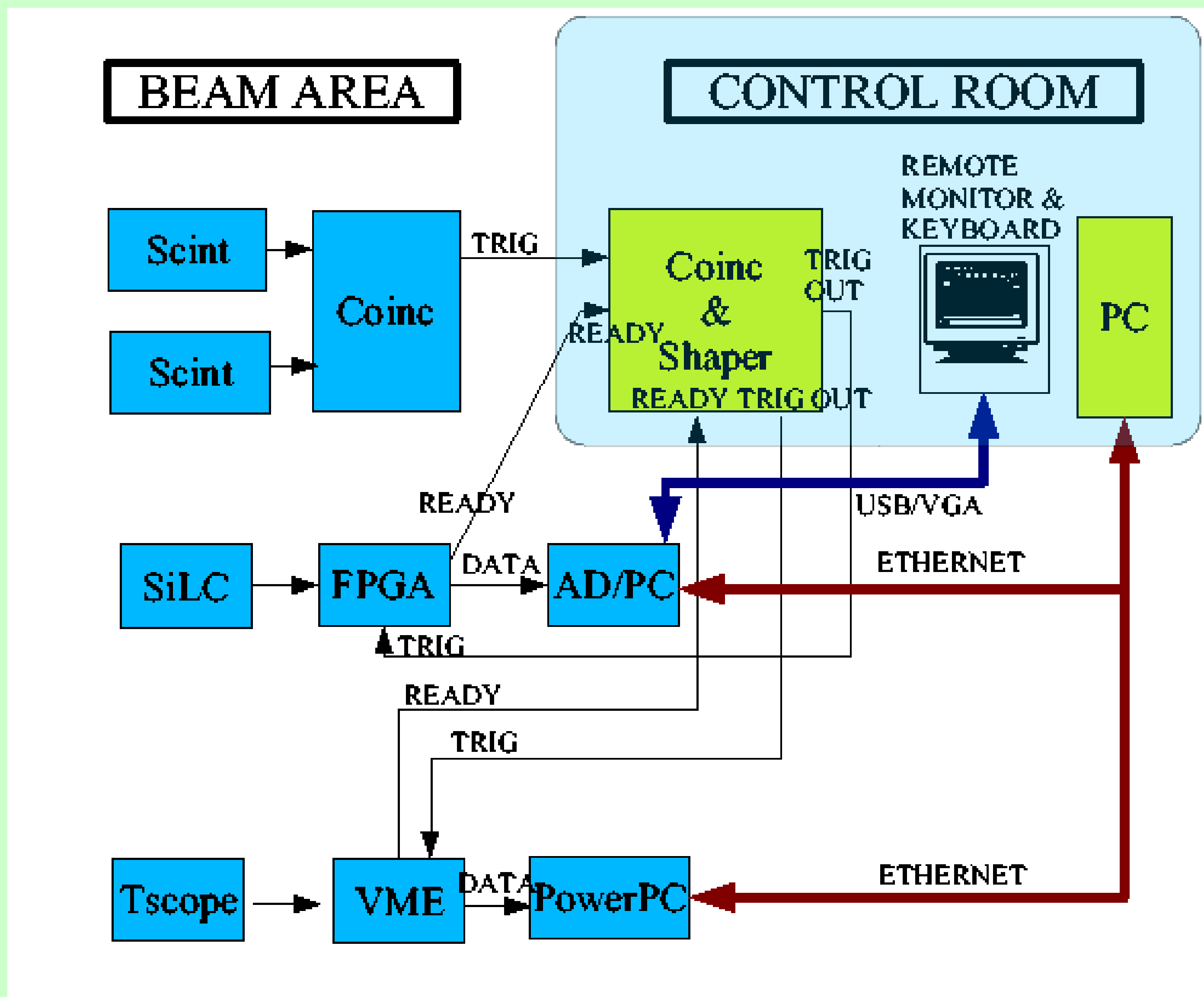
- Construction of the detector prototypes: **CERN, IEKP-Karlsruhe, LPNHE-Paris &** IHEP Vienna, Hamamatsu providing the sensors)
- Mechanics: DESY,LPNHE Paris, **IFIC Valencia**
- FE and readout electronics: **LPNHE-Paris**
- DAQ hardware: **DESY for beam telescopes, LPNHE-Paris for SiLC**
- DAQ software: **DESY, LPNHE-Paris, CU Prague**
- Test in test bench prior to go to test beam: **LPNHE-Paris,** IEKP Karlsruhe, CU Prague,
- Beam Telescopes and Beam infrastructures: DESY, OSU Obninsk, **CU Prague**, **IFCA**.
- Analysis tools: **CU Prague**, OSU Obninsk, LPNHE Paris
- Participation to the run: HIP Helsinki, IEKP Karlsruhe, OSU Obninsk, LPNHE Paris, CU Prague, IFIC Santander and contribution of DESY (beam & telescopes)

October 23 to November 3 2006

SiLC test beam at DESY

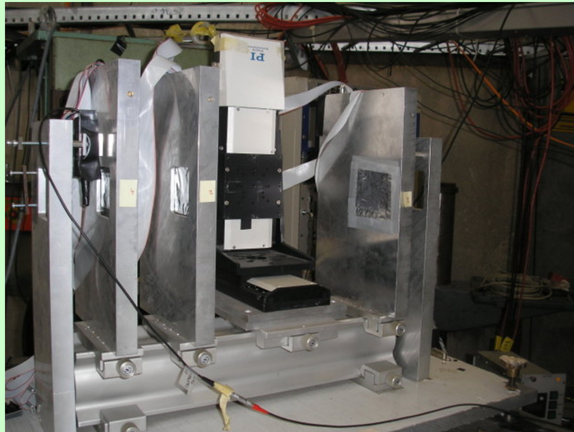


Test beam DAQ system in DESY for SiLC

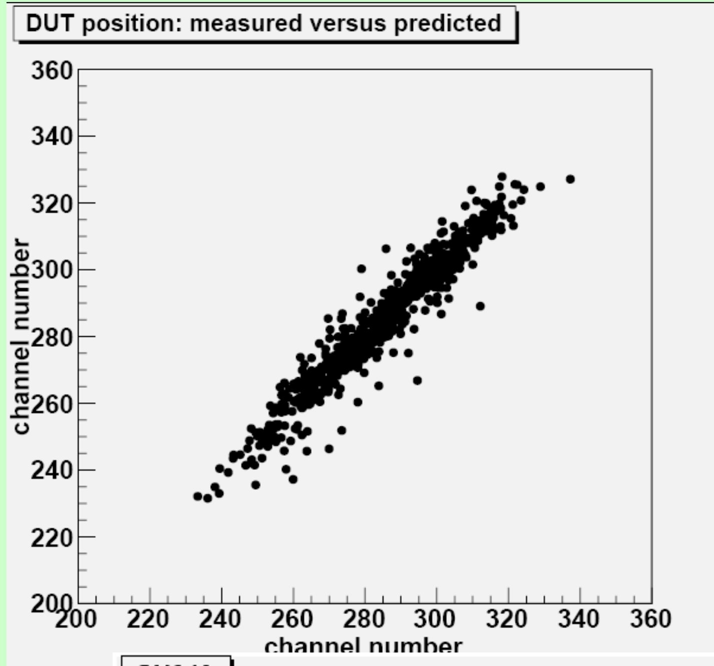


Test set-up 1: Two CMS modules
First one read out by 4VA1
Second one read out by
VA1&180nmUMC

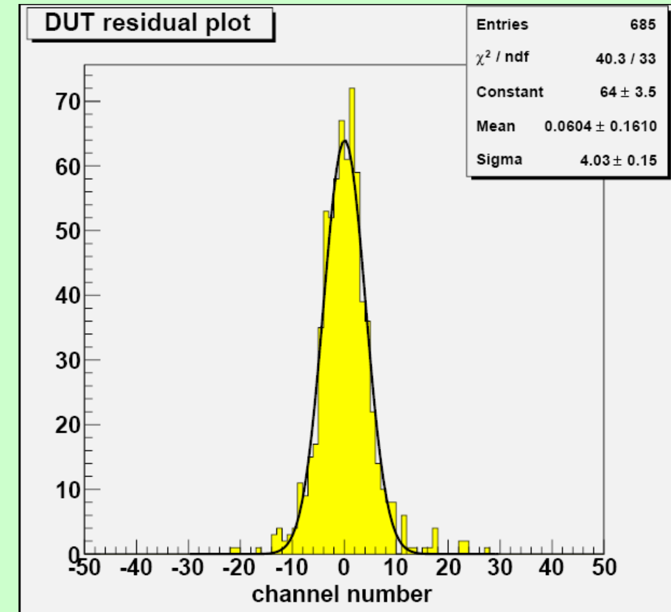
Test set-up 2: one GLAST module
read out by VA1&180nmUMC

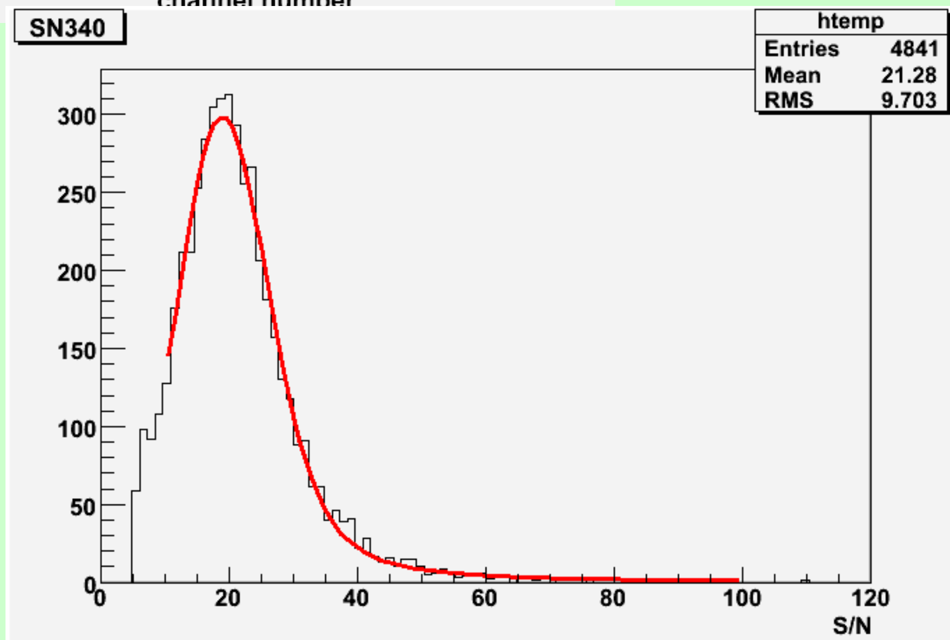


DESY Beam test analysis



Correlation beam telescopes & Silicon detector, based on the CMS-4VA1 module



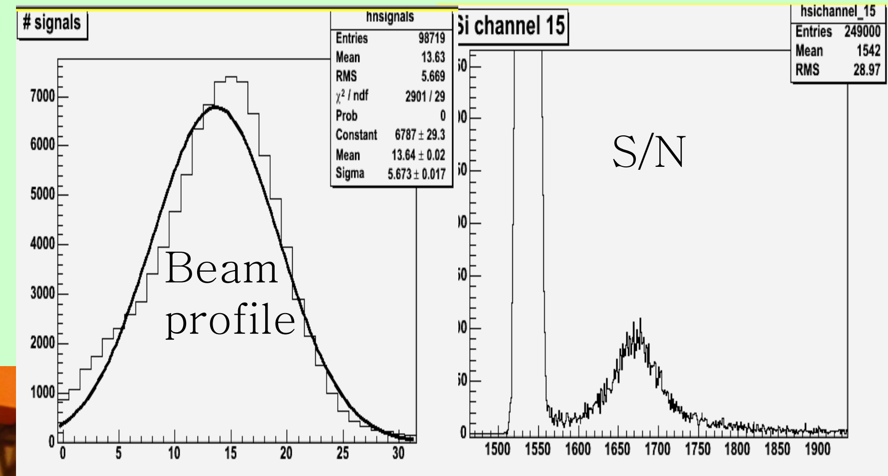


Bias voltage	S/N (MPV)
200	13.62 +/- 0.33
260	15.79 +/- 0.29
299	15.70 +/- 0.25
350	**16.52 +/- 0.73**

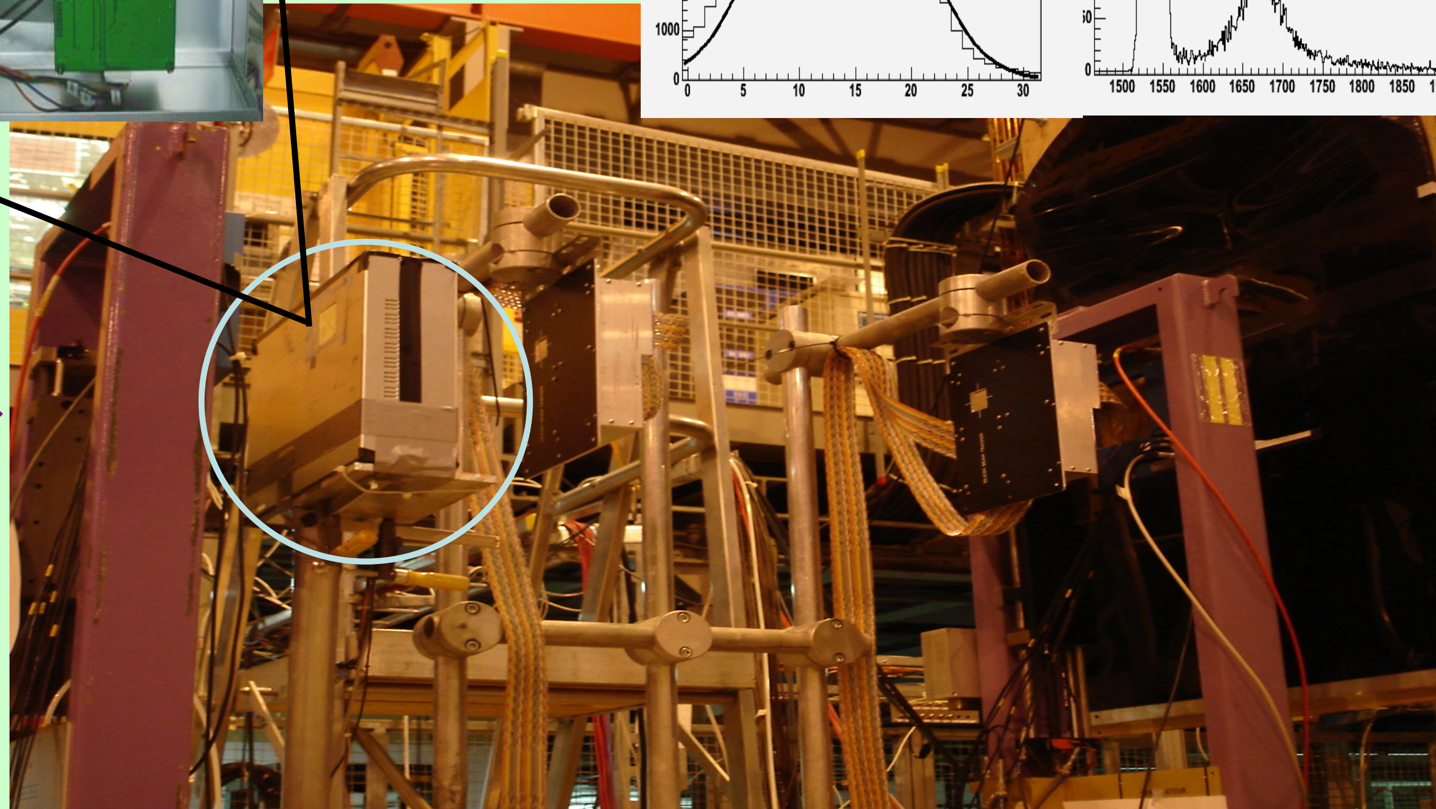
Signal from the CMS-4VA1 module

Beam Test at CERN *(Korean team)*

Test on Single sided 5 " wafer prototype (ETRI)



150 GeV electron beam



2007 Workpackages for SiLC/EUDET

WKP 0: Beam test in DESY (April 2007) with 130nm preprototypes.

WKP 1: Beam tests at CERN (July 2007)= « Rehearsal » for November run:

- 2 modules made of **new** single-sided sensors
  readout: VA1(ref)+ **130nm(preproto)**
- 3D-planar module test

WKP2: Beam test at CERN (Nov. 2007)

- Prototype 60x60cm2, new single-sided sensors, lecture VA1+130nm,
- First test beam of UCSC long ladder + TOT FE readout chip
- Expected to have first alignement systems (Michigan & IFCA)
- Expected to have first cooling system

- *Other SiLC collaborators will join these beam tests and foresee to bring other detector prototypes.*

SCIPP ToT readout: Testbeam Plans (Dreams?) for Late 2007

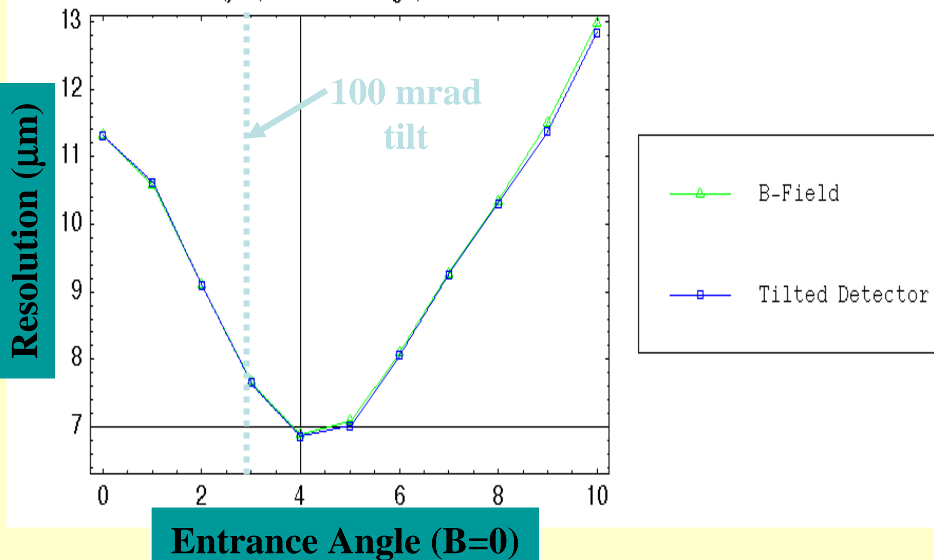
by Bruce Schumm (SCIPP&UCSC)

CDF Layer00 Sensors

Dimensions:	type A : 1.48x7.84 cm^2
	type B : 0.85x7.84 cm^2
Depletion Voltage:	$60\ V < V_{dep} < 100\ V$
Uniformity of V_{dep}:	$< 20\%$
Biasing scheme :	Poly resistors on both sides
Poly resistor values:	$4.5 \pm 0.5\ M\Omega$
passivation :	SiO_2 0.5 μm thick
implant strip width :	8 μm
implant depth :	>1.0 μm
doping of implant:	$> 1 \cdot 10^{14}$ ions/cm^3
width of Al strips :	7-8 μm
thickness of Al strips:	>1 μm
resistivity of Al strips:	$< 20\ \Omega \cdot cm$

2-3 μsec shaping time plus ~10 daisy-chained sensors ➔ stringent requirement on **leakage current**, **bias resistance**

Single CDF L00 sensor may be satisfactory, but "long" ladder may be single sensor plus equivalent capacitive load.



SCIPP simulation for ToT readout of long ladder:

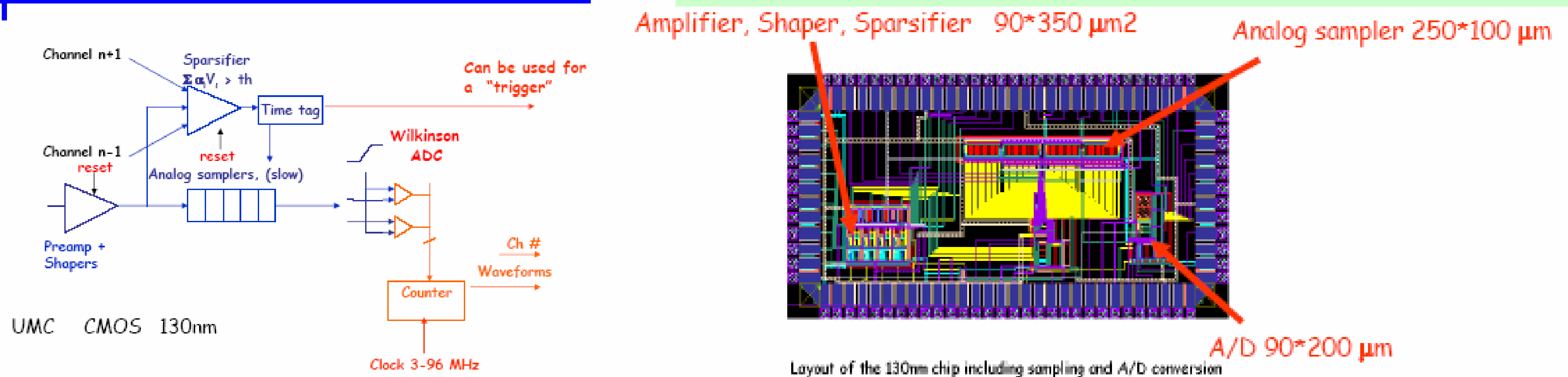
Expect 7 μm resolution, but with strong dependence on entrance angle (efficiency also).

Want to explore this in testbeam run.

Implementing new 130 nm chip: SiTR-130_1

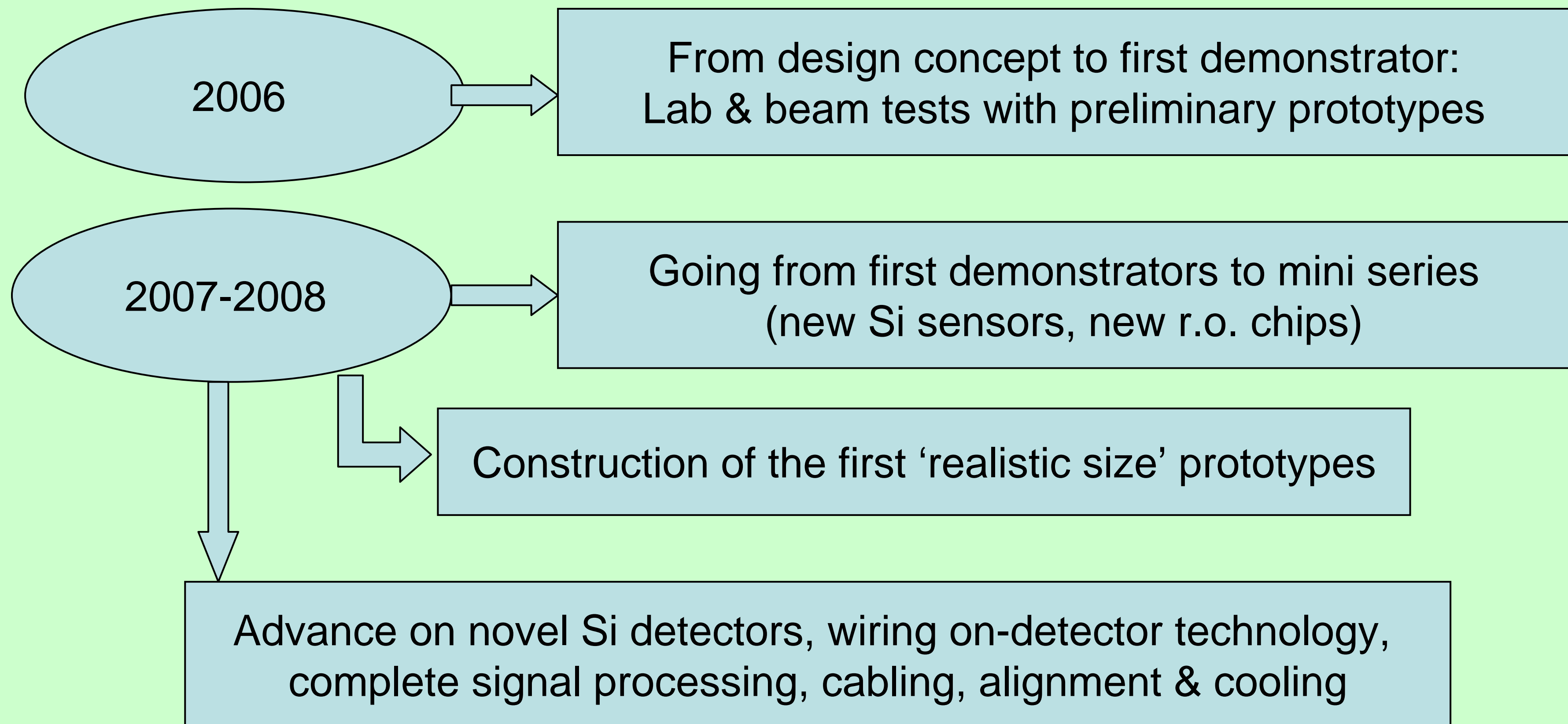
Implies lot of work: quite challenging!

- Testing the full functionality: analogue component, pipeline, digitization included in this chip



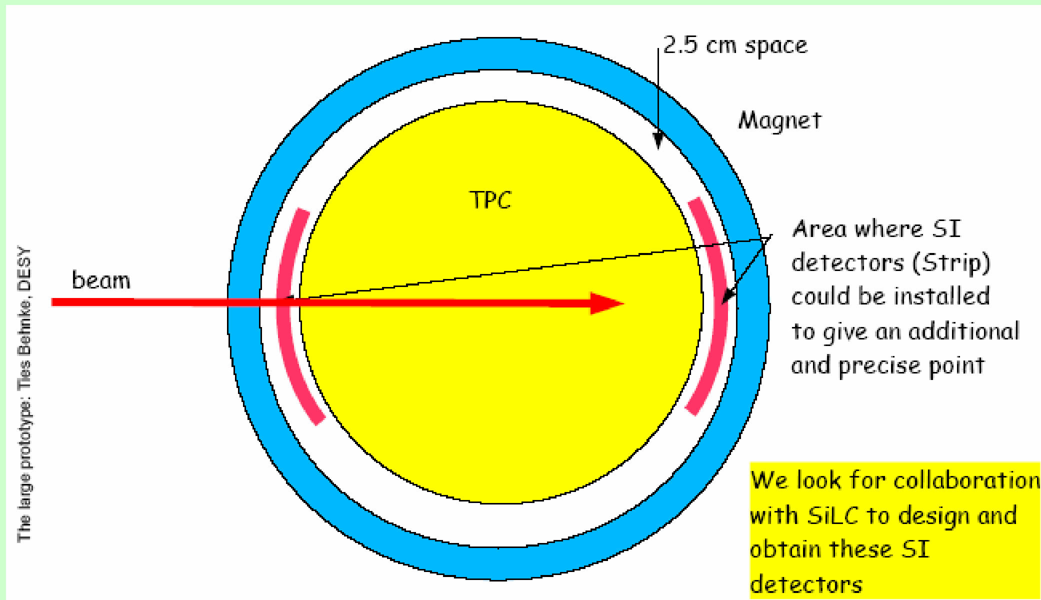
- **Rebuild a DAQ** hardware and software for this new processing of the detector information.
- Test it on the Lab test bench before going to test beam

Transitions of phase:



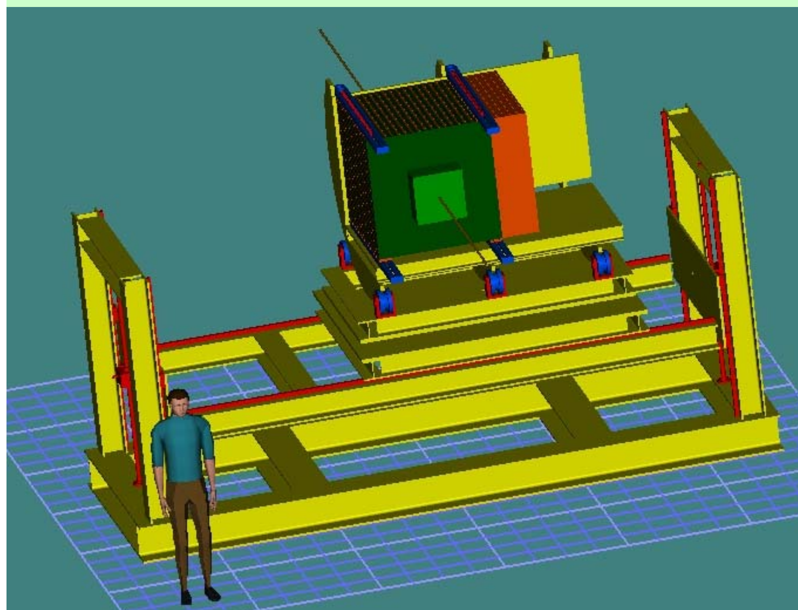
In 2006, the first SiLC test beam has triggered the unification of the European collaborative efforts.
The 2007 SiLC beam tests will include the contributions of Asia and US

2008 & beyond: combined test beams

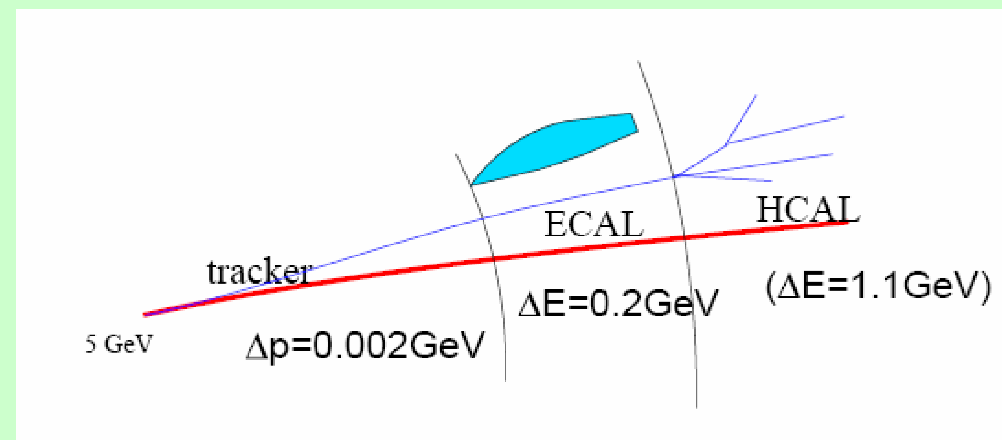


Testbeam with TPC Field Cage & strip layer surrounding it: SET(LDC)

Test beam with pixel detectors: tests on internal tracking region & Vertex + Silicon tracker



Testbeam with Si-W calorimeter & few Silicon strip layers in front: experience particle flow



Concluding REMARKS

- SiLC has made impressive advances especially this last year and half, on all R&D fronts.
- The new R&D era that SiLC has started this last year is demanding another scale of means in terms of money and people.
- SiLC is attracting more and more institutions but most importantly more FTE that are collaborating to the work
- What is clearly needed is the support from all our funding agencies and thus a strong support of this panel will be essential

We are very much indebted to the valuable contributions of all our collaborators; a special thanks to:

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