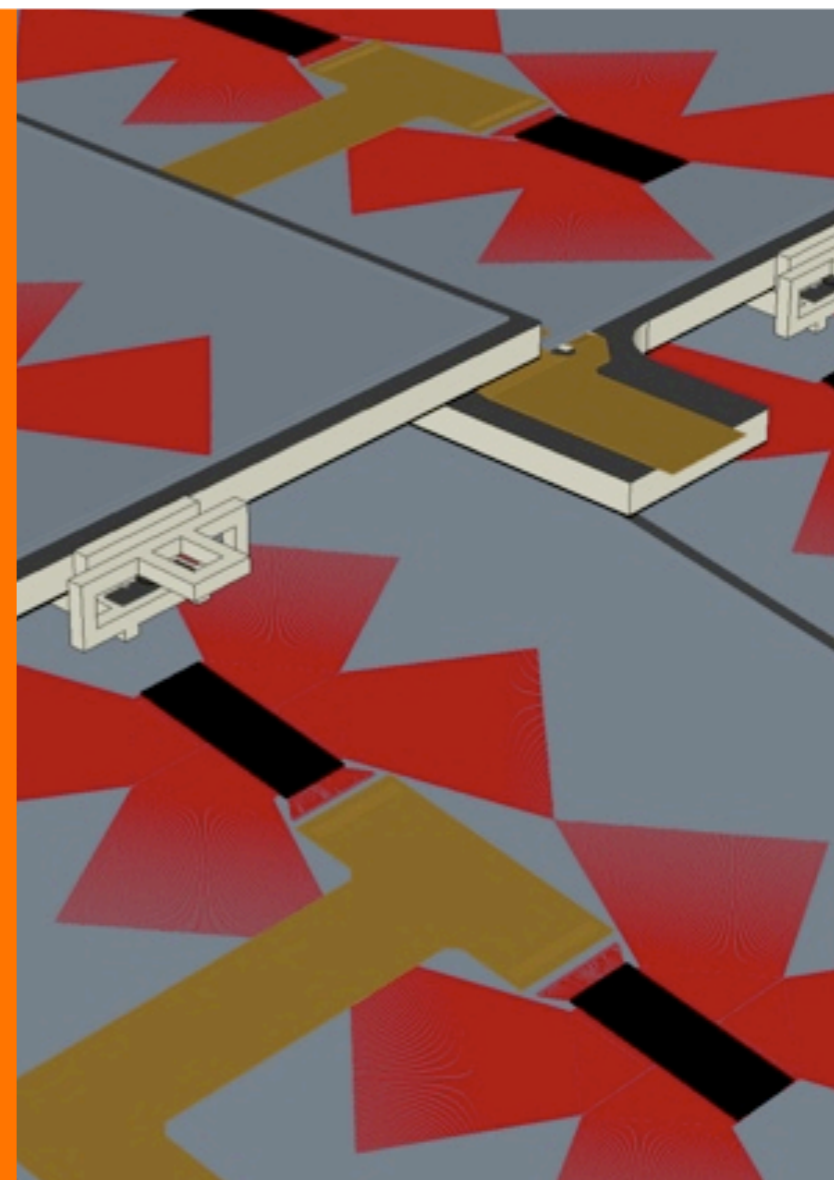


The SiD Tracker Module: R&D Status and Plans



Tim Nelson



SiD



SLAC

ILC Tracking R&D Review

BILCW07 - Beijing - February 6, 2007



The Silicon Dilemma

Asymptotic P_T resolution of silicon tracking is unmatched.

However, silicon places two critical requirements in opposition:

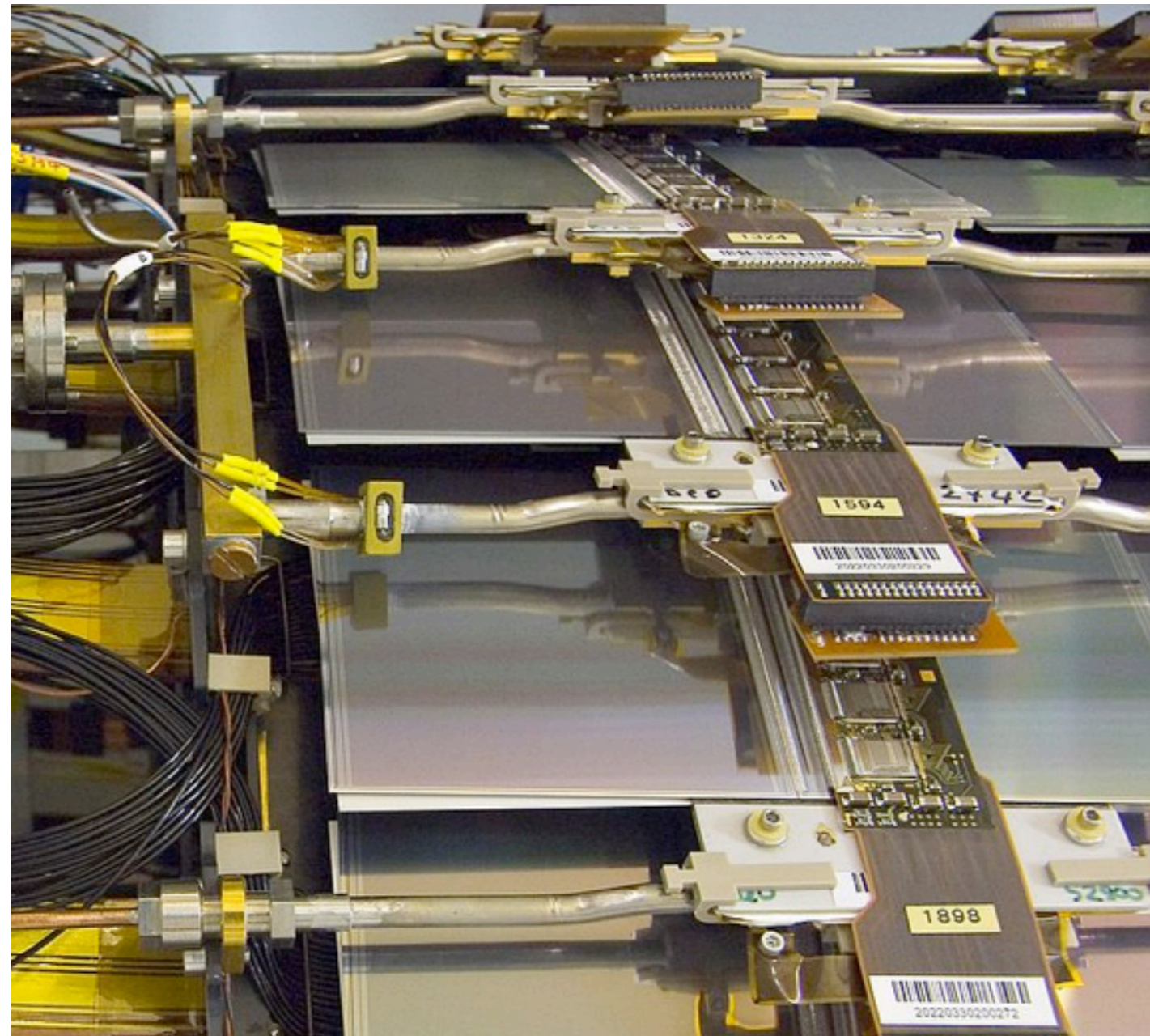
- ✦ minimal material in tracking volume
- ✦ tracking throughout a large volume

Low-mass silicon detectors have been small, because they are...

- ✦ able to implement expensive and labor-intensive designs on a small scale
- ✦ able to keep readout and cooling material outside of limited tracking volume

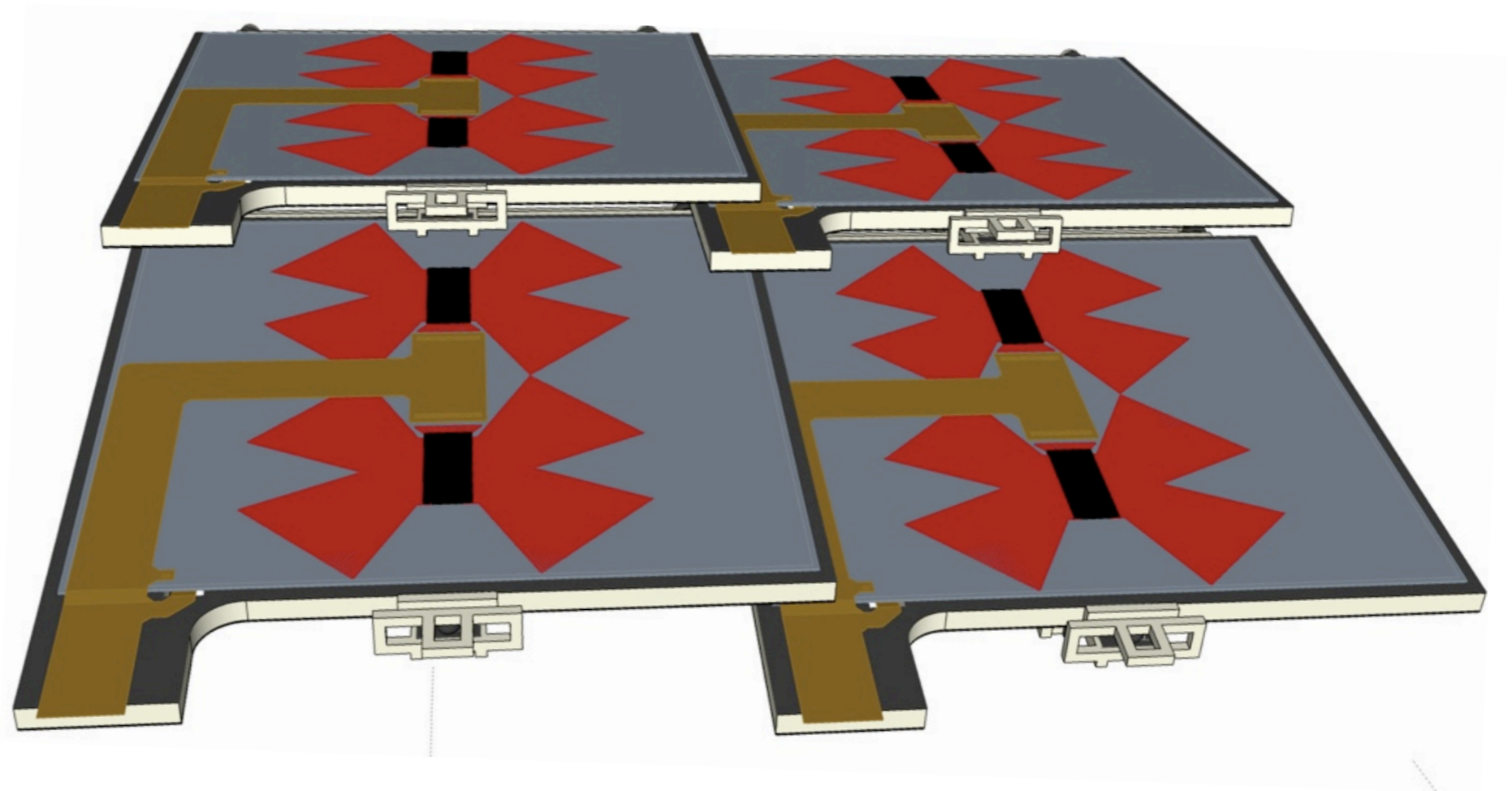
Module Essentials

- Sensor
- Readout Chip
- Hybrid
- Cable
- Support
- Cooling



Module Essentials Redefined

- ⬢ Sensor
- ⬢ Readout Chip
- ⬢ Hybrid
- ⬢ Cable
- ⬢ Support
- ⬢ Cooling



SiD Material Budget

SiD Tracker Material
V0.23

Tim Nelson

January 14, 2007

$$\frac{\delta p_t}{p_t^2} = a \oplus \frac{b}{p_t \sin\theta}$$

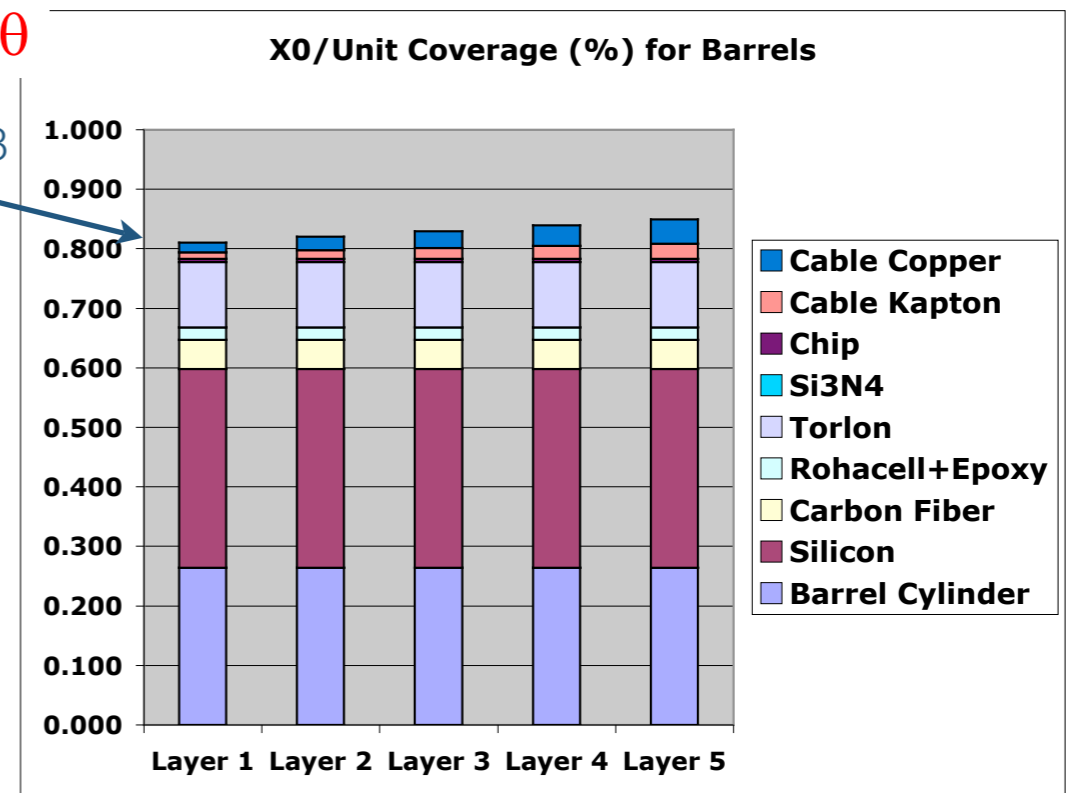
$$b = 1.4 \times 10^{-3}$$

1 Introduction

This document describes the current understanding of material necessary for an ILC tracking detector based on the SiD detector concept and utilizing short silicon readout modules. While no description of detector material is ever complete or perfectly precise, a reasonable model of this material is necessary to estimate multiple scattering and secondaries that impact the physics mission of the tracker. The detector components will be described briefly, accompanied by an accounting of the material these they represent.

2 Description of Components

The detector itself is divided into two segments, barrel and endcap. In addition, there are various components necessary for mechanical support, power supply and electronic readout. These three



Assumes solid barrel cylinders

Mass penalty for having a large number of readout channels drastically reduced.



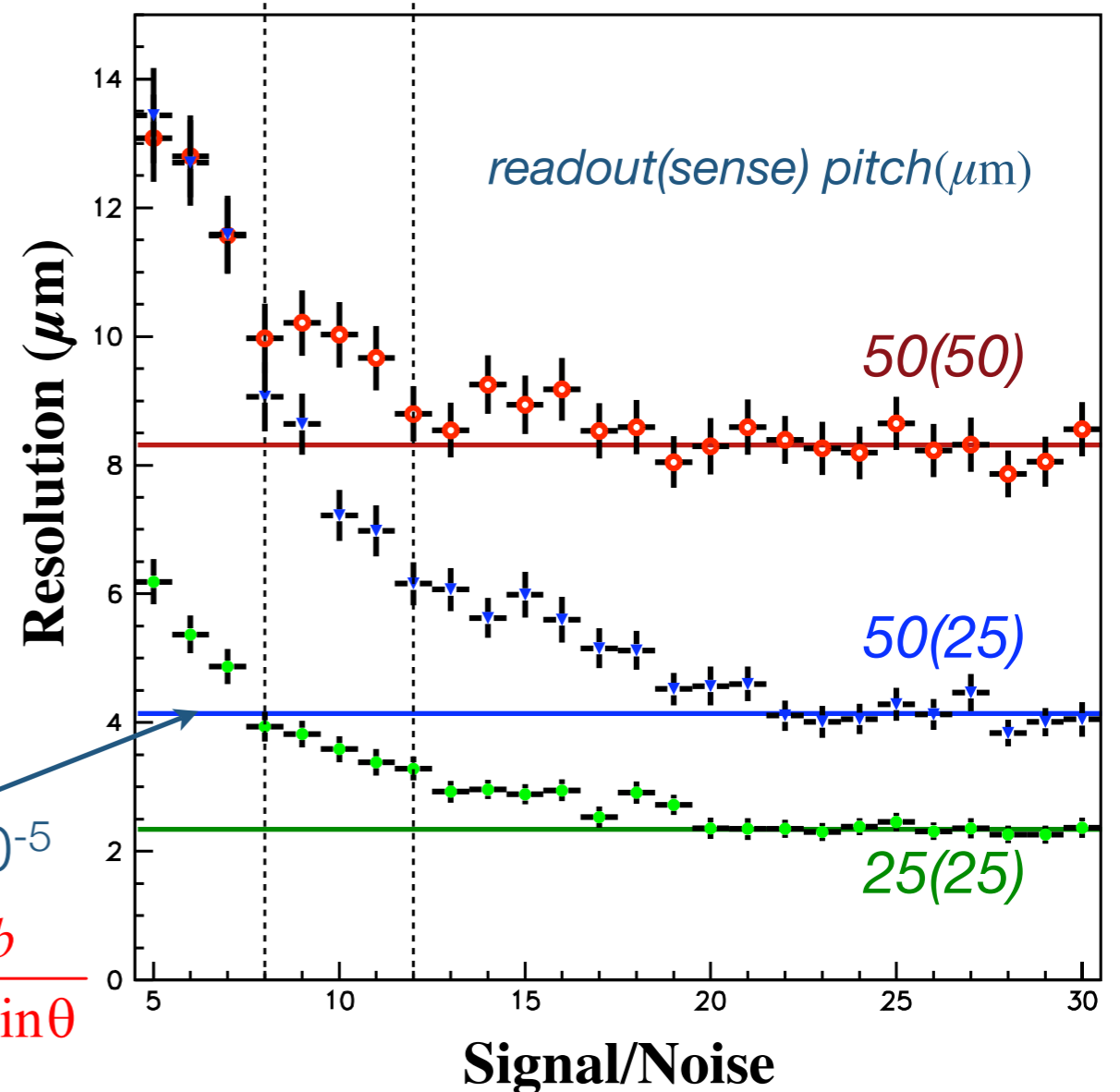
Optimization

Finer readout granularity:

- ⬢ shorter strips
 - ⬢ reduces background occupancy
 - ⬢ improves pattern recognition
 - ⬢ increases S/N → improves resolution
- ⬢ finer pitch
 - ⬢ improves resolution

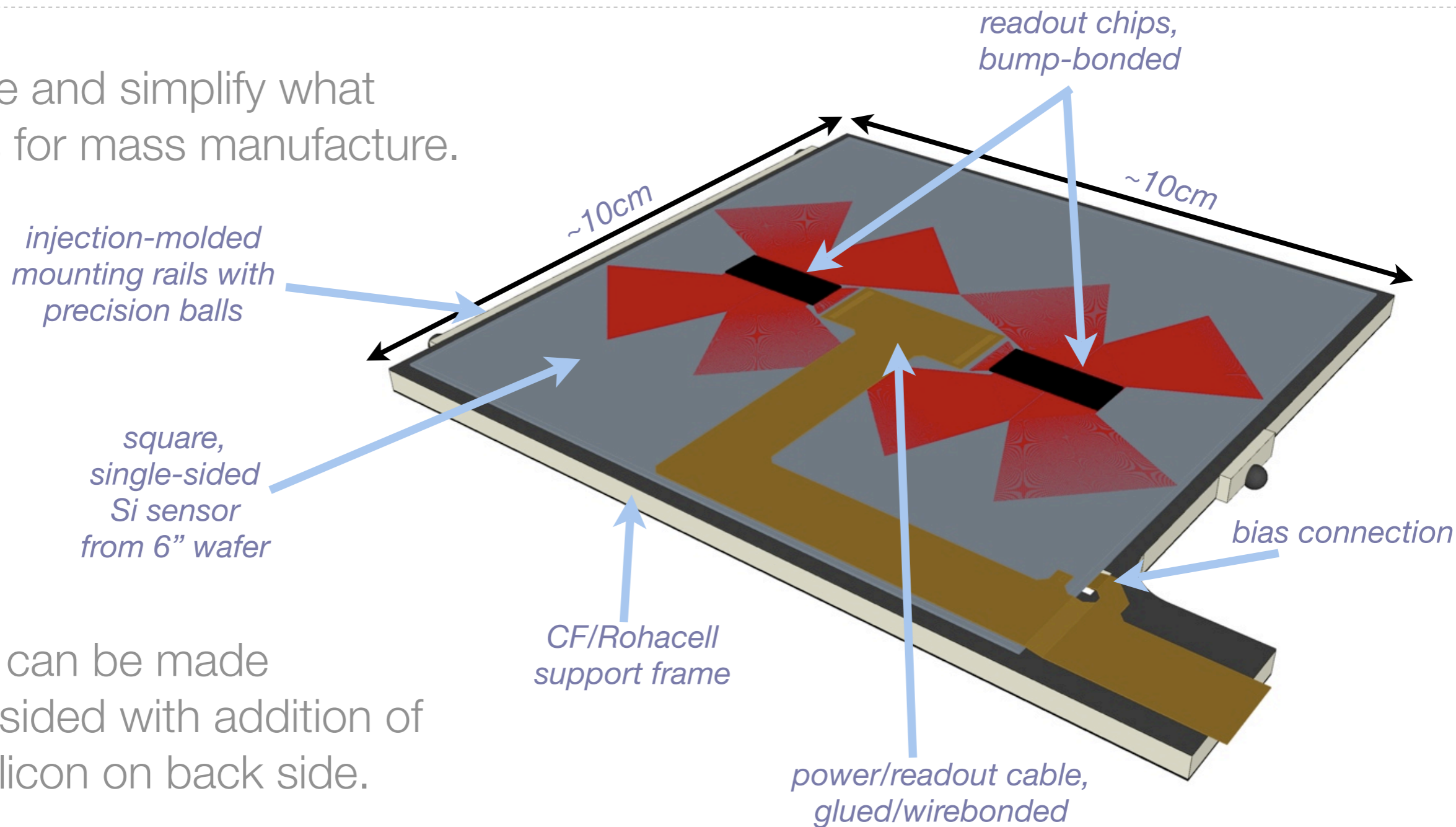
$$a = 1.1 \times 10^{-5}$$

$$\frac{\delta p_t}{p_t^2} = a \oplus \frac{b}{p_t \sin \theta}$$



Barrel Module (Baseline)

Minimize and simplify what remains for mass manufacture.



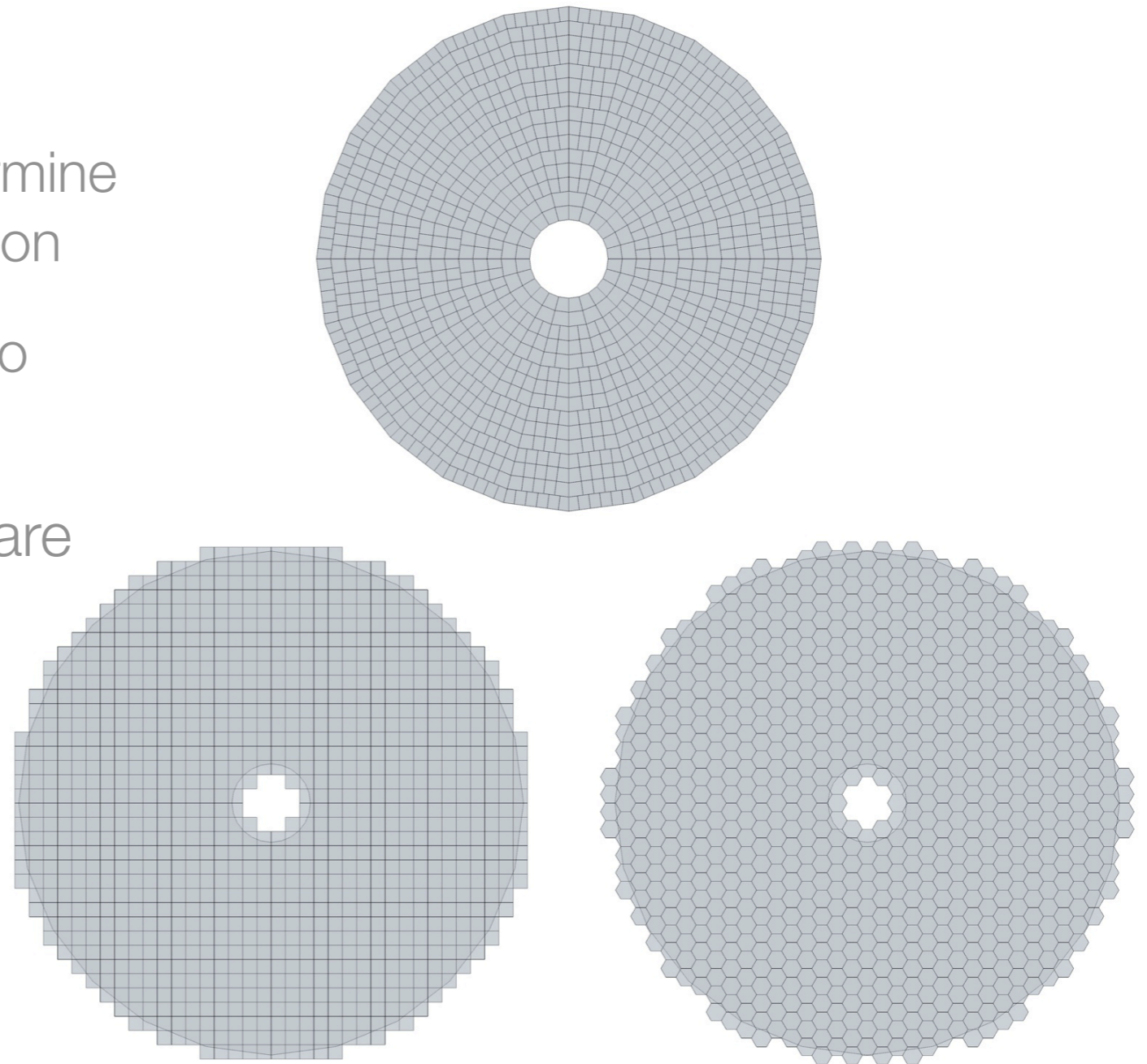
Module can be made double-sided with addition of same silicon on back side.



Disk Module

- ⦿ Forward layout still in question:
 - ⦿ Simulation effort required to determine most advantageous strip orientation
 - ⦿ Module concept flexible enough to accommodate all eventualities

- ⦿ Issues demanding full prototypes are independent of module shape
 - ⦿ RF pickup from novel readout
 - ⦿ industrial manufacture of support



Plan prototypes of both barrel and disk modules: two generations each

Module R&D

Components

Readout Chip - SLAC, UCSC, Brown U.

Sensor - SLAC, FNAL, Purdue, UNM, U. Tokyo

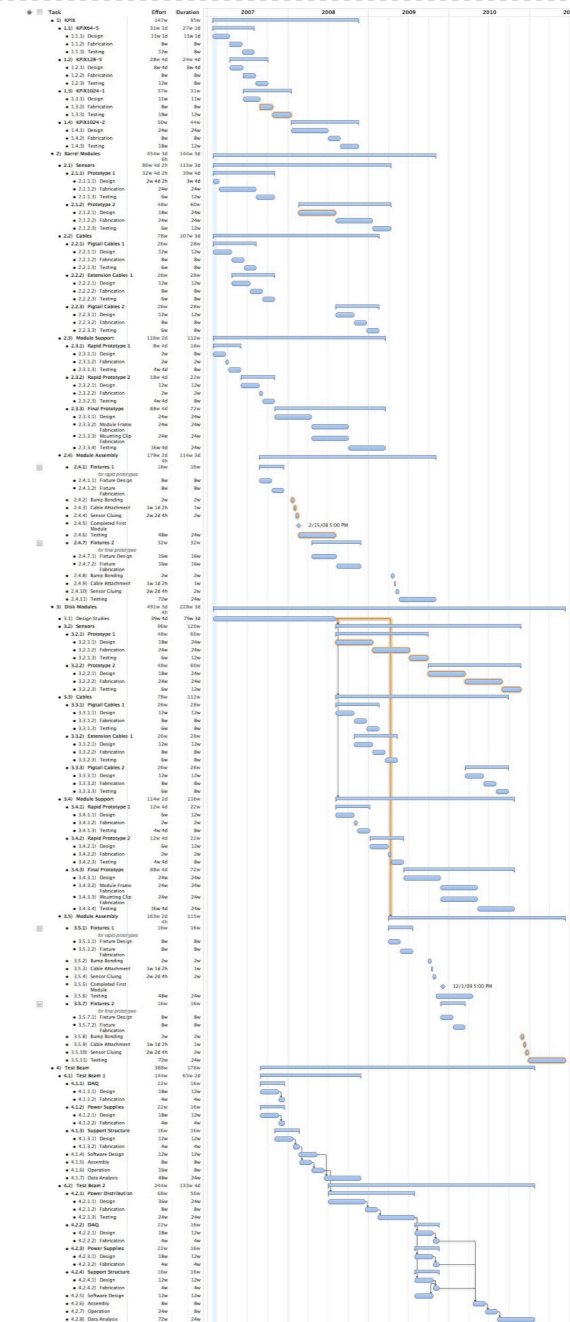
Cables - UNM, SLAC

Support & Mounting - SLAC, FNAL

Assembly - SLAC, UC Davis, FNAL

Power & DAQ - SLAC

Testing - SLAC, FNAL, UNM, Purdue



Silicon Readout at the ILC



power pulsing

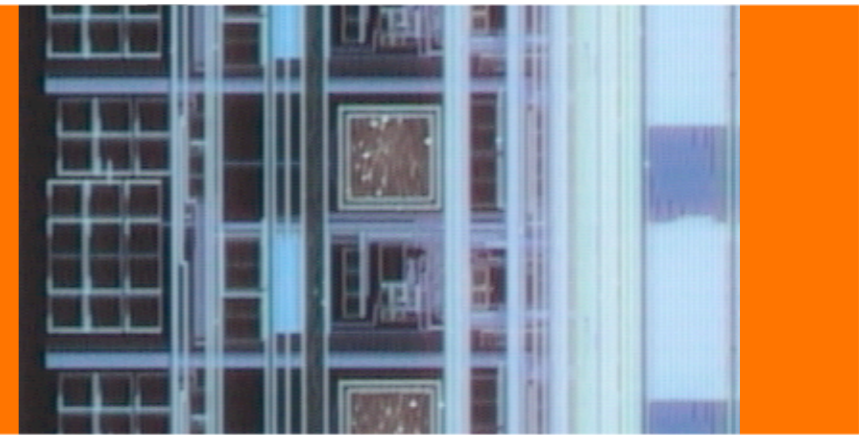
- ☀ starve front end for current between trains
- ☀ eliminates need for direct cooling

buffered readout

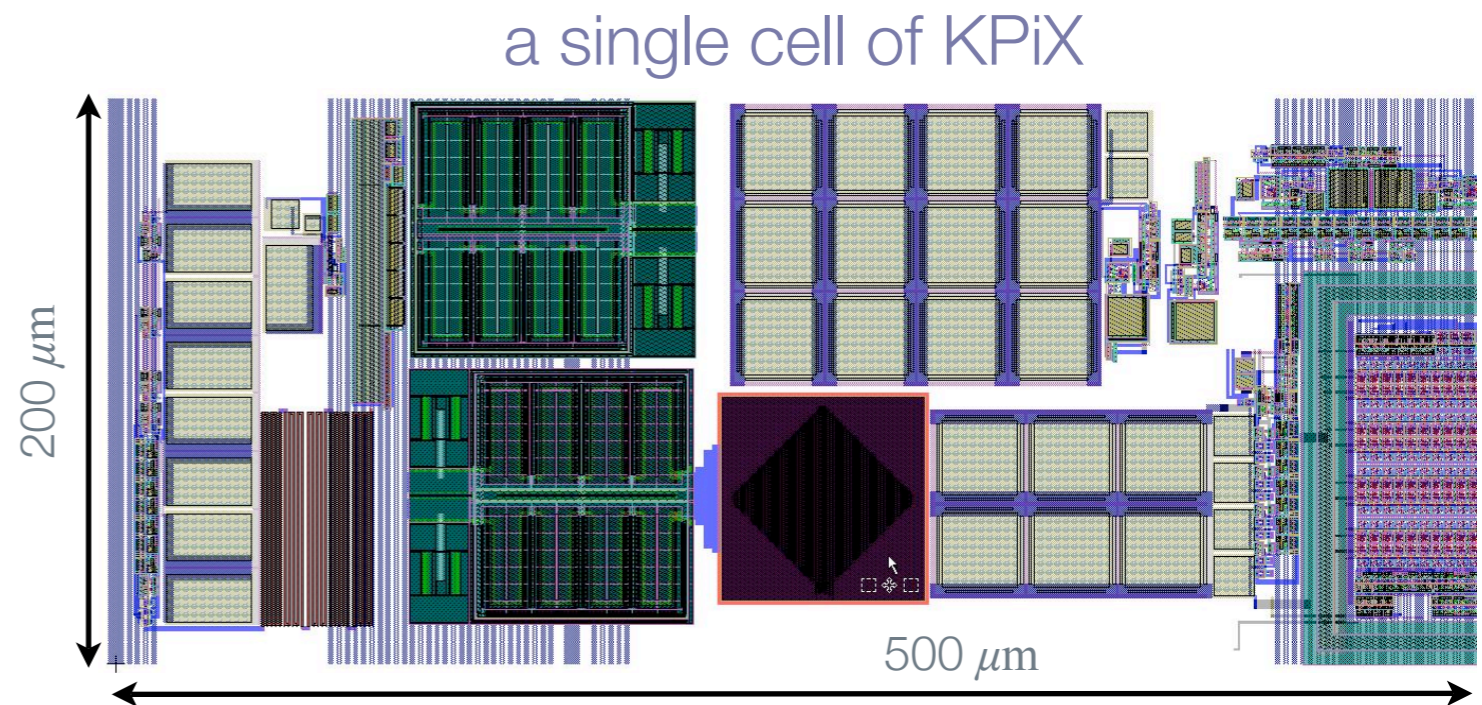
- ☀ store signals in analog buffers for digitization between trains
- ☀ quiet operation during acquisition allows mounting directly to sensor

Elimination of hybrid and direct cooling reduces mass and simplifies assembly

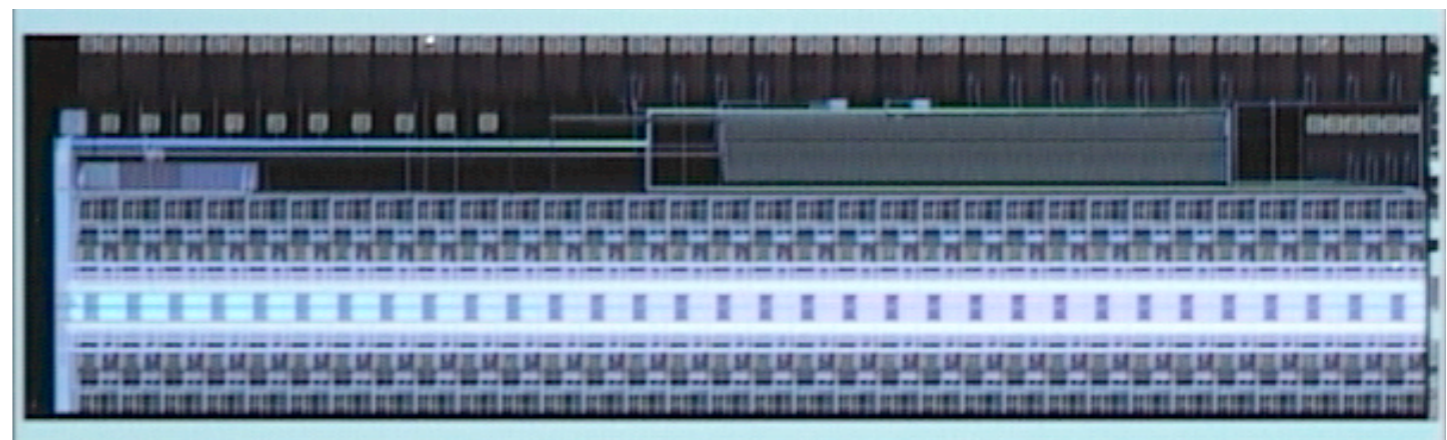
KPiX (Baseline)



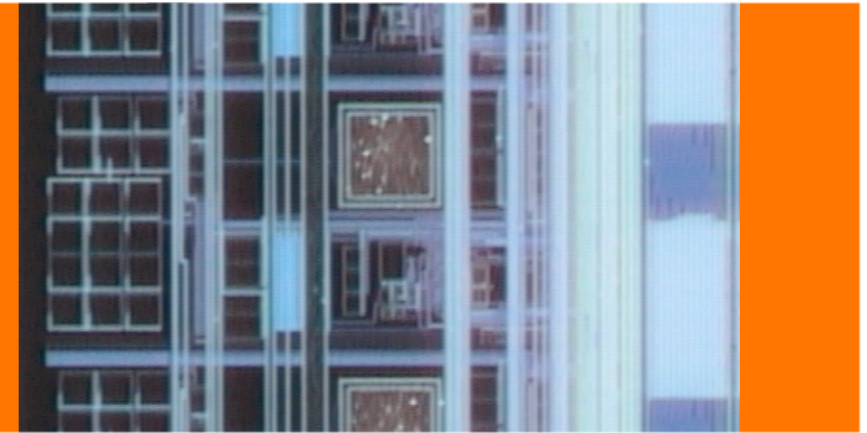
- Development at SLAC began for Si-W ECal
- 0.25 μm TSMC
- 1024 channels
- power-pulsed: $P_{avg} = 20 \text{ mW}$
- 4 time-stamped analog buffers
- designed for bump-bonding
- nearest-neighbor logic added for use in tracker



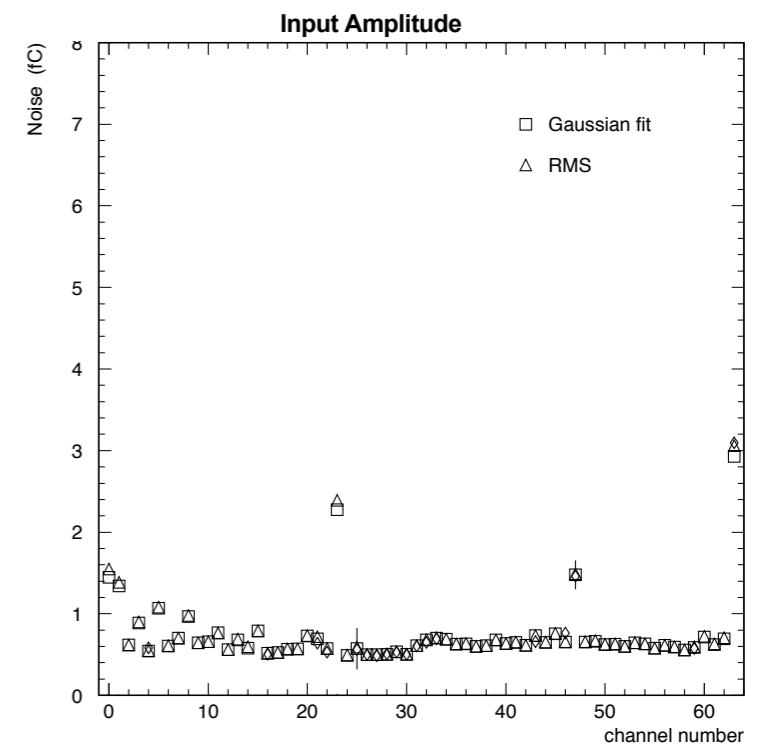
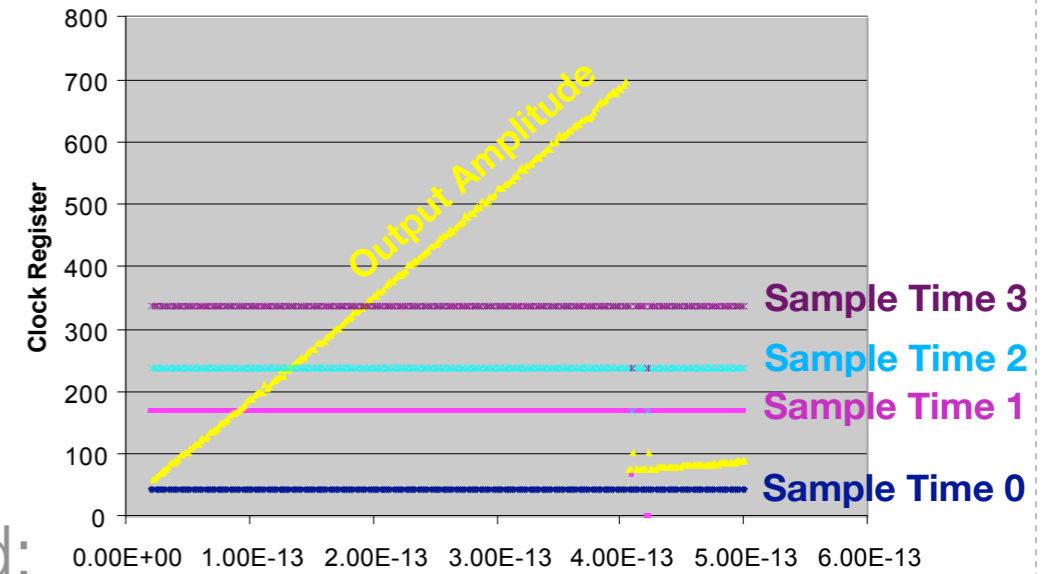
KPiX64



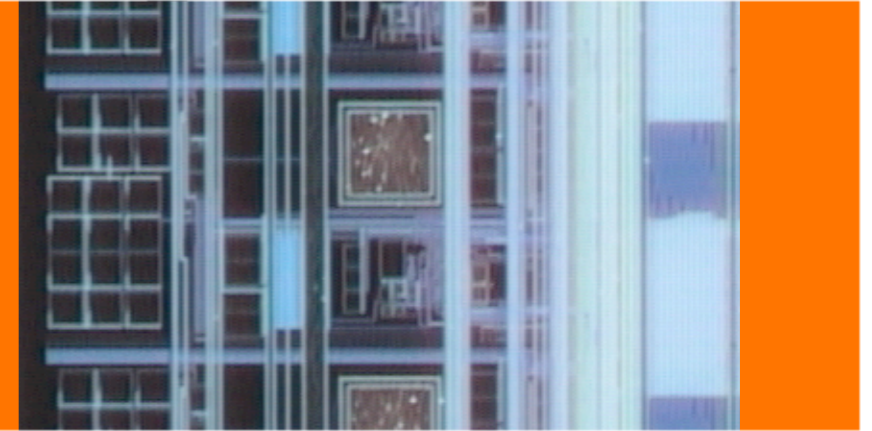
KPiX - Status



- 🍷 64-channel prototypes: now testing KPiX64-4
- 🍷 Time-stamping and linear response verified
- 🍷 Operational quirks largely resolved
- 🍷 Channel-to-channel gain variations understood: solution not yet agreed upon
- 🍷 First noise measurement: $ENC=1000+30^{\circ}C$
 - 🍷 expected is $200+25^{\circ}C$
 - 🍷 suspect issues with test setup
 - 🍷 getting serious about noise: new test board



KPiX - Plans

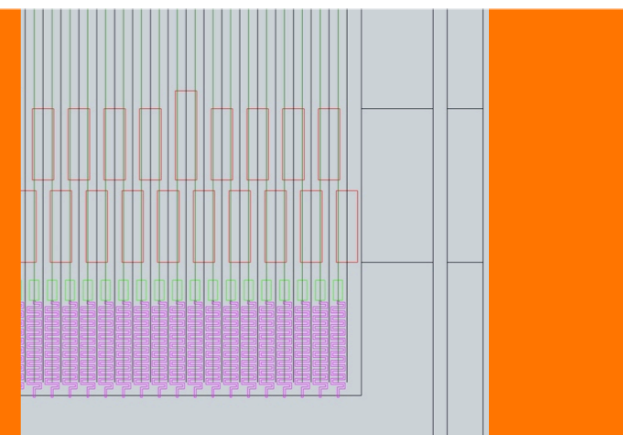


Tied to MOSIS schedule:

- 🔸 one more *KPiX64* with remedy to gain variations
- 🔸 one *KPiX128* to test for issues scaling with chip size
- 🔸 *KPiX1024-1* delivered Q4 2007 followed by exhaustive testing, assembly and operation of first module prototypes (including test beam operation)
- 🔸 anticipate a second *KPiX1024* in late 2008

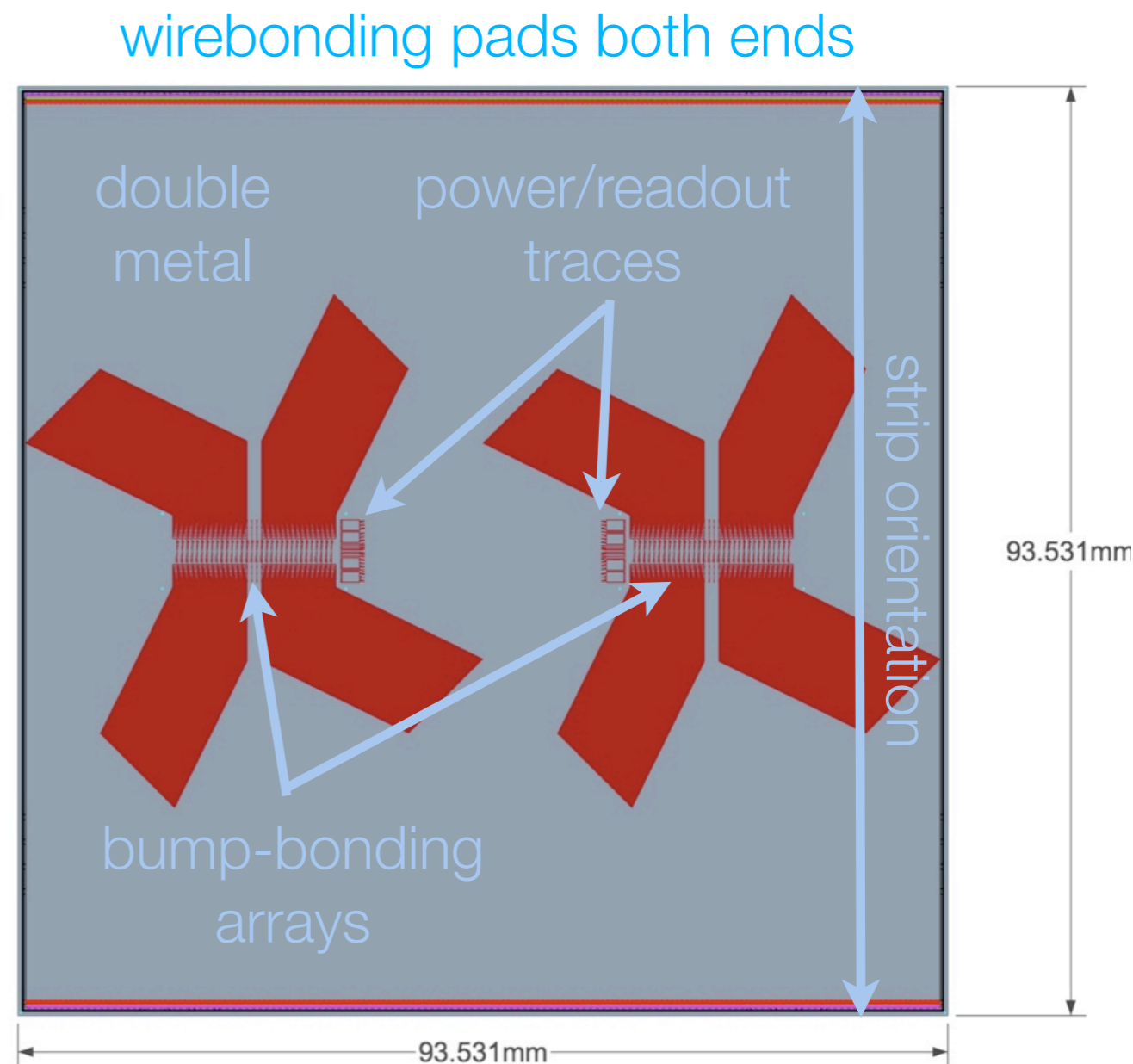
50-50 joint effort with ECal group

Silicon Sensors (Baseline)

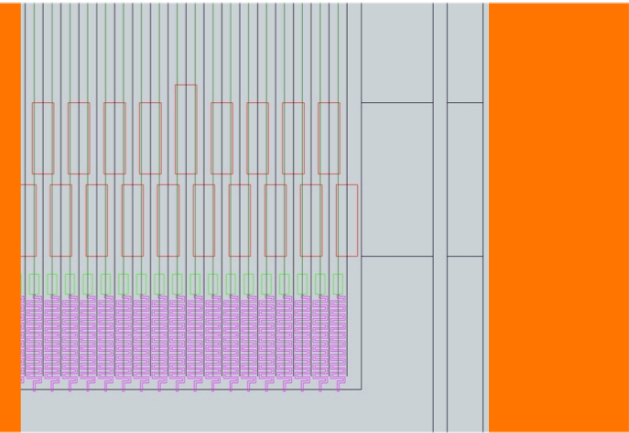


- 🔸 300 μm , single-sided p+/n silicon
- 🔸 AC-coupled, poly-biased
- 🔸 50(25) μm readout(sense) pitch

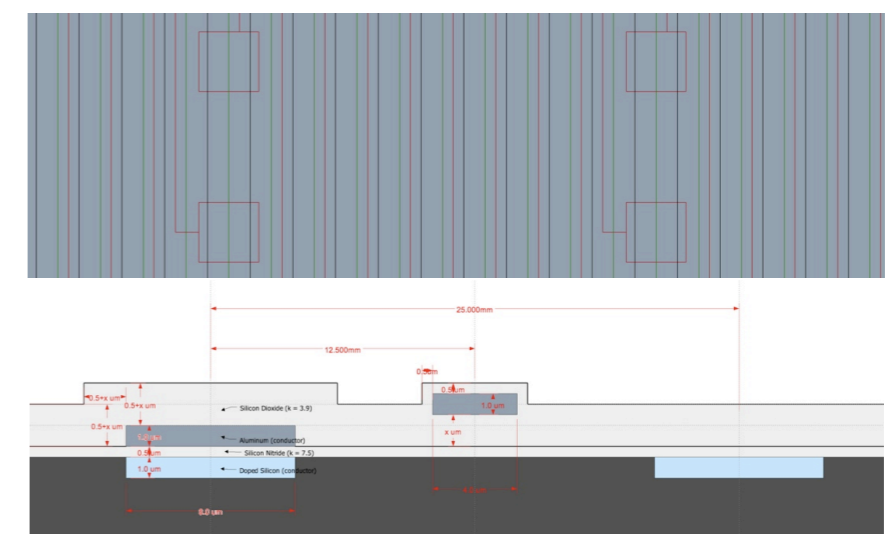
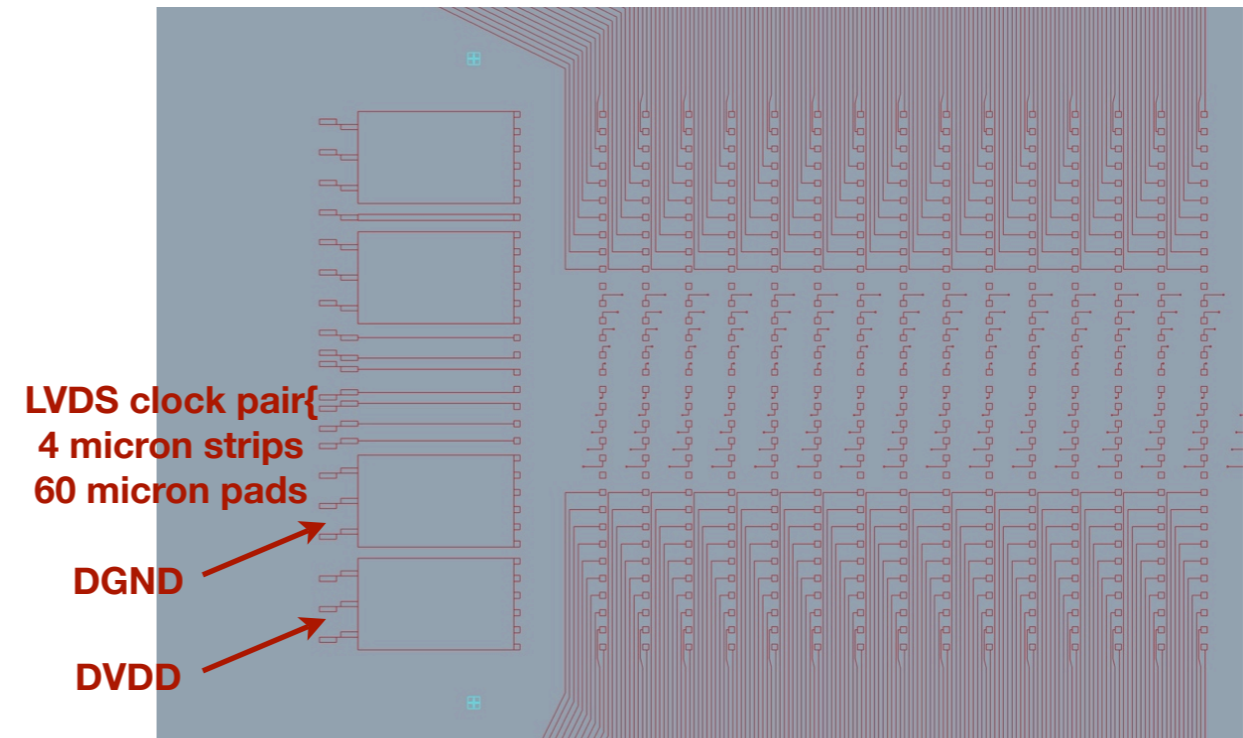
Parameter	Specification
Wafer size	6-inch
Active area	92.031 mm X 92.031 mm
Number of readout (sense) strips	1840 (3679)
Depletion voltage	<100V
Junction breakdown	>200V
Leakage current	< 4 μA at 150V
Strip width	7-8 μm
Coupling capacitance	>10pF/cm
Interstrip capacitance	<1.2pF/cm
Polysilicon bias resistor value	20 \pm 2 M Ω
Not working strips	<20



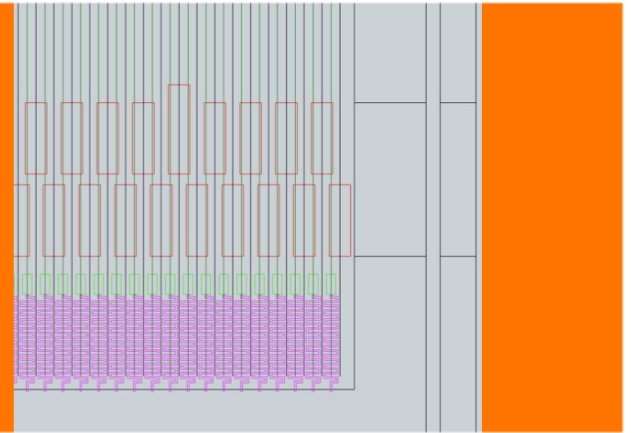
Silicon Sensors - Status



- ⦿ Prototype design and specs developed by SLAC and FNAL
- ⦿ Review with external panel held last November
 - ⦿ refinement of specification
 - ⦿ ANSYS capacitance modeling
 - ⦿ optimization of clock traces/pads: ~3500e⁻ pedestal shift worst-case
 - ⦿ simulation of power/ground traces: similar in magnitude to clock effects



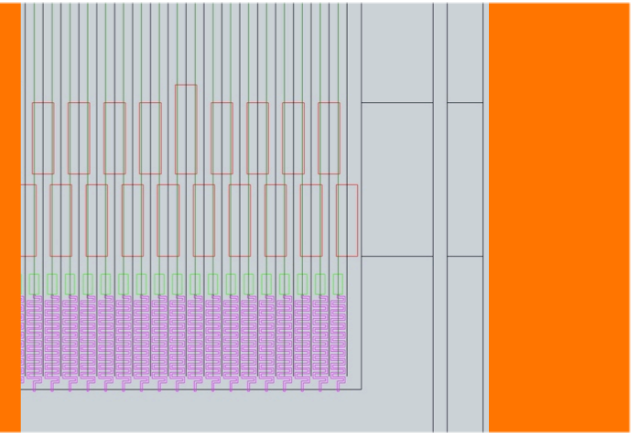
Silicon Sensors - Plans



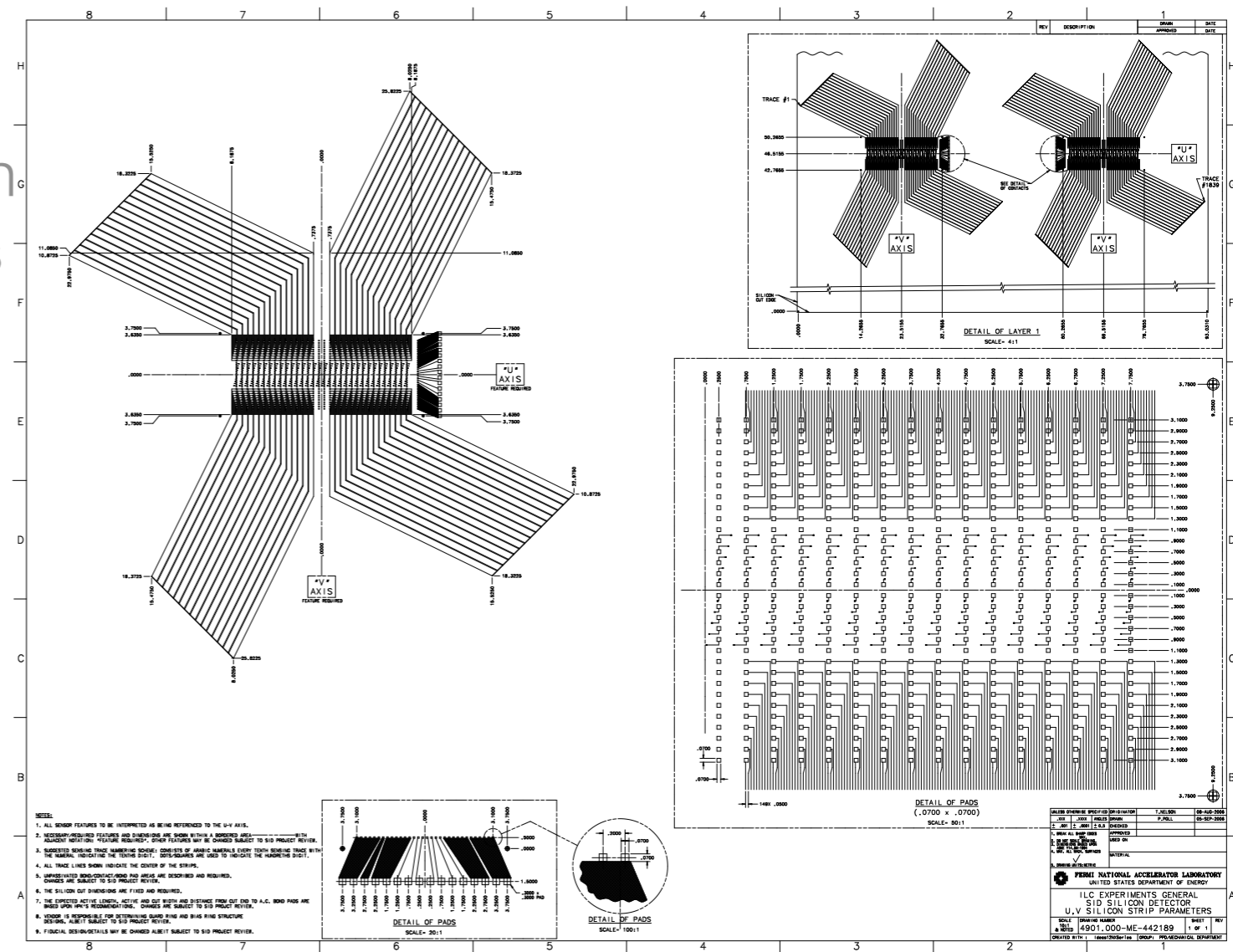
- ❏ Submission for first barrel prototype to HPK ~March 1
- ❏ UNM preparing to lead full testing and QA program on sensors
 - ❏ Establish that delivered prototypes could be put into production
 - ❏ Verify capacitance calculations
 - ❏ test coupling of clock pads/lines and power traces to underlying readout strips
- ❏ Testing with readout chips
 - ❏ *KPiX1024* at SLAC, UNM, FNAL, Purdue
 - ❏ Test short strips with LSTFE at UCSC
 - ❏ Benchmark alongside thin silicon with SVX4 at Purdue



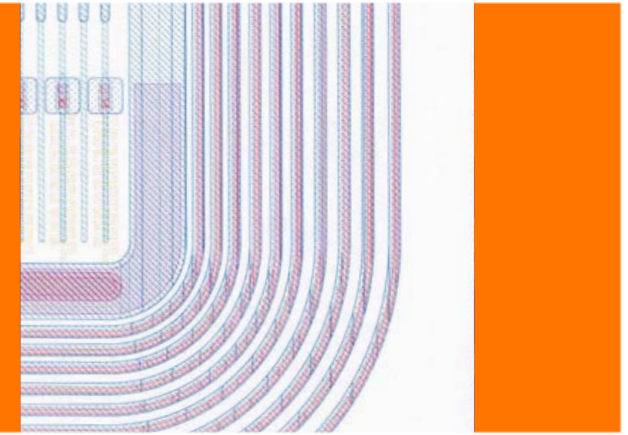
Silicon Sensors - Plans



- Plan two sensor prototypes each for both barrel and disk modules
- Second disk prototype may be unnecessary during R&D phase, depends upon...
 - success of barrel modules
 - configuration of forward disks



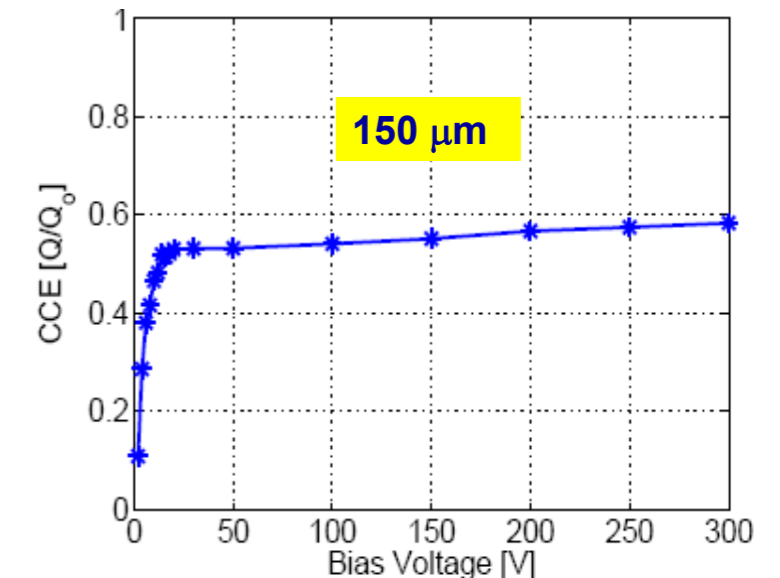
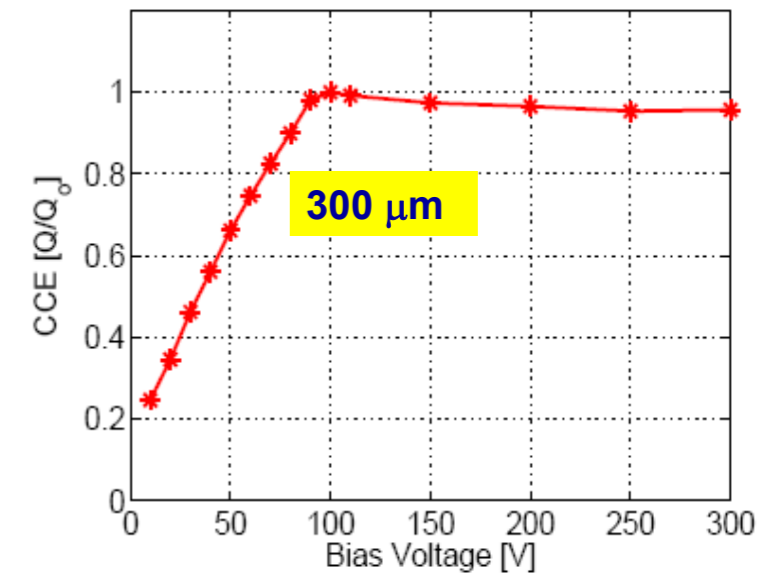
Thinned Sensors



Prototyping sensors on thinned silicon at Purdue

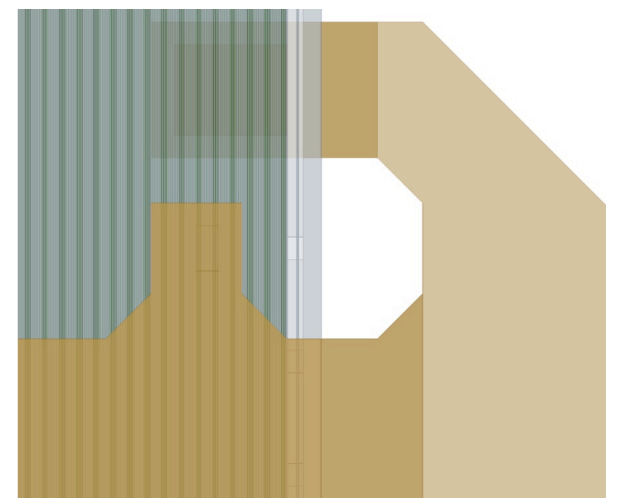
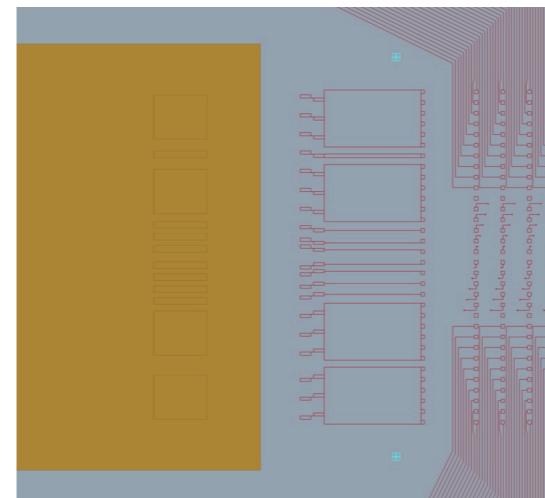
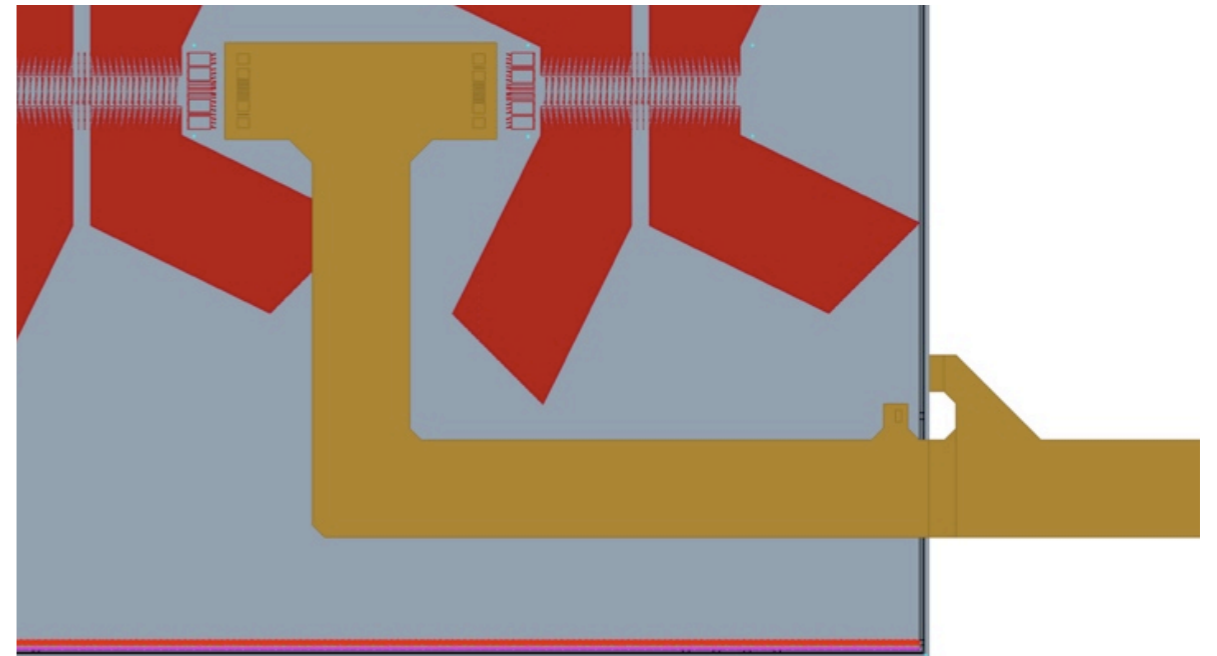
- 🍯 CDF Layer 00 mask design
- 🍯 150, 200, 300 μm thickness
- 🍯 Only yield issue is breakage of entire wafers
- 🍯 Bias voltage, charge collection, etc. as expected
- 🍯 Tested successfully with SVX4 readout: *KPiX* next

If *KPiX* achieves expected noise performance, 200 micron silicon will not compromise resolution

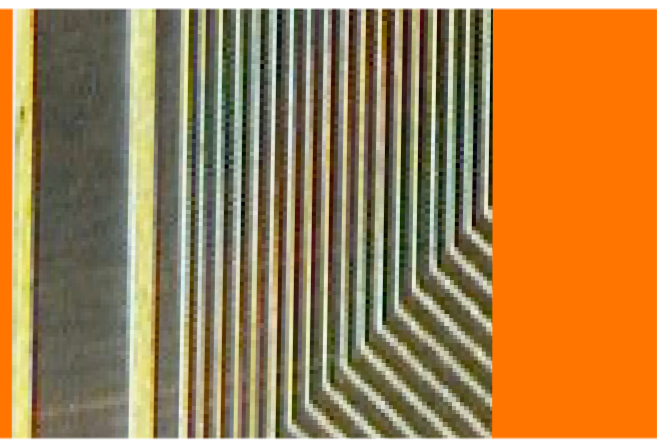


Cables

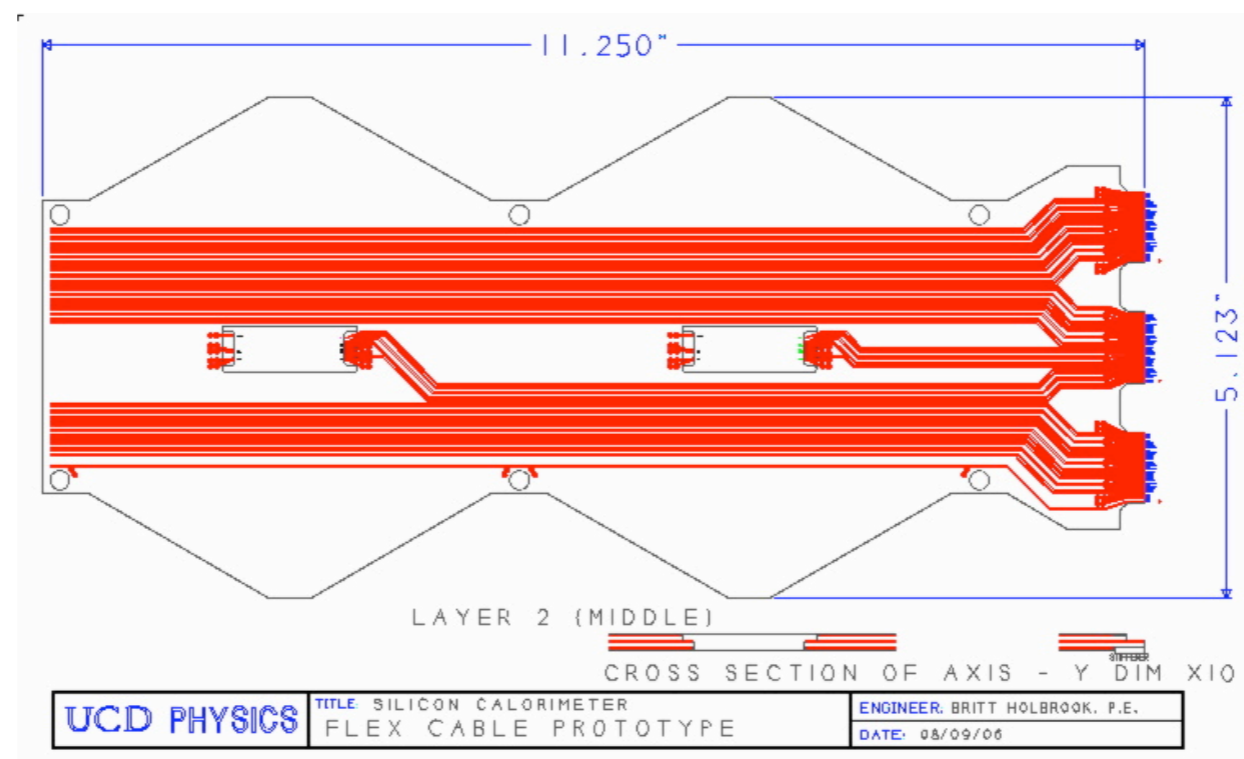
- ❏ ¼-ounce copper on 50 μ m Kapton
- ❏ 2 power+ground pairs <0.5 Ω /trace
- ❏ 8 narrow control/readout lines
- ❏ HV pair for sensor bias
- ➔ cable width ~1 cm
- ❏ pigtail includes surface mounts for filtering sensor bias and *KPiX* power
- ❏ long but simple extension cables to concentrator boards at ends of barrels: several viable mini-connector options



Cables - Status/Plans



UNM beginning cable design: UC Davis ECal cable provides initial reference

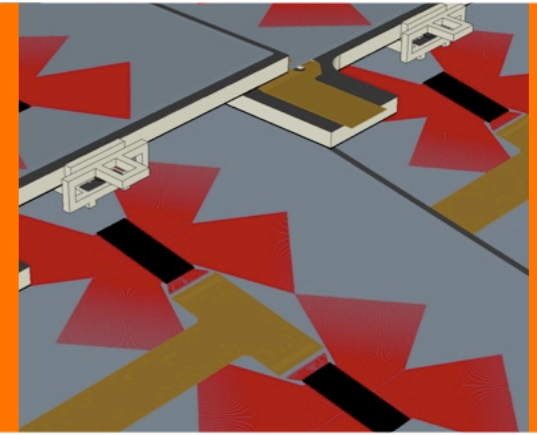


pigtail design for each module design: 2 barrel + 2 disk

one extension each for barrel and disk

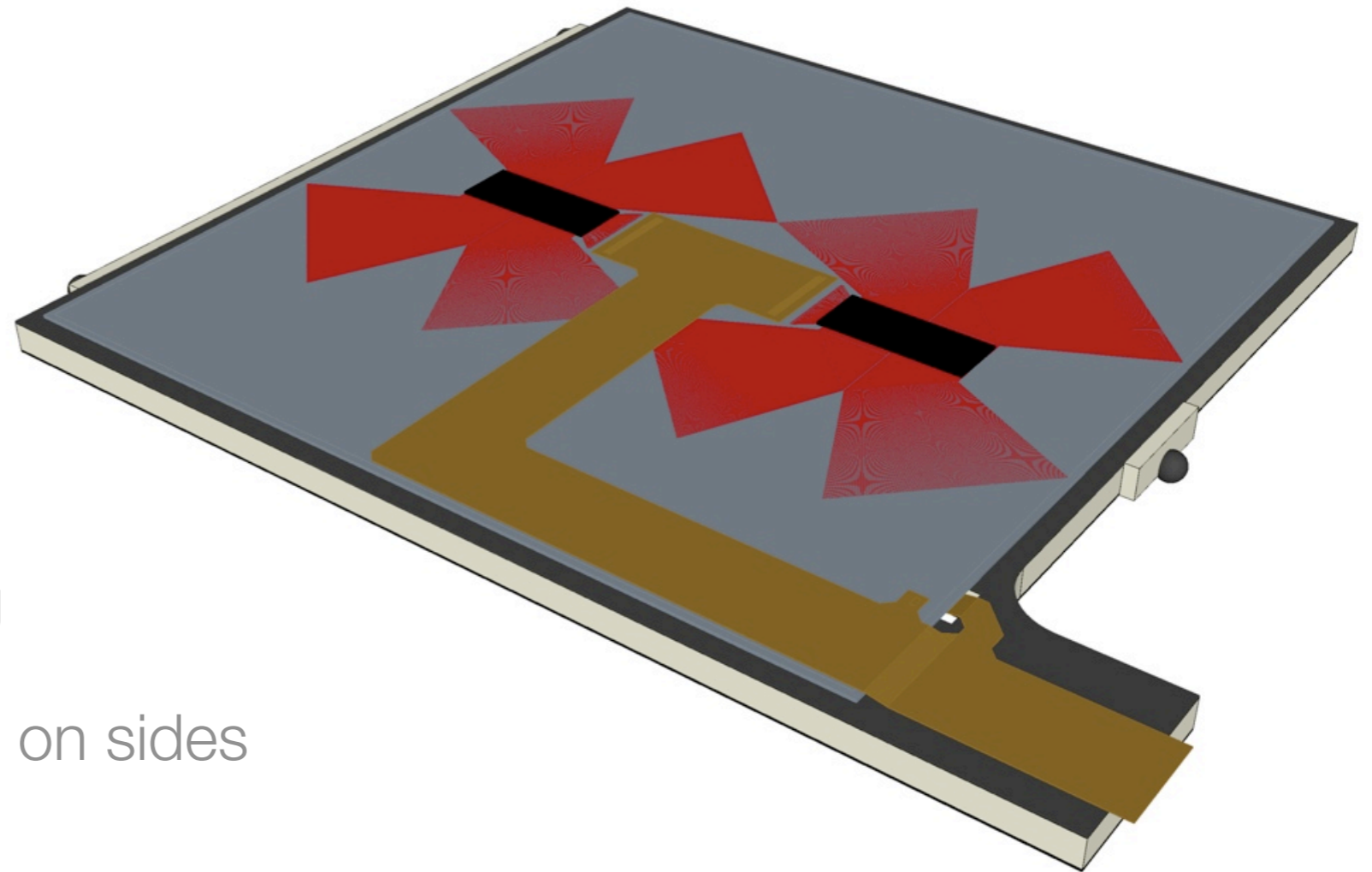


Module Support

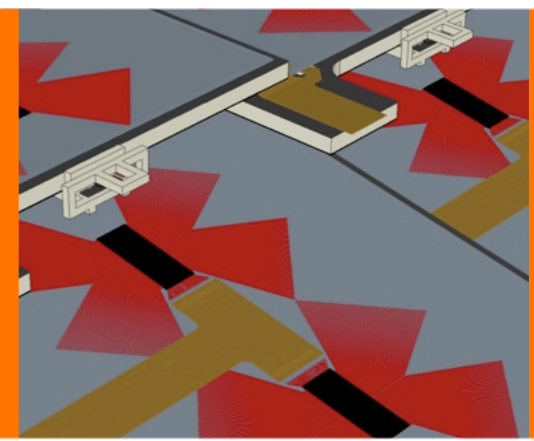


Can be minimal

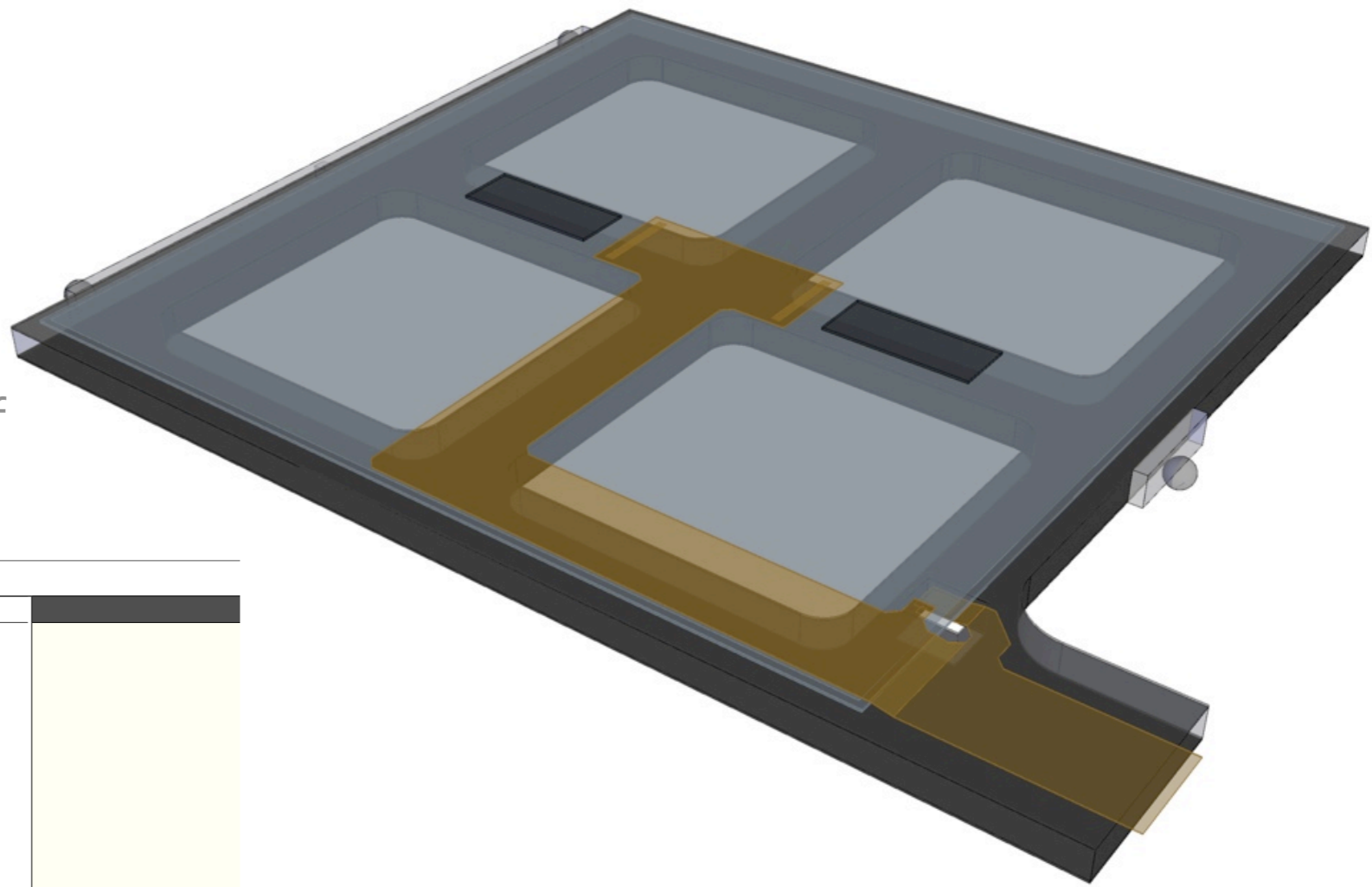
- ⬢ Hold silicon flat
- ⬢ Facilitate handling
- ⬢ Provide stable positioning
- ⬢ Allow for silicon mounting on sides



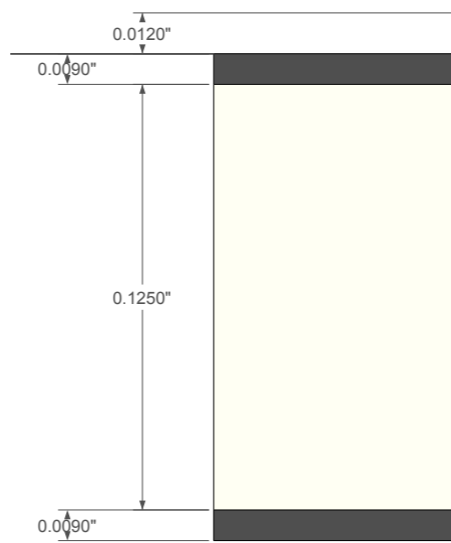
Module Support



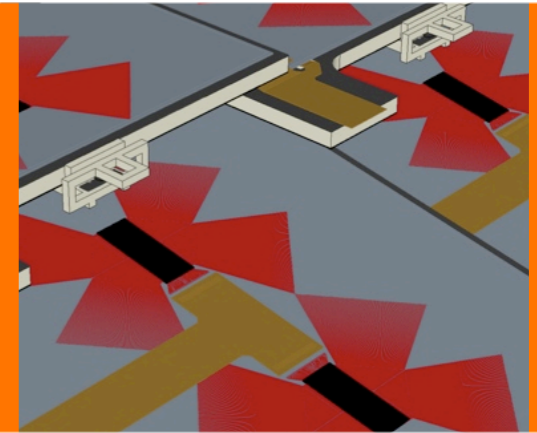
- ⊞ Pair of 60-60-60, 0.009" high-modulus CF sheets
- ⊞ 0.125" Rohacell sheet
- ⊞ 50% void, CF under chip
- ⊞ Handle / cable strain relief



Produced in sheets and cut by water jet



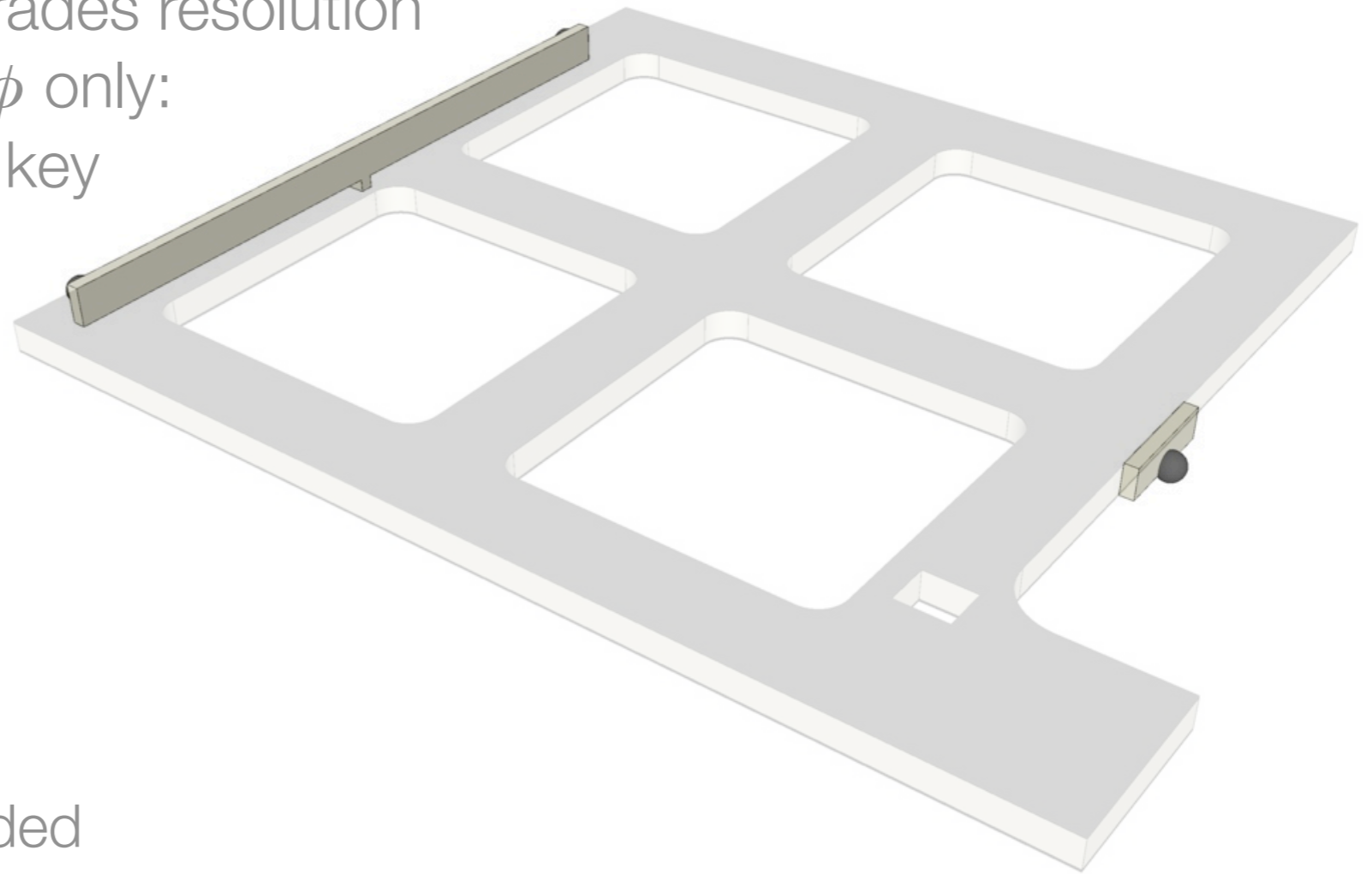
Module Mounting



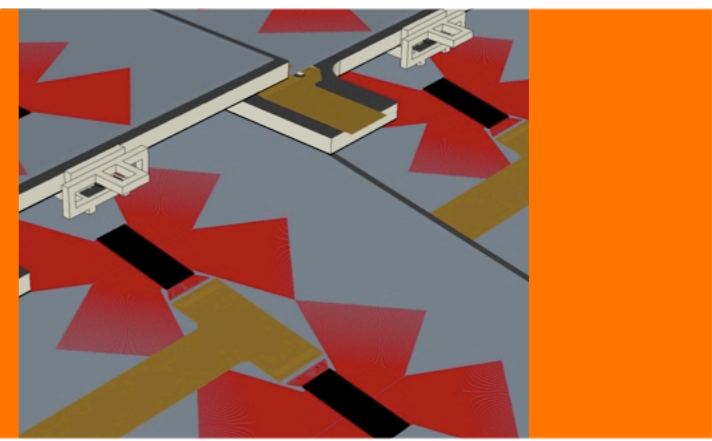
Axial strip misalignment degrades resolution for standalone if tracker is $r-\phi$ only: mounting repeatability is the key

Goal: $100\mu\text{rad}$

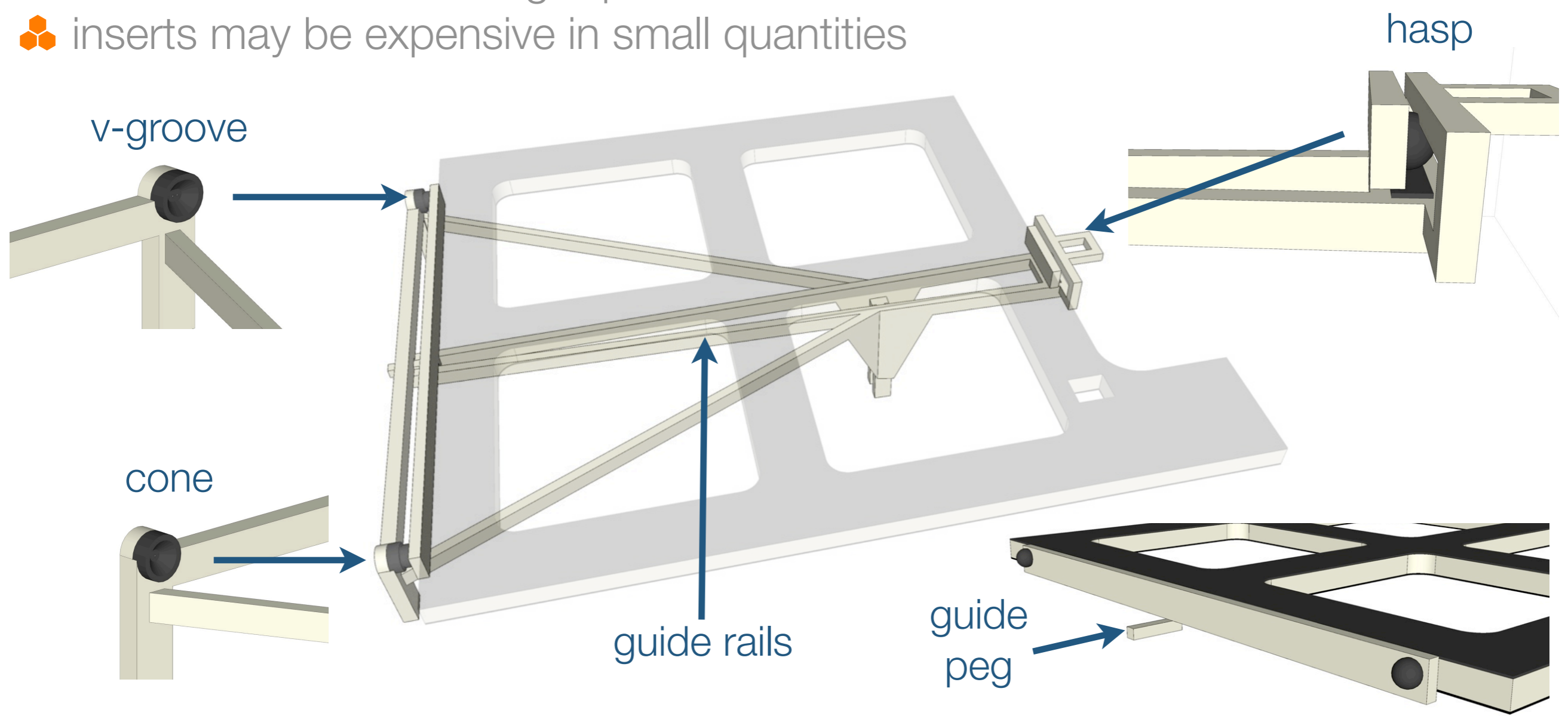
- ⬢ 30% CF-filled Torlon rails
 - ⬢ Modulus = 1/3 7075 Al
 - ⬢ CTE = Si + $3 \times 10^{-6}/^{\circ}\text{K}$
- ⬢ Mounting balls
 - ⬢ 0.125" Si_3N_4 , insert molded
 - ⬢ extremely hard, precise, light, inexpensive



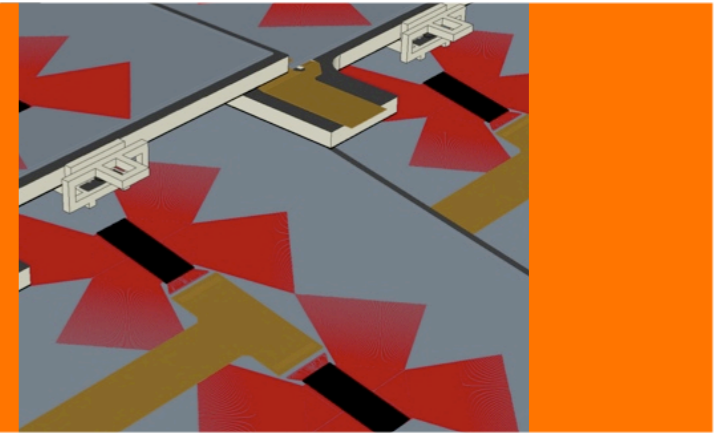
Module Mounting



- CF-filled Torlon mounting clip with custom Si_3N_4 inserts
- inserts may be expensive in small quantities



Module Support - Plans



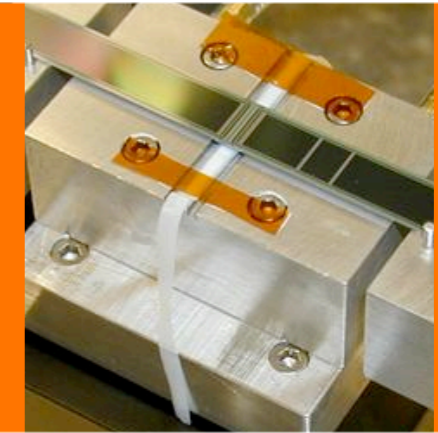
- Developed 3-d model of mounting scheme with input from Solvay (Torlon), Victrex (PEEK) and Ceradyne (Si_3N_4) with eye toward industrial manufacture
- Need FEA and bench testing to optimize frame & clip designs
- Two sets of rapid prototypes to refine concepts in both barrel and disk
 - first RP for barrel modules in March: CMM tests on mating repeatability
 - second RP for first modules and to develop final prototype design/tooling
- Final prototypes industrially produced: tool design/fabrication is a large NRE

Since standalone tracks are rare and have low P_T , all-Torlon may prove sufficient. Bench testing and simulation can answer this question.

R&D costs significantly lower if Torlon mating parts meet our requirements



Assembly



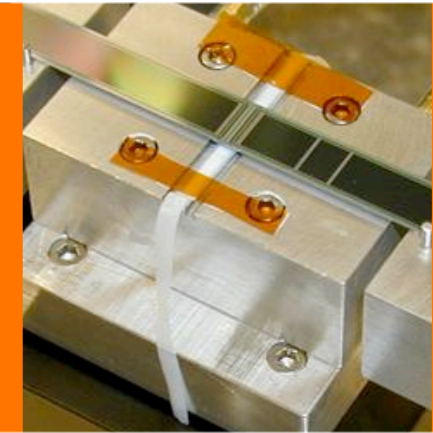
- Most parts/assembly by outside vendors

- bump bonding
- module frames
- mounting rails
- mounting clips

- Performing only specialized work in-house results in simple production

- attaching mounting rails to frames
- cable gluing
- bias connection
- cable wirebonding
- sensor gluing
- accept/reject testing
- wirebond encapsulation

Assembly - Plans



- ❏ Bump-bonding: benefitting from UC Davis expertise
- ❏ Will develop fixtures for each set of module prototypes
 - ❏ First set to test assembly concept with first barrel/disk module prototypes
 - ❏ Second set designed to simulate production fixtures for final barrel/disk module prototypes

Goal: simple, massively parallel production that minimizes dependence on expensive equipment and time-consuming procedures (e.g. alignment via CMM)

Test Beam



Require at least two test beam activities:

- ❏ Test beam with first barrel modules in early 2008:
 - ❏ standalone power supplies and small-scale DAQ
- ❏ Test beam with several planes of final barrel modules and first disk prototypes in early 2010:
 - ❏ full prototype DAQ and power distribution system

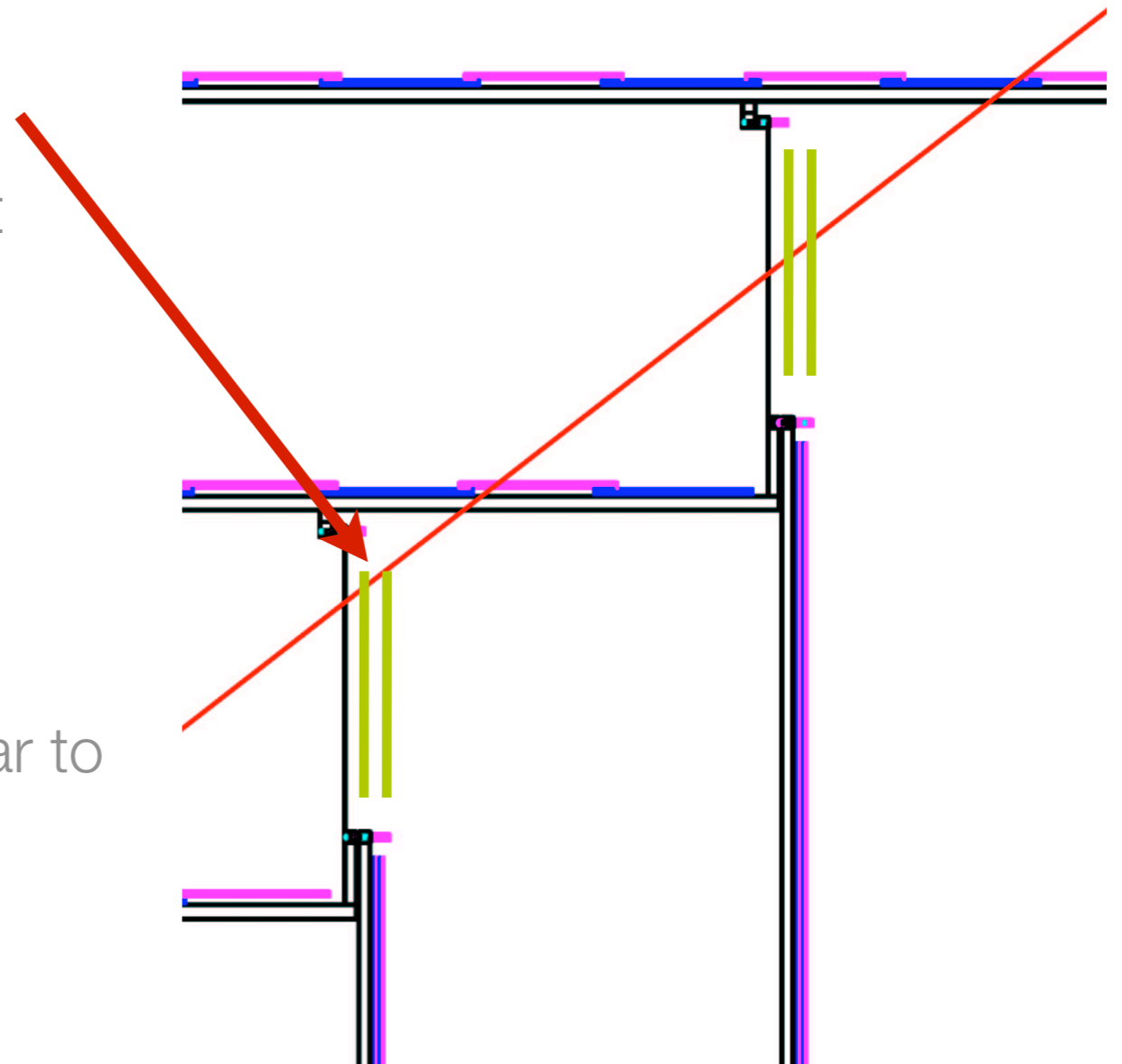
We will want to participate in joint test beams with other subsystems (esp. VTX and ECal) as opportunities present.

Power/Readout Distribution

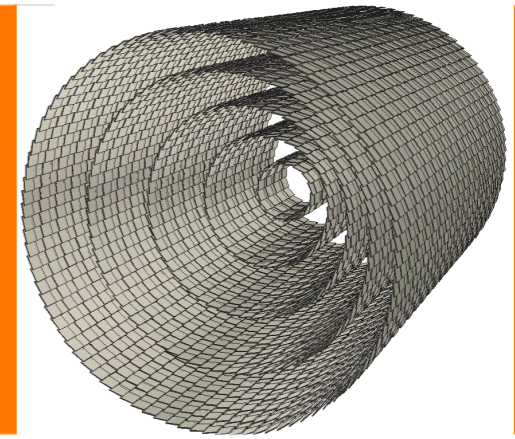


Concentrator boards distribute power, readout and control for ~20 modules each

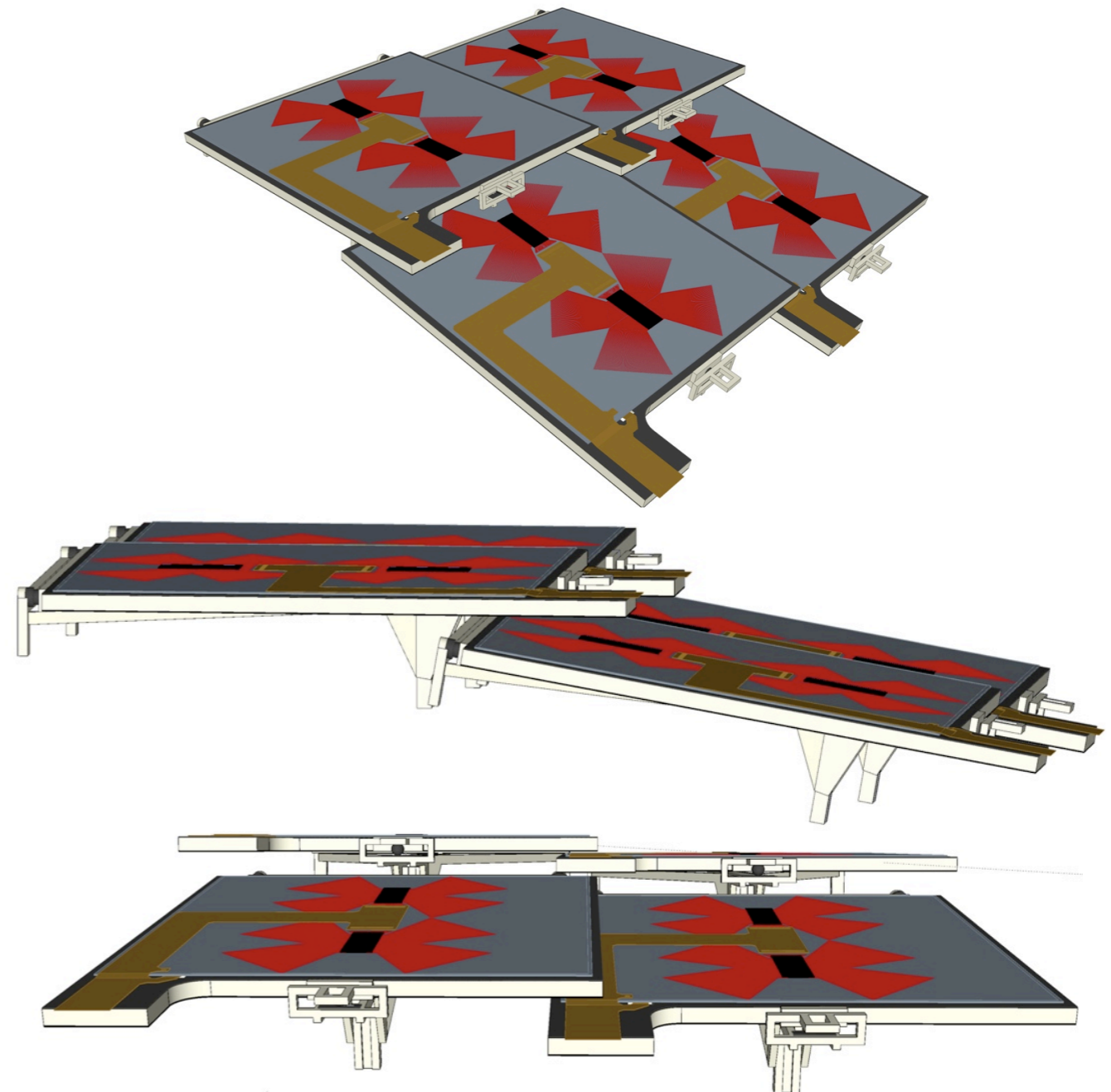
- ⦿ Existing optical transceivers easily meet data rate and power/cooling envelopes
- ⦿ Power is more difficult
 - ⦿ Plan DC-DC conversion to reduce incoming cable plant: no easy solution
 - ⦿ power pulsing presents problems similar to those in VTX but much less severe
 - ⦿ charge pump w/ power buffering?
 - ⦿ serial powering?

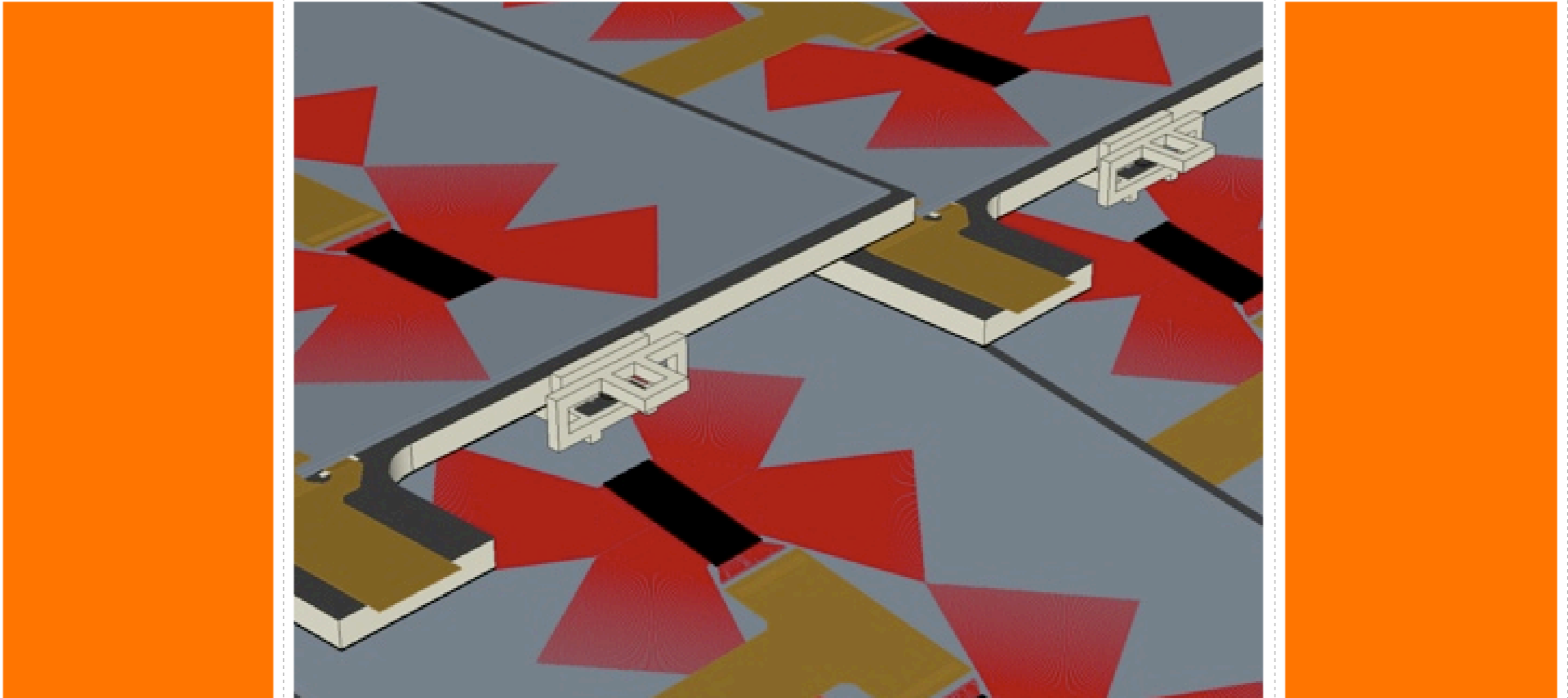


Summary



- ❏ Innovative, somewhat aggressive approach to module design
- ❏ Potential rewards justify risks
 - ❏ ~0.5% X_0 for single-sided modules, 300 μm silicon including cable stack
 - ❏ inexpensive, mass-produced components
 - ❏ simple assembly and installation
- ❏ Important to have alternate plans: wirebonded *KPiX* or UCSC LSTFE
- ❏ Major work (and funding) required





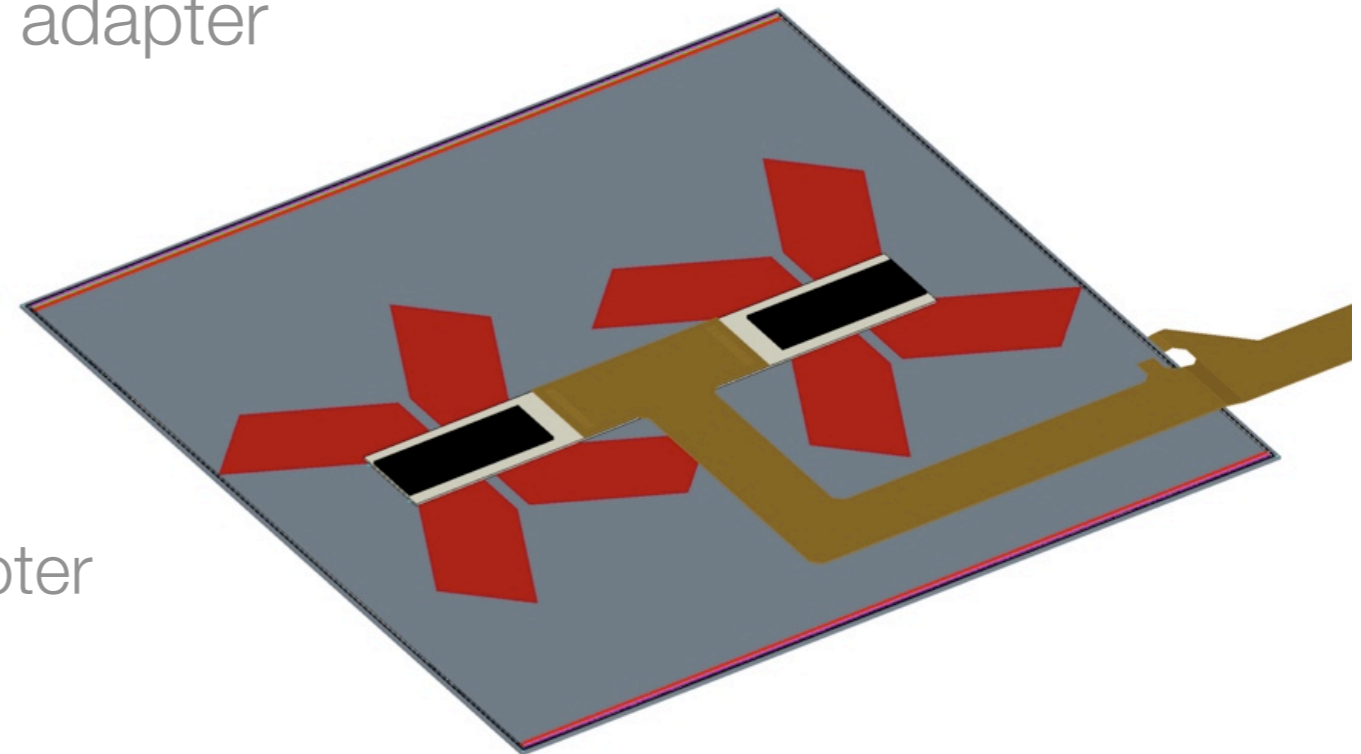
Additional Slides

Backup Plan?

- ❏ Introduction of a small flip-chip style adapter
 - ❏ Chips bump-bonded to adapter
 - ❏ Adapter bump-bonded or wirebonded to sensor
 - ❏ Readout/power on top side of adapter

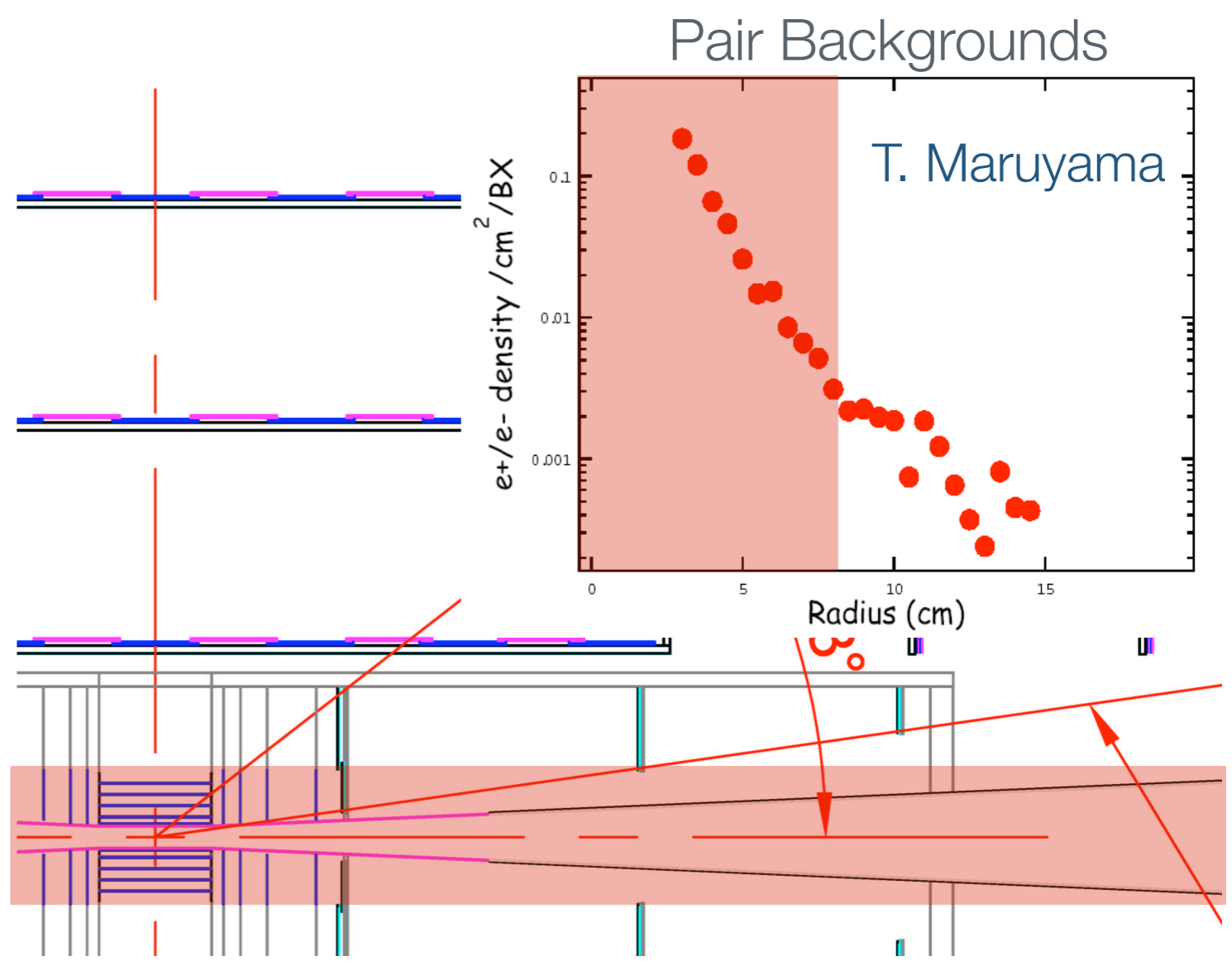
- ❏ Production of wirebondable KPiX chip is possible, but options for mechanical assembly are relatively distasteful

- ❏ Parallel development of UCSC LSTFE is an important contingency for SiD tracker



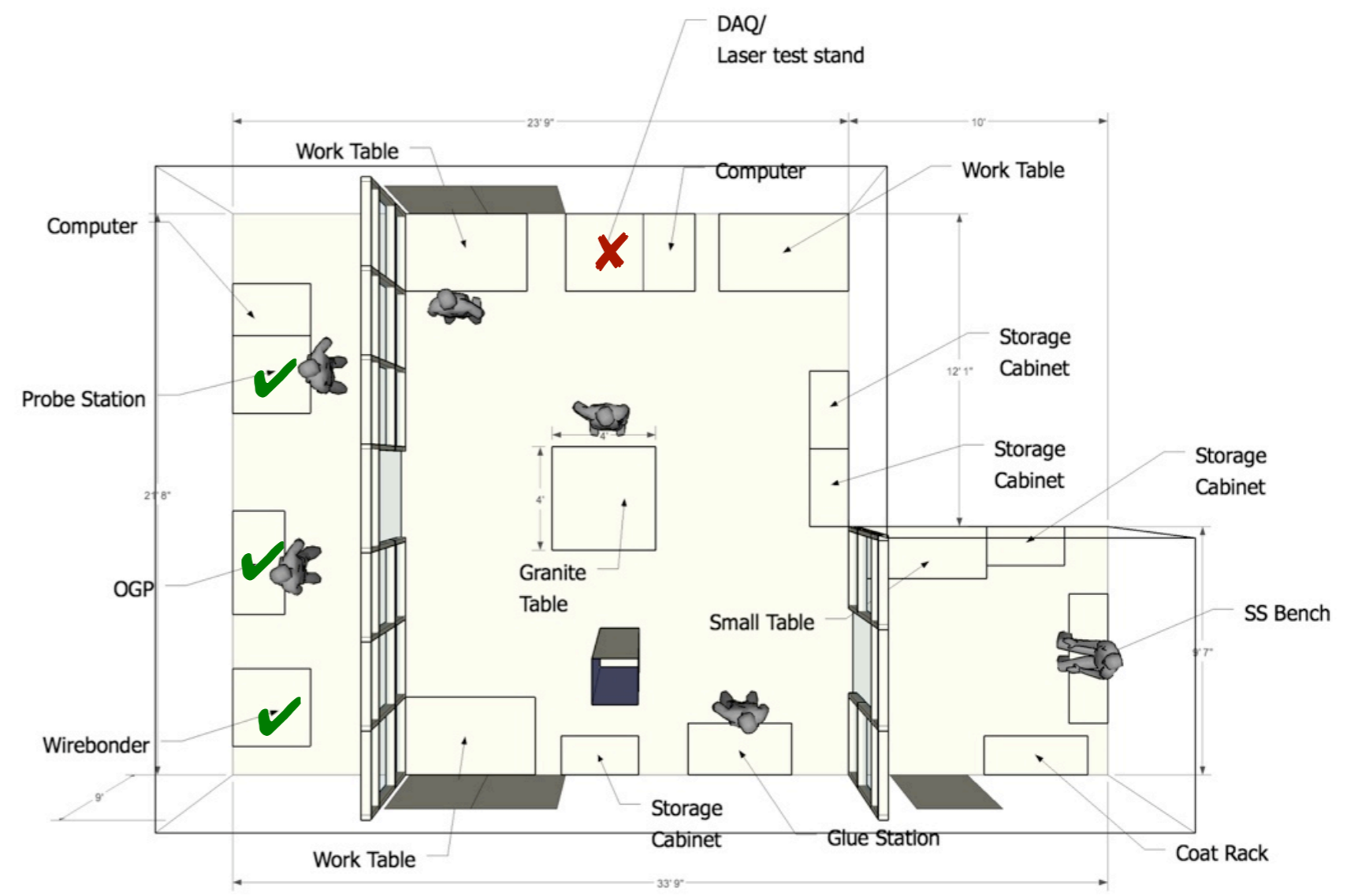
Far Forward Region

- Only one small piece of far-forward disks will be problematic for baseline KPiX-based design
- If so, this piece could easily become part of VXD

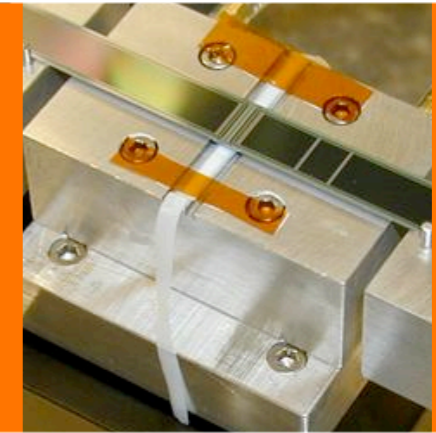


SLAC Laboratory Facilities

- ❏ Plans for silicon laboratory/cleanroom at SLAC well underway
- ❏ Pending support in a tough FY07
- ❏ 3 of 4 major pieces of equipment in hand



Assembly Precision



Repeatability is the key to strip alignment

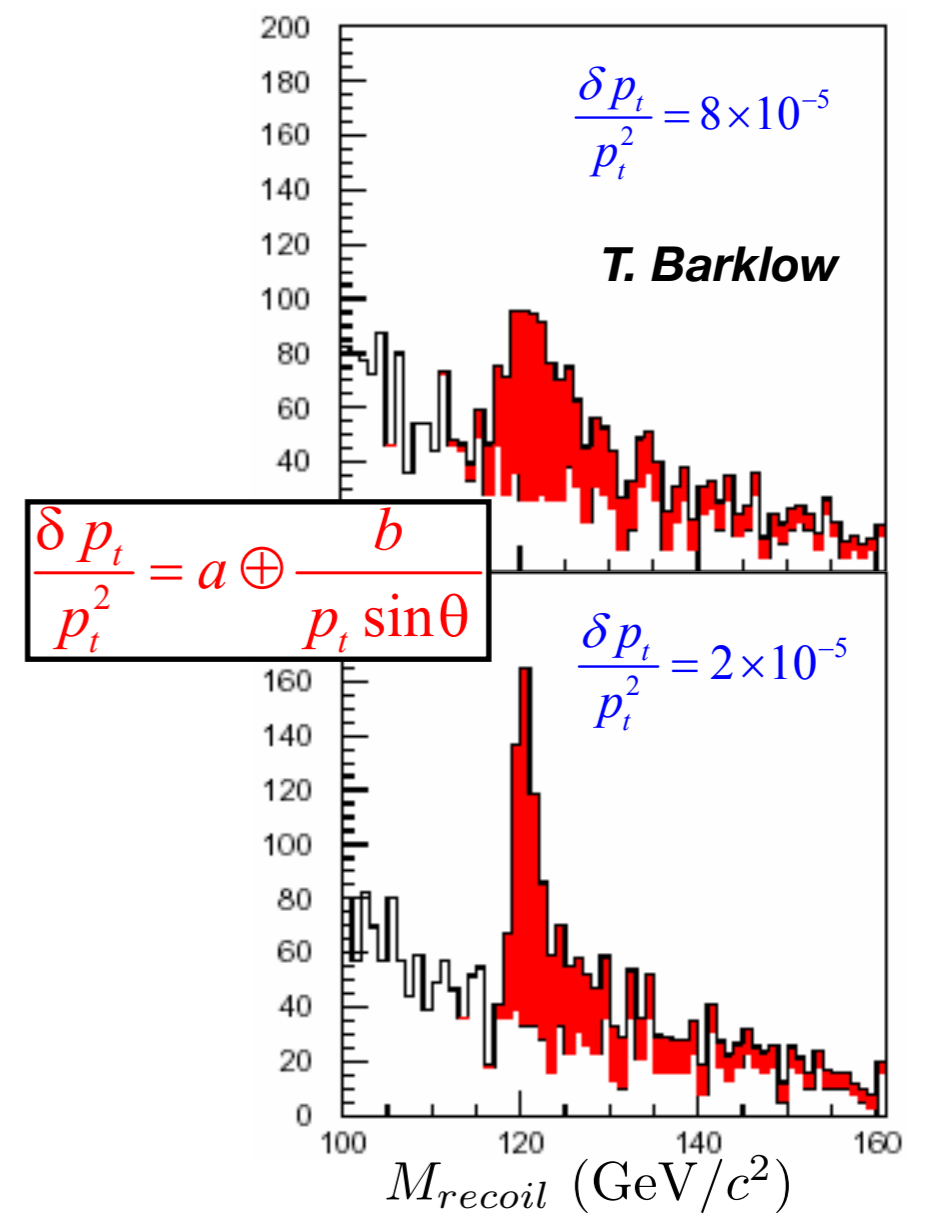
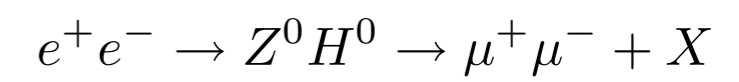
- 🔸 Sensor→Frame: frame clips to assembly fixture exactly as to mounting clip
 - ➡ strip orientation w.r.t. fixture reproduced w.r.t. mounting clips
- 🔸 Clips→Barrel: clips attach to assembly fixture exactly as to module frames
 - ➡ strip orientation preserved when frames are clipped onto barrel supports

Homogeneity and surface finish of mating parts are the critical elements.
Materials and fabrication techniques must be chosen with these factors in mind.

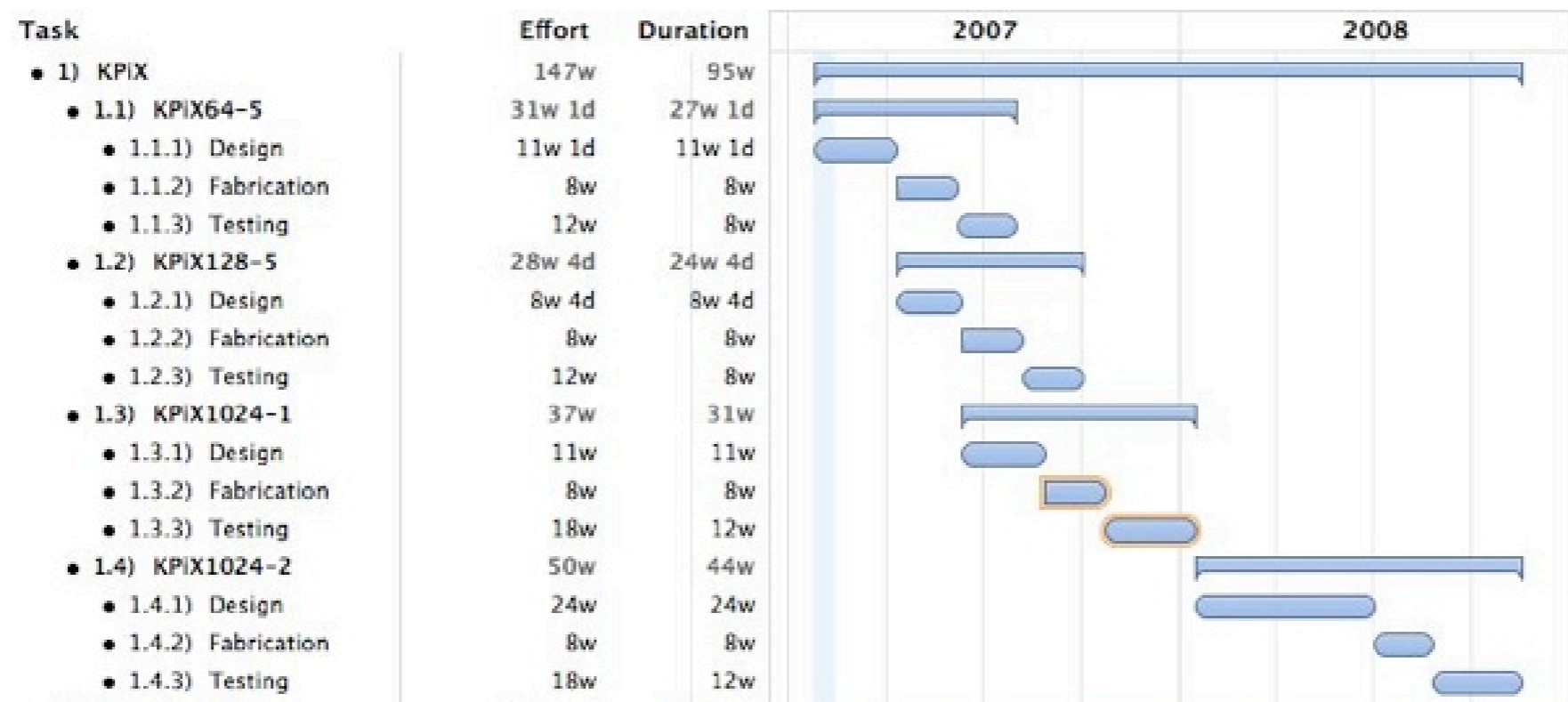
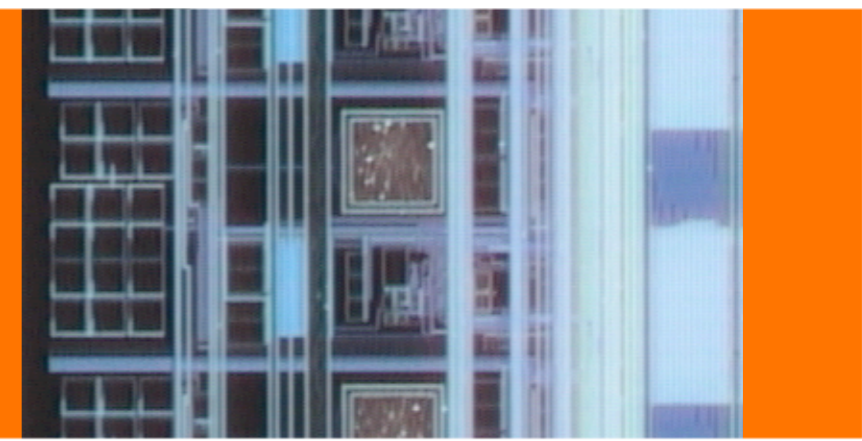
Tracking Requirements

SiD tracking must...

- 🍯 provide superior asymptotic P_T resolution (“a”)
- 🍯 place minimal material in tracking volume (“b”)
- 🍯 provide tracking throughout a large volume
- 🍯 be efficient and robust against backgrounds
- 🍯 be robust against accidents and aging



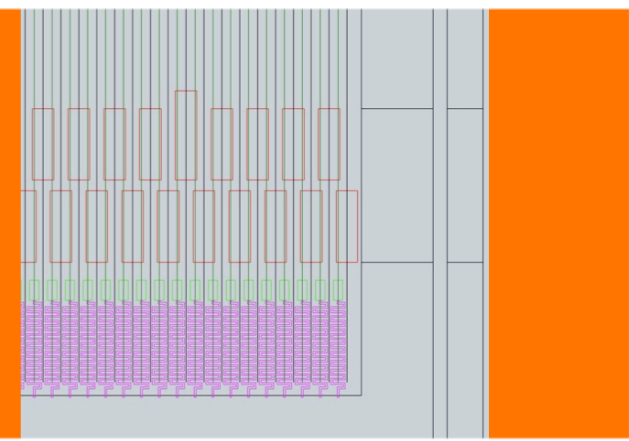
KPiX - Plans



Resource	2007	2008	2009	2010	2011	Totals
M&S	83K	50K	-	-	-	133K
Staff	0.25	0.25	-	-	-	0.5
Postdocs	-	-	-	-	-	-
Elec. Eng.	0.25	0.25	-	-	-	0.5
Mech. Eng.	-	-	-	-	-	-
Students	0.25	0.25	-	-	-	0.5
Technicians	0.25	0.25	-	-	-	0.5

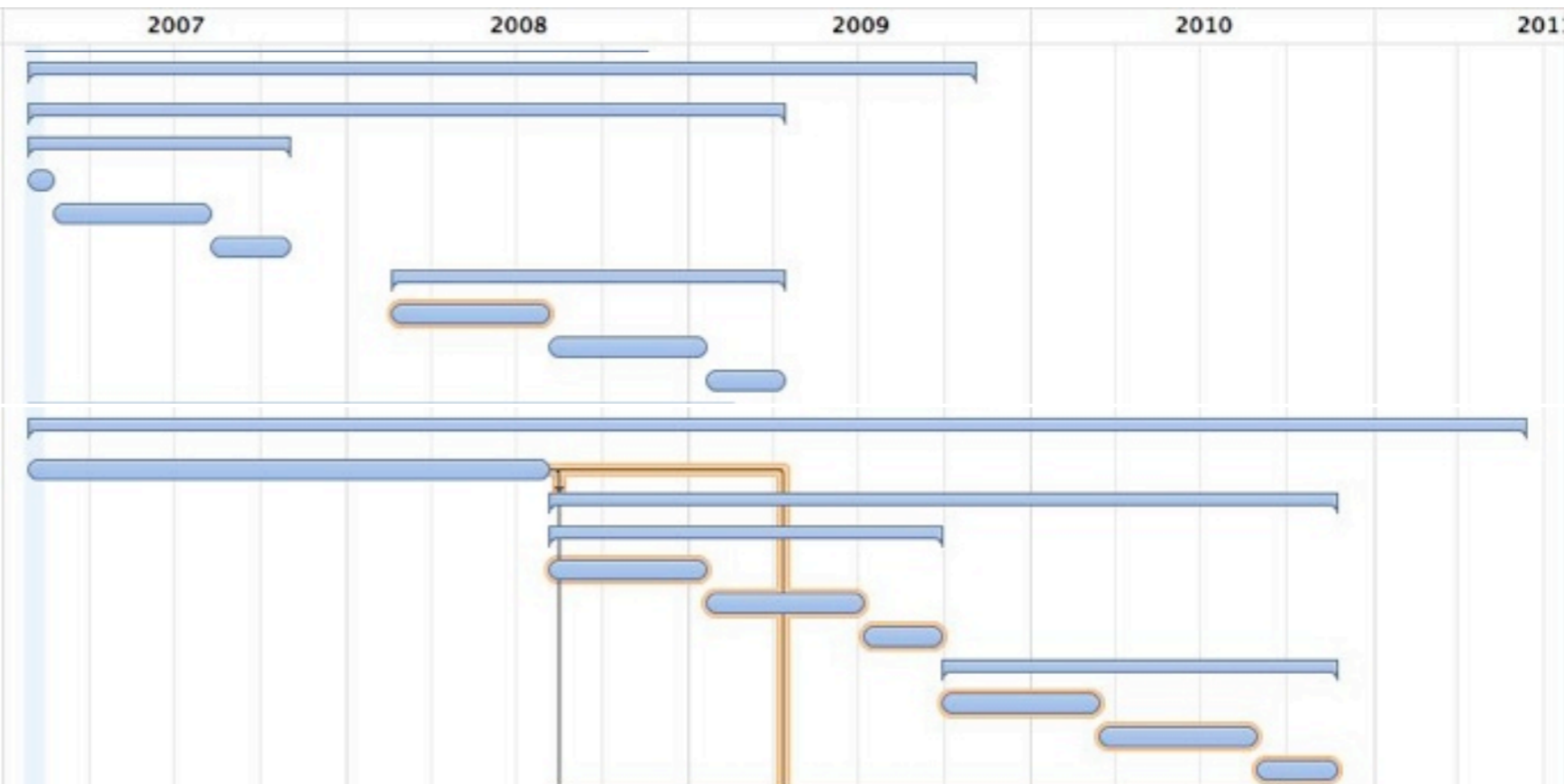


Silicon Sensors - Plans



- Task
- 2) Barrel Modules
 - 2.1) Sensors
 - 2.1.1) Prototype 1
 - 2.1.1.1) Design
 - 2.1.1.2) Fabrication
 - 2.1.1.3) Testing
 - 2.1.2) Prototype 2
 - 2.1.2.1) Design
 - 2.1.2.2) Fabrication
 - 2.1.2.3) Testing
- 3) Disk Modules
 - 3.1) Design Studies
 - 3.2) Sensors
 - 3.2.1) Prototype 1
 - 3.2.1.1) Design
 - 3.2.1.2) Fabrication
 - 3.2.1.3) Testing
 - 3.2.2) Prototype 2
 - 3.2.2.1) Design
 - 3.2.2.2) Fabrication
 - 3.2.2.3) Testing

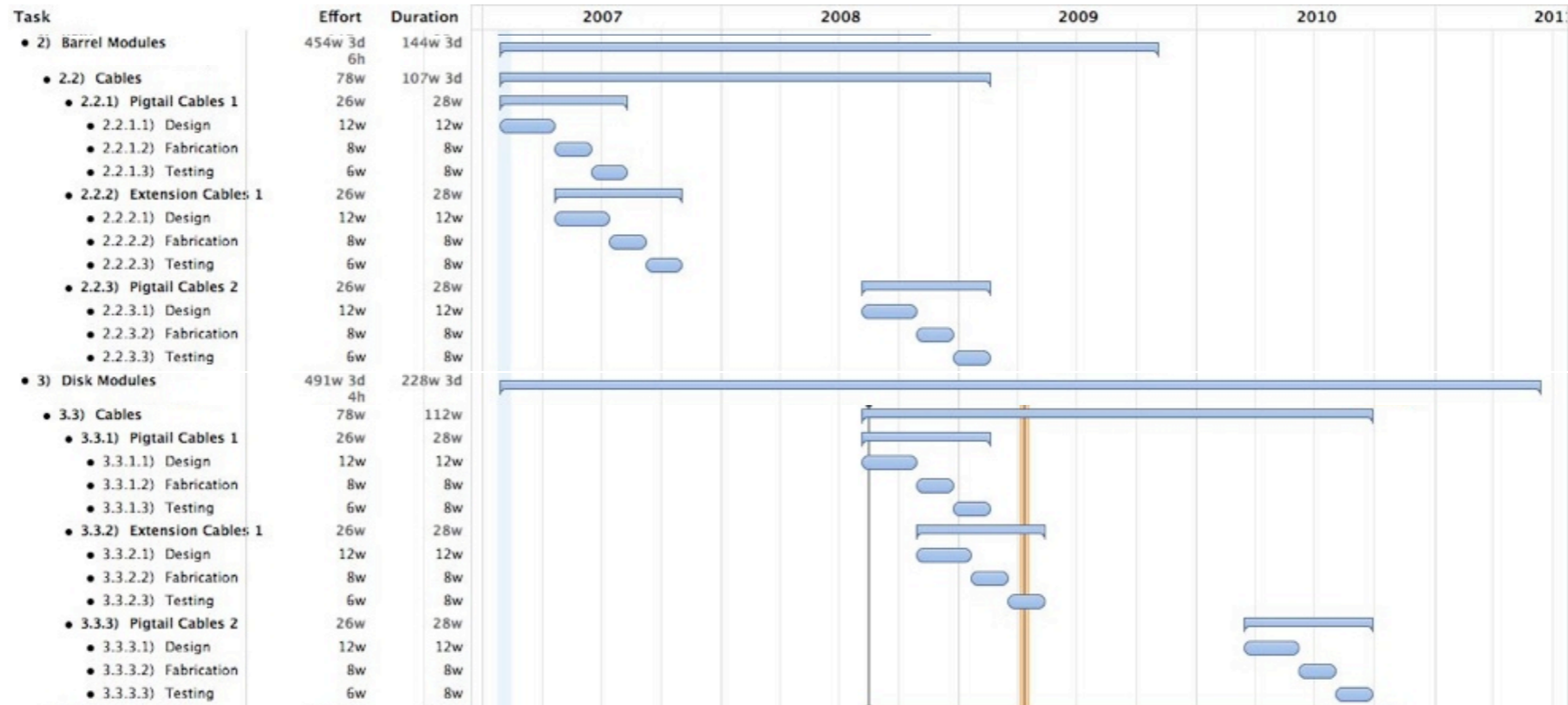
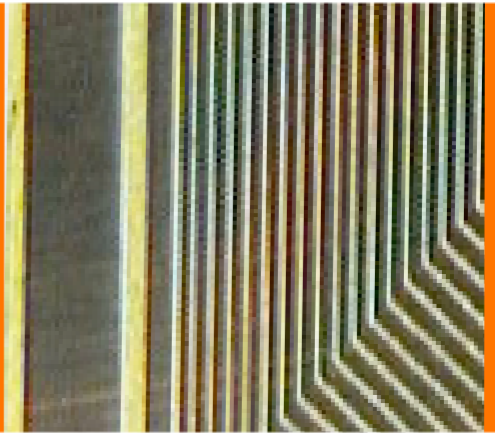
Effort	Duration
454w 3d 6h	144w 3d
80w 4d 2h	115w 3d
32w 4d 2h	39w 4d
2w 4d 2h	3w 4d
24w	24w
6w	12w
48w	60w
18w	24w
24w	24w
6w	12w
491w 3d 4h	228w 3d
39w 4d	79w 3d
96w	120w
48w	60w
18w	24w
24w	24w
6w	12w
48w	60w
18w	24w
24w	24w
6w	12w



Resource	2007	2008	2009	2010	2011	Totals
M&S	100K	-	200K	100K	-	400K
Staff	-	0.25	0.25	0.25	-	0.75
Postdocs	-	-	-	-	-	-
Elec. Eng.	-	-	-	-	-	-
Mech. Eng.	-	-	-	-	-	-
Students	0.25	-	0.5	0.25	-	1.0
Technicians/Designers	-	0.5	0.5	0.5	-	1.5



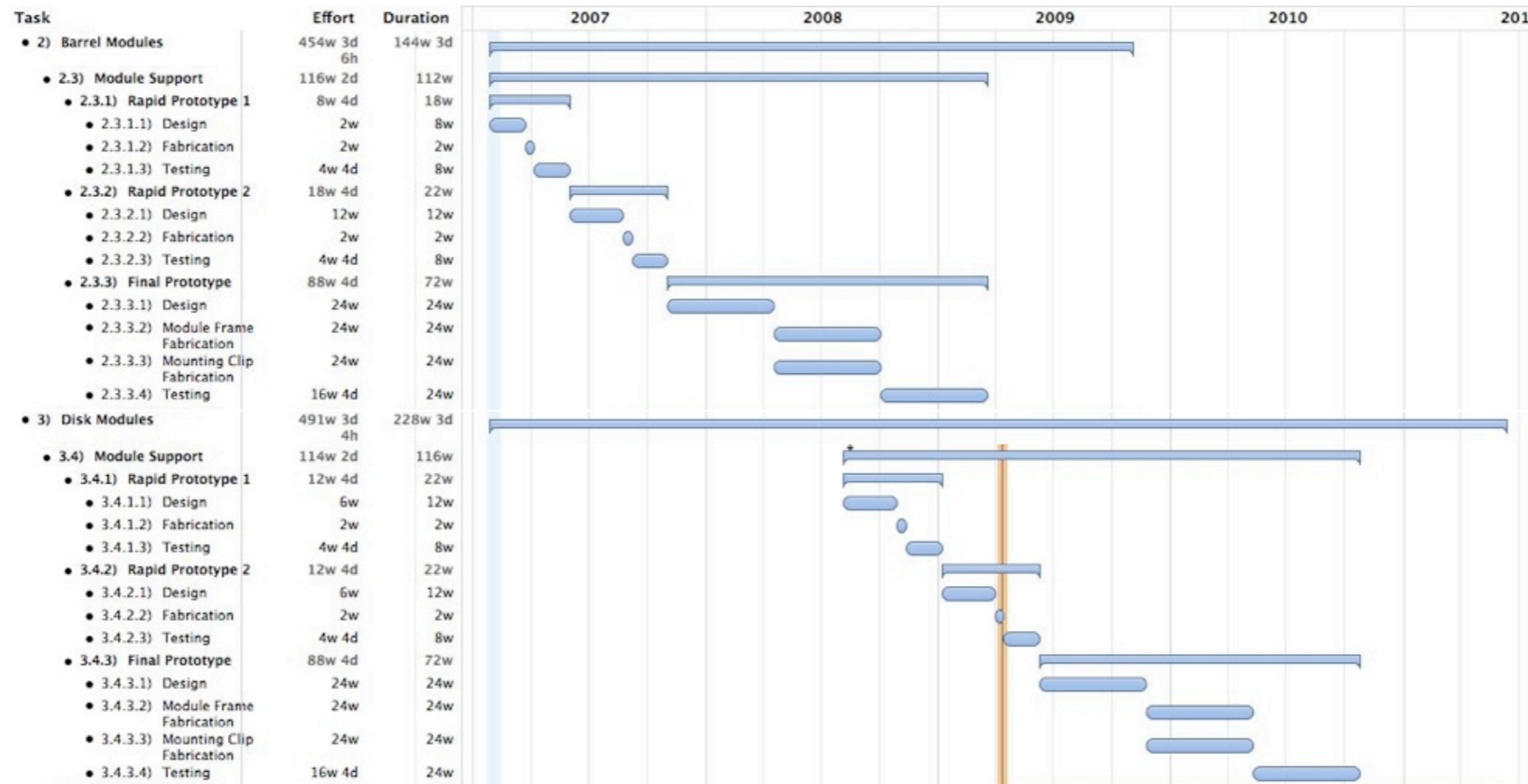
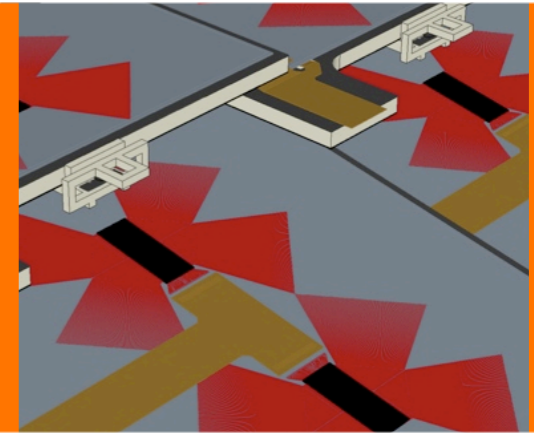
Cables - Plans



Resource	2007	2008	2009	2010	2011	Totals
M&S	30K	-	40K	10K	-	80K
Staff	0.25	-	0.25	-	-	0.5
Postdocs	-	-	-	-	-	-
Elec. Eng.	0.5	0.5	0.25	0.25	-	1.5
Mech. Eng.	-	-	-	-	-	-
Students	0.25	-	0.25	0.25	-	0.75
Technicians	-	-	-	-	-	-



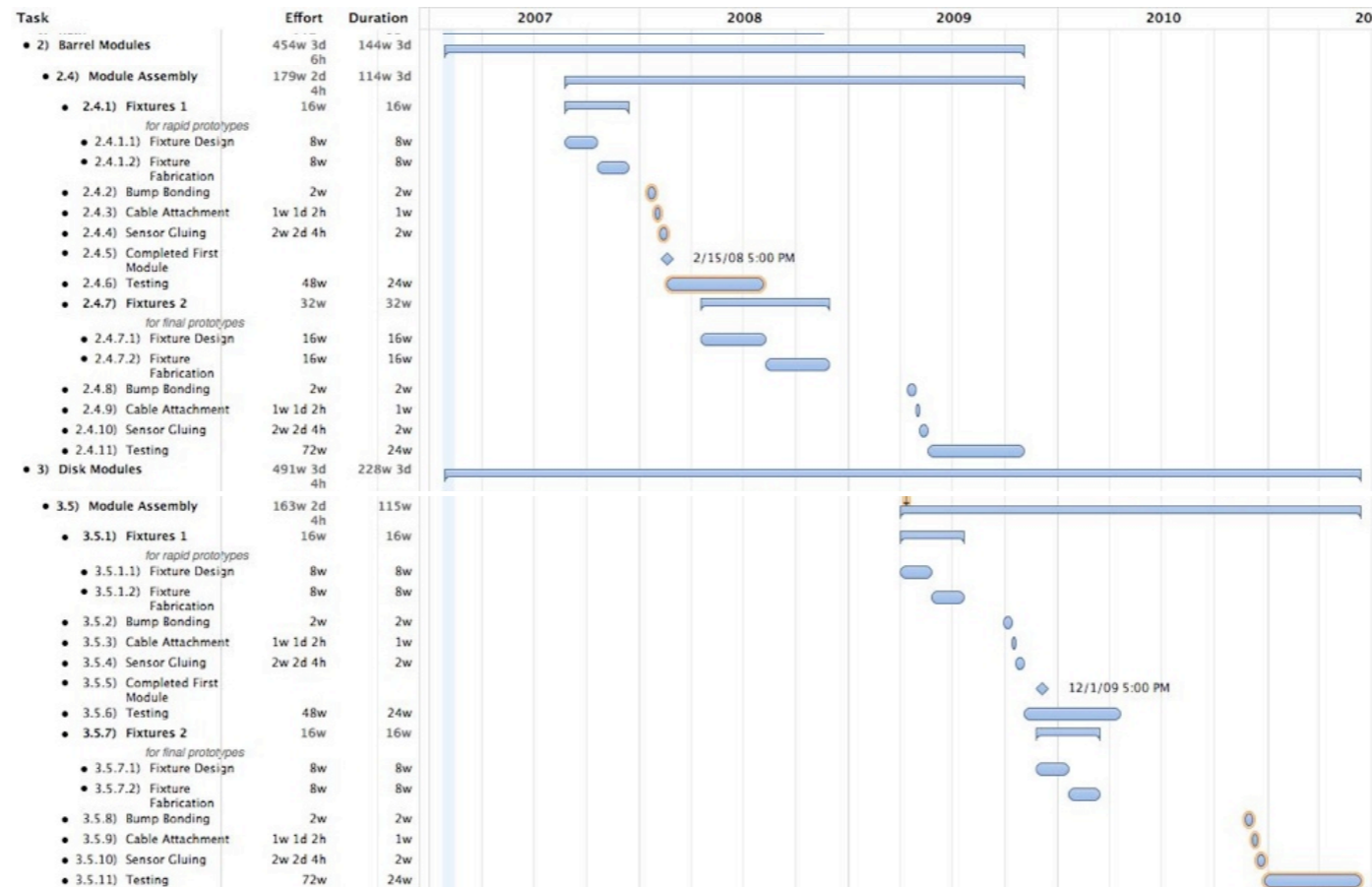
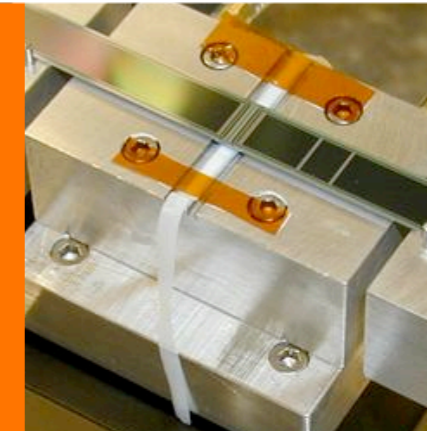
Module Support - Plans



Resource	2007	2008	2009	2010	2011	Totals
M&S	10K	160K	30K	150K	-	340K
Staff	0.5	0.5	0.25	-	-	1.25
Postdocs	-	-	-	-	-	-
Elec. Eng.	-	-	-	-	-	-
Mech. Eng	0.25	0.5	0.5	-	-	1.25
Students	-	-	-	-	-	-
Technicians/ Designers	0.25	-	0.25	0.25	-	0.75



Assembly - Plans



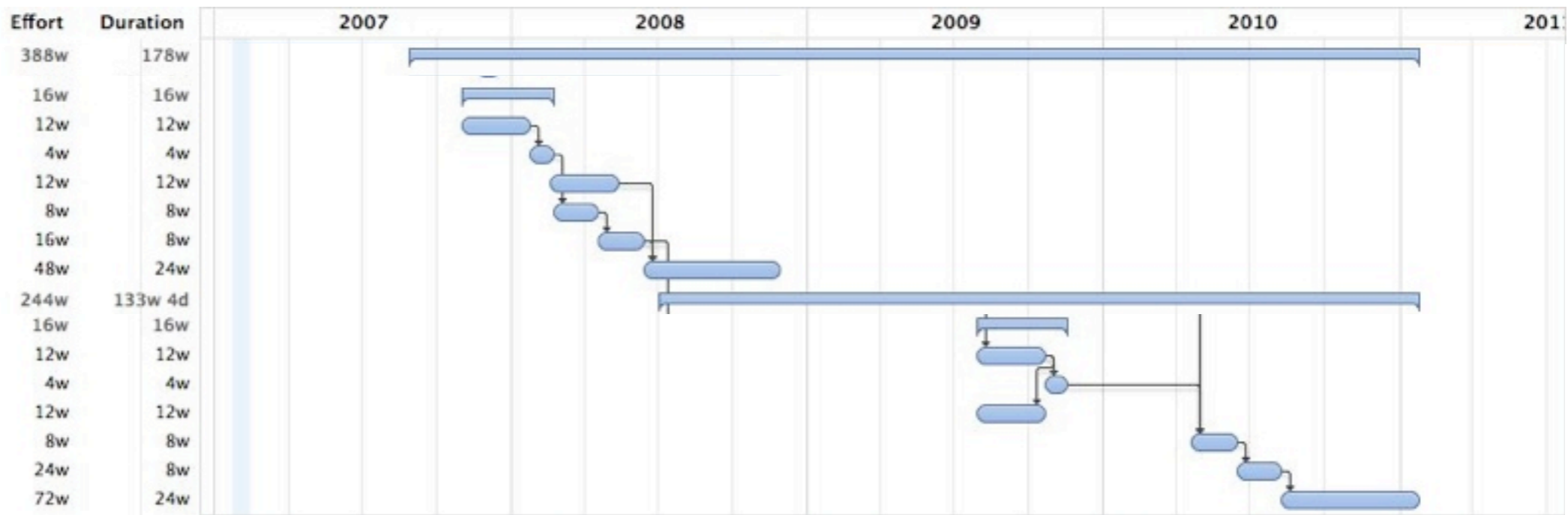
Resource	2007	2008	2009	2010	2011	Totals
M&S	25K	10K	20K	10K	-	65K
Staff	-	0.25	0.25	0.25	0.25	1.0
Postdocs	-	0.5	0.5	0.5	0.5	2.0
Elec. Eng.	-	-	-	-	-	-
Mech. Eng	0.25	0.25	0.25	0.25	-	1.0
Students	-	-	0.5	0.5	0.5	1.5
Technicians/ Designers	0.25	0.25	0.25	0.25	0.25	1.25



Test Beam - Plans



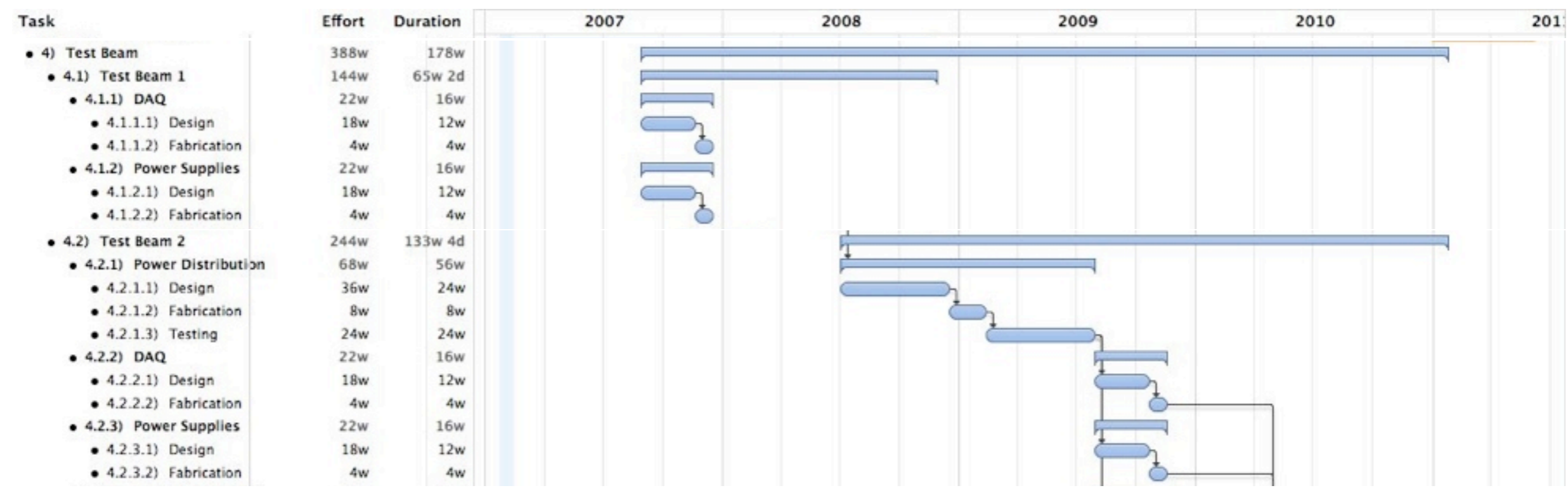
- Task**
- 4) Test Beam
 - 4.1.3) Support Structure
 - 4.1.3.1) Design
 - 4.1.3.2) Fabrication
 - 4.1.4) Software Design
 - 4.1.5) Assembly
 - 4.1.6) Operation
 - 4.1.7) Data Analysis
 - 4.2) Test Beam 2
 - 4.2.4) Support Structure
 - 4.2.4.1) Design
 - 4.2.4.2) Fabrication
 - 4.2.5) Software Design
 - 4.2.6) Assembly
 - 4.2.7) Operation
 - 4.2.8) Data Analysis



Resource	2007	2008	2009	2010	2011	Totals
M&S	-	5K	-	10K	-	15K
Staff	-	0.25	-	0.25	-	0.5
Postdocs	-	-	-	0.25	0.25	0.5
Elec. Eng.	-	-	-	-	-	-
Mech. Eng.	-	0.25	0.25	-	-	0.5
Students	-	0.5	0.25	0.5	0.5	1.75
Technicians/ Designers	-	0.25	-	0.25	-	0.5



Power/Readout Distribution



Resource	2007	2008	2009	2010	2011	Totals
M&S	-	10K	5K	10K	-	25K
Staff	-	-	-	-	-	-
Postdocs	-	-	-	-	-	-
Elec. Eng.	0.25	0.25	0.25	-	-	0.75
Mech. Eng.	-	-	-	-	-	-
Students	-	-	0.5	-	-	0.5
Technicians / Designers	-	-	0.25	-	-	0.25

