HCAL heat dissipation and power management

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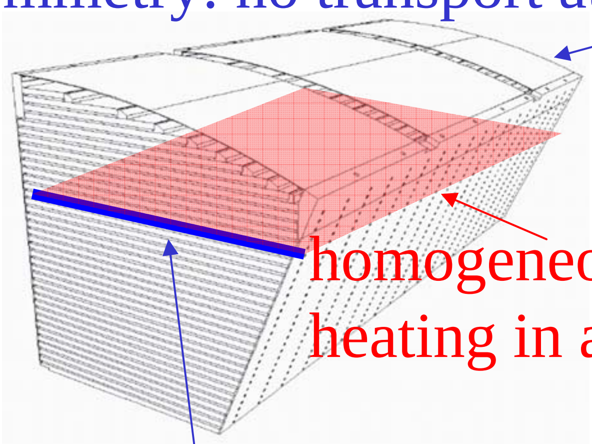
Rough ideas, calculations and numbers

What is easy?   Where are problems?

- Heat transfer
- Charge storage for pulsed operation

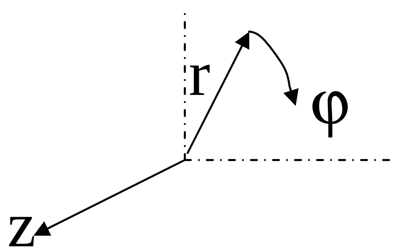
Heat transfer

symmetry: no transport at z=0m



homogeneous
heating in all gaps

cooling at the ends: z=±2.2m



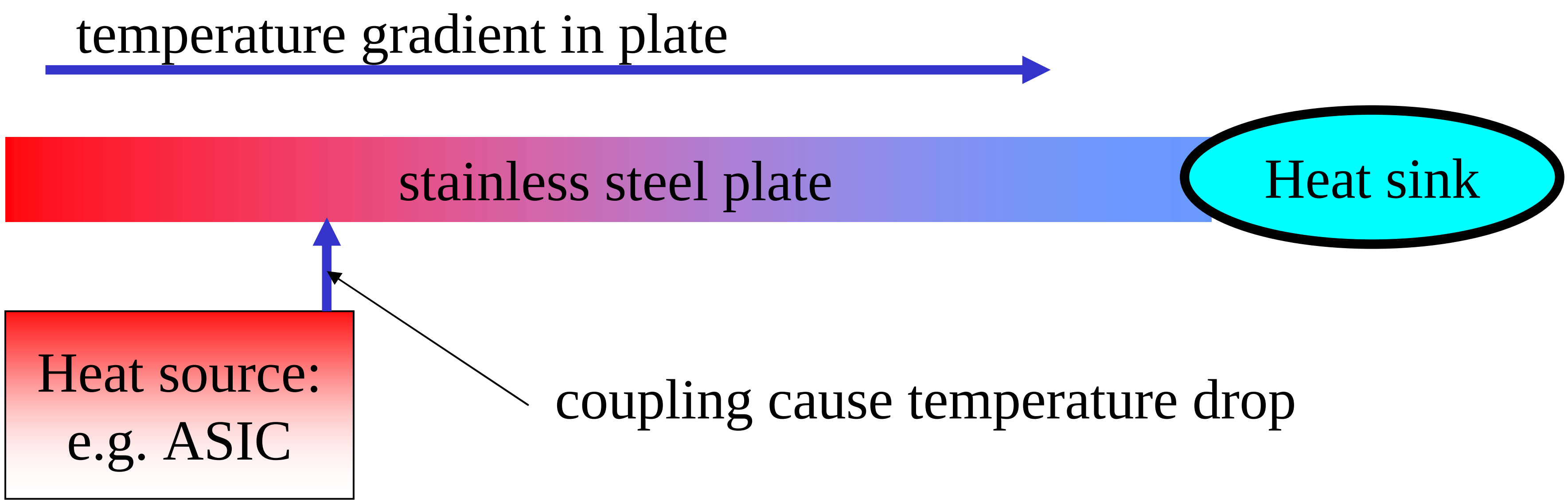
Heat transport in directions:

φ homogeneous heating:
➡No heat transfer in φ

r alternating structure
with air gaps
every air gap is heating
➡No heat transfer in r

z cooling at end plate
Heat flows in solid material,
air gaps too small, no convection

Heat transfer



Heat transfer in steel plate: Basic parameters

Heat production:

Power: P_{chan}=40μW/chan

ASIC: 25μW/chan

HV: +15μW/chan: 50V*0.3μA

Infrastructure: + ??

Geometry:

N_{chan} = 1000/m^2

D_{steel} =2cm (thickness)

L_{heat} = 2.2m (length)

Material constants:

Stainless steel: Which one?

λ_{steel} =15W/Km other publication 15-25W/Km

κ_{steel} = 3.7MJ/m^{3}K

Easier geometry: One direction "z" for transport

Energy conservation:

energy in "dz" = heat flow inside steel + heat from electronic

$$\kappa \, dVolume \frac{\partial T}{\partial t} = -dArea_{transvers} \frac{\partial \Delta Q_{out-in}}{\partial t} + P_{chan} N_{chan} dArea_{heating}$$

Heat transport: $$\frac{\partial Q}{\partial t} = -\lambda_{steel} \, Area_{transverse} \frac{\partial T}{\partial z}$$

$$\kappa_{steel} \, d_{steel} \frac{\partial T}{\partial t} = \lambda_{steel} \, d_{steel} \frac{\partial^2 T}{\partial z^2} + P_{chan} \, N_{chan}$$

Solution after long heating

Long heating: $$\frac{\partial T}{\partial t} = 0$$

No heat transport at z=0 (Symmetry point)

$$T \quad = \quad -(z^2 - L_{heat}^2)\,\frac{P_{chan} N_{chan}}{2\lambda_{steel} d_{steel}}$$

For L_{heat}=2.2m the temperature raise at z=0m: T(0m) = 0.33K

Every thing is from formula, so it is easy to adapt, when getting more accurate information: tile-size, power,....

OK, but keep end well cooled!!!!!!

and take care to add not many more heat sources !!!!

Time dependence

Fourier transformation with components parameterized by τ, $\alpha(\tau)$

elements: A $e^{-(t/\tau)}$ cos($2\pi\alpha$(x/L_{heat}))

α is part of the wavelength inside the steel plate

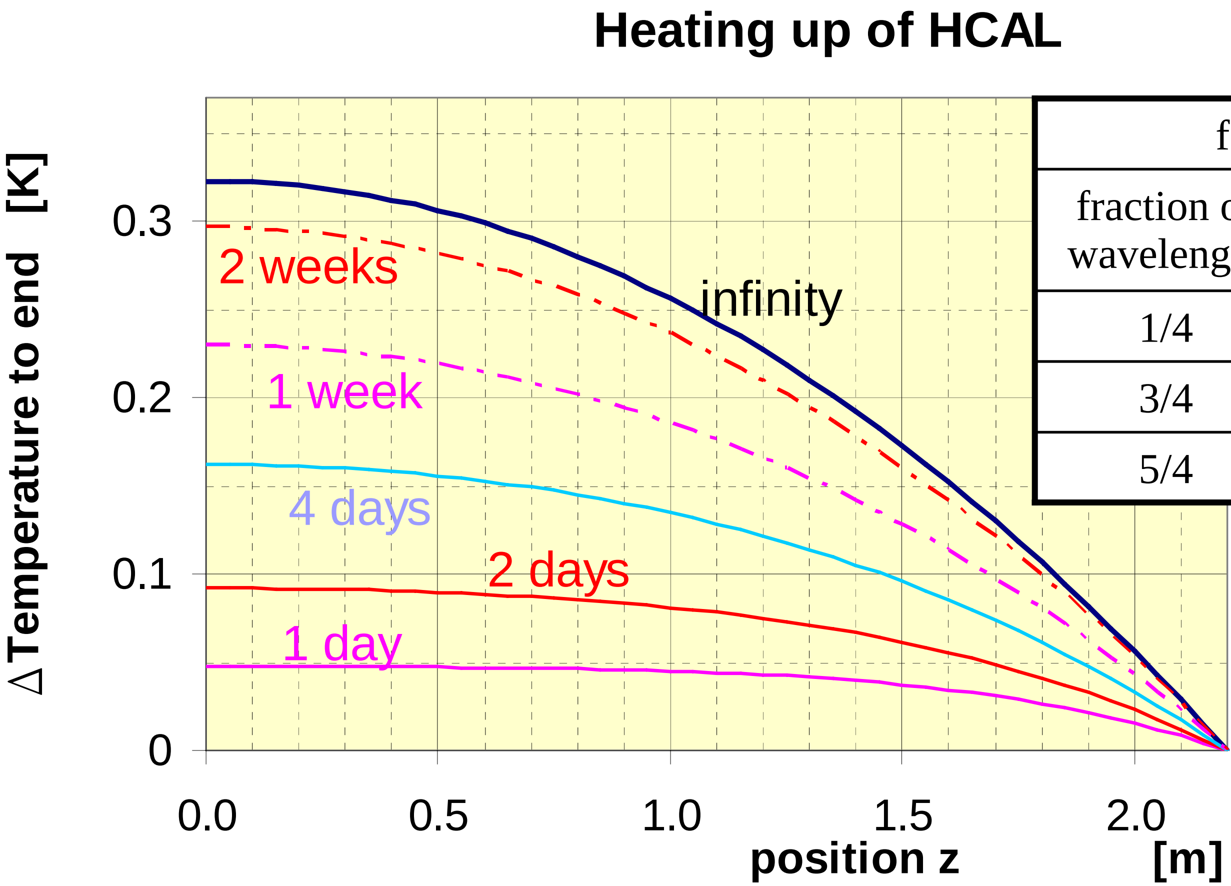
One cooled end, and one with to heat flow: α = (1/4, 3/4, 5/4,....)

$$\tau = \frac{\kappa_{steel} L_{heat}^2}{4\pi^2 \lambda_{steel} \alpha^2}$$

Slowest component (α=1/4) :

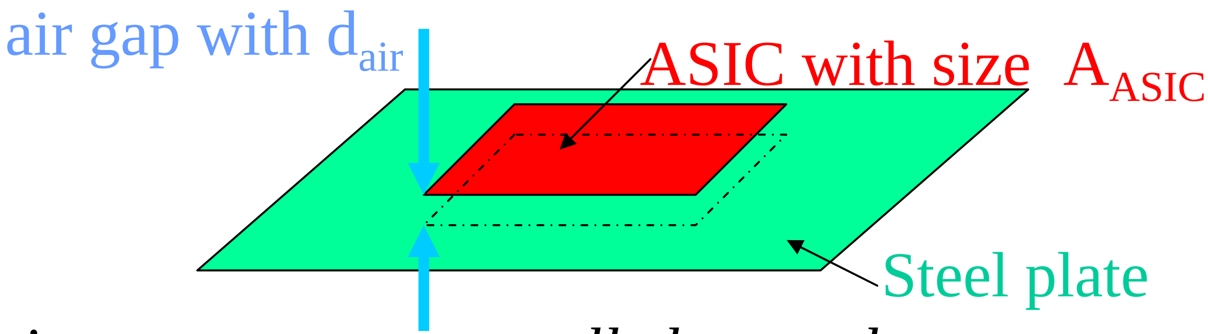
τ = 5.6 days

Heating HCAL



fourier components		
fraction of wavelength	time constant	relative amplitude
1/4	5.6 days	+ 103%
3/4	0.6 days	- 4%
5/4	0.2 days	+1%

Heat transfer: ASIC to steel



Basic parameters: *not really known, but to get a guess:*

λ_{air}= 24mW/Km (Nitrogen)

A_{ASIC}= 4cm^2

d_{air}=1mm

P_{ASIC}=(64channel)*P_{chan}=1.6mW

Temperature difference at air gap:
without convection (small gap)

$$\Delta T_{gap} = \frac{1}{\lambda_{air}} P_{ASIC} \frac{d_{air}}{A_{ASIC}}$$

$\Rightarrow$ ΔT_{gap} = 0.2K OK!!!!!

Charge storage for pulsed operation

Boundary conditions:

Bunch train of 0.6ms every 200ms:

- power down the "hungry" electronics
- store enough charge locally, to reduce cables out of ILC-detector and EMI-problems

⇒ Store the charge at the end of the gap on data concentrator

- minimize components and heating inside the gap

Basic parameters:

P_{chan}=25μW/channel (ASIC)

N_{chan}=1000/m^2

A_{plane}=2m^2 (typically)

R_{train}=5Hz (repetition rate)

T_{train}=1ms (switch on time)

V_{pulsed}=3.3V (operation voltage of ASIC)

Required charge / current

Charge for train:

$$Q_{train} = \frac{P_{chan}}{V_{pulsed} R_{train}} N_{chan} A_{plane} \quad = 3\text{mC/(train plane)}$$

Current during train:

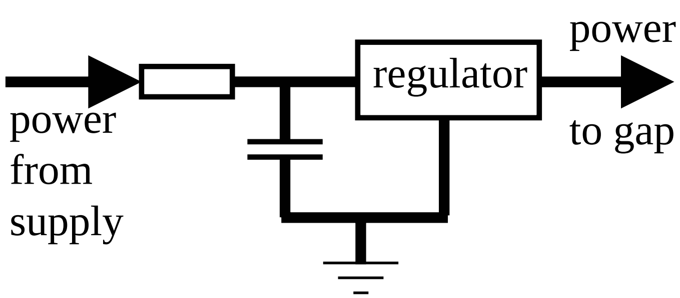
$$I_{train} = \frac{Q_{train}}{T_{train}} \quad = 3\text{A/plane}$$

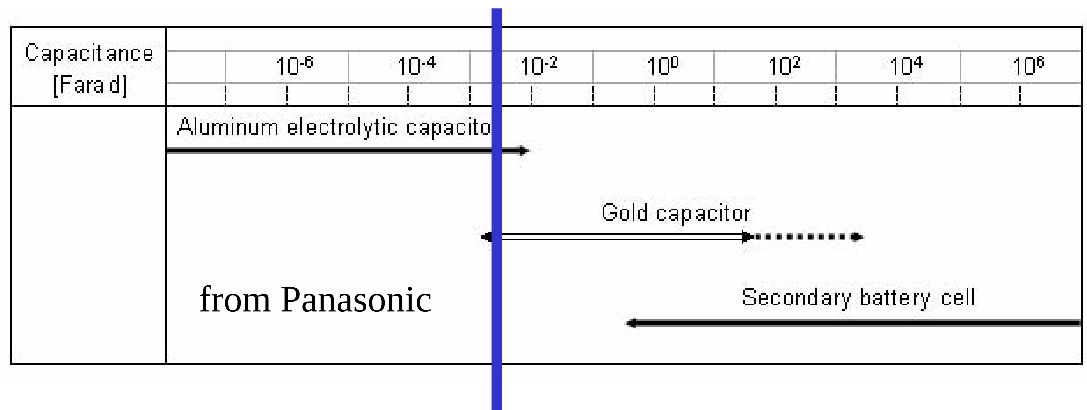
→ Values do not look critical,
but to be handled with a some effort

Straight forward solution

Idea: Store the charge at end of the gap in data concentrator
put a voltage regulator before the current enters the gap
avoid fast current jumps on the cables to power supply

Available capacitors:





3.3mF=7·470µF

7 capacitors á 470μF (7.3mm*4.3mm*4.5mm) are sufficient
discharge voltage drop 0.5V , so additional heat is small
Stored local energy is small: 0.2J/plane , no risk of fire

Lots of details and other concepts to be evaluated

Power: Just first step, What else?

Lots of details and other concepts to be evaluated

Not touched at all:

- Waves inside Power-GND system
  Large planes: 2.2m$\times$1m:
  λ=2.2m is equivalent to ν=90MHz
- Current transfer inside the gap
- What is needed locally at ASIC?
  Is ASIC/SiPM/PCB sensitive?
- Regulator for fast reaction

$\Rightarrow$ Lot of work inside that work package

Outlook

Heating:

- Active electronics in the gap is no heat problem

  but keep eyes open for updates on power, pad size,
- Heat flows to end of gap, where it has to be cooled

Power for pulsed operation:

- energy storage for pulsed operation is feasible

  Not touched: Lot of items

It looks promising for going ahead

Lot of work will be needed for details