first results of

HaRDROC

Hadronic Rpc Detector Read-Out Chip

IN2P3/LAL+IPNL+LLR

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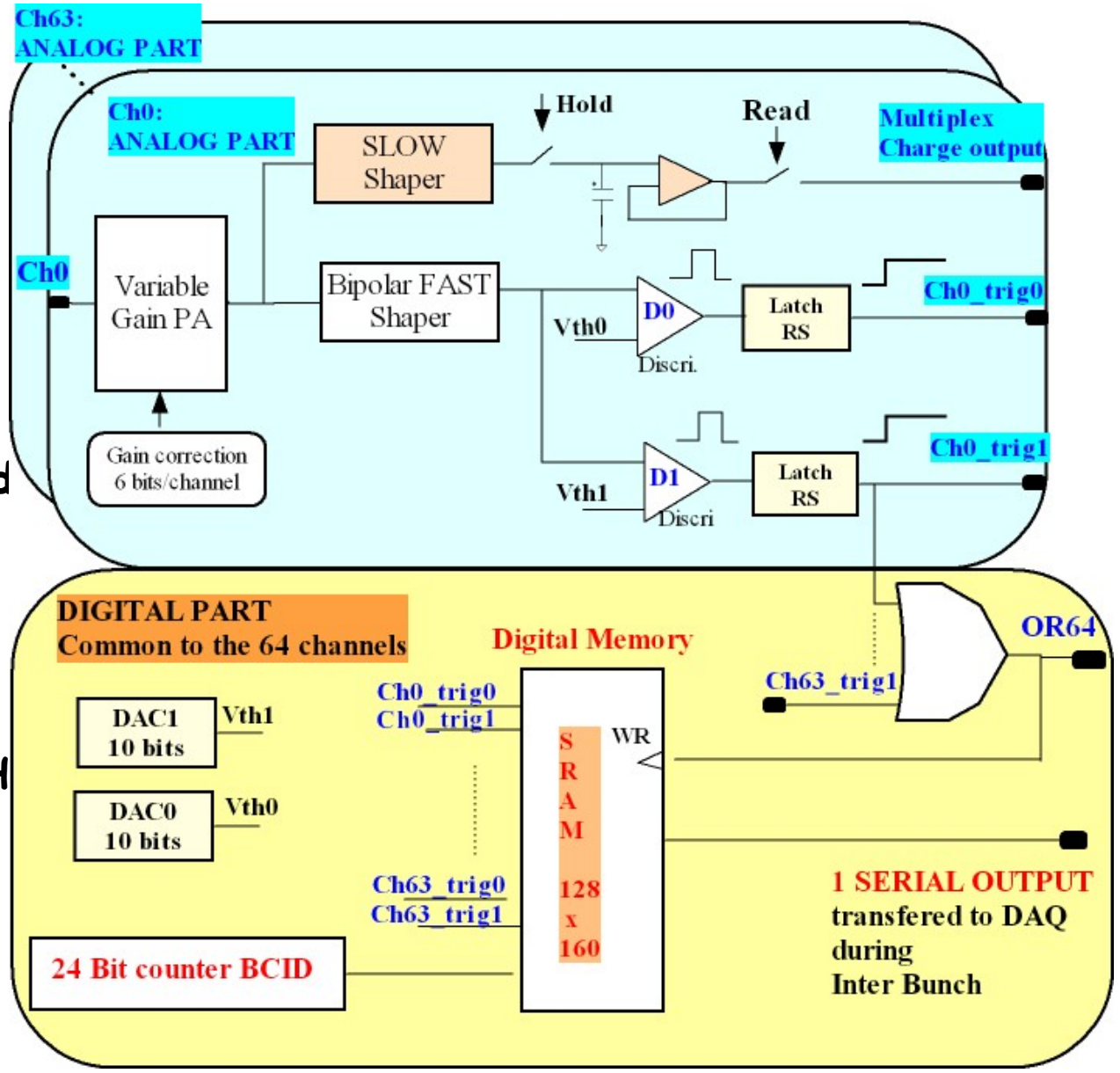
It is gonna heat, hopefully, there is the power pulsing

© Rammstein, J Fleury

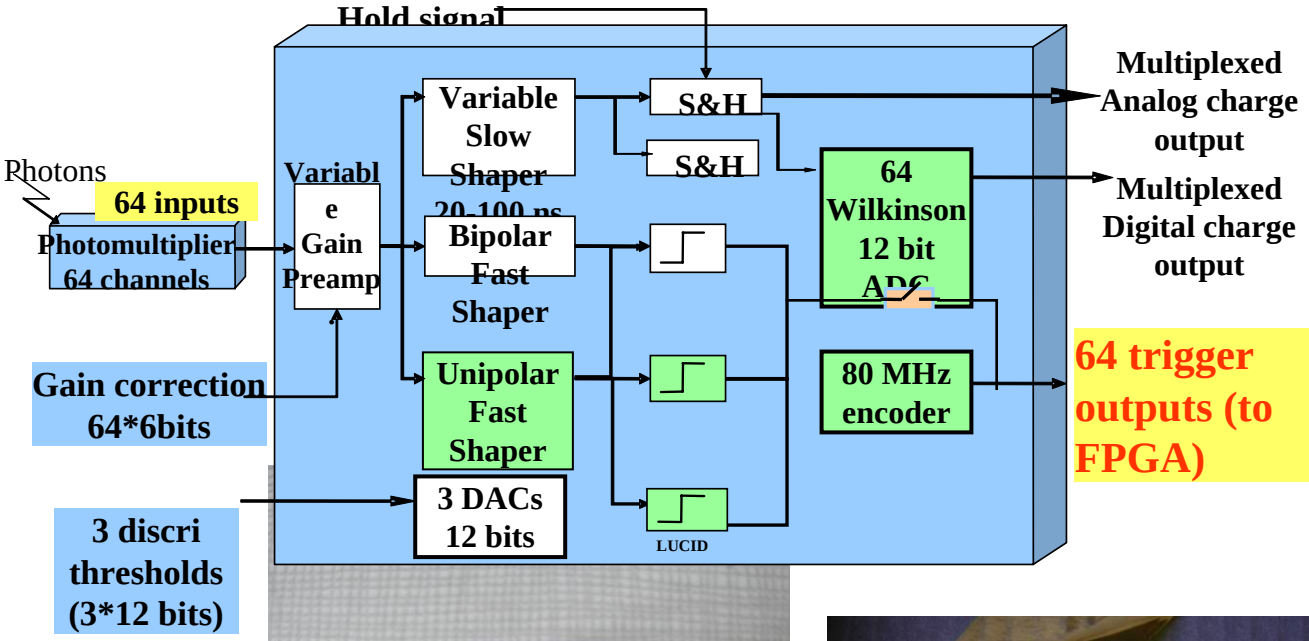
HaRDROC architecture

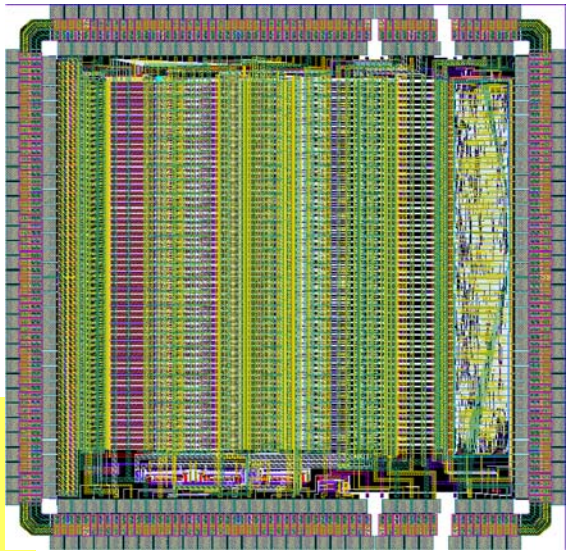
- Full power pulsing
- Digital memory: Data saved during bunch train.
- Only one serial output @ 5MHz
- Store all channels and BCID for every hit. Depth = 128 bits
- Data format : 128(depth)*[2bit*64ch+24bit(BCID)+8bit(Header)] = 20kbits
- Based on MAROC ASIC, but several design changes

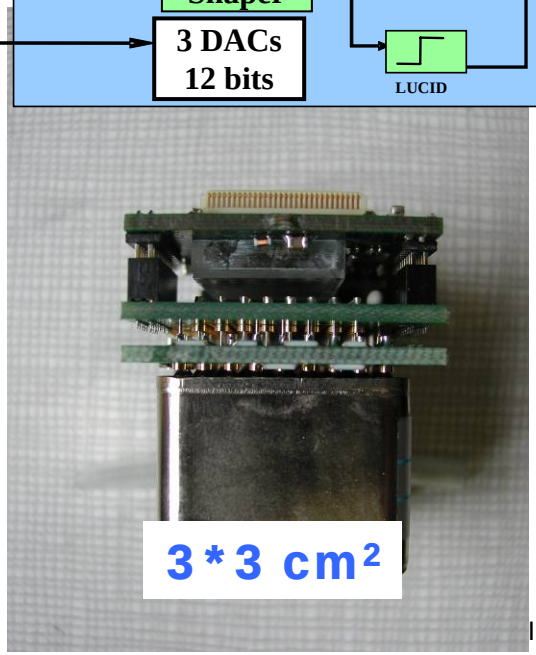


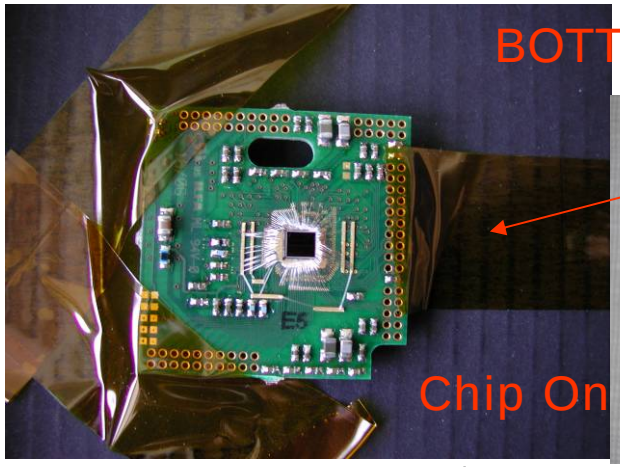
MAROC 'Multi-Anode Readout Chip' for ATLAS lumi

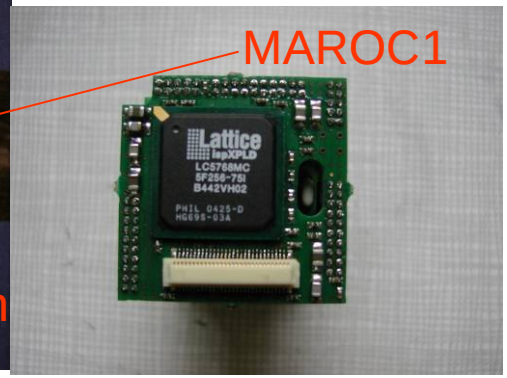
- **Complete front-end chip for 64 channels multi-anode photomultipliers**
  - Auto-trigger on 1/3 p.e. at 10 MHz, 12 bit charge output
  - SiGe 0.35 µm, 12 mm2, Pd = 350mW



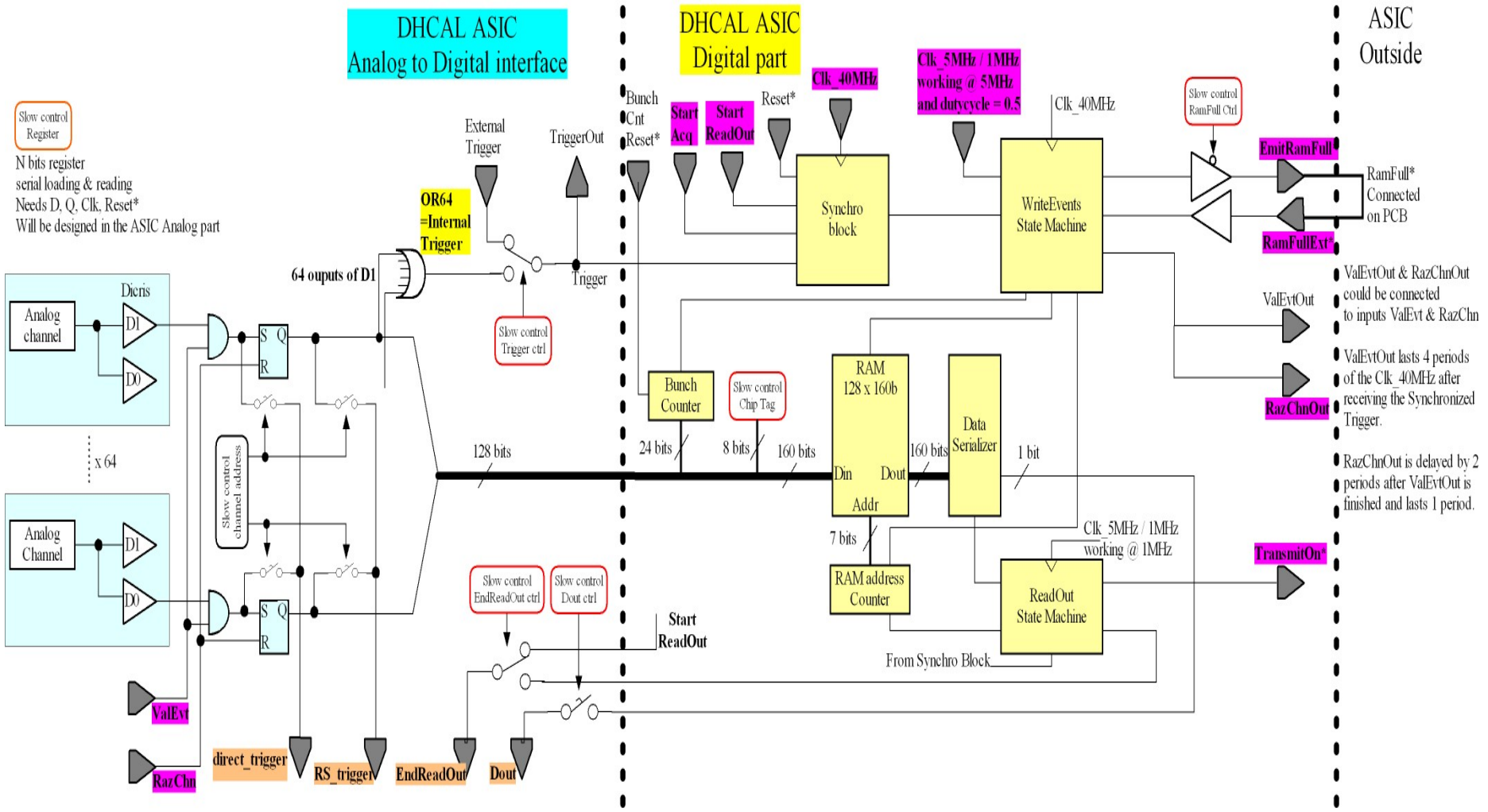






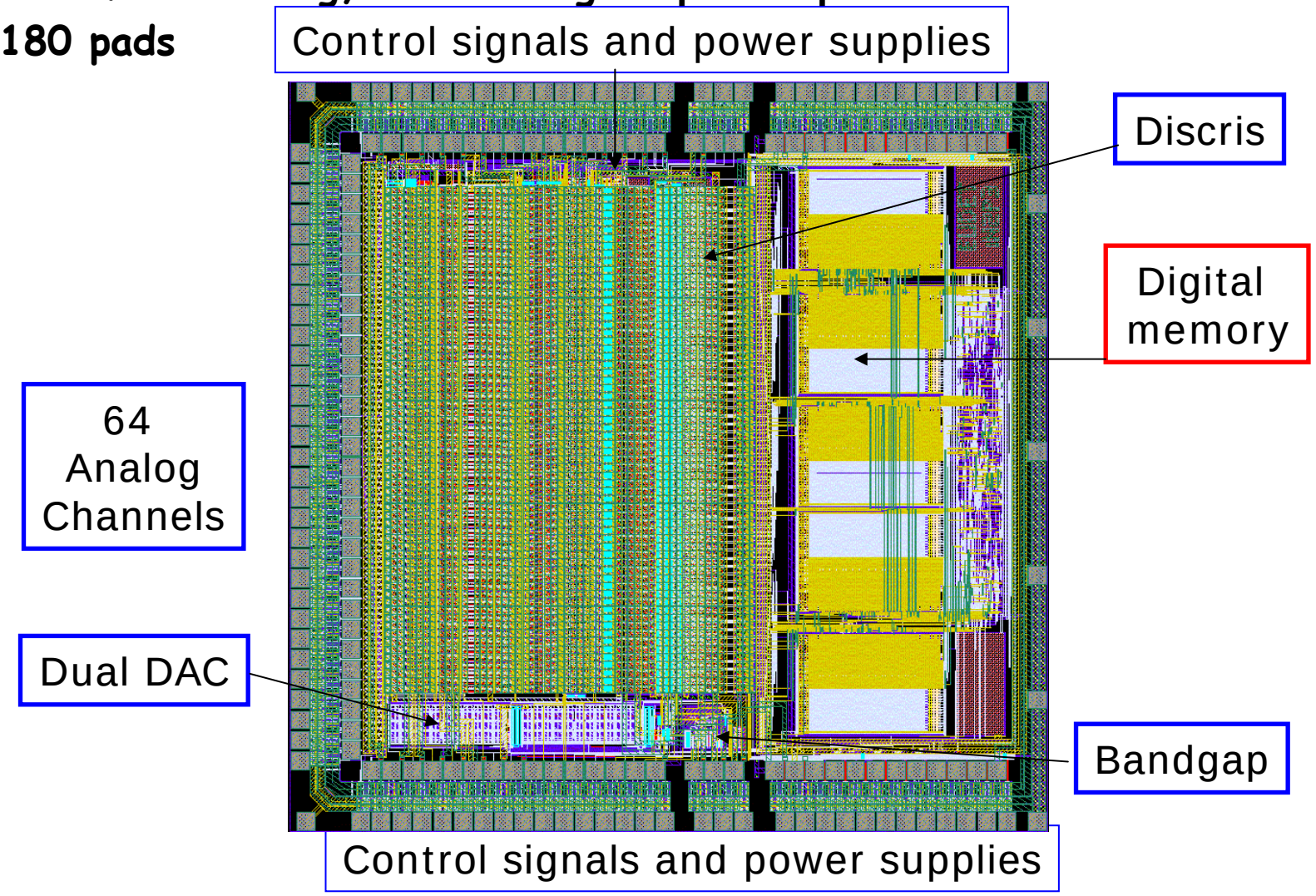


HARDROC1: digital part



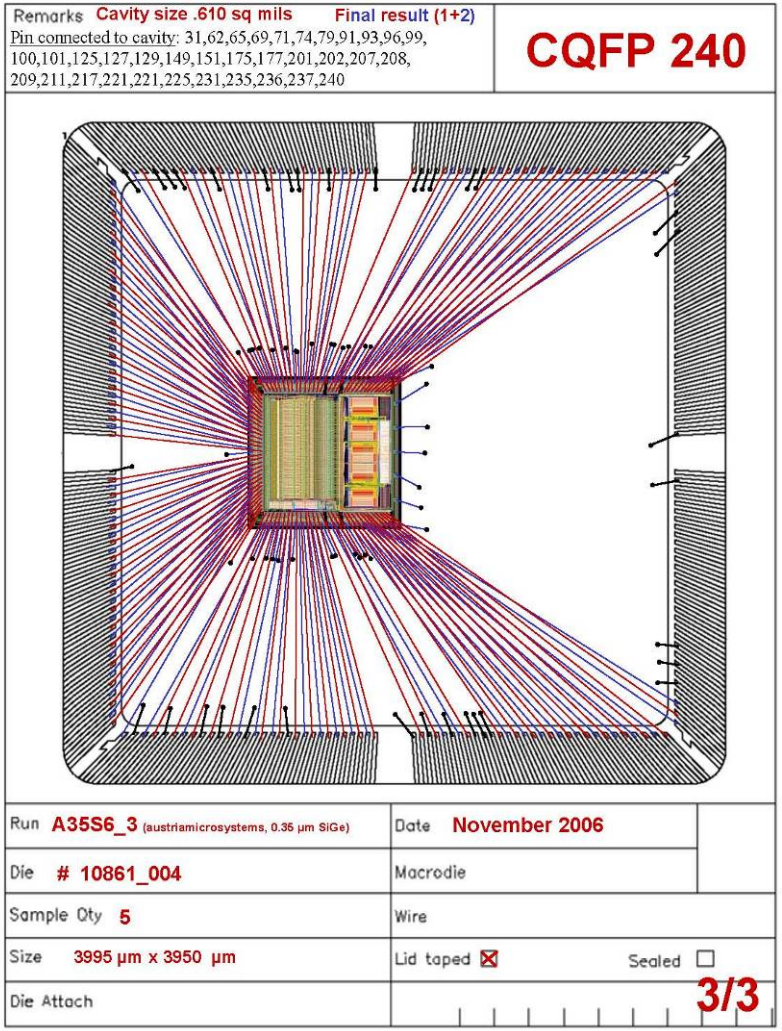
HaRDROC layout (SiGe technology)

- 64 inputs, 1 data output
- Vss of the analog, mix and digital part separated
- 180 pads

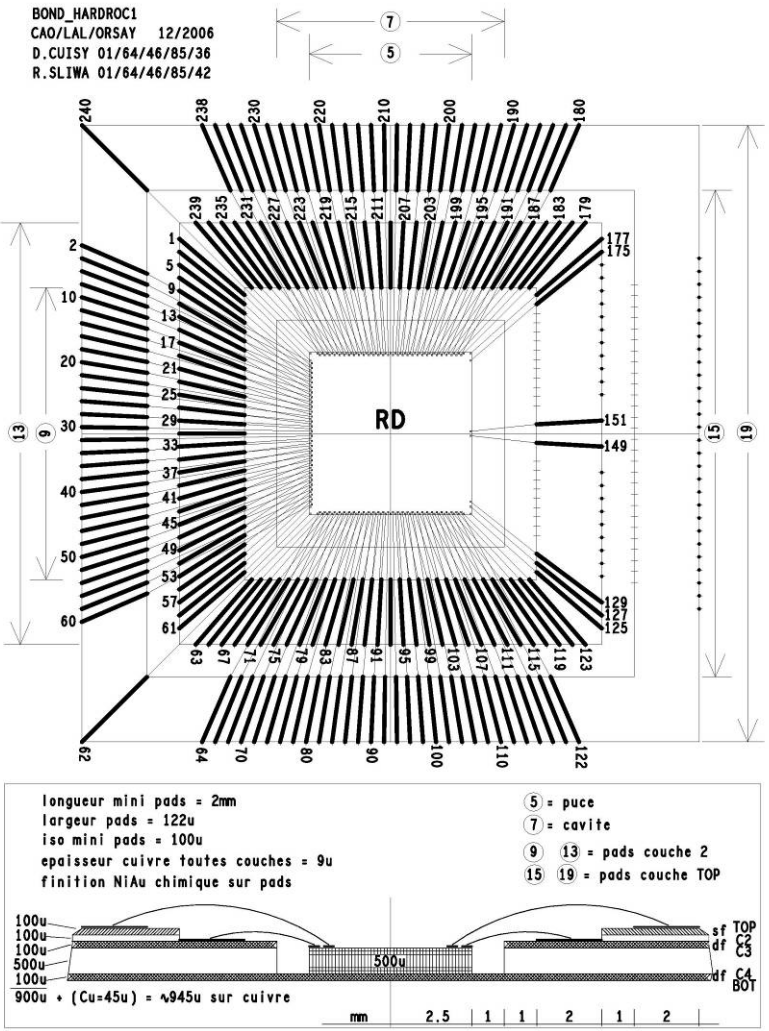


Bonding of Hardroc1

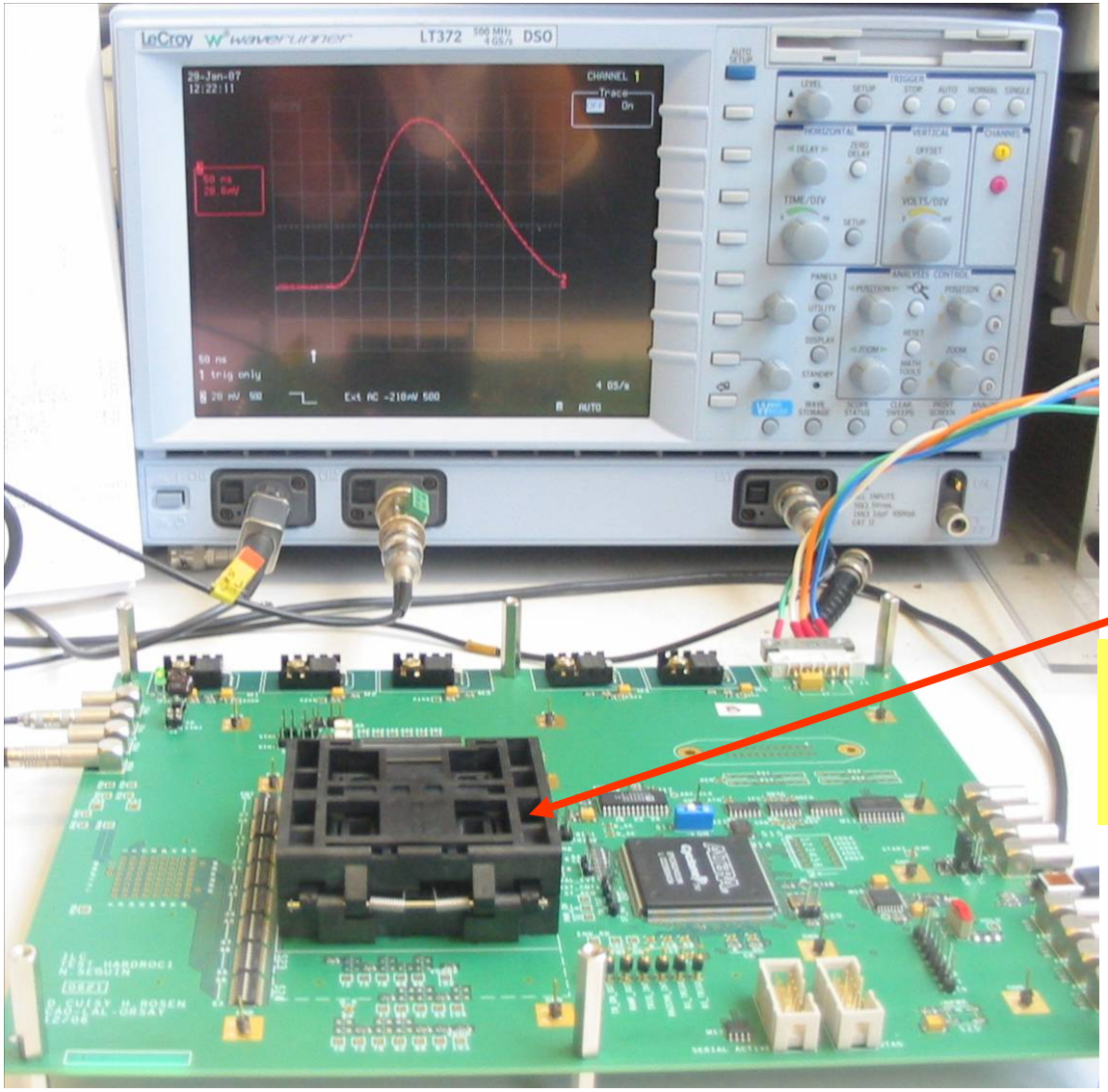
CQFP240 package

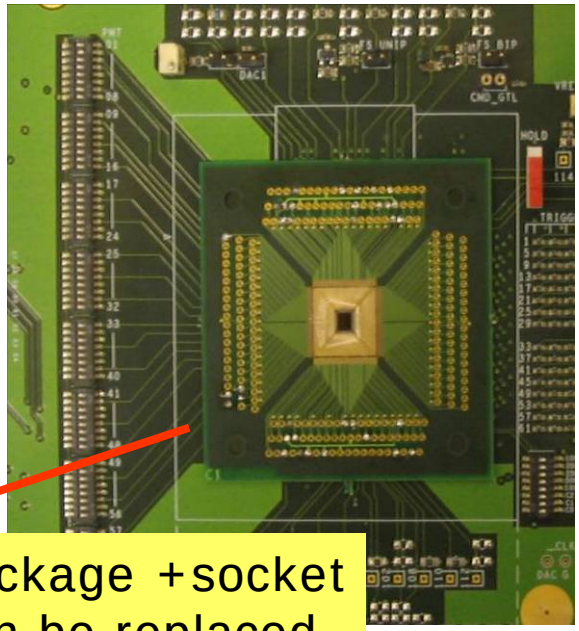


Chip On Board



HARDROC1: TESTBOARD with chip packaged



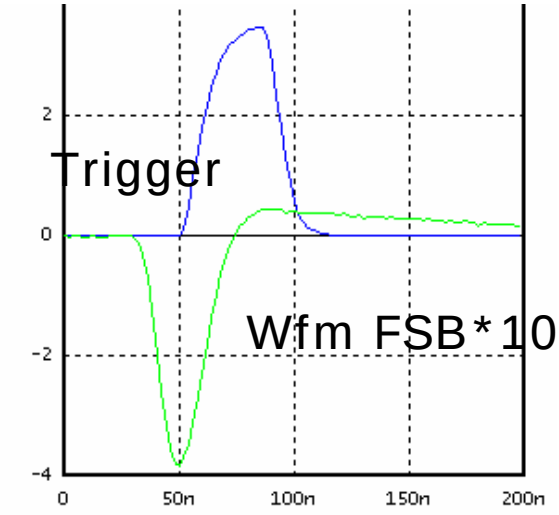


Package +socket can be replaced by COB version

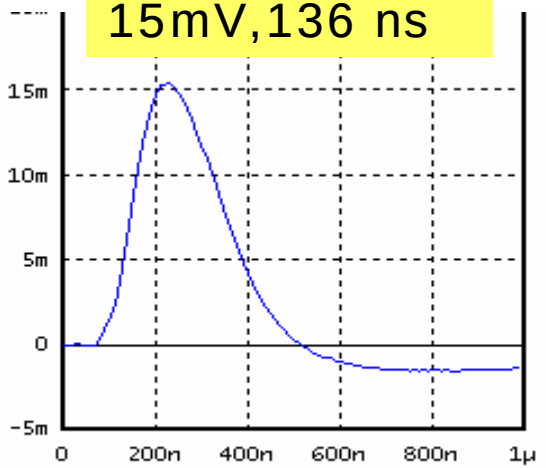
HARDROC1: First measurements

- DC points: OK
- Noise OK despite the CK40MHz in the chip
- DC value of FSB output measured on the 64 channels:
  <>=2V, σ=1.3mV
- DC_SS of the 64 Ch.
  <>=1.10V σ=1.9mV
- Trigger down to 10-30 fC

FSB with Qin=30 fC

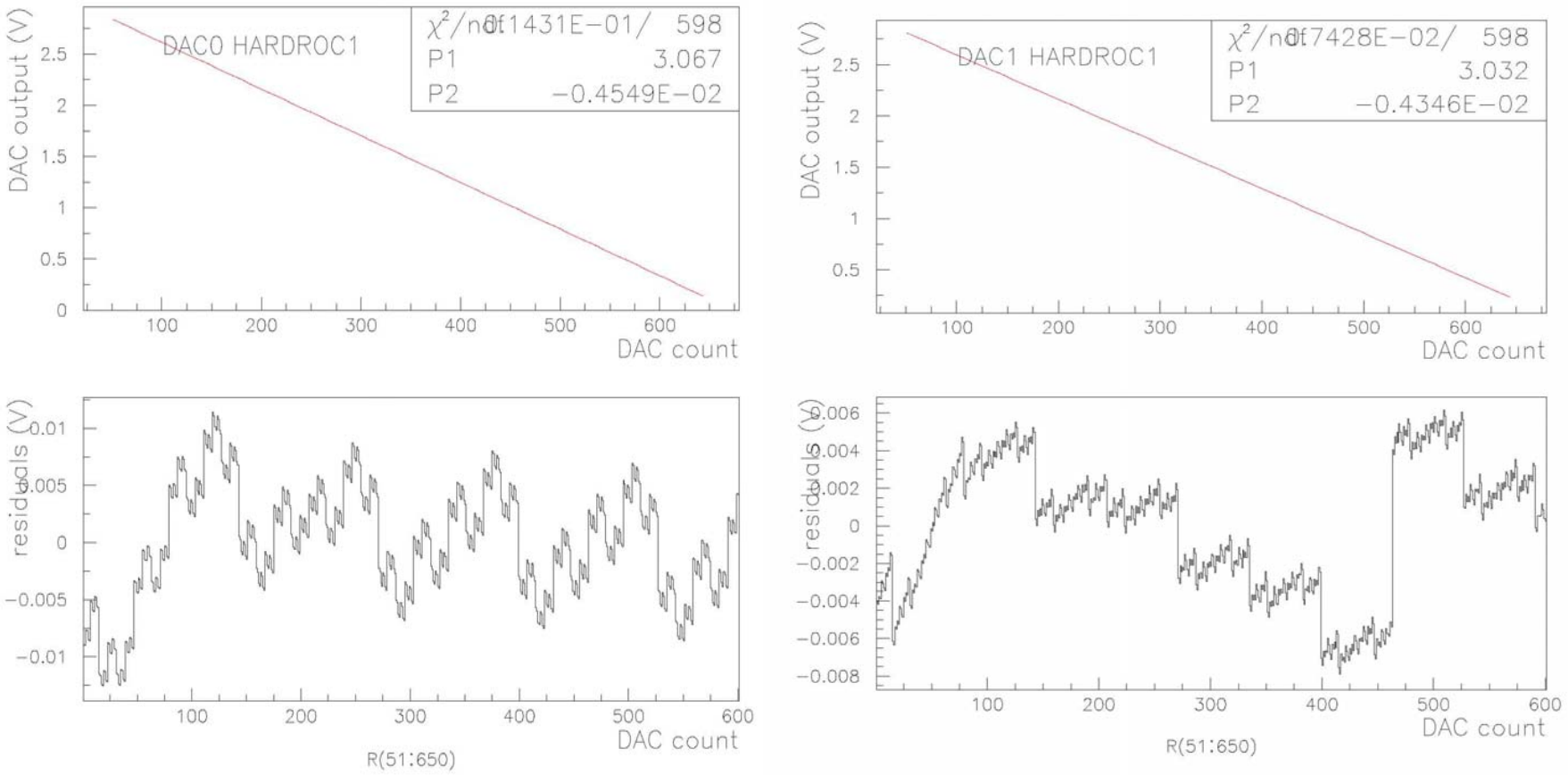


SS: Qin=100fC
15mV,136 ns



HARDROC1: Integrated DACs linearity

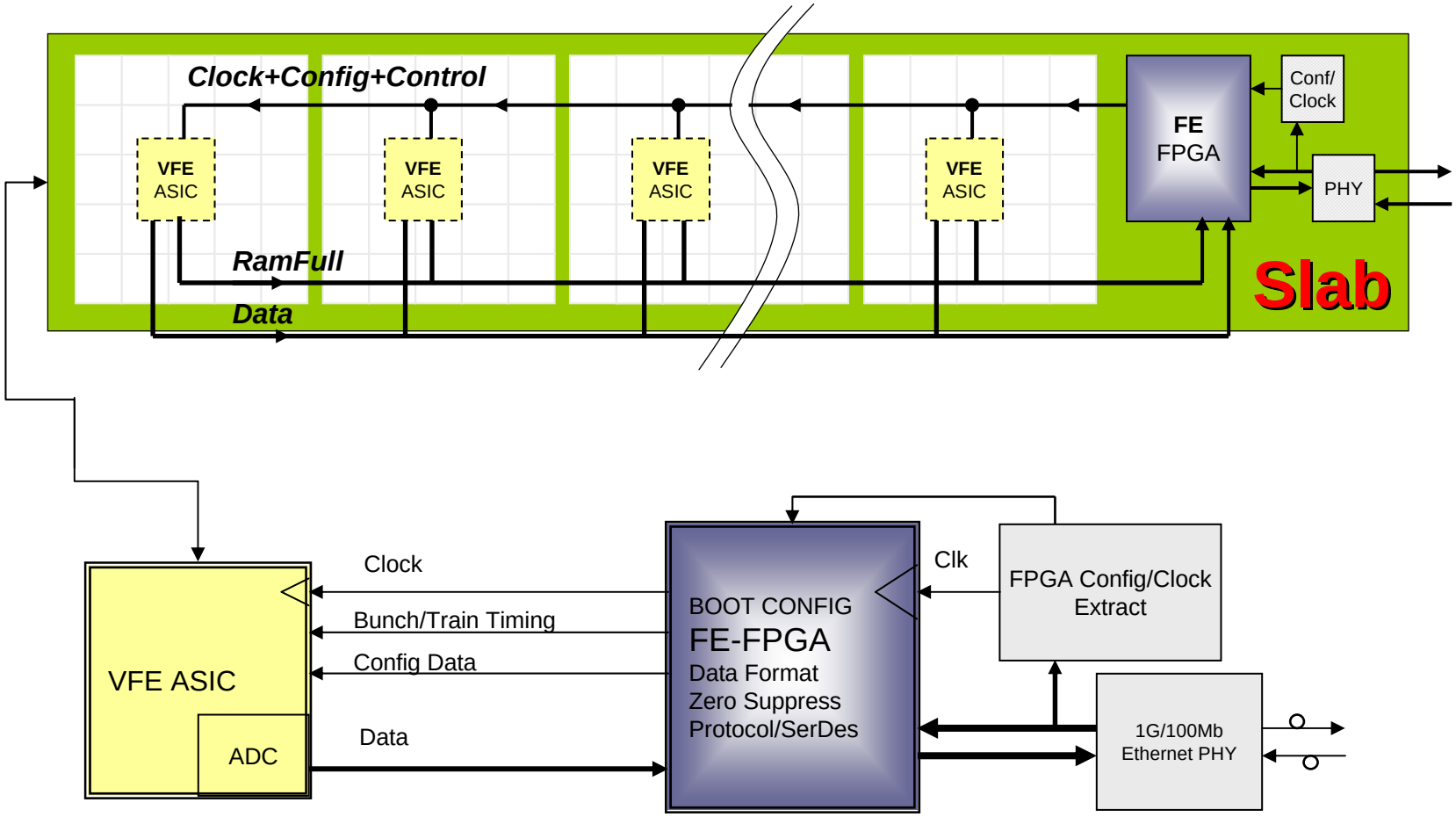
- 2 integrated DACs to deliver Threshold voltages
- Residuals within ±10 mV / 3V dynmaic range



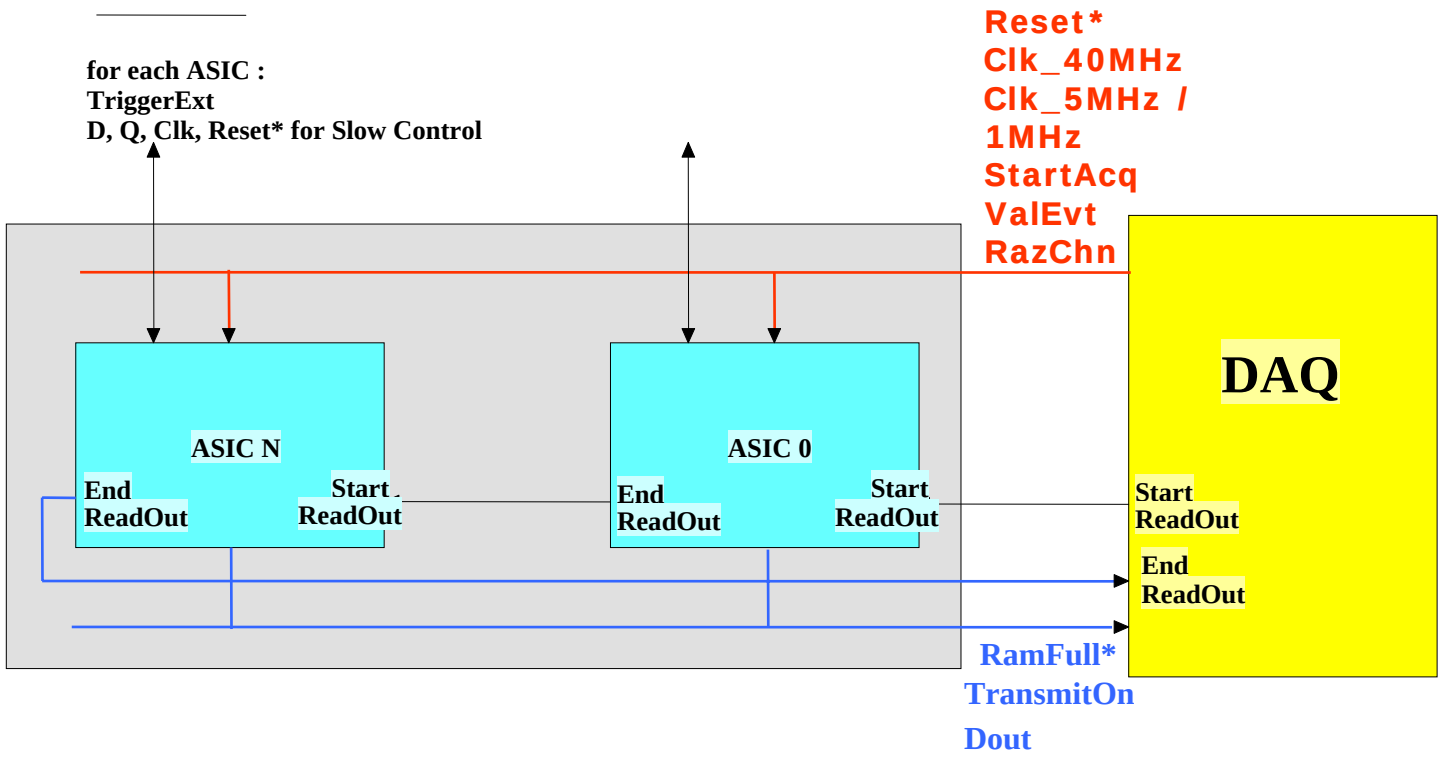
Digital architecture towards 2nd generation DAQ

ECAL, AHCAL, DHCAL

detector readout

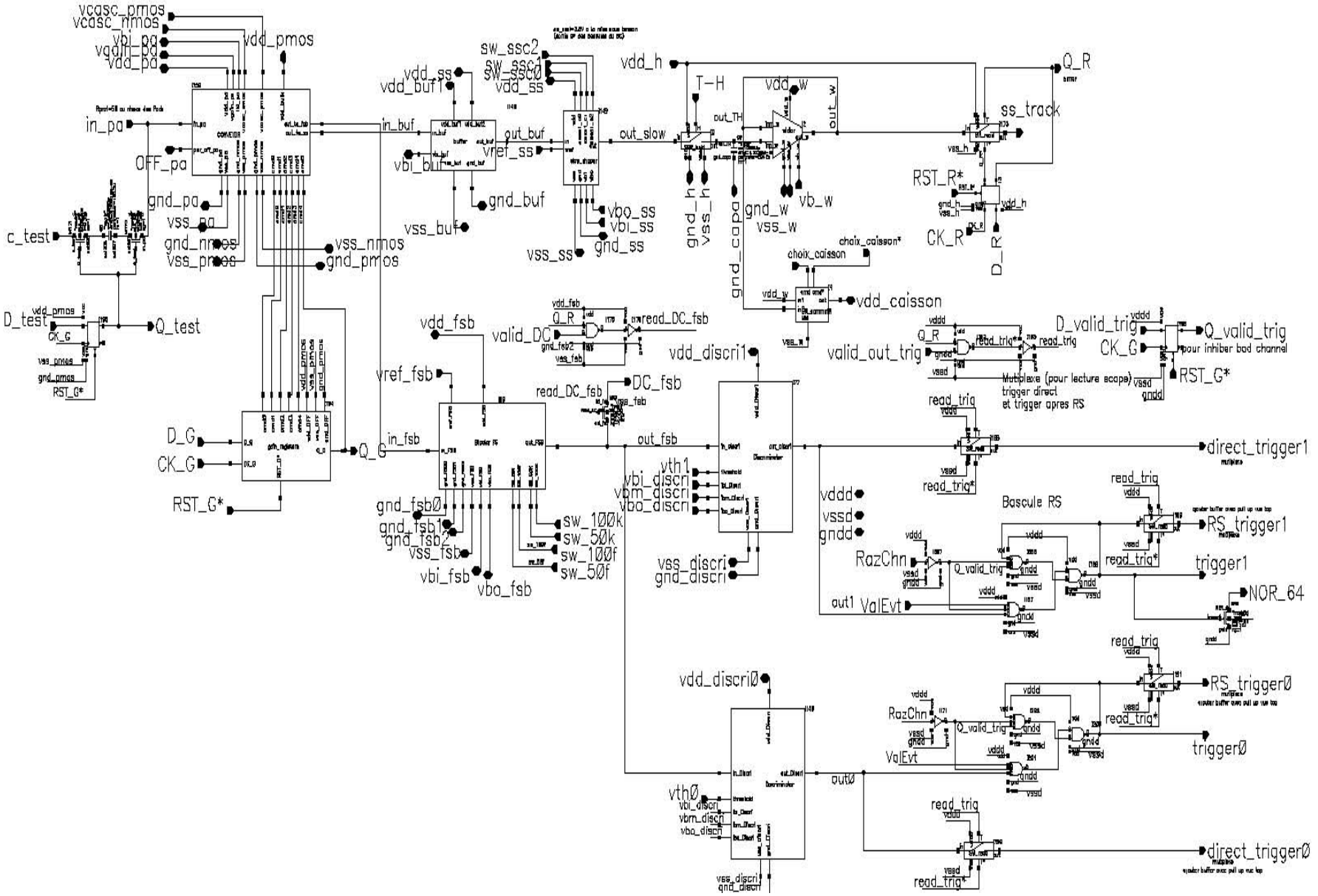


Digital signals

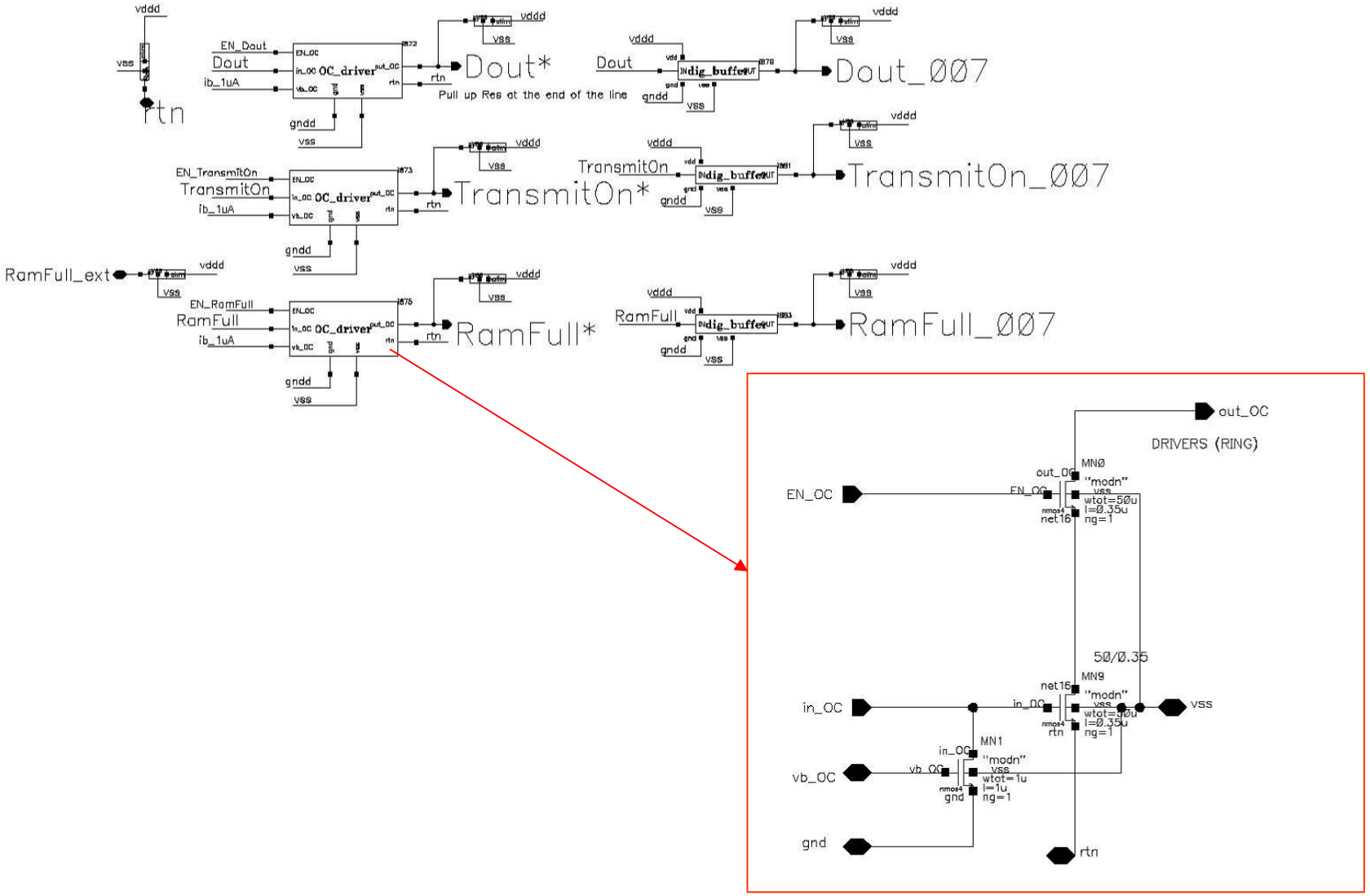


Signal name	INPUT/OUPUT	Valid on	Common	Adaptation	Single/Diff
Reset*	INPUT	LOW	YES	YES	SINGLE
Clk_5MHz / 1MHz	INPUT	RISING	YES	YES	DIFF
Clk_40MHz	INPUT	RISING	YES	YES	DIFF
StartAcq	INPUT	HIGH	YES	YES	SINGLE
ValEvt	INPUT	HIGH	YES	YES	DIFF
RazChn	INPUT	HIGH	YES	YES	DIFF
StartReadOut	INPUT	HIGH	NO	NO	SINGLE
EndReadOut	OUTPUT	HIGH	NO	NO	SINGLE
TransmitOn	OUTPUT	HIGH	YES	YES	SINGLE
Dout	OUTPUT	-	YES	YES	SINGLE
RamFull*	BIDIR	LOW	YES	YES	SINGLE
TriggerExt	INPUT	RISING	NO	NO	SINGLE
TriggerOut	OUTPUT	RISING	NO	NO	SINGLE

ONE_CHANNEL


vcasc_pmos
vcasc_nmos
vbi_pa
vdd_pa
vdd_pmos
in_pa
OFF_pa
gnd_pa
vss_pa
gnd_nmos
vss_pmos
vss_nmos
gnd_pmos
c_test
D_test
Q_test
vdd_pmos
CK_G
vss_pmos
gnd_pmos
RST_G*
D_G
CK_G
RST_G*
Q_G
vdd_ss
vdd_buf1
in_buf
vbi_buf
vss_buf
gnd_buf
out_buf
vref_ss
sw_ssc2
sw_ssc1
sw_ssc0
vdd_ss
vbo_ss
vbi_ss
gnd_ss
vss_ss
out_slow
vdd_h
T-H
vdd_w
out_TH
out_w
gnd_h
vss_h
gnd_capa
gnd_w
vss_w
vb_w
ss_track
Q_R
RST_R*
CK_R
D_R
choix_caisson*
choix_caisson
vdd_caisson
vdd_fsb
valid_DC
read_DC_fsb
vref_fsb
DC_fsb
in_fsb
out_fsb
gnd_fsb0
gnd_fsb1
gnd_fsb2
vss_fsb
vbi_fsb
vbo_fsb
sw_100k
sw_50k
sw_100f
sw_50f
vdd_discri1
vth1
vbi_discri
vbm_discri
vbo_discri
vss_discri
gnd_discri
valid_out_trig
D_valid_trig
CK_G
Q_valid_trig
pour inhiber bad channel
RST_G*
Multiplexe (pour lecture acapo)
trigger direct
et trigger apres RS
read_trig
read_trig*
direct_trigger1
vddd
vssd
gndd
Bascule RS
RS_trigger1
trigger1
RazChn
Q_valid_trig
ValEvt
out1
NOR_64
vdd_discri0
vth0
out0
RS_trigger0
trigger0
direct_trigger0

Bussed Digital Signals (Outputs)



PINOUT of Hardroc1

pin number	pin name	connect to	DC voltage	DC Current	Bias
1	in<2>	detector	0.8V		
29	in<30>	detector			
30	in<31>	detector			
31	**gnd_pa**	**gnda**			
32	in<32>	detector			
60	in<60>	detector			
61	in<61>	detector			
62	**vssi**				
63	in<62>	detector			
64	in<63>	detector			
65	**gnd_pa**	**gnda**			
66	**vdd_pad**		3,5V		
67	**vdd_pa**	**vdda**	3.5V		connected to 231
68	ctest				

PINOUT of Hardroc1

69	**gnd_nmos**				
70	vcasc_pmos		1V		divider 1K,2.5K
71	**vssa**				
72	vcasc_nmos		1,5V		divider 1.5K,2K
73	**vdd_buf1**				
74	**gnd_buf**	**gnda**			
75	**vdd_pmos**				
76	ibi_otadac		0.8V	178uA	100K to gnd_bg
77	**vdd_dac**				
78	ibo_otadac		0.6V	28uA	1K to gnd_bg
79	**gnd_dac**				
80	***Q_R***				LVTTL ASIC input
81	***hold***				LVTTL ASIC input
82	vcasc_dac		1V		divider (10K,25K)
83	***D_R***				LVTTL ASIC input
84	iref_dac		0.5V	13uA	150K to v_bg
85	***CK_R***				LVTTL ASIC input
86	vref_otadac		2V		(200K,50K) to v_bg
87	***rst_R****				LVTTL ASIC input

PINOUT of Hardroc1

88	**vdd_bg**				
89	pwr_on_dac				Slow Control
90	ibi_otabg		2.6V	25uA	100K to gnd_bg
91	**gnd_bg**				
92	ibo_otabg		2,5V	2.5mA	1K to gnd_bg
93	**vssa**				
94	vth0				
95	**vdd_d0**				
96	**gnd_d**				
97	**vdd_d1**				
98	vth1				
99	**vssm**				
100	**vssd**				
101	**gndd**				
102	**vddd2**				
103	**vddd**				
104	ib_rec		0.8V	106uA	25K to vddd
105	***pwr_on_d***				LVTTL ASIC input

PINOUT of Hardroc1

106	***Val_Evt***				LVDS ASIC input (from DAQ)
107	***Val_Evt****				
108	***out_RazChn_int***				LVTTL ASIC output
109	***rst****				LVTTL ASIC input
110	***Raz_Chn***				LVDS ASIC input
111	***Raz_Chn****				
112	***CK_40M***				LVDS output (from DAQ)
113	***CK_40M****				
114	***CK_5M***				LVDS output (1/8 de 40M)
115	***CK_5M****				
116	***out_trig_int***				LVTTL ASIC output (NOR64 or ext)
117	***trigger_ext***				LVTTL ASIC input
118	***End_ReadOut***				LVTTL ASIC output
119	***Start_ReadOut***				LVTTL ASIC input
120	NC1				
121	***Start_Acq***				LVTTL ASIC input
122	**vddd2**				
123	***rst_counter****				LVTTL ASIC input

PINOUT of Hardroc1

124	NC				
125	**vssd**				
126	NC				
127	**vssd**				
128	NC				
129	**vssd**	**gndd**			
130	NC				
131…	NC				
...148	NC				
149	**vssd**				
150	NC				
151	**vssd**				

PINOUT of Hardroc1

152…	NC				
…174	NC				
175	**vssd**				
176	NC				
177	**vssd**				
178	NC				
179	**vddd2**				
180	NC				
181	**rtn**	**rtn**			DC=0 ou 0,5V
182	***RamFull_ext***				LVTTL ASIC input
183	***RamFull****				OC ASIC output : LVTTL (testboard)
184	RamFull_007				Test point (NC to DAQ)
185	***Dout****				OC ASIC output : LVTTL (testboard)
186	Dout_007				Test point (NC to DAQ)
187	***TransmitOn****				OC ASIC output : LVTTL (testboard)
188	TransmitOn_007				Test point (NC to DAQ)
189	***rst_SC****				LVTTL ASIC input

PINOUT of Hardroc1

190	***Q_SC***				LVTTL ASIC input
191	***D_SC***				LVTTL ASIC input
192	***out_RS_trig1***				LVTTL ASIC output (to DAQ)
193	***CK_SC***				LVTTL ASIC input
194	***out_RS_trig0***				LVTTL ASIC output (to DAQ)
195	***pwr_on_ss***				LVTTL ASIC input
196	out_trig1				LVTTL ASIC output (Lemo)
197	***pwr_on_a***				LVTTL ASIC input
198	out_trig0				LVTTL ASIC output (Lemo)
199	**vddd**				
200	**vddd2**				
201	**gndd**				
202	**vssd**				
203	**vdd_d2**	**guard ring for discriminators**			
204	ibi_d		0.8V	27uA	100K to vdda
205	ibm_d		2.5 V	25uA	100K to gnd
206	ibo_d				100K to gnd

PINOUT of Hardroc1

207	**gnd_d**				
208	**vssm**				
209	**vssa**				
210	v_bg		2,5V		
211	**gnd_fsb1**				
212	out_fsb				
213	vref_fsb		2V		(2.7K external in //2.2K,300) to v_bg
214	ibo_fsb		2.3V	22uA	100k to gnd
215	**vdd_fsb**				
216	ibi_fsb		2.4V	41uA	60K to gnd
217	**gnd_fsb0**				
218	out_Q				
219	**vdd_w**				
220	ib_otaq		1V	450uA	5592 to vdd
221	**gnd_w**				
222	**gnd_capa**				
223	EN_otaq				

PINOUT of Hardroc1

224	ib_w		0.8V	11uA	25K to vdd
225	**gnd_ss**				
226	ibo_ss		0.8V	10.7uA	25k to vdd
227	**vdd_ss**				
228	ibi_ss		0.8V	10.7uA	25K to vdd
229	vref_ss		1,1V		(11K,14K) to v_bg
230	ib_buf				50K to vdd
231	**gnd_nmos**				
232	vgain_pa		3.5V		300//300 to vdd
233	**vdd_pa**				
234	ib_pa		0.7V	6uA	500K to vdd
235	**vssa**				
236	**vssi**				
237	**gnd_pa**				
238	in<0>	detector			
239	in<1>	detector			
240	**vssi**				

Slow Control of Hardroc1

CELL	BIT#	BIT NAME
Dig_bias	1	EN_RamFull
	2	EN_Dout
	3	EN_TransmitOn
	4	EN_out_discri
	5	Header 0
	6	Header 1
	7	Header 2
	8	Header 3
	9	Header 4
	10	Header 5
	11	Header 6
	12	Header 7
	13	bypass_chip
	14	EN_out_trig_int
	15	EN_trig_int
	16	EN_trig_ext
	17	EN_out_raz_int
	18	EN_raz_int
	19	EN_raz_ext
	20	Not used

CELL	BIT#	BIT NAME
One_Channel0	21	Valid_trig channel 0
One_Channel1	22	Valid_trig channel 1
	…	…
One_Channel63	84	Valid_trig channel 63
dual_dac_10bits	85	B0 0
	86	B0 1
	…	…
	94	B0 9
	95	B1 0
	96	B1 1
	…	…
	104	B1 9
	105	ON_otadac
	106	ON_dac
	107	ON_otabg
One_Channel0	108	Test ch 0
One_Channel1	109	Test ch 1
	…	…
One_Channel63	171	Test ch 63

Slow Control of Hardroc1

CELL	BIT#	BIT NAME
One_Channel0	172	Preamp gain cmd0 ch 0
	173	Preamp gain cmd1 ch 0
	174	Preamp gain cmd2 ch 0
	175	Preamp gain cmd3 ch 0
	176	Preamp gain cmd4 ch 0
	177	Preamp gain cmd5 ch 0
One_Channel1	178	Preamp gain cmd0 ch 1
	179	Preamp gain cmd1 ch 1
	…	…
	183	Preamp gain cmd5 ch 1
One_Channel2	184	Preamp gain cmd0 ch 2
	185	Preamp gain cmd1 ch 2
	…	…
	189	Preamp gain cmd5 ch 2
	…	…
One_Channel63	550	Preamp gain cmd0 ch63
	551	Preamp gain cmd0 ch63
	…	…
	555	Preamp gain cmd0 ch63

CELL	BIT#	BIT NAME
Bias	556	ON_pa
	557	ON_buf
	558	ON_ss
	559	ON_w
	560	ON_otaq
	561	ON_fsb
	562	ON_discri
	563	Valid_DC
	564	Sw_50f
	565	Sw_100f
	566	Sw_100k
	567	Sw_50k
	568	Choix_caisson
	569	Sw_ssc2
	570	Sw_ssc1
	571	Sw_ssc0

SUMMARY and NEXT STEPS

- **HaRDROC**
  - ASICs received end of December 06
  - Testboard in Orsay to evaluate the analog performance of one HARDROC
  - First analog measurements are in good agreement with expected results
  - 7 testboards have been produced and will be available at the end of February to be sent in labs (IPN Lyon, LLR, Londres, Protvino...)
  - Help is welcome to test the chip, in particular the digital part

- **PCB** (see V. Ammosov presentation)
  - 4 (packaged) HARDROCs to read RPCs
    - => evaluation of the analog and digital part (daisy chain)
    - => PCB design
  - Similar PCB development for ECAL (see Annexe)