Status and plans for DHCAL in Europe

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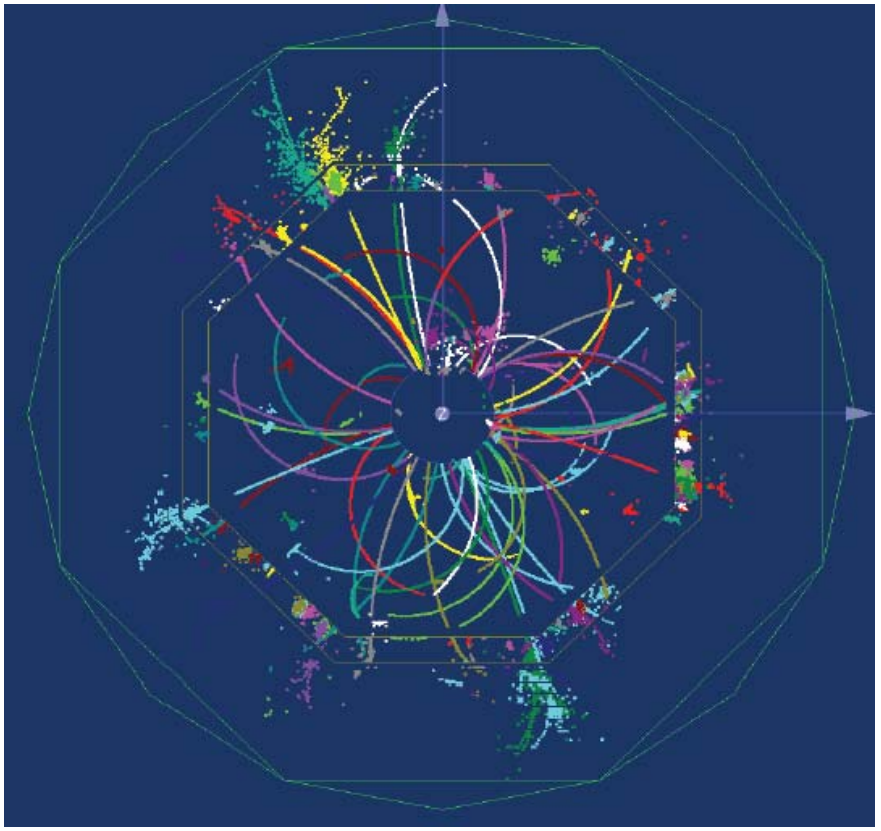
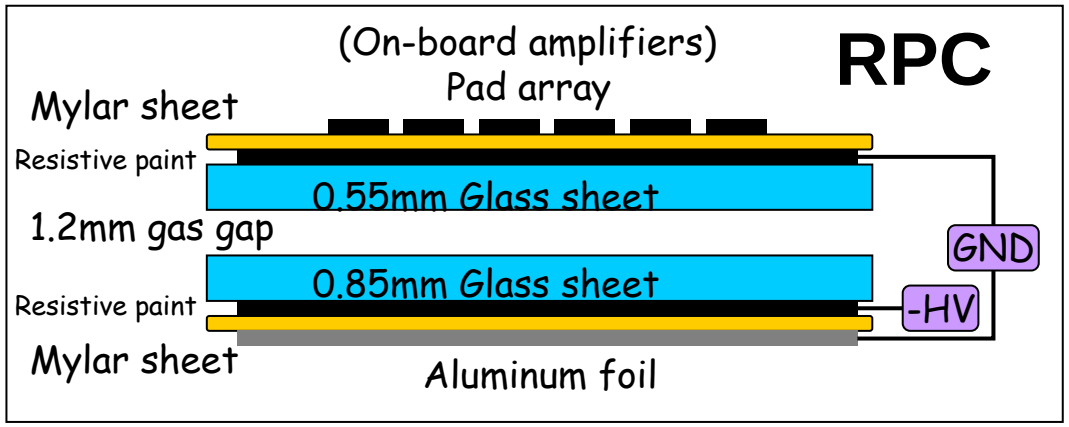
IHEP, Protvino

DHCAL motivation for ILC

- **Particle Flow Approach requires high longitudinal and transverse granularity in calorimetry for precise jet measurement**
- **It implies highly segmented steel sandwich calorimeter (HCAL) for hadrons**
- **Digital Hadron Calorimeter (DHCAL) may provide fine segmentation (~1cm^2) with simplest read out system which is enough for neutral hadron pattern recognition and μ ID**

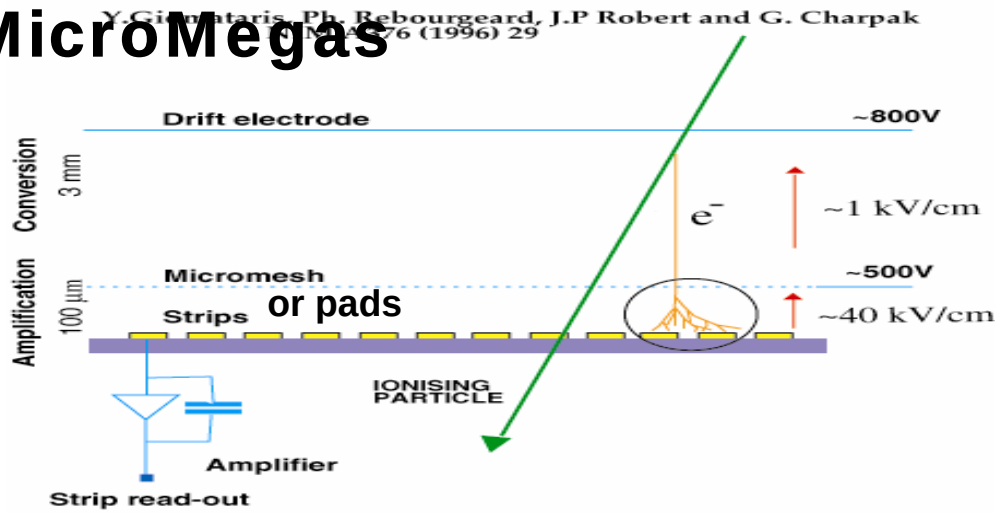


Gaseous active medium candidates



IHEP (Protvino) + collaborators

MicroMegas

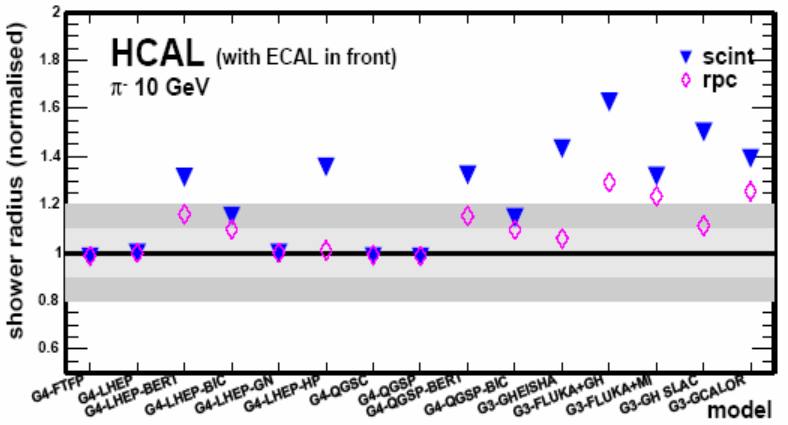


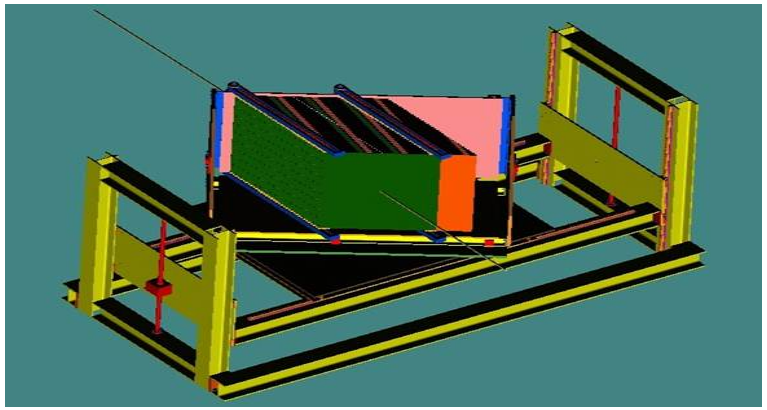
LAPP (Annecy) + collaborators

1m^3 DHCAL prototype

- **It is needed to validate gaseous approaches, read out scheme; to compare with MC smulations and Sc. HCAL**
- **If 1x1 cm2 cells and 40 layers with 20 mm steel plates as absorber then ~400,000 channels are needed**
- **Collaboration between IPNL, LAL, LLR, LAPP, Saclay – France; CERN; CIEMAT- Spain; IHEP- Russia is forming to perform this within CALICE and EUDET framework**
- **Biggest challenge (and cost) – read out electronics is responsibility of IPNL, LAL, LLR FE ASIC is needed**
- **This is as 2nd step towards the ILC**

Comparison of hadron shower simulation codes by G Mavromanolakis





Status: RPC performance and design

1.2 mm monogap glass RPC, saturate avalanche mode

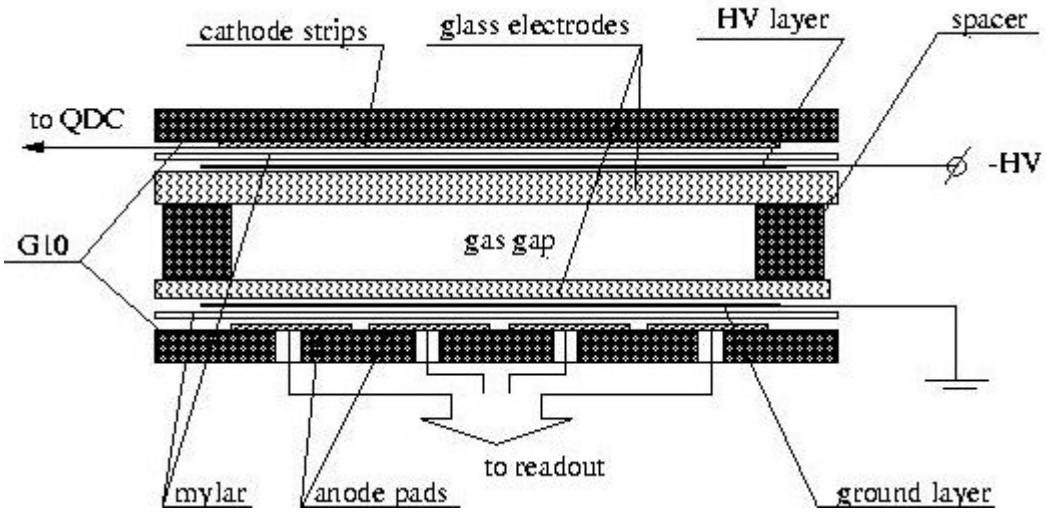
98% eff , 1 kV plateau, ~1.4 mult

Combined RPC – mult < 1.1

N	Item	Thick, mm
1	Anode printed board	1.0
2	Insulated mylar	0.05
3	Graphite coverage	0.05
4	Glass anode	0.55
5	Gas gap	1.2
6	Glass cathode	0.85
7	Graphite coverage	0.1
8	Insulated mylar	0.2
9	Cathode PB	0.5
	Thickness budget	4.5
	Max thickness	<8.0
	Room for FEE	~ 3.5

Anode PCB – internal surface for pads, external one for RO electronics

Cathode PCB – internal surface for long strips for QDC read out (control)



Combined RPC

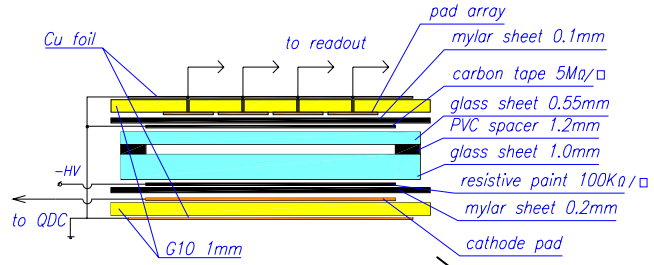


Fig.1a Standard glass RPC.

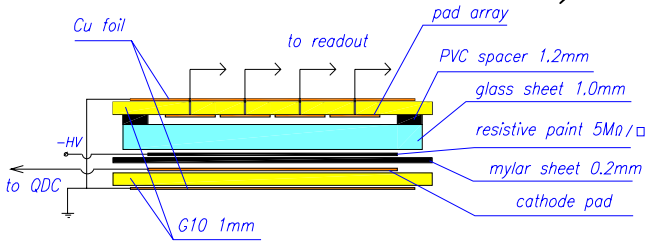
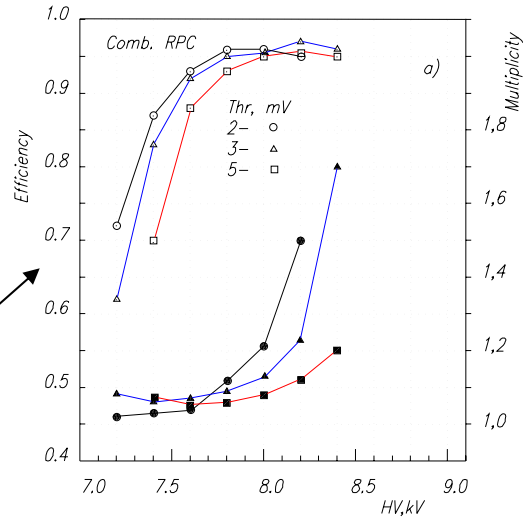


Fig.1b Combined RPC.



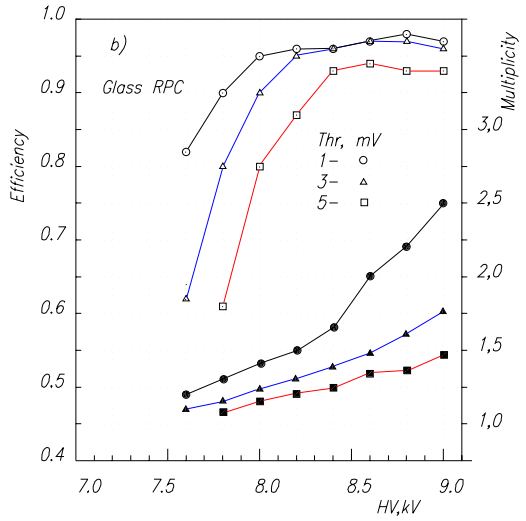


Fig. 3

Status: 1m2 RPC plane

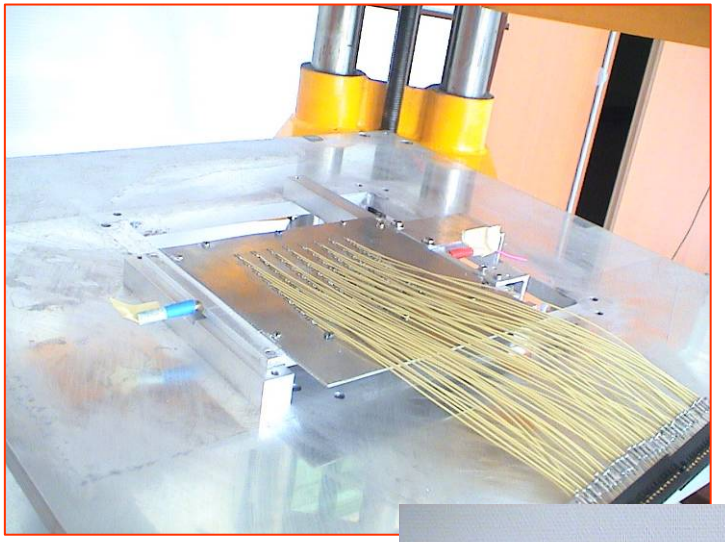
Test of 1 m2 RPC plane

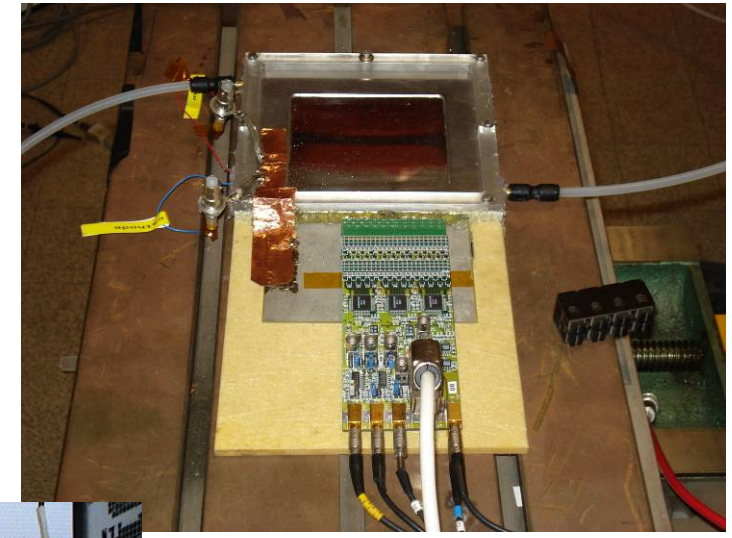
Cosmic ray trigger
Using scint counters
96x6 cm2
2 counters - top
1 counter – bottom

TFE/IB/SF6=90/5/5
gas mixture

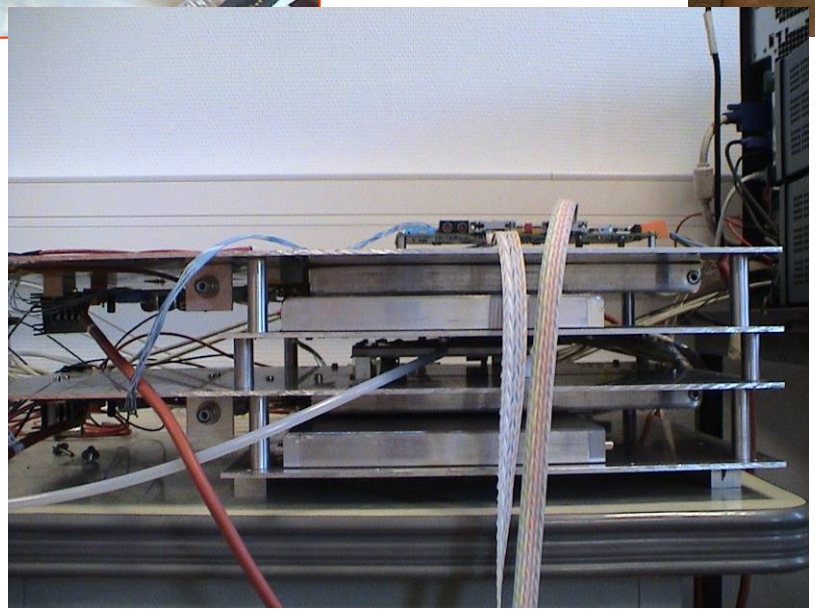
robust design,
eff~94%, non uni <2%

IPNL test bench





2 GRPCs
8x8 pads
is built with
IHEP

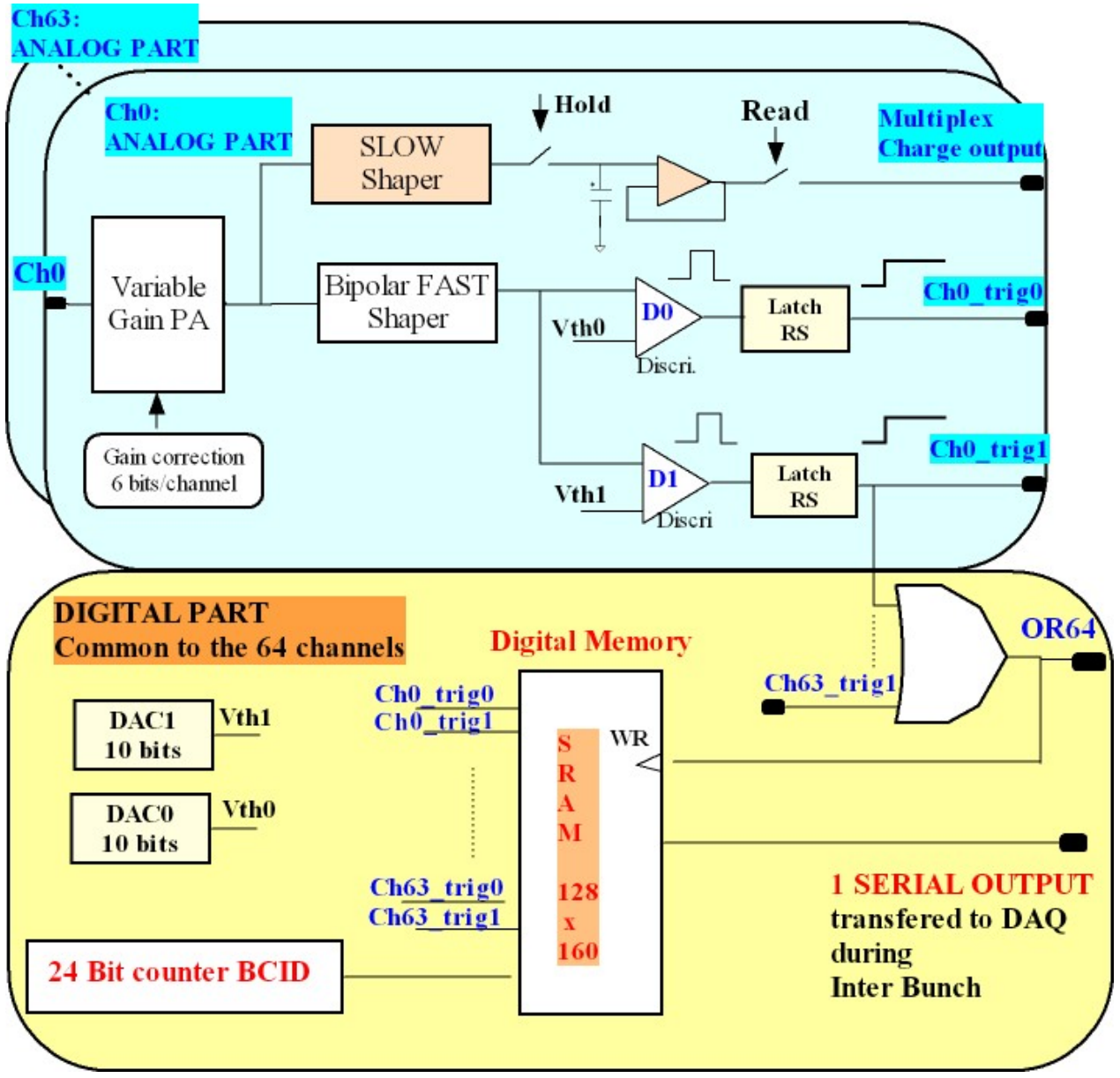


µMEGASs
8X8 pads is built with Saclay
6X16 pads is built with CERN

ASIC - HaRDROC architecture

NSM

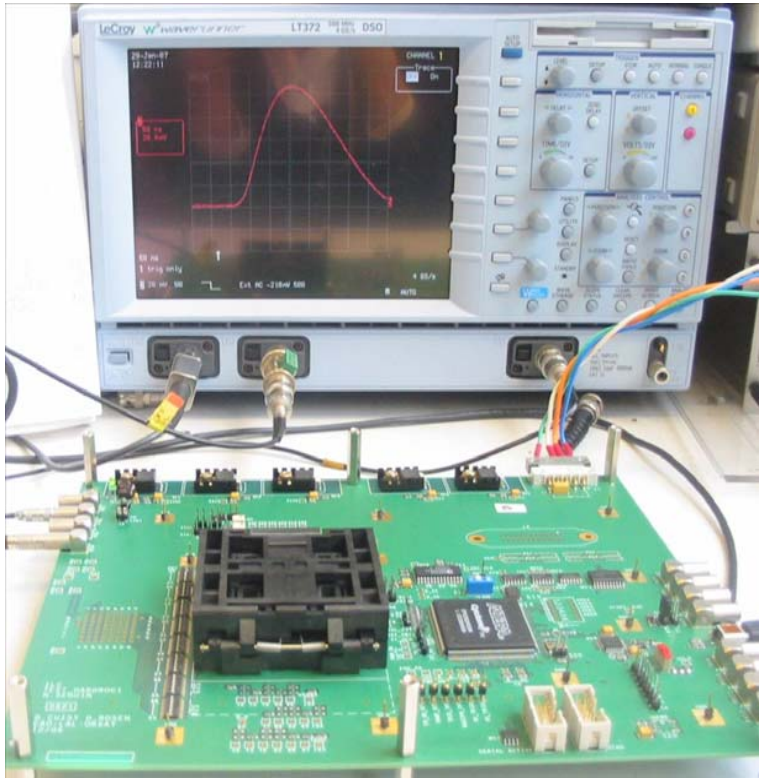
- Full power pulsing
- Digital memory: Data saved during bunch train.
- Only one serial output
- Store all channels and BCID for every hit. Depth = 128 bits
- Data format : 128(depth)*[2bit*64ch +24bit(BCID)+8bit(Header)] = 20kbits
- Sequential readout @ 1 MHz



HaRDROC Status

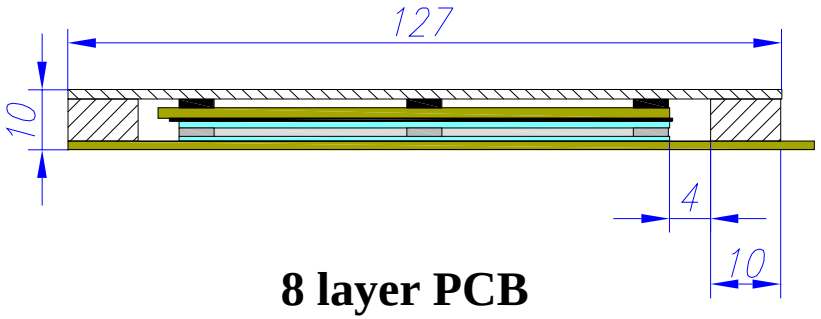
- 1-st iteration ASICs received end of December 06
- Testboard in Orsay to evaluate the analog performance of one HARDROC
- First analog measurements are in good agreement with expected results
- 7 testboards have been produced and will be available at the end of February to be sent in labs (IPN Lyon, LLR, Londres, Protvino...)

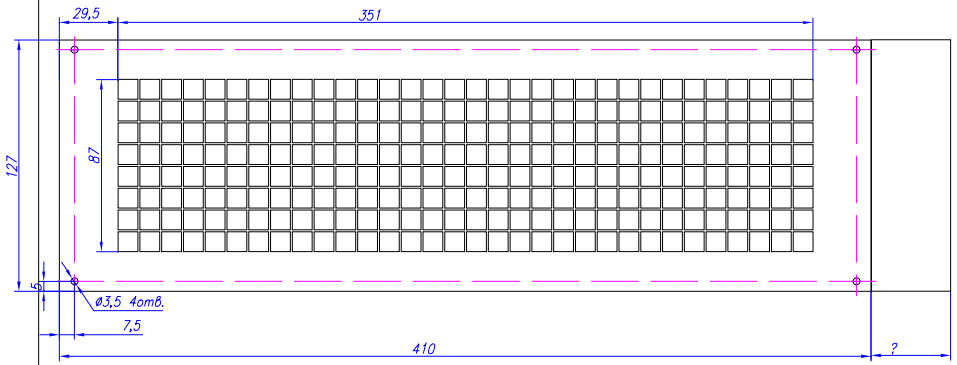
NSM



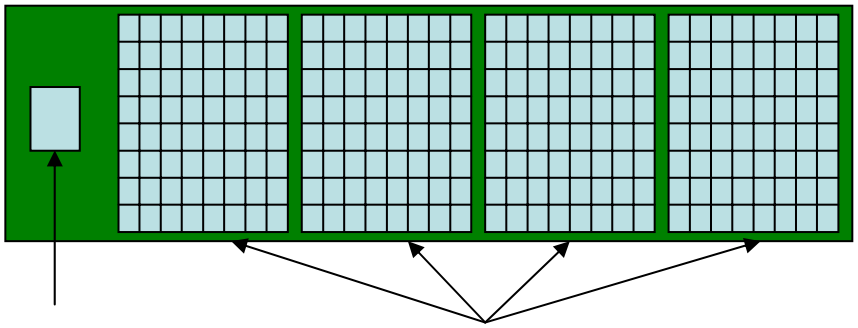
Plans: 8x32 pads RPC and µMegas

RPC





8 layer PCB



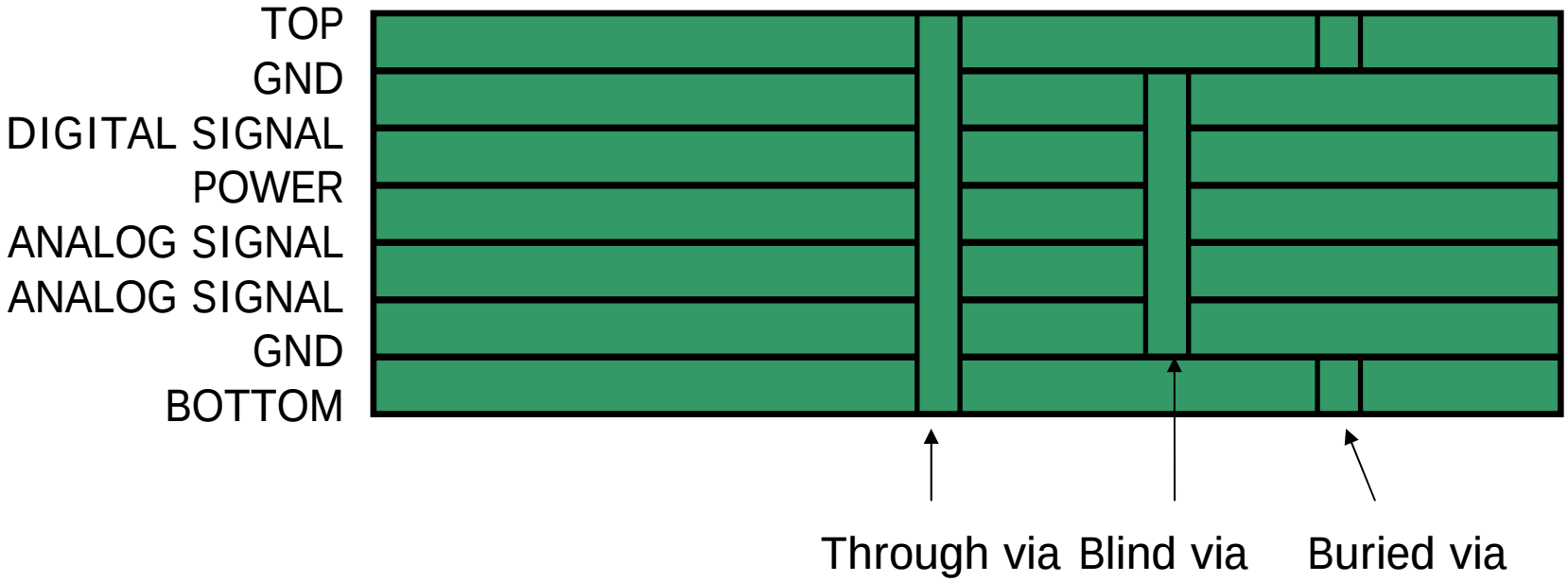
FPGA

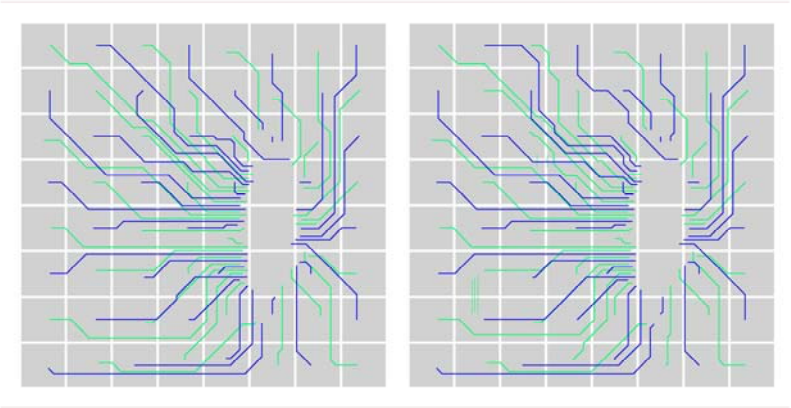
4 areas of 64 pads of 1 sq cm : bottom layer
Hardroc external components : top layer

- PCB and chambers in March07
- Tests in April07 with cosmics
- Tests in July07 with test beam

PCB Layout in 8 layers (solution1)

Hervé MATHEZ

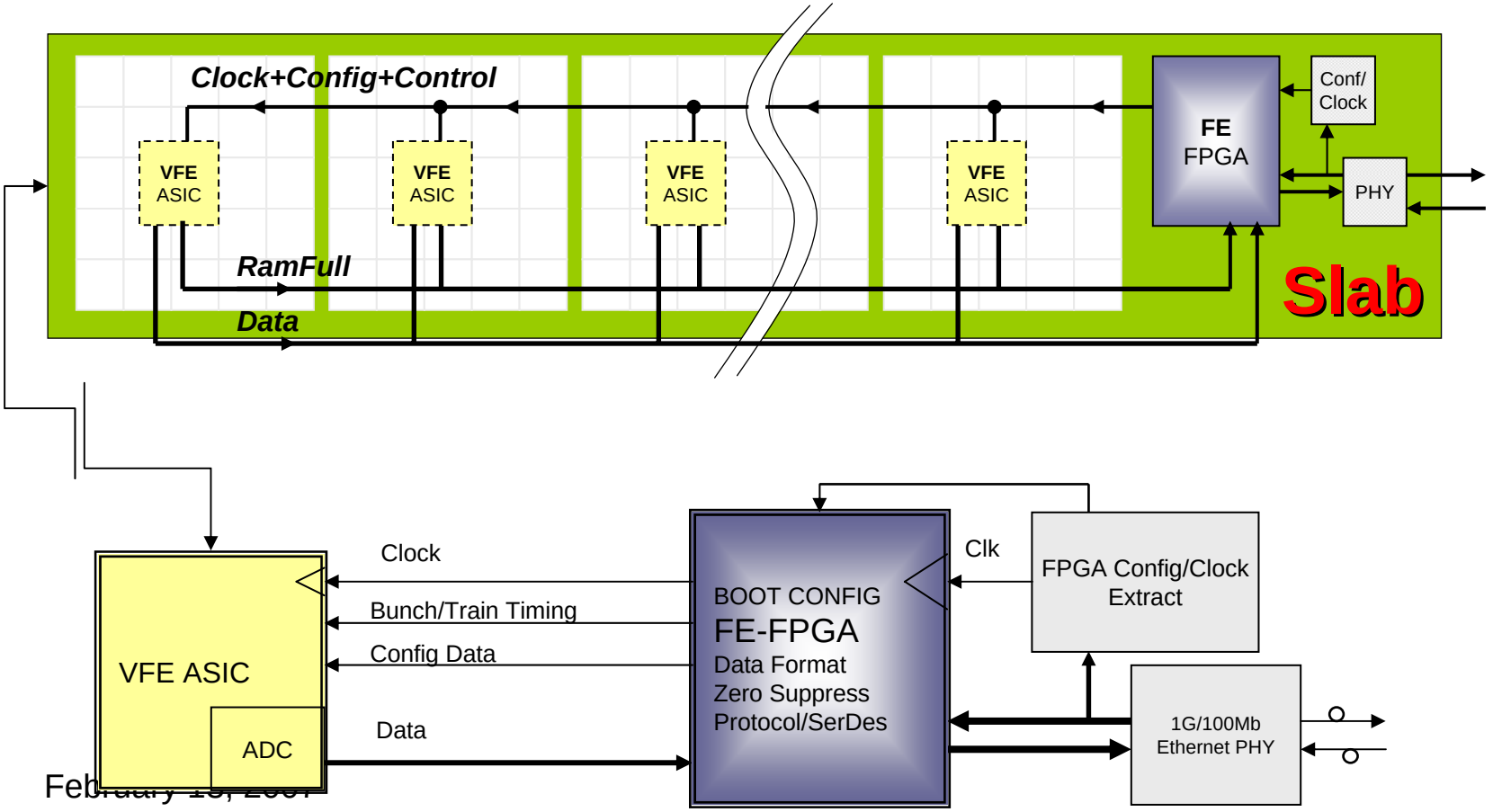




Digital architecture towards 2nd generation DAQ

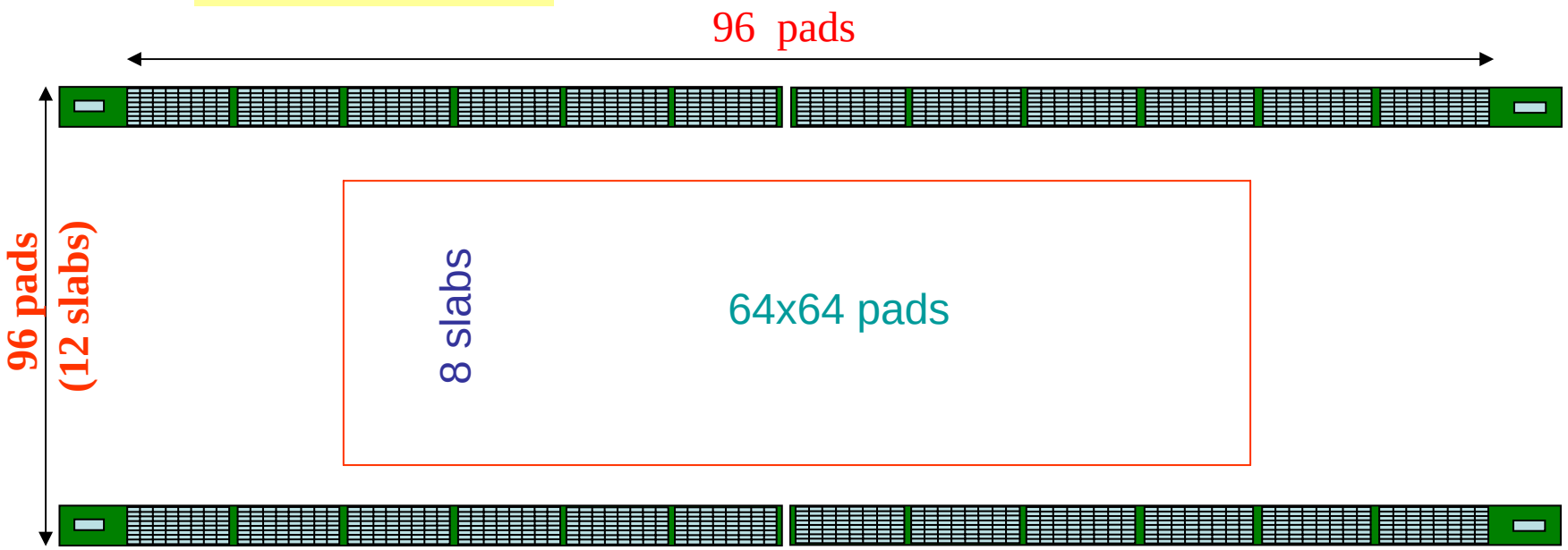
ECAL, AHCAL, DHCAL **detector readout**

NSM



Plans: 1 m3 prototype

1 m2 RPC plane



96x96 pads → 64x64 pads ?

2 times less expensive but pure comparison with Sc. HCAL?

Summary

- **It seems that European collaboration for DHCAL is created**
- **DHCAL R&D was carried out already for**
  - RPC: is done
  - MicroMegas: is in progress
- **8x32 pads RPC and μMegas chambers to validate readout system**
  - Tests in April07 with cosmics
  - Tests in July07 with test beam
- **~1m³ prototype**
  - 1st RPC and μMegas 1m2 planes at the end of 2007
  - full stack at the end of 2008
  - to decrease the cost it is desirable to consider lower lateral chamber dimensions (64x64 pads for example)

More close collaboration is needed

Is 8x32 pads PCB optimal ?

Alternative proposal:

- **8x8 pads PCB as basic unit**

  Can be used for existing 8x8 pads chambers, ANL 16x16 pad RPC, Mini DHCAL prototype to measure response for electrons with 10/20 layers with 64 pad RPCs

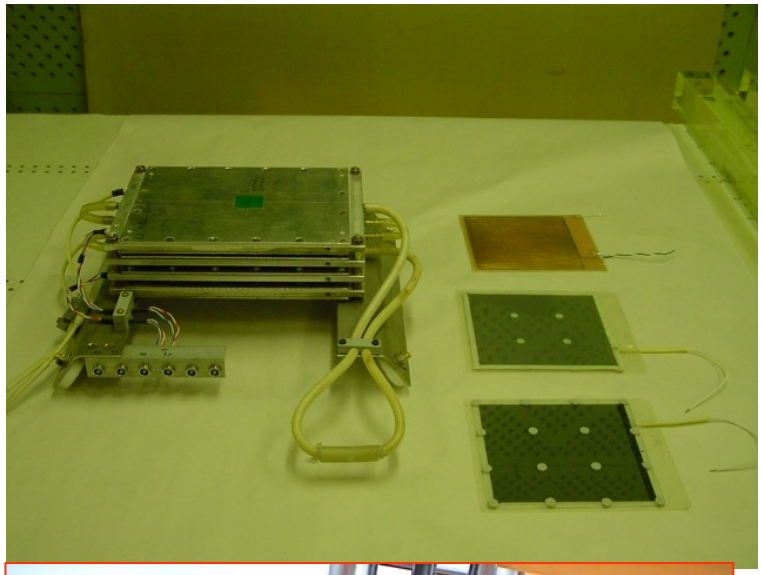
- **8x16 pads PCB to check all cross talks**

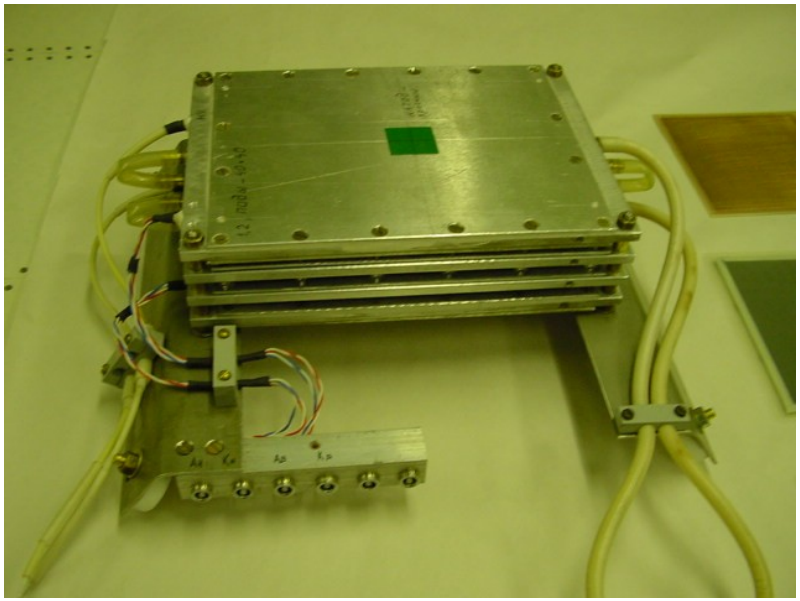
Can be used with 8x16, 16x16 (ANL), 8x32 pad chambers

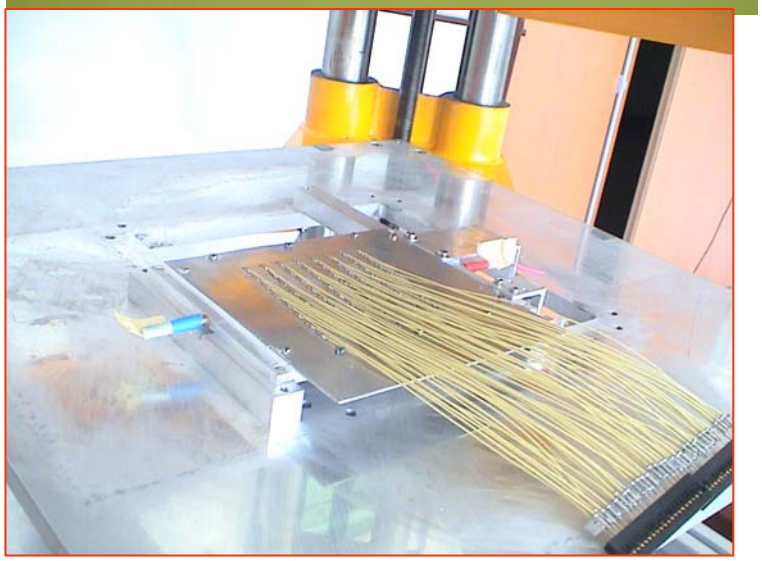
Approach for 1m2 RPC can be checked

For IHEP RPCs design should be used for inside and outside gas volume options

64 pads RPC







64 pads RPC as basic unit

64 pads RPC

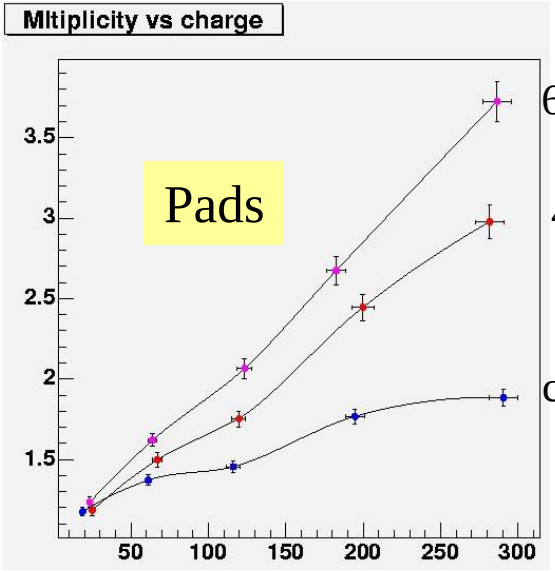
As element of 1m2 RPC plane with 10000 ch.

- **Is ASIC on board or on side ?**
- **If ASIC is on side anode pads PB is designed**
- **Open or closed from anode ?**
- **Combined 64 pads RPC ?**
- **Gas system**
- **HV system**
- **Slow control (temperature, pressure)**
- **Charge read out from cathode**
- **Full acquisition (anode pads and cathode)**

Anode pads PB

Prototyping of anode printed board for 64 pads of 1 cm2 with printed lines to side:

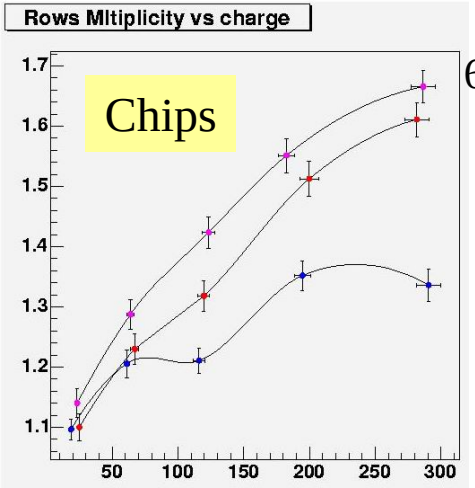
1. 2 layer PB – huge cross talks
2. 4 and 6 layer PBs – CT is still larger than for coaxial cables



6 layers

4 layers

coax

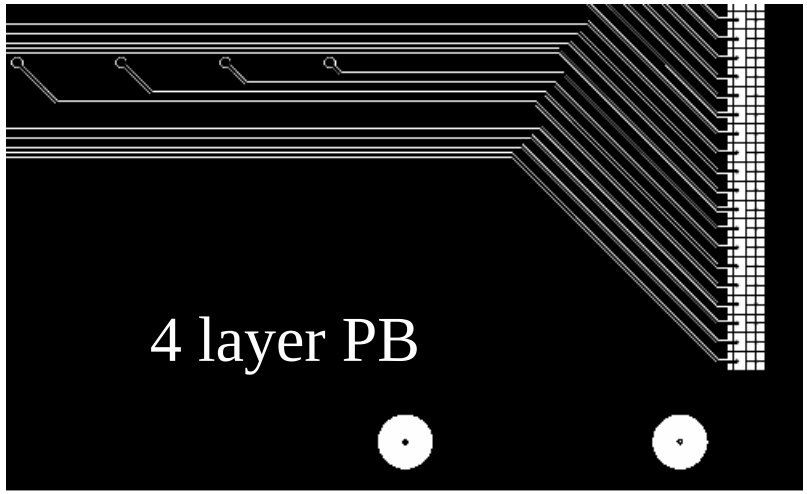


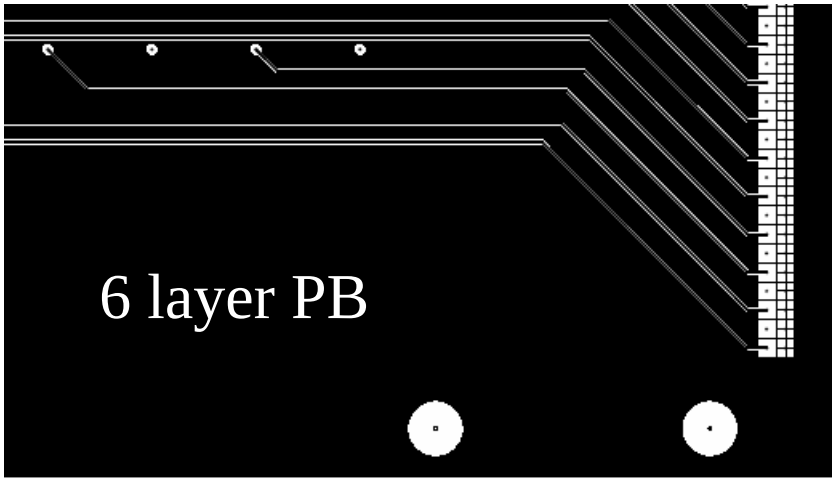
6 layers

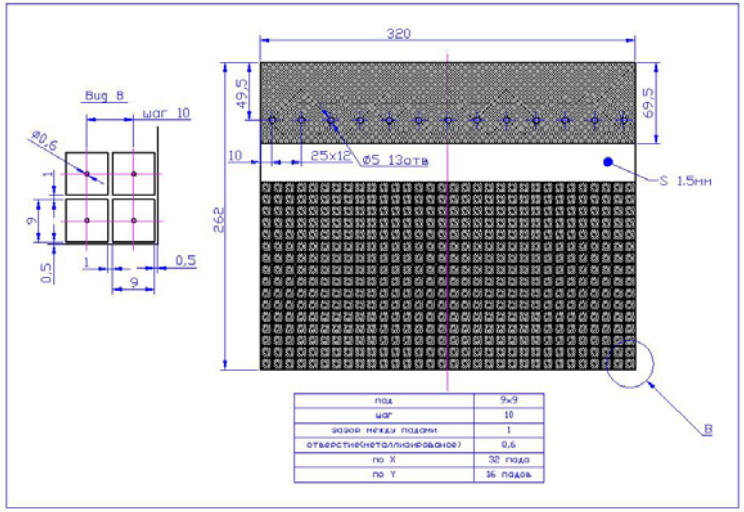
4 layers

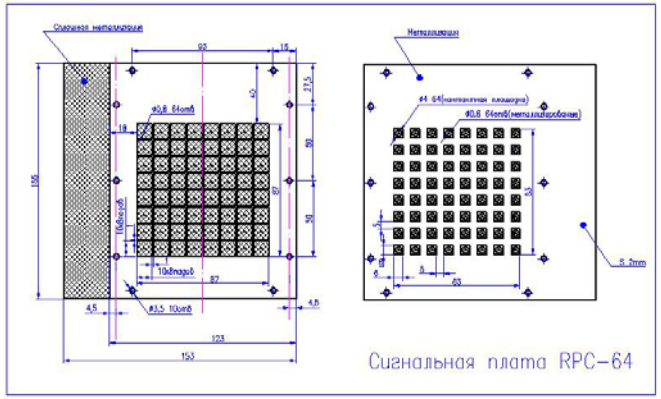
coax

Anode pads PB









Decided to return to 2 layer PBs with coaxial cables

Mini DHCAL prototype

To measure response for electrons with 10/20 layers

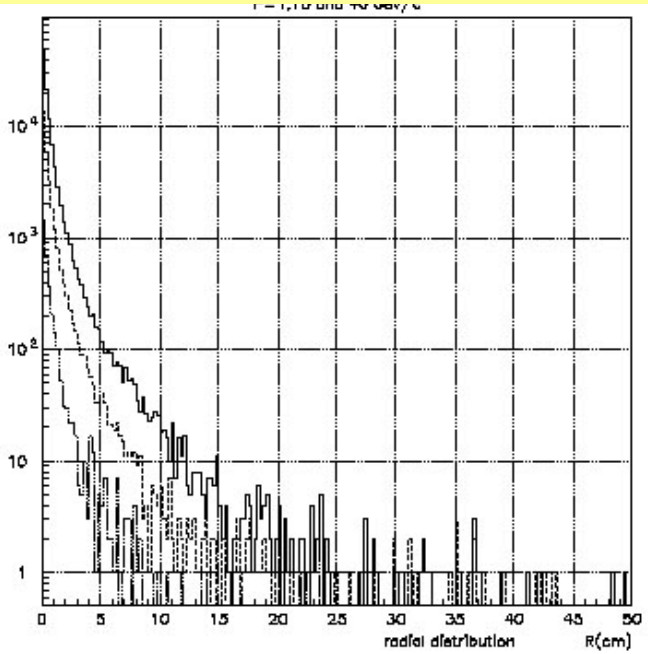
sampling: 4/2 cm steel + 0.65 cm RPC plane

sensitive area 9x9 cm^2 (8x8 pads of 1x1 cm^2, 1 mm spacing)

GEANT3 simulation of transverse containment

p_e=1,10,40 GeV/c

Diff. distr.



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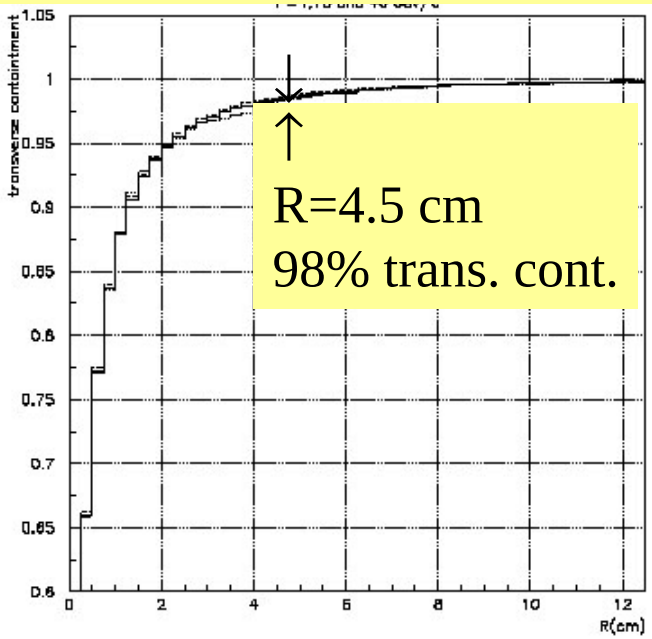
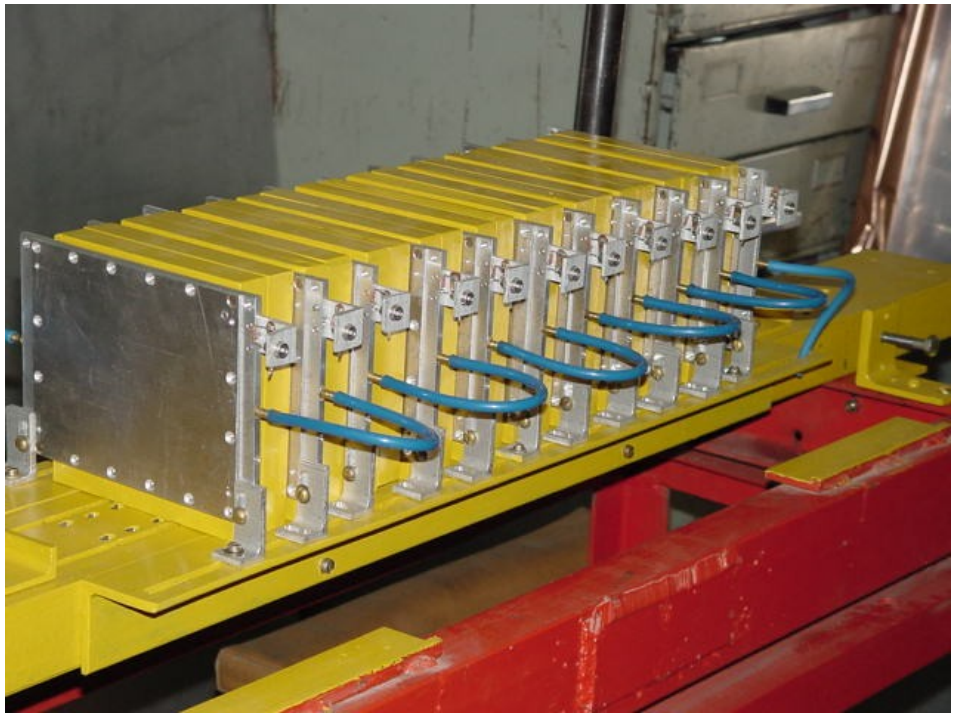


Mini DHCAL prototype

Goal – first digital measurements of electromagnetic showers and comparison with simulations.

Usage of minimal number of RO channels ! (640/1280 ch.)

Most hard case for digital calorimetry !



Readout summary

	Item	DCAL	KPix	HaRDROC
FE ASIC	**Current version**	v2	v3	v1
	Current ch# /final ch#	64/64	64/1024	64/64
	Test	Almost done	Ongoing	Started?
	Additional submission	No	Yes	?
	Overall status	Almost done	Ongoing	Ongoing
Readout system for PS	**Conceptual design**	Done	No	No
	FE board	Design finished	No	No
	Concentrator	Design started	No	No
	Data Collector	Design ongoing	No	No
	Trigger Timing module	Specified	No	No
	DAQ software	Started	No	No

- If funding permits, given current progress
  - The 1st PS stack would (naturally) be: RPC + DCAL based readout
  - The 2nd PS stack would be: GEM + ? Readout
- DCAL readout will be validated through the slice test (Apr.07, MTBF)

Costs and Funding

A) Slice test is funded by LCDRD06, LDRD06 and ANL-HEP, and Fermilab funds

B) Prototype section not yet funded, but…

Stack	Item	Cost	Contingency	Total
RPC stack	**M&S**	607,200	194,600	801,800
	Labor	243,075	99,625	342,700
	Total	**850,275**	**294,225**	**1,144,500**
GEM stack*	**M&S**	400,000	165,000	565,000
* Reusing most of the RPC electronics	**Labor**	280,460	40,700	321,160
	Total	**680,460**	**205,700**	**886,160**
Both stacks	**M&S**	1007,200	359,600	1366,800
	Labor	523,535	140,325	663,860
	Total	**1,530,735**	**499,925**	**2,030,660**

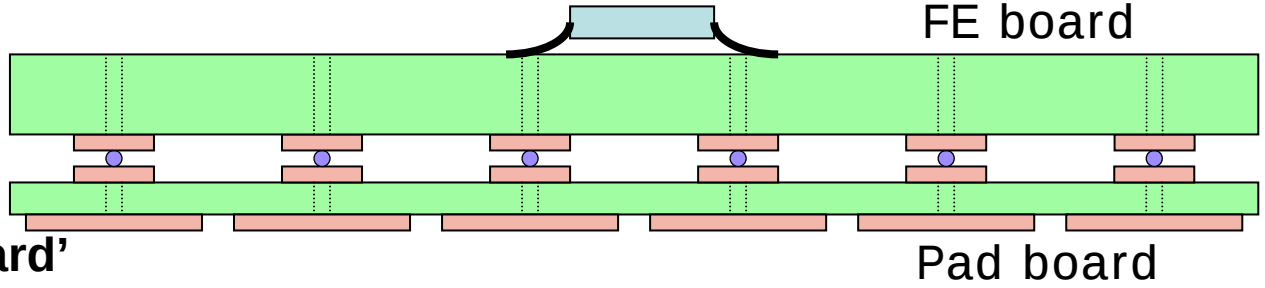
Proposal for supplemental funds for $500k/year over two years submitted to DoE
With continuing resolution, it is not very promising … wait one more year?

DHCal test beam plan

- US RPC + GEM: staged approach
  - Feb.- Mar. 2007: GEM chamber characteristics run at Fermilab MTBF
    - This will be done using 100 channel ADLink PCI based DAQ card
  - April 2007: “slice test” at Fermilab MTBF
    - Slice test: mini-calorimeter stack (~10 layers)
      - Active medium: 8 RPCs + 2 GEMs, 16x16cm^2 active area in each chamber
      - Absorber: 4mm copper + 16mm steel
    - Validate DCAL chip + readout system for prototype section
      - Readout system as close as possible to the 1m^3 prototype section
    - Limited data/simulation comparison
  - Later 2007:
    - RPC: finish slice test, analyze data, prepare for prototype section
    - GEM: continue on R&D, some beam test with KPix chip
  - 2008: construction and test of prototype section (if funding permits)
    - Construct 1st prototype section: RPC + DCAL readout
      - European RPC effort: join the effort and supply part of the RPC’s
    - Detailed test program in Fermilab test beam
    - Construct 2nd prototype section: GEM + ? Readout
- MicroMegas
  - 2007: construct 1 50x50cm^2 chamber for beam test
  - 2008: construct 1 layer of 100x100cm^2 prototype

Pad board and FE board (1)

G Drake (ANL)



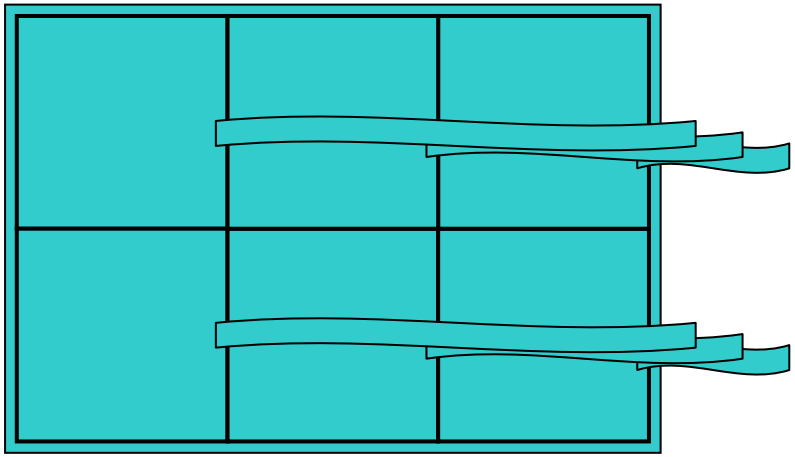
New Concept

Split old ‘Front-end board’

‘front-end board’ highly complex and difficult
blind and buried vias + large board => (almost) impossible to manufacture
split into two boards to eliminate buried vias

Pad boards

four-layer board containing pads and transfer lines
can be sized as big as necessary
relatively cheap and simple
vias will be filled



Front-end boards

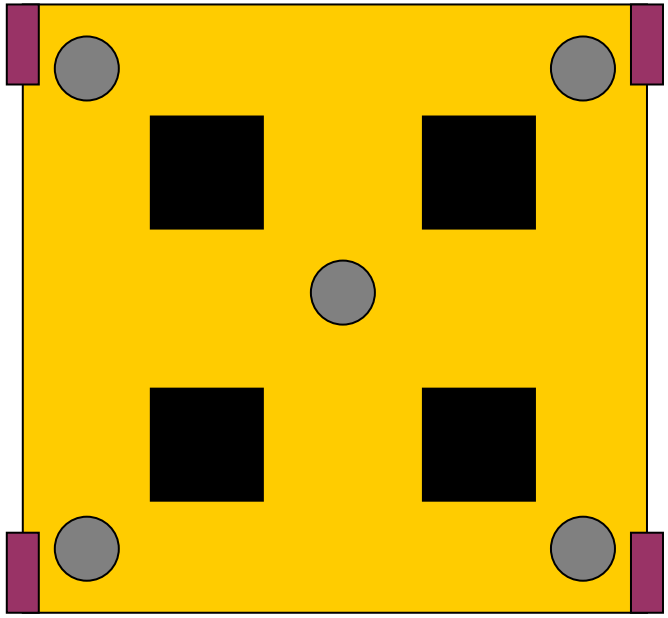
eight-layer board
16 x 16 cm^2
contain transfer lines, houses DCAL chip
expensive and tough to design

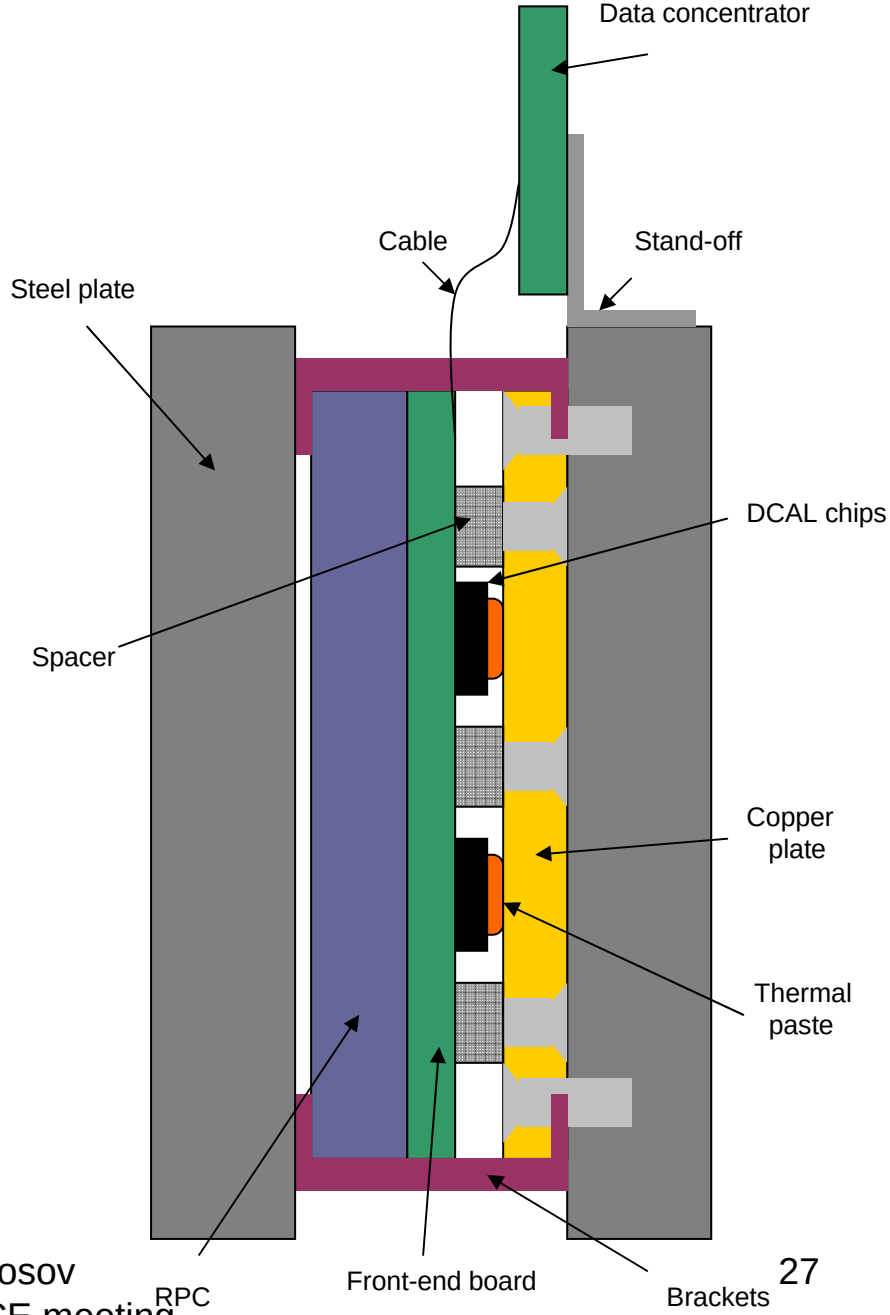
Connections

board to board with conductive glue on each pad (being tested)
cables for connection to data concentrators

Assembly

Not to scale….





Assembly procedure

Screw spacers to copper plate
Screw copper plate to steel plate
Apply thermal paste to DCAL chips
Glue front-end board onto spacers
Attach RPC with clips to copper plate
Mount data concentrator and connect

• HV	Test FNAL unit with filters	Iowa	
• Gas mixin	Explore acquiring premixed gases		Iowa
• Beam telescope	Build one 4x4 cm2 counter	UTA	
• Mechanical structure	Build absorber stack	ANL	
•	Think about glue dispenser		
•	Find scanning table		
• ASIC testing	Complete testing		ANL
• Pad boards	Test gluing		ANL
• Front-end boards	Complete design		ANL
• Data concentrators	Complete design		ANL
• Data collectors	Complete schematic	Boston	
• Timing and trigger module	Decide on CAEN module/identify programmer		
• DAQ software	Acquire VME-PCI bridge	ANL	
•	Start programming		