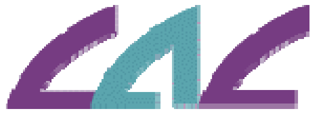


prototype PCB for on detector chip integration

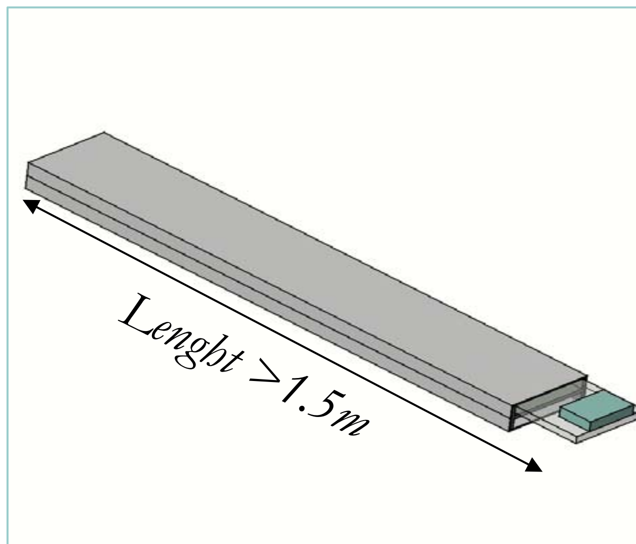
D.Cuisy, J. Fleury, C. de La Taille

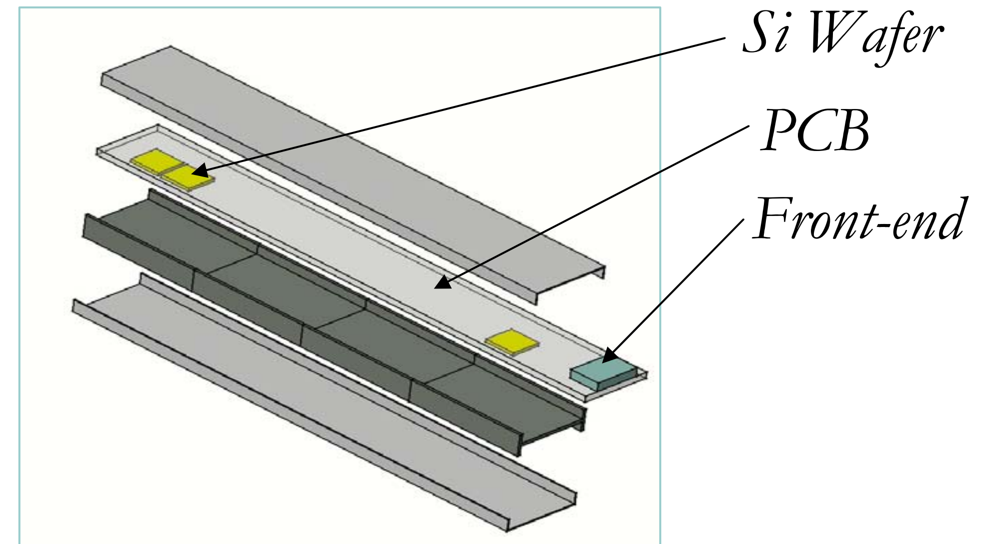
- This presentation is addressing PCB issues from the detector to the edge of the slab
- The issues are :
  - Keep active layer thin
    - for moliere Radius
    - For ECAL thickness and coil cost
  - Keep crosstalk around .1%
  - Keep cost low or at least reasonnable
  - Ensure a good assembling yield

The TDR option

- Very front end electronic on the edge of every slab
- Single long PCB for each detection layer (1.5m long)
- Long lines carriing isgnals to the VFE electronic

→Crosstalk issues
→Noise issues
→Thickness issues





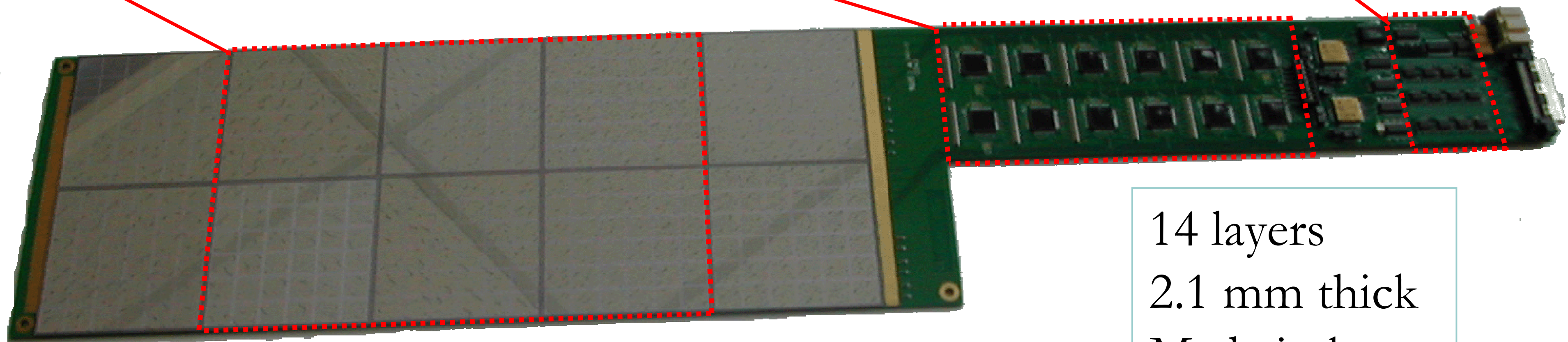
The physic prototype (2003)

Can't extrapolate to a full detector length

<u>6 active wafers</u>
Made of 36 silicon PIN diodes
→ 216 channels per board
Each diode is a 1cm² square

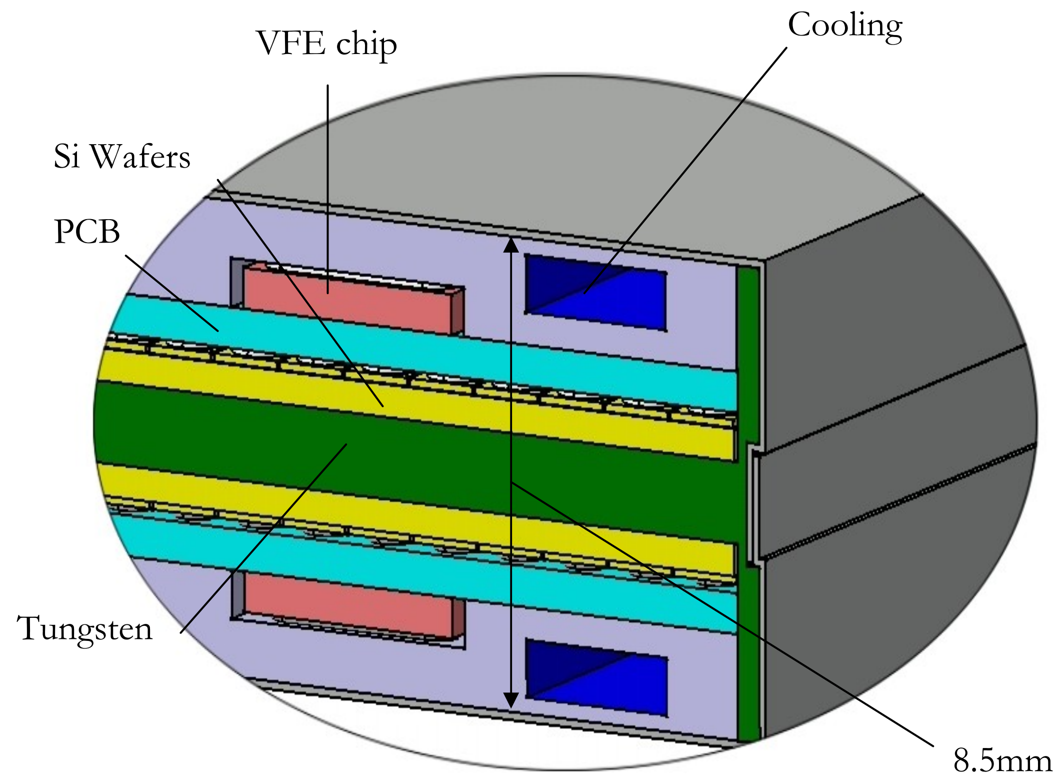
<u>12 FLC_PHY2 front-end chip</u>
18 channels per chip
13 bit dynamic range

<u>Line buffers</u>
To DAQ part
Differential



14 layers
2.1 mm thick
Made in korea

Embedded chip - the cooled option (2004)

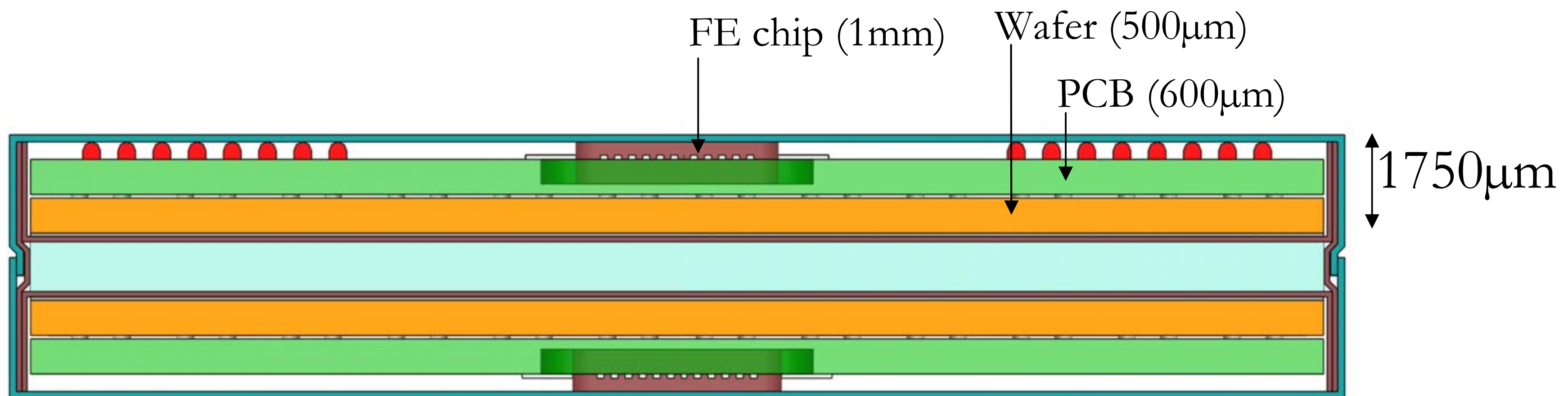


The not-cooled option (2005)

Due to power pulsing first encouraging results

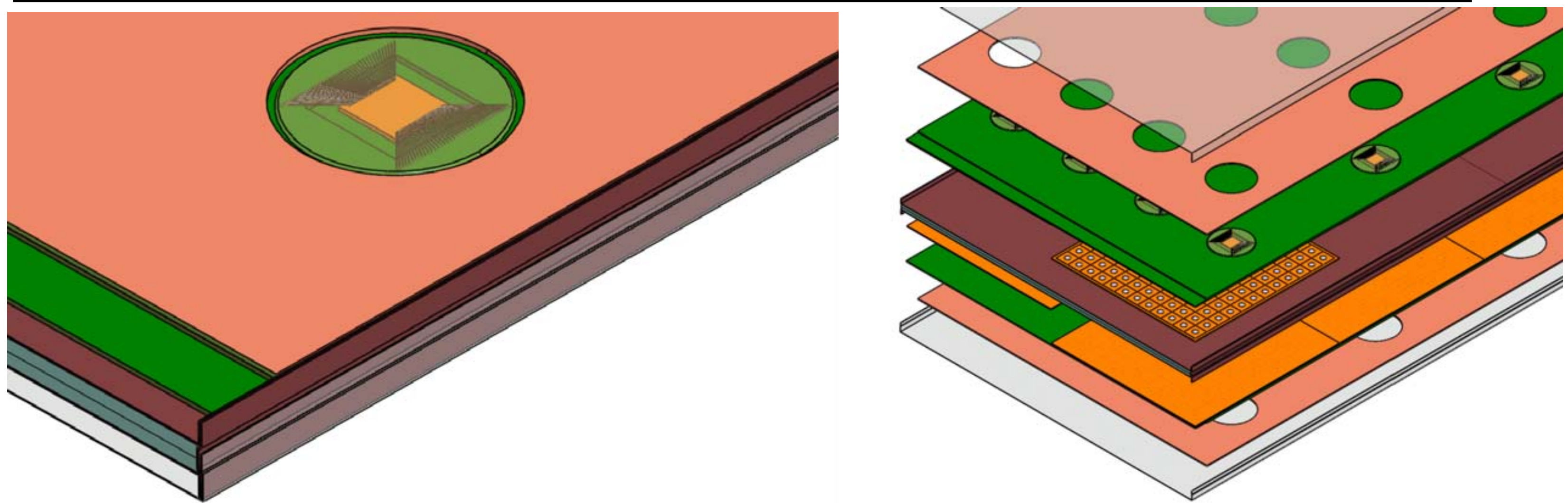
- Power consumption divided by 100 in the slab
- Cooling can be done without liquid

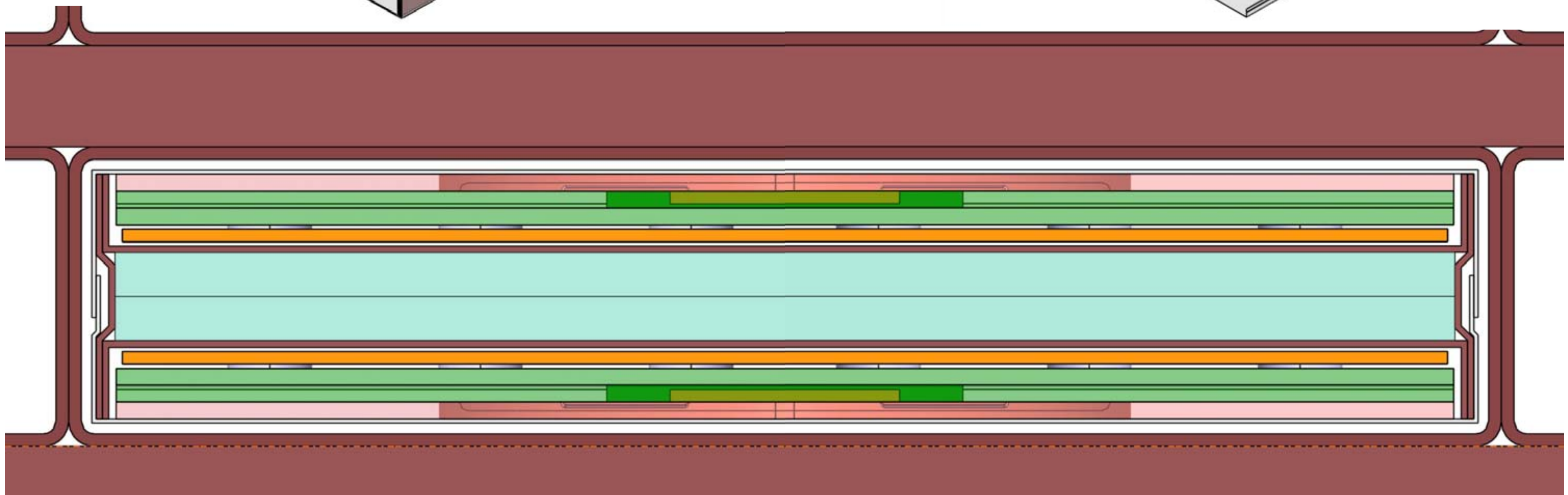
→Thinner
→Simpler
→Cheaper



Pictures : M. Anduze

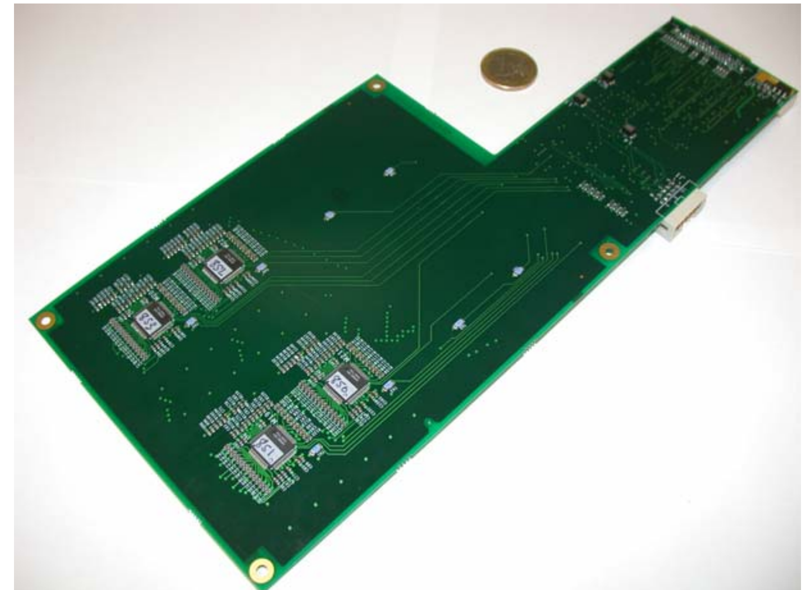
The not cooled not packaged option (FEV4)





FEV4 : New PCB description

- Compatible physics prototype
- Same size as FEV3
- 1 active wafer (instead of 2 for FEV3)
- Chip buried in the PCB

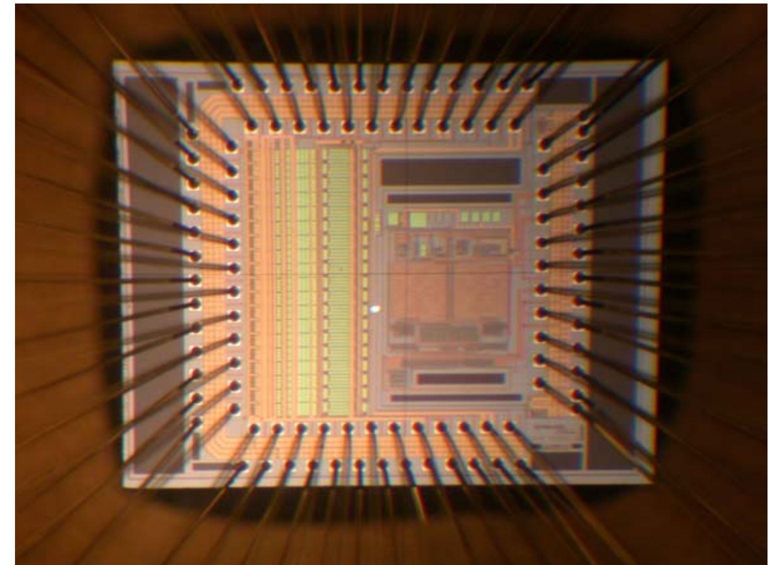


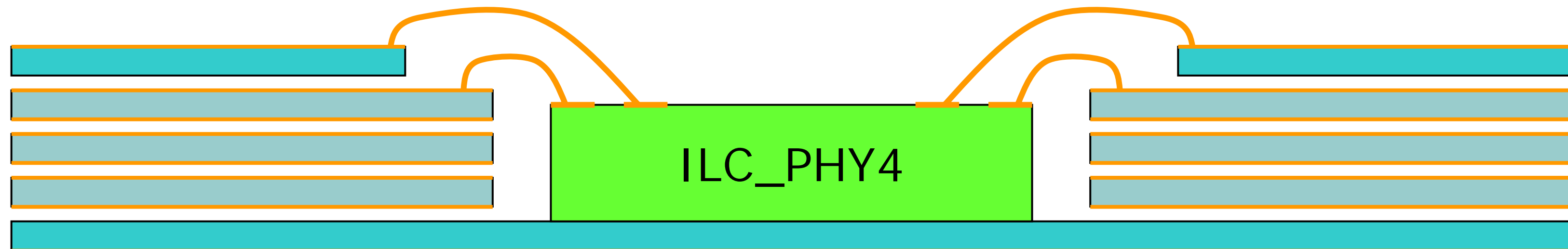
FEV4 – stack up description

Function	Layer
SIG/GND	TOP
SIG/GND	L2
GND	L3
GND	L4
VCC	L5
SIG/GND	L6
GND	L7
PADS	BOT

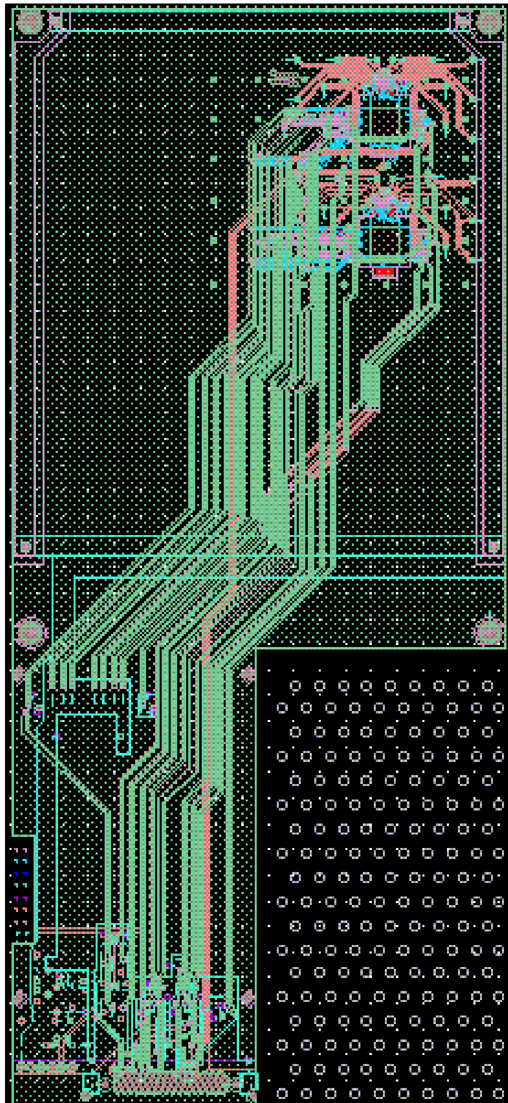
Single sided
Double sided
Double sided
Double sided
Single sided

950μm

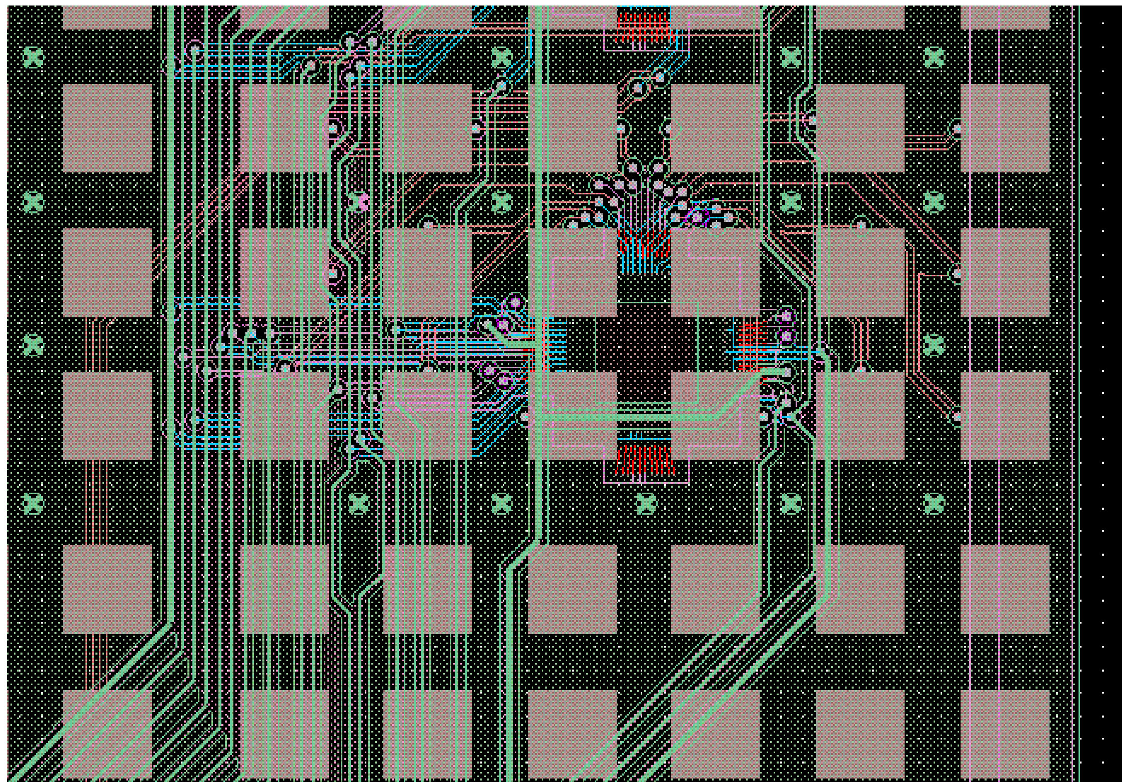




FEV4 – signal density



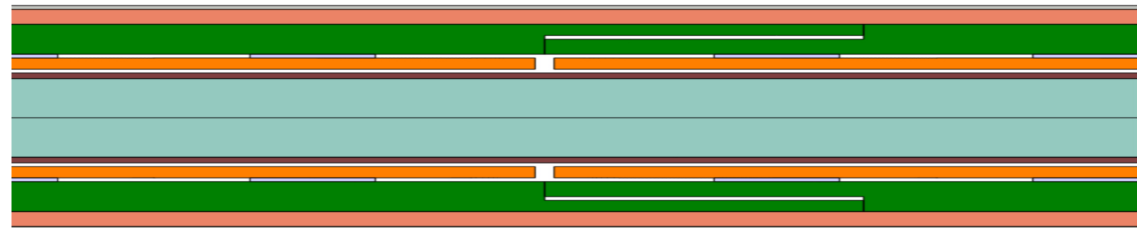
Difficulty are already foreseen to carry signals from one stitchable PCB to another

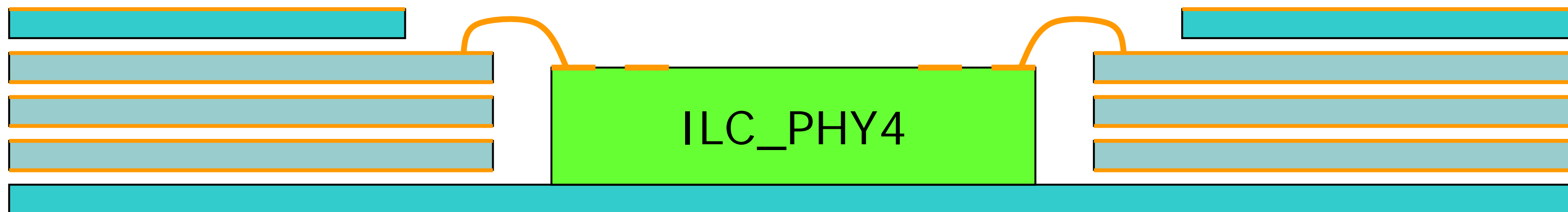


- Chip on board test
  - First prototype of chip in board
- Thin PCB coupling measurement
- Chip in beam test
  - Technology is 0.35µ
  - Analog part is very close to final version
  - Digital missing
- Power pulsing test

FEV4 – missing features

- 5*5 mm² pads
- Stitching
- Daisy chain
- Flat buried chip





- PCB is a key issue for the eudet module assembling.
- PCB is not only holding FE and wafer and is a major part for the detector performance.
  - Crosstalk
  - Pickup noise