SKIROC

New generation readout chip for ECAL

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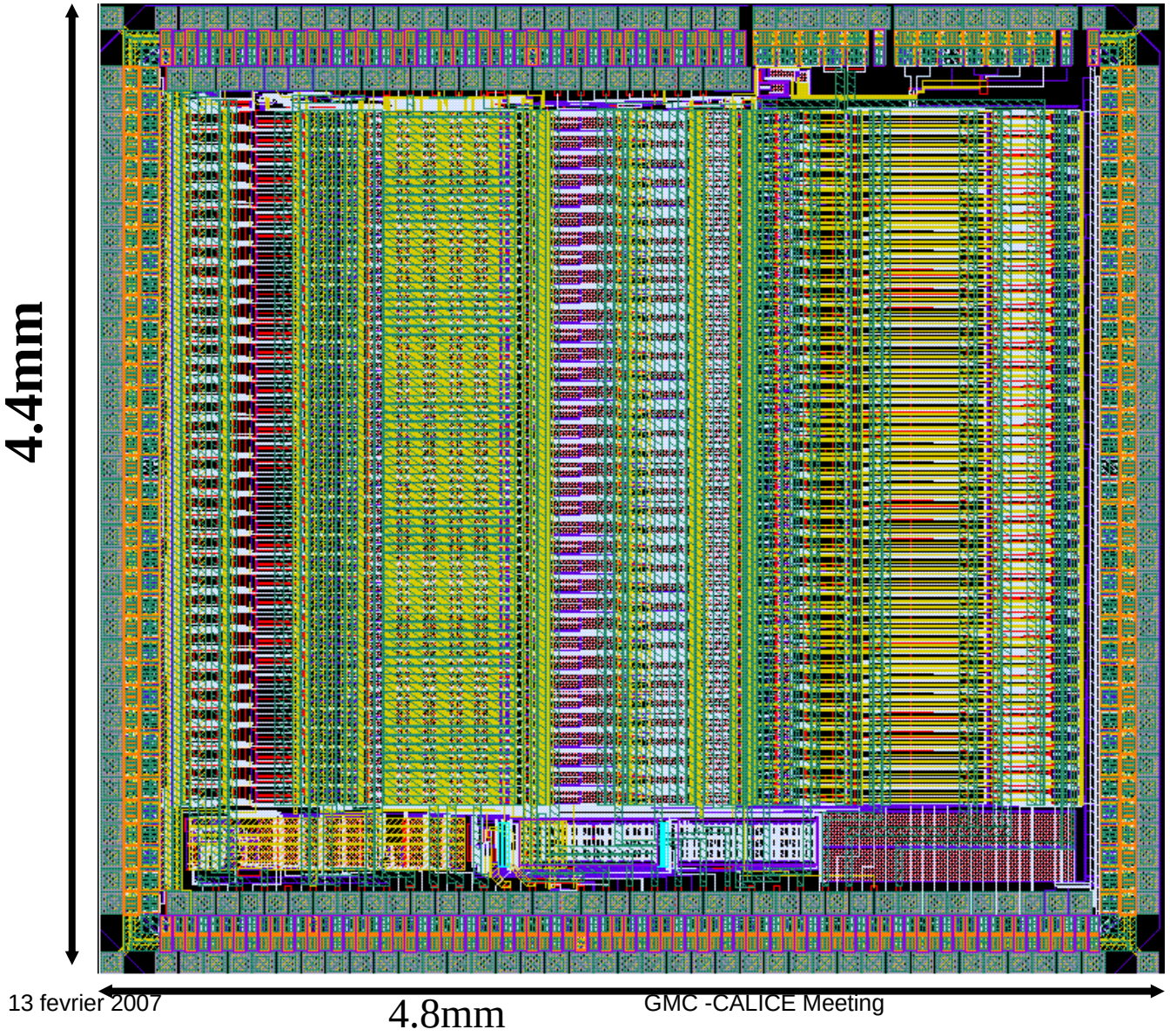
DESY CALICE meeting

SKIROC -> Silicon Kalorimeter Integrated Read Out Chip



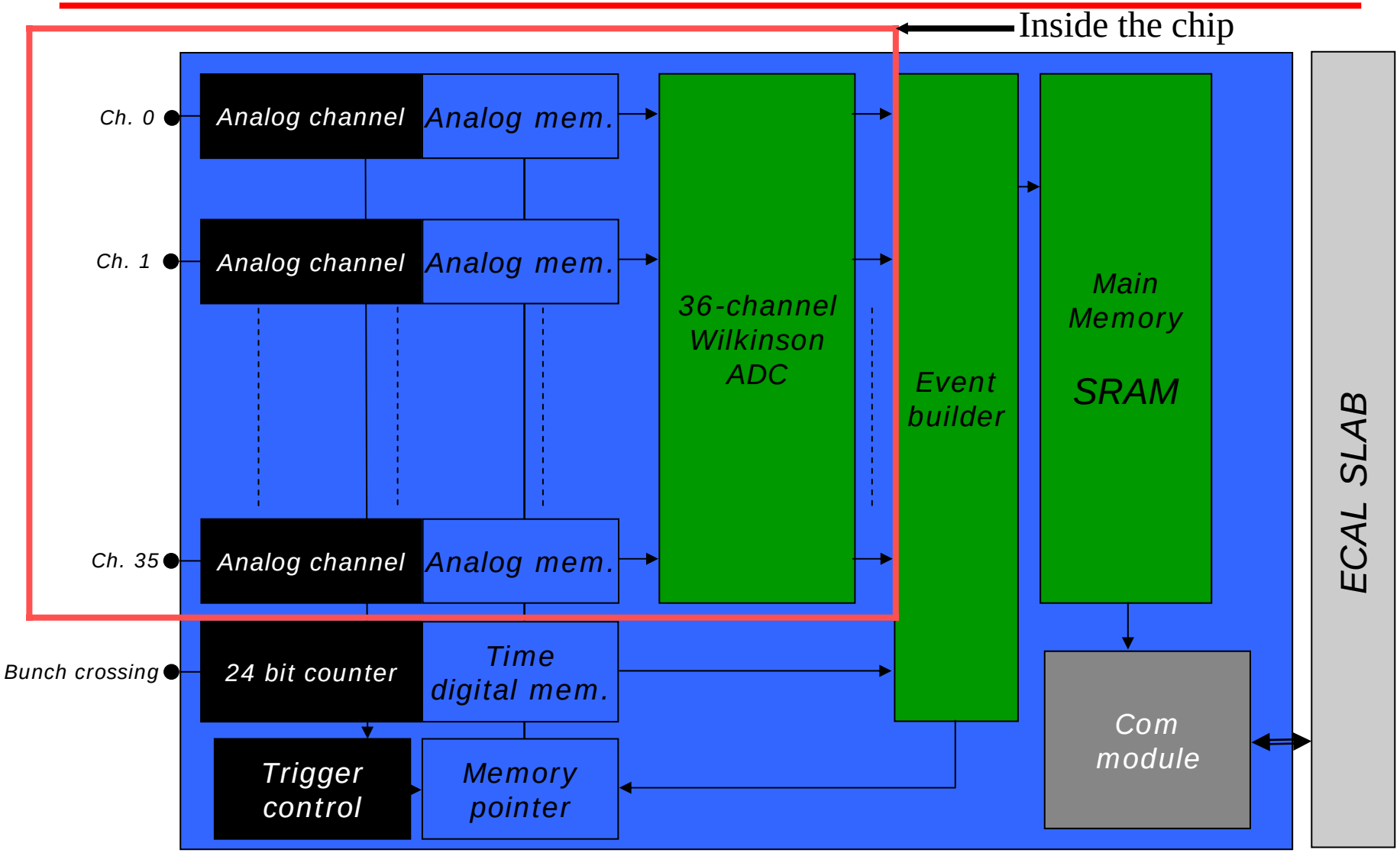
- ECAL read out
- Silicon PIN detector
- 36 channels
- Compatible new DAQ

Main features

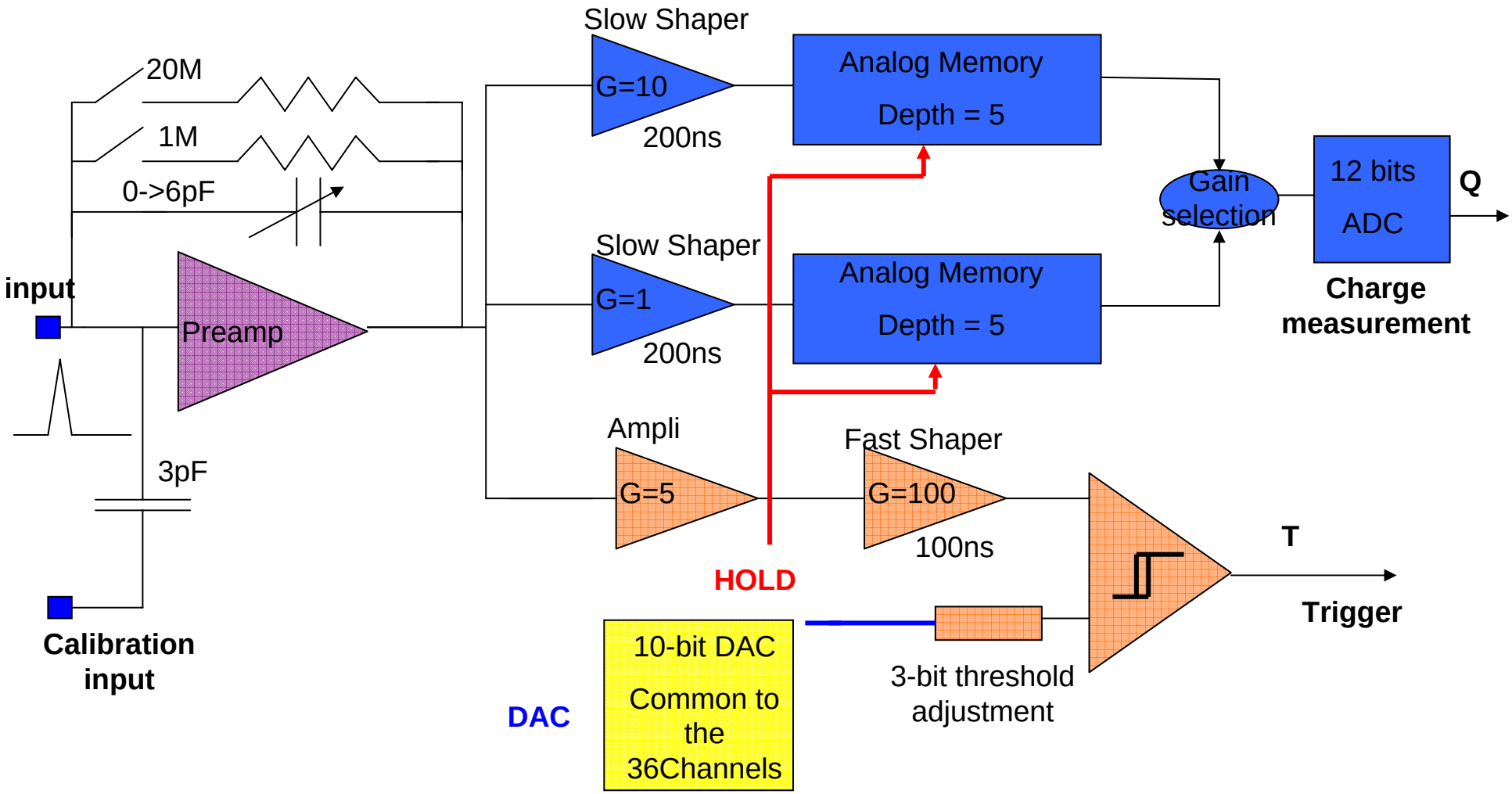
- Designed for 5*5 mm² pads
- 36 channels (instead of 72 to reduce cost of prototype)
- Detector AC/DC coupled
- Auto-trigger
- 2 gains / 12 bit ADC → 2000 MIP
- Power pulsing → Programmable stage by stage
- Calibration injection capacitance
- Embedded bandgap for reference voltage
- Embedded DAC for trigger threshold
- Compatible with physic proto DAQ
  - Serial analogue output
  - External "force trigger"
- Probe bus for debugging
- 24 bits Bunch Crossing ID
- SRAM with data formatting
- Output & control with daisy-chain

} Digital on FPGA for tests

Block scheme of EUDET ECAL FEE



One channel description

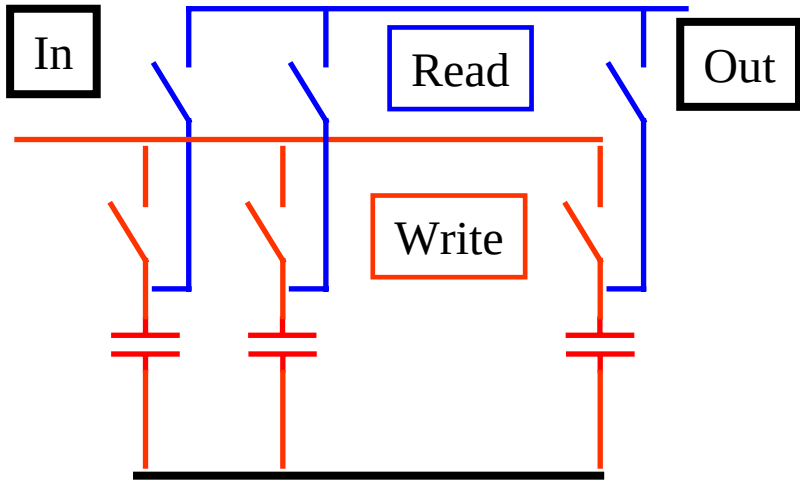


Trigger

- **Whole chip triggered when 1 channel triggers**
- **External trigger for pedestal measurement**
- **Trigger threshold adjustable channel by channel :**
  - 10 bits common for global coarse tuning
  - 3 bits fine tuning channel by channel

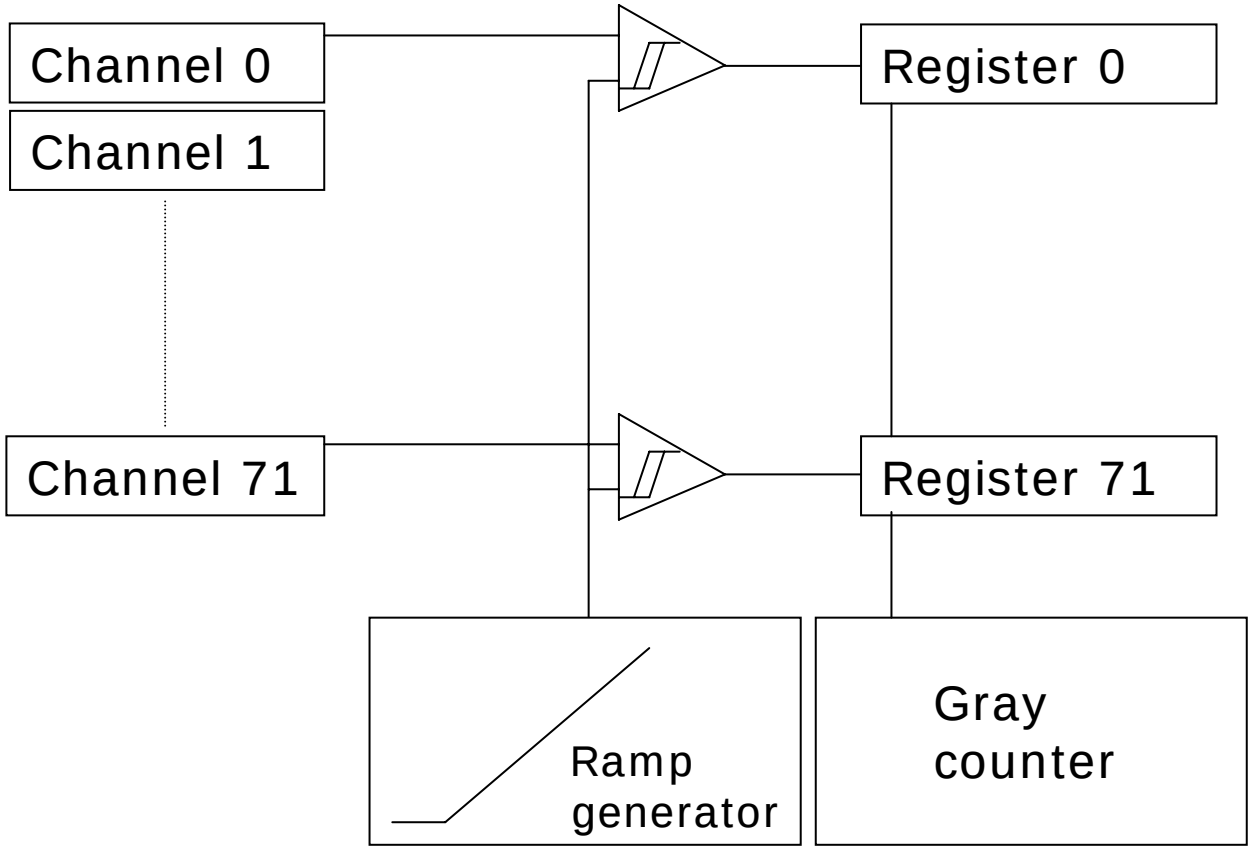
Analog memory : SCA

- **Depth : 5**
- **Architecture :**
  - Voltage write/ voltage read
  - 1 buffer per capacitor
  - Capacitor : 2pF
- **Difficulty : storage is very long**



Principle of a « voltage-write, voltage-read » analog memory

Wilkinson ADC

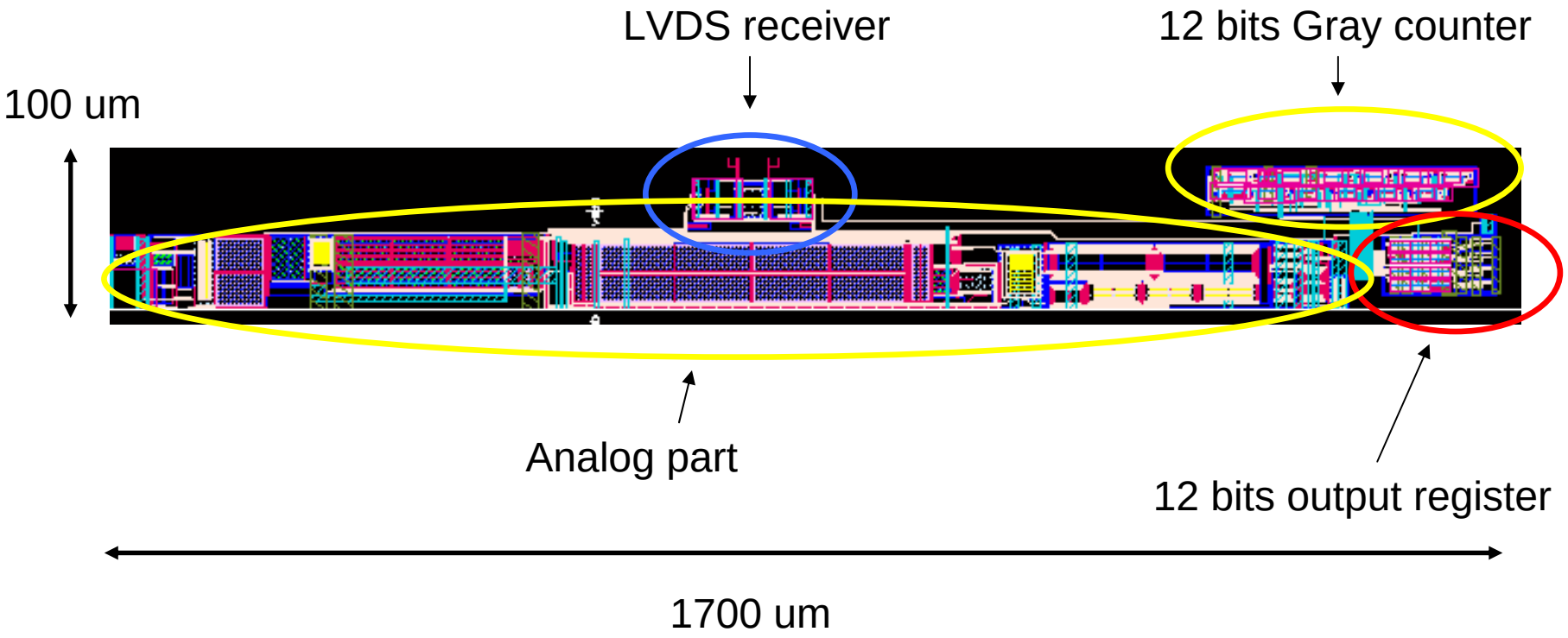


LPCC ADC

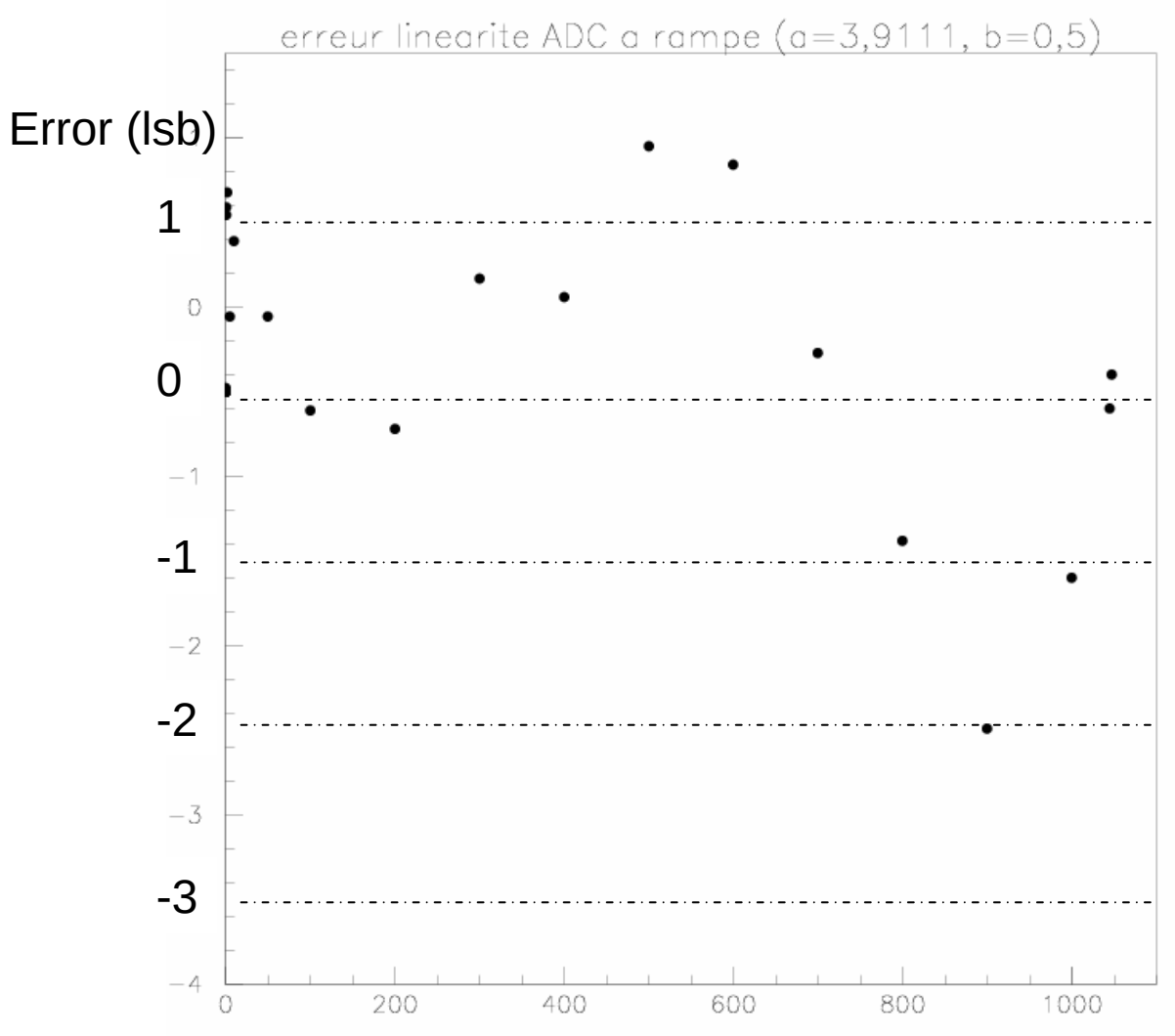
- **Main characteristics**
  - Fully differential structure (MC to MD input stage)
  - 1V input dynamic range
  - 12 bits output Gray code
  - Counting frequency: 50MHz → 82μs conversion time
  - Power supply: 3.5V (analog) and 2.5V (digital)
  - Power consumption < 3mW
- **One channel submitted in september 06**

LPCC Ramp ADC: layout (1 channel)

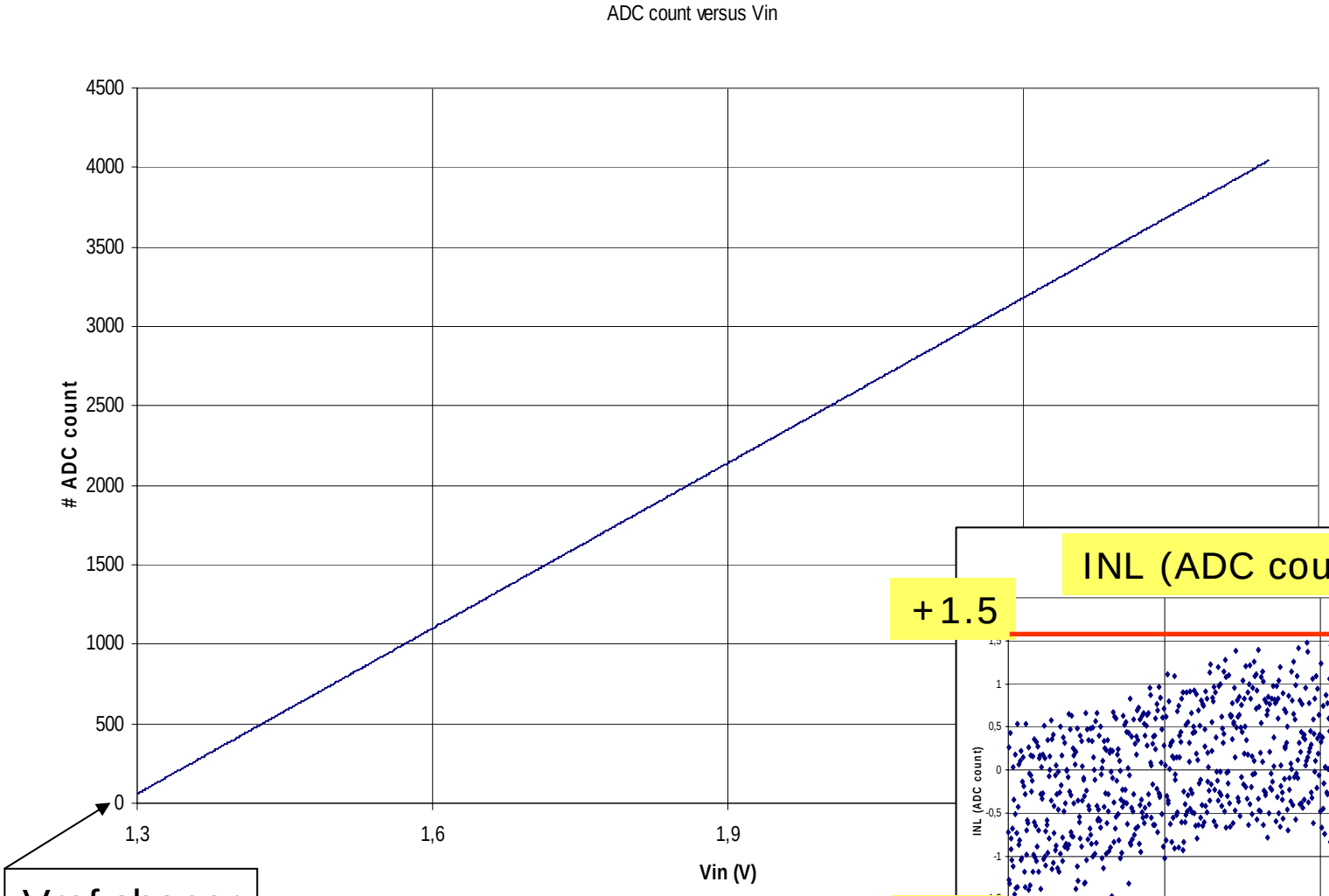
©G. Bohner (LPCC)



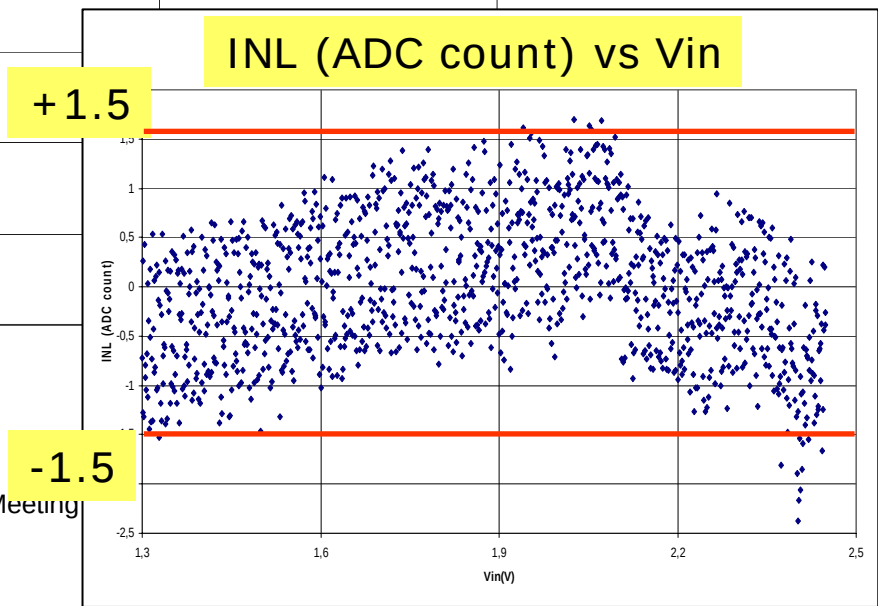
LPCC ADC : Linearity error (simulation)



MAROC2 : Wilkinson ADC linearity (Backup)



Vref shaper



SKIROC : dedicated to measurement

- Not designed for test beam but pure prototype
- 250 probing point embedded
- two 36 channel ADCs (LPCC + LAL as a backup)
- DAC 10 bits for threshold + 3 bits for fine tuning channel by channel
- Bandgap for reference voltages
- Digital on FPGA : flexibility

Conclusions

Second generation ASIC for ECAL read-out exists now

- SKIROC was submitted on nov 06
- It will come back in march 07
- Test board is now in preparation
- Digital bloc will be in FPGA to be tested together