SiD ECAL Status and Plans

David Strom – University of Oregon

- Detector concept
- Second sensor prototypes
- Cable status
- KPiXs news
- Test beam plans
- Energy resolution
- Simulations needed

Si-W work – personnel and responsibilities

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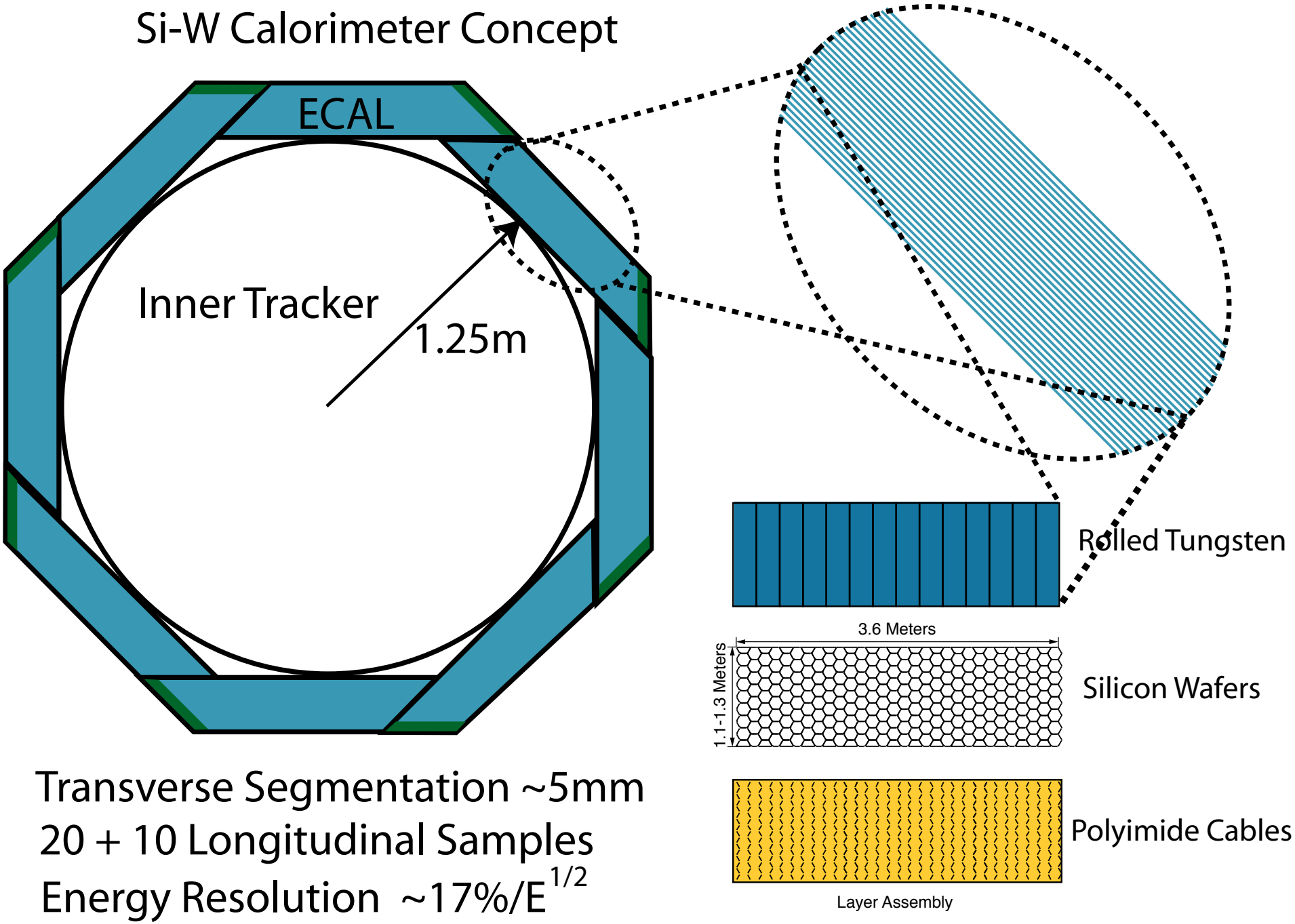
Annecy	BNL	UC-Davis	Oregon*	SLAC
Mechanics	**Electronics**	**Bump Bonding** **Cabling** Mechanics	**Si Detectors** Mechanics Simulation	**Electronics** Mechanics **Simulation**

* This work includes contributions from Oregon students Mary Robinson and Asher Tubman.

Si-W Calorimeter Concept



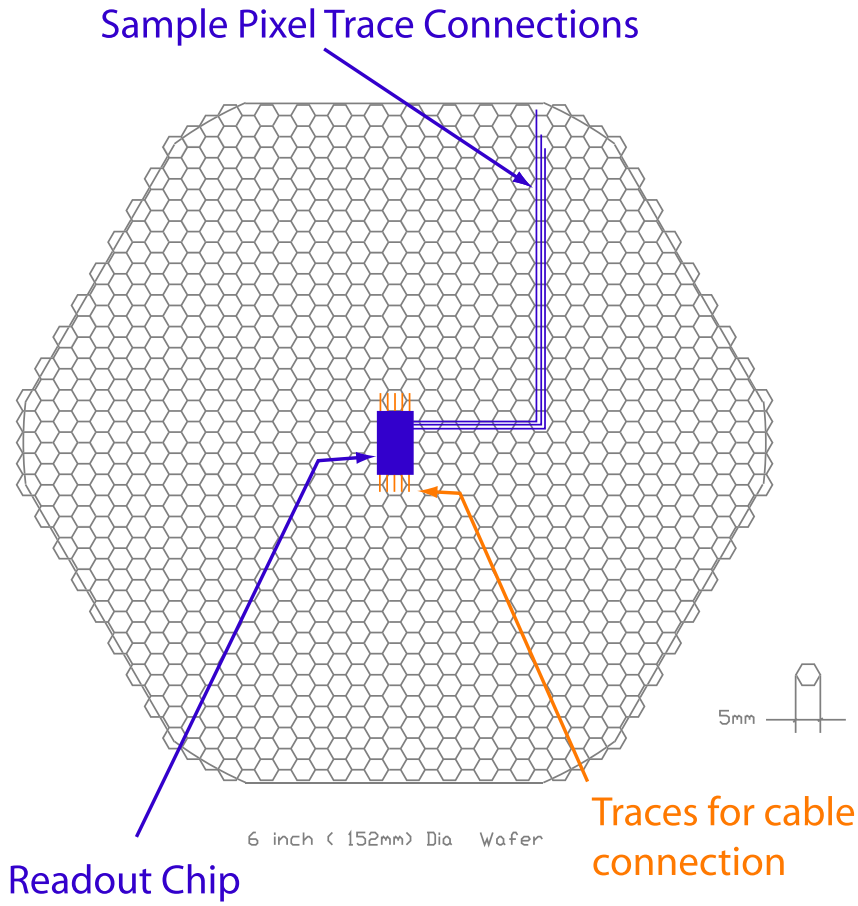
Transverse Segmentation ~5mm

20 + 10 Longitudinal Samples

Energy Resolution ~17%/$E^{1/2}$

Silicon Concept

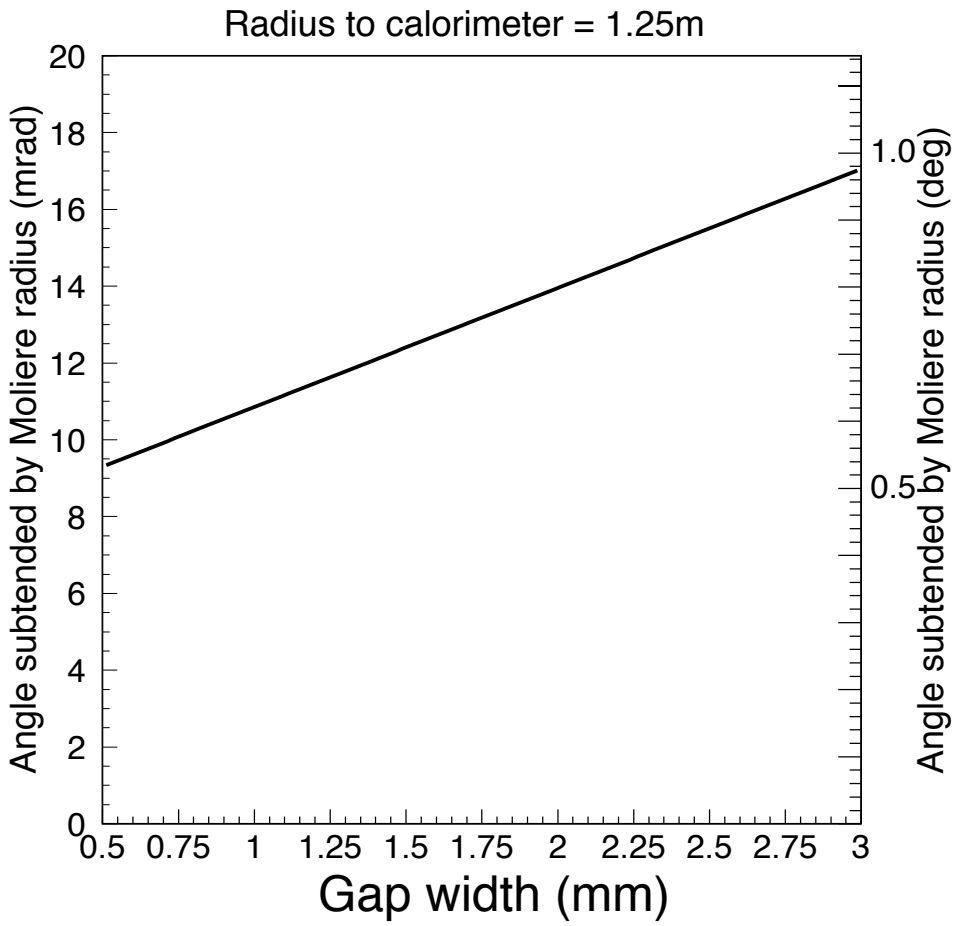
- Readout each wafer with a single chip
- Bump bond chip to wafer
- To first order cost independent of pixels /wafer
- Hexagonal shape makes optimal use of Si wafer
- Channel count limited by power consumption and area of readout end chip
- May want different pad layout in forward region



Critical parameter: gap between tungsten layers.

Config.	Radiation length	Molière Radius
100% W	3.5mm	9mm
92.5% W	3.9mm	10mm
+1mm gap	5.5mm	14mm
+1mmCu	6.4mm	17mm

Assumes 2.5mm thick tungsten absorber plates



Need to separate EM clusters so that track-EM cluster association can be performed

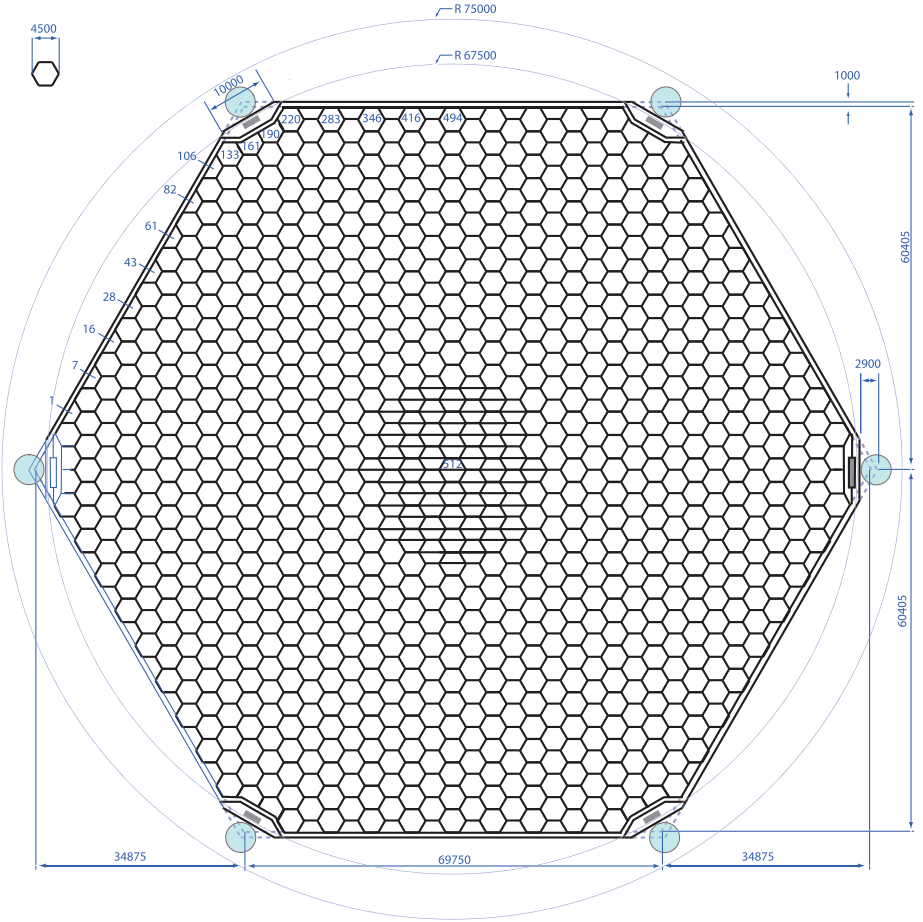
Impact of gap on PFAs is not yet quantified with simulations

Changes to sensor geometry:

- Current detectors have 757 pixels. Try for 1024 pixels
- Optimize stray capacitance for cold machine
- Current detectors do not have vertices removed
- Increase bump-bonding pad size to $70\,\mu$m $\times$ $70\,\mu$m (allows for easy gold stud bonding)

New detector layout

- $973 + 51$ pixels
- Possible top side bias
- Vertices removed to allow for spacers
- Long dimension of the pixel is 4.5 mm
- Pixel area is $(3.63\,\mathrm{mm})^2$
- Maximum radial dimension of active area is < 67.5 mm



Implication for dead space

- Dead space is dominated by edges

- Hexagonal detectors give lowest possible dead space

$$f_{dead} = \frac{4(w_g + c)}{\sqrt{3}h} \sim 5\%$$

where w_g is the guard ring thickness (1mm) and c is half the clearance between detectors (0.4mm). For proof http://arxiv.org/abs/math.MG/9906042/

- Lost area at vertices is about 0.7%

- Lost area for top side bias is about 1.4%

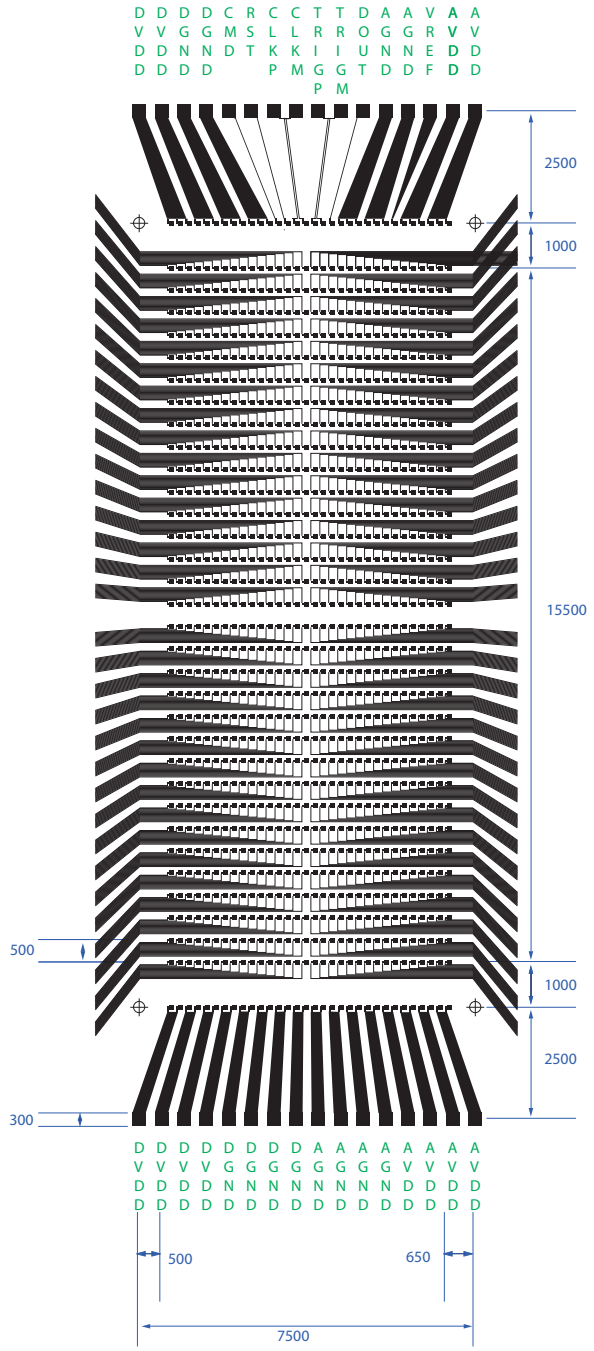
- Trace layout minimizes maximum capacitance

- Use thinner traces near KPiXs chip

- Low resistance power and ground connections

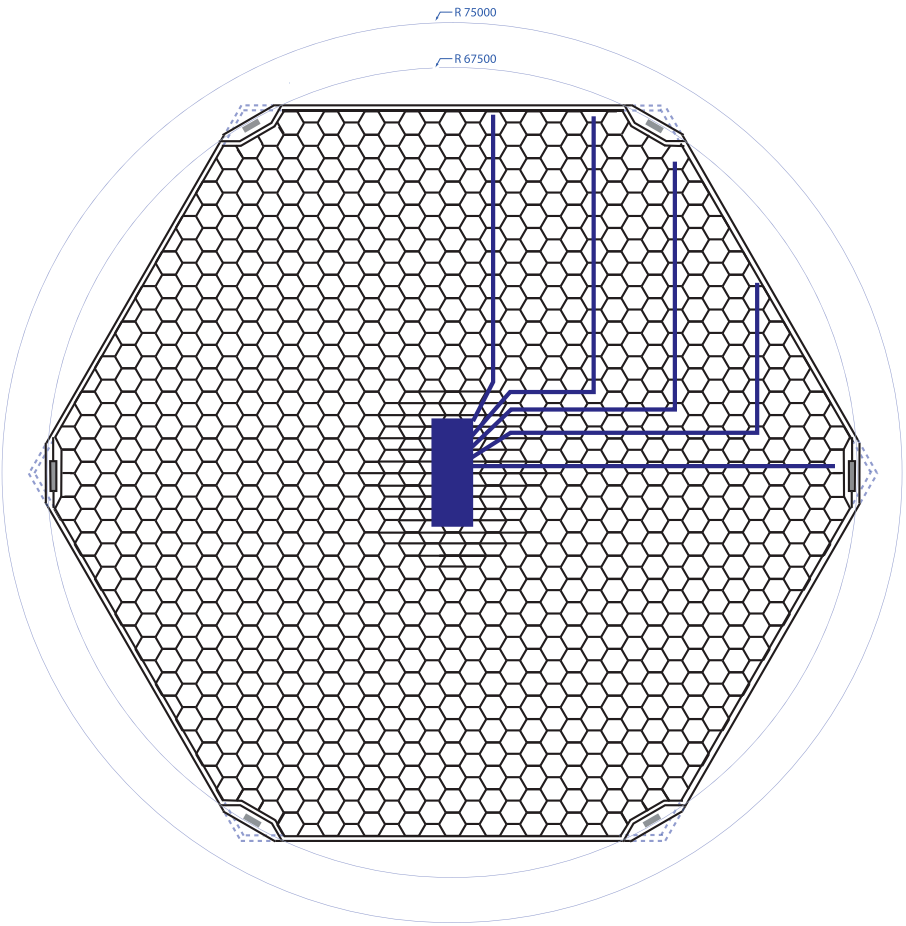
$\Rightarrow$ total resistance for power and ground $\sim 50\,\mathrm{m}\Omega$ or 50Ω/channel

- Symmetric clock signals



- Suggested trace routing

- Spread out traces to keep input capacitance constant



Detector Thickness: Stick with $\sim 300\,\mu$m detectors

Depletion depth is given by

$$d = \sqrt{2 k_{Si} \epsilon_0 \mu \rho (V + V_{bi})}$$

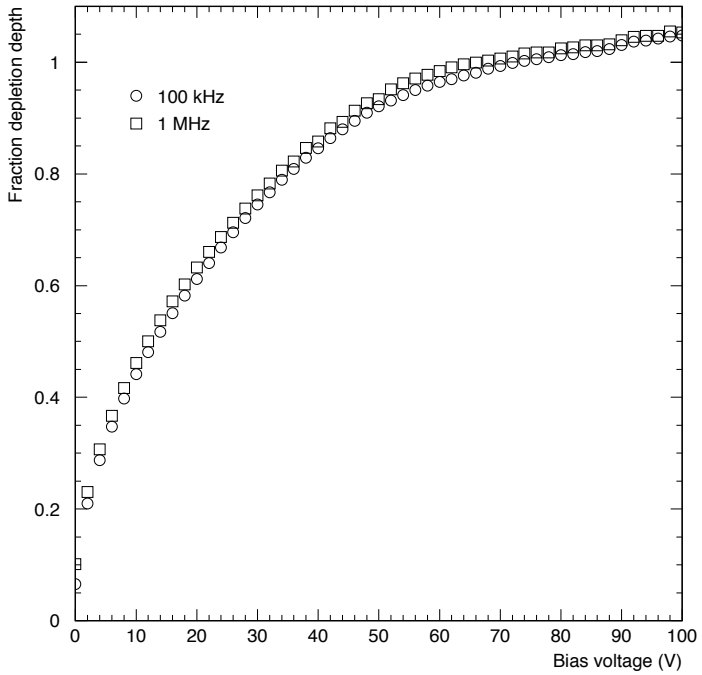
where

μ is the mobility,

ρ is the resistivity,

V is the bias voltage,

V_{bi} is the built in voltage.



- Increasing the detector thickness to 500μm could require bias voltages as high as 300 Volts.

- To keep detectors cheap we want to have minimal requirements on ρ

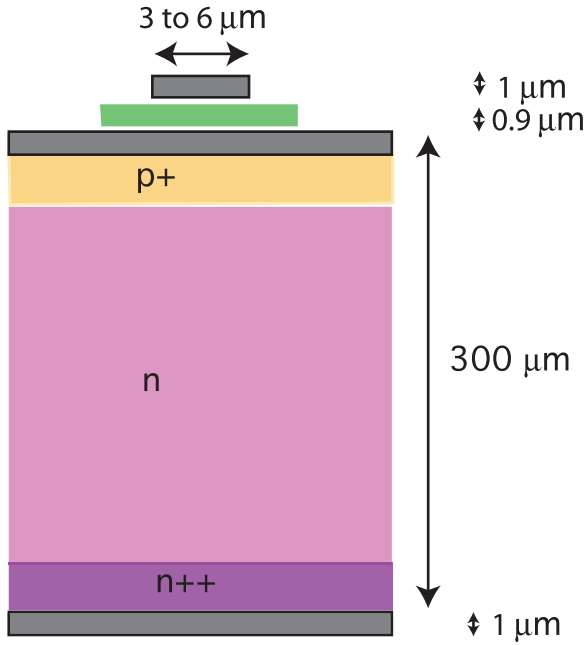
Silicon Detector Summary

• Designed to minimize cost of silicon production:

– detectors are DC coupled

– oxide thickness kept thin to decrease cost

– only extravagance is top side bias



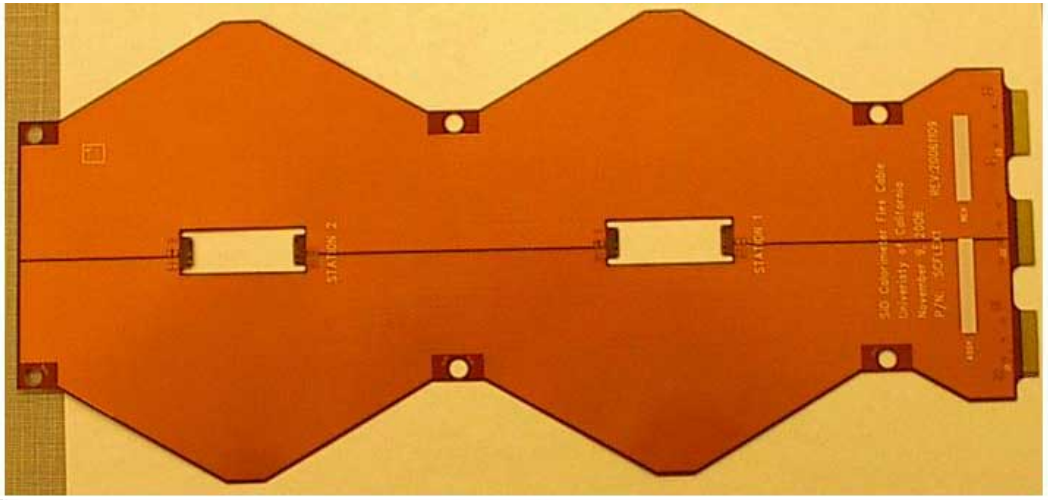
First quote from vendors in line with expectations
We can buy 40 detectors if we get requested funds

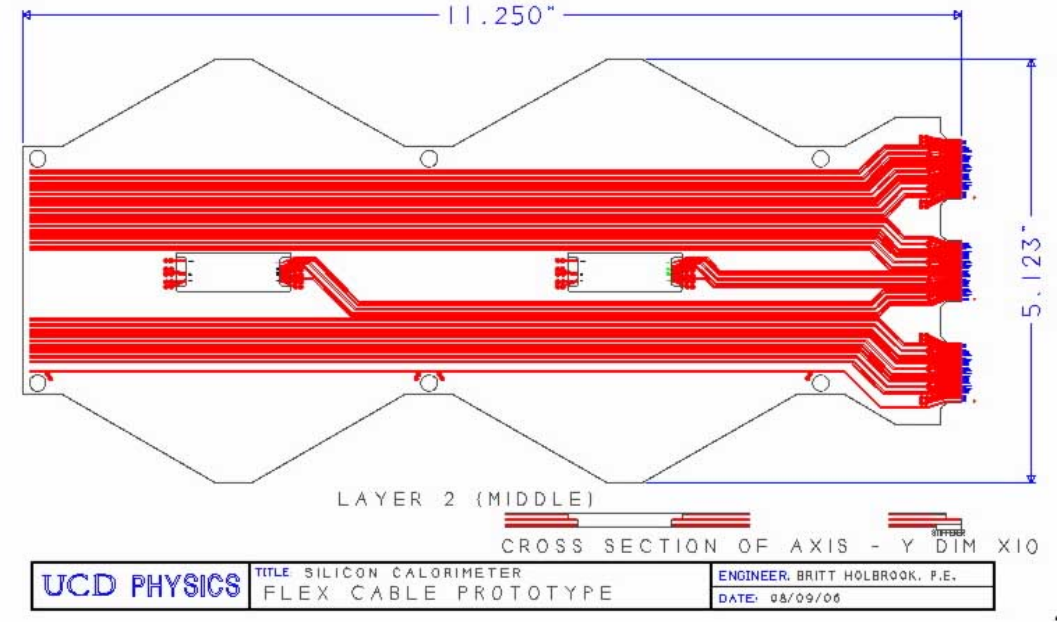
Flex Cable Development (UC Davis):

- First prototype with 2 chip stations has been fabricated.

- Each cut-out has inner lips which can be used for either wire-bonding or some other Technology.

- The layout has a buried layer for signals, sandwiched between power and ground layers.



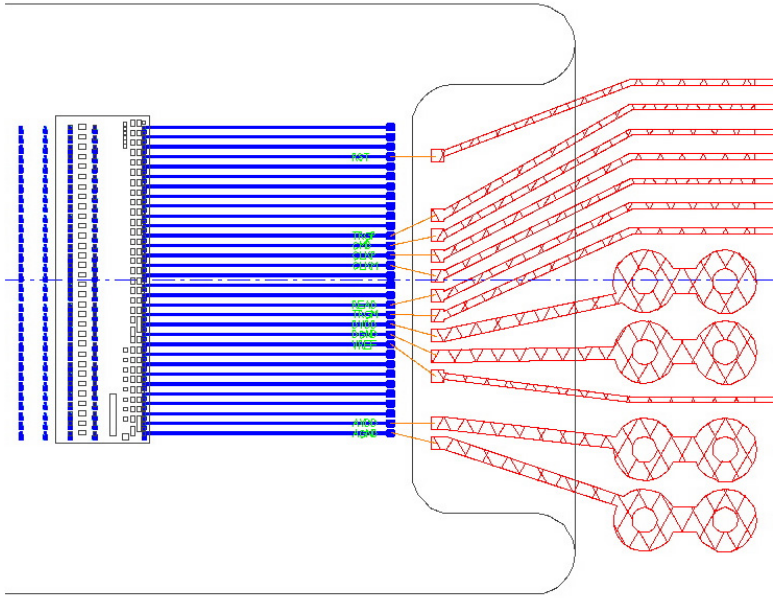


Davis, cont.

A test-board housing two KPix chips is being fabricated.

The flex cable will be wire-bonded directly to the KPix chips.

Another board to interface with the test board/DAQ is being designed.



Next Steps:

• A prototype long cable with 6-8 chip stations will be attempted. Some alignment issues for vias and other manufacturing concerns will be addressed.

• Gold-bumps will be investigated as a possible solution for connecting to the Si sensor wafer. Under bump metallization will most likely be necessary.

• LCRD funds support a part time technician (Tiffany Landry) for this work. Senior Engineer (Britt Holbrook) who does the design work is supported by University funds.

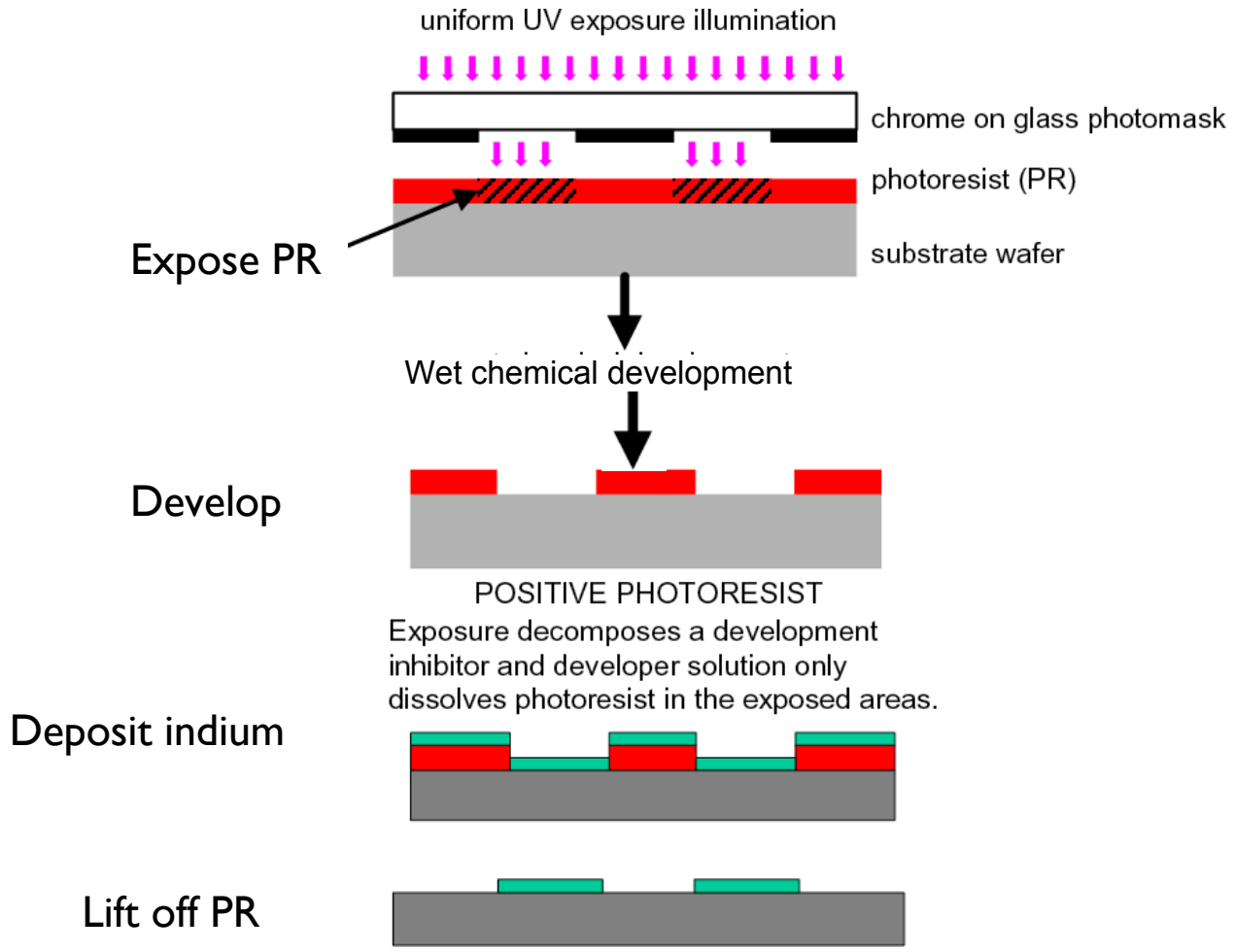
Photolithography

UC Davis has facilities for compete bump process with indium bumps using photo-lithography

- Class 100 clean-room
- PR spinning, development
- Mask making
- Aligner, UV exposure
- Ti/W sputtering

Physics Lab facilities include:

- Indium deposition
- Bump bonder

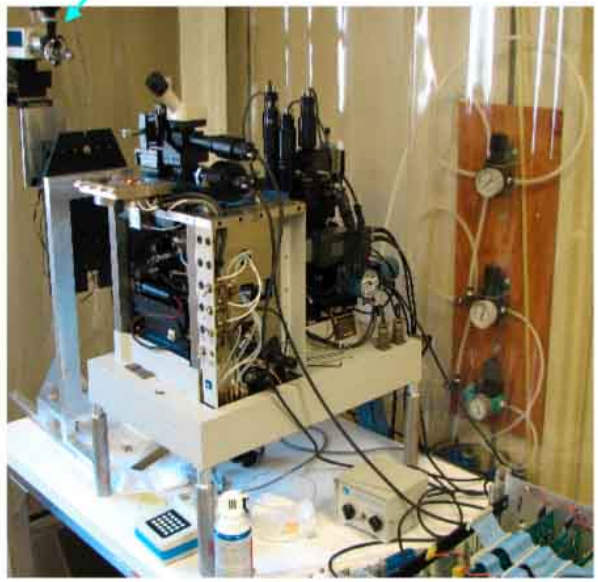


UV exposure through mask

Indium deposition

Ti/W sputter

IR Camera **Bump Bonding**



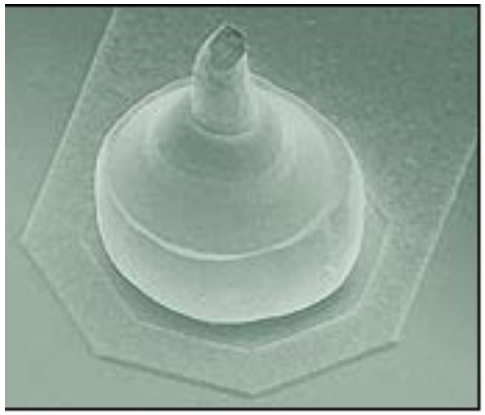
Investigating gold-bumps for connection to chip and cable for final assembly:

• Commercial processes are often designed to bond two wafers of chips to each other

• Gold stud bonding is similar to wire bonding and can easily operate on our 200 μm pitch

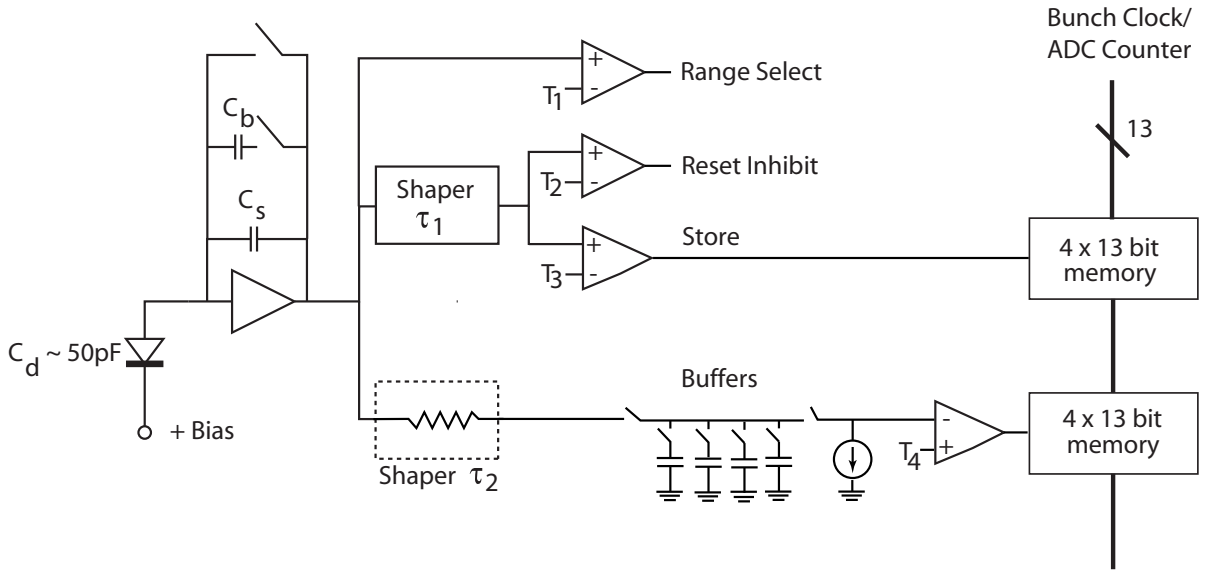
• Commercial machines can apply 16 bumps/second (68 seconds/detector)

• Possible drawback is gold contamination of silicon (should be no worse than wire bonds) May require Ti/W barrier as for indium bonding.



KPiXs News

Extremely Simplified Schematic

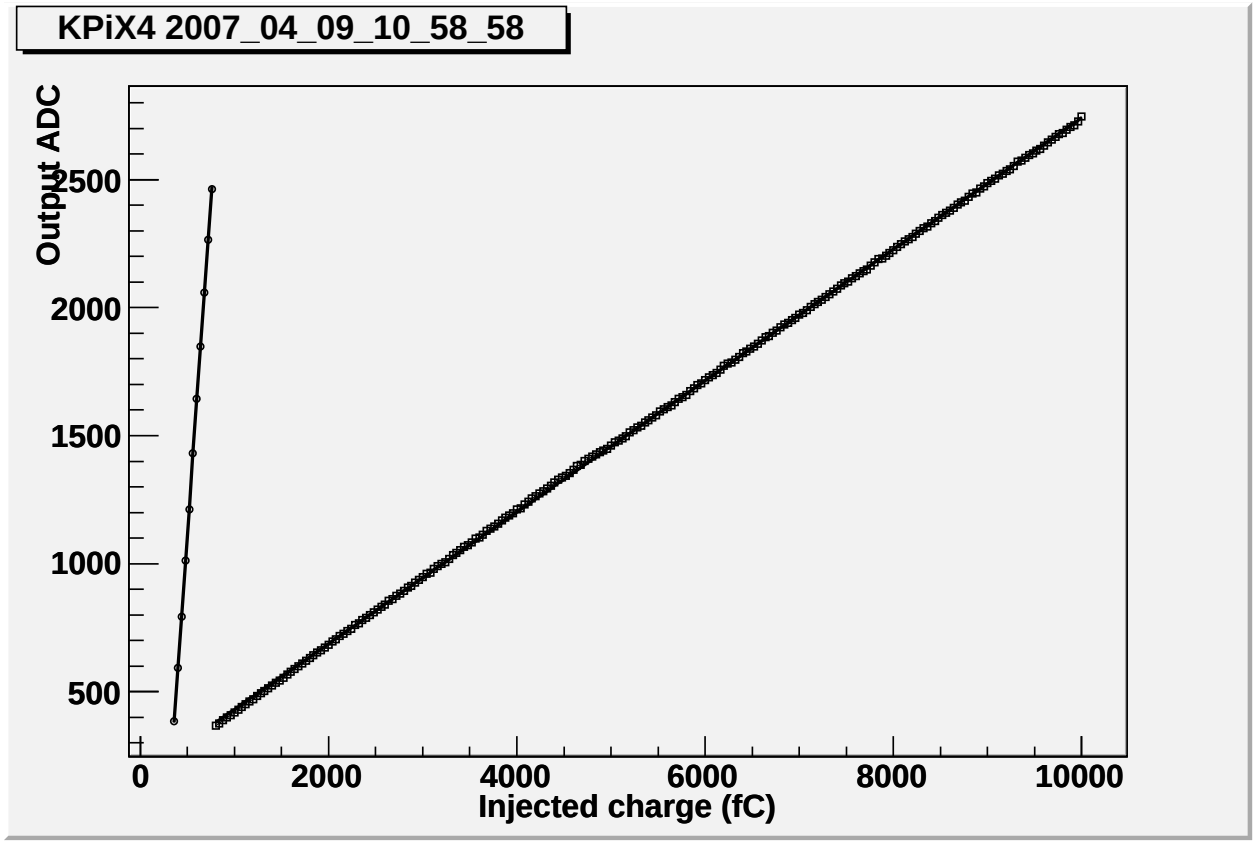


- KPiX can store up to four four pairs of analog charges and time stamps per train
- Low noise performance at output of shaper paramount
- Power pulsing causes no problems
- Digitization occurs between trains
- Novel scheme feedback scheme used to get up to 16 bit dynamic range ($C_b = 25 \times C_s$)
- Range switching occurs at about 1V

New Features on KPiX

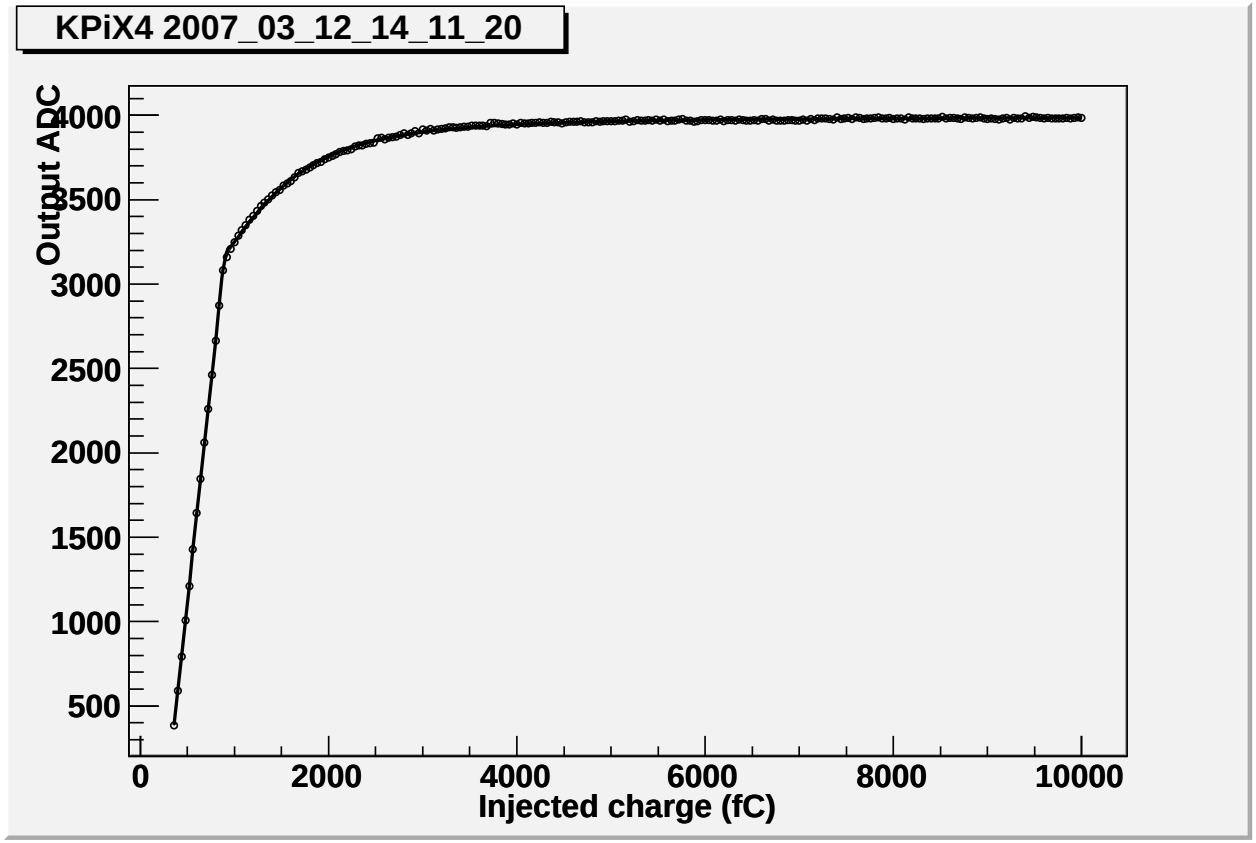
- Improved Analog/Digital isolation (KPiX 3 and KPiX 4)
- Polarity switching (not shown) (KPiX 3)
- External trigger for test beam use (KPiX3)
- Nearest neighbor switching (KPiX4)
- Improved shaper (KPiX4)
- Optional double gain mode for tracking (KPiX4)

Novel Feature works:



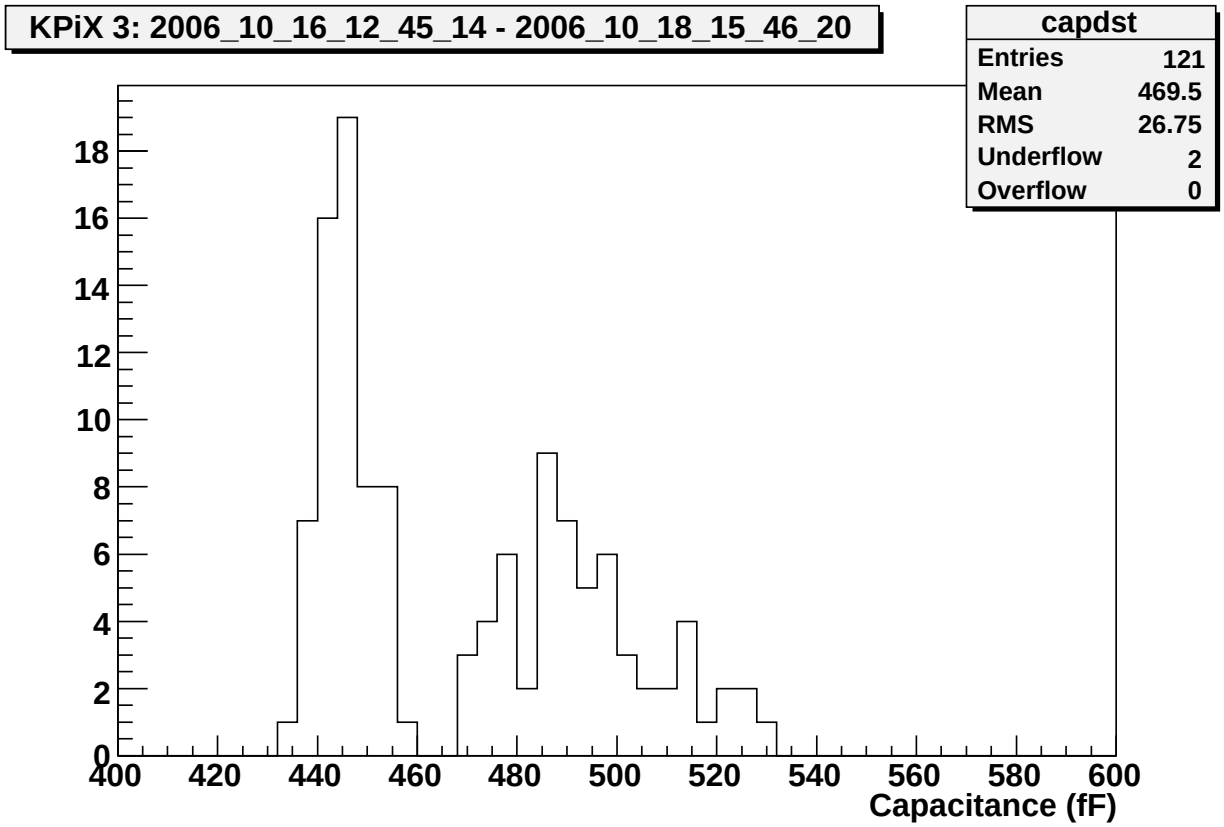
Shows whole chain works properly.

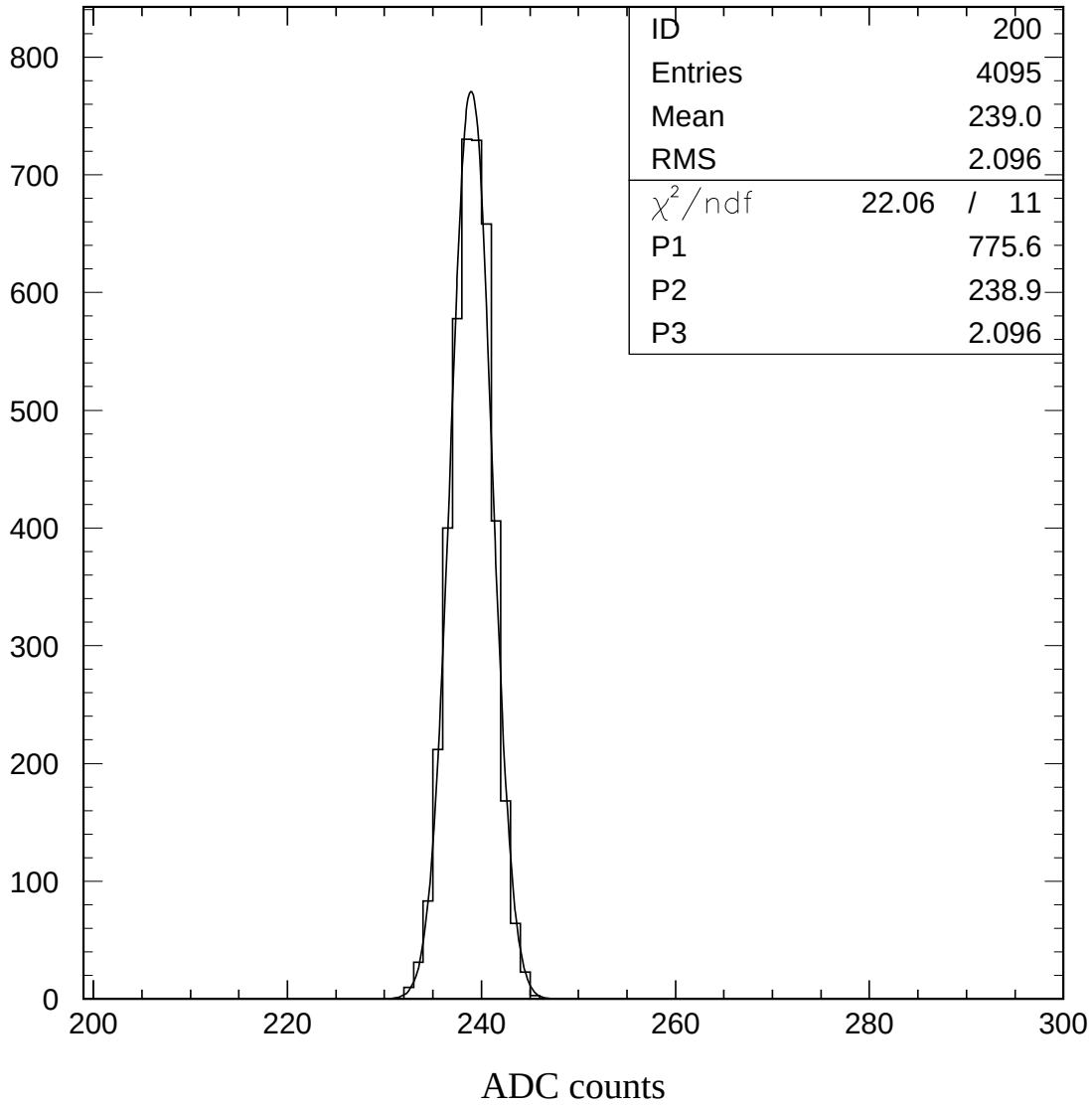
KPiX saturations gracefully (range switching disabled here):



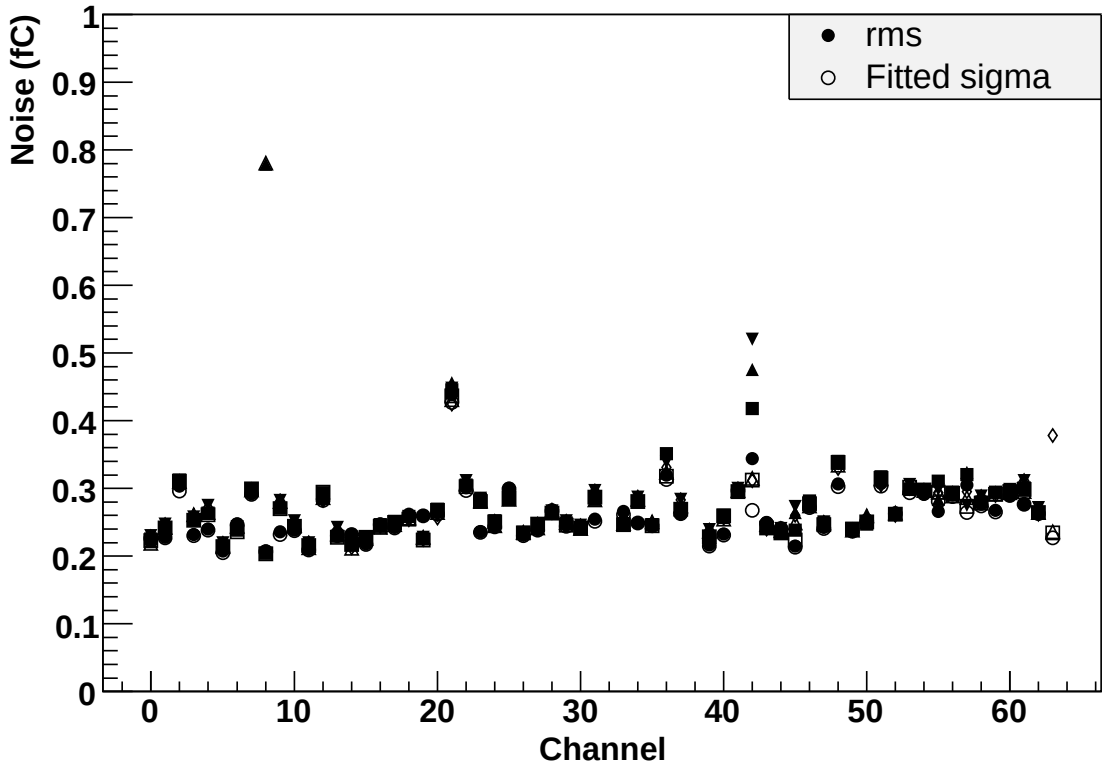
We expect similar behavior for the high gain scale. Linear range of high gain extends well beyond nominal 400fC. We expect low gain scale to extend well beyond nominal 10,000fC.

One can adjust the range threshold to measure the charge amp gain, or equivalently the size of its feedback capacitor





Typical noise in the ADC corresponds to less than 0.5 fC.



Some of the outliers are channels with extra connections – KPiX4 a factor of 2 better than KPiX3. This KPiX was wire bonded to a small strip detector.

Status

• Almost all functionality of KPiX has been demonstrated (e.g. range switching, bias current adjustment, external trigger, noise at reasonable level for calorimeter test beam measurements)

• Currently running a KPiX wire-bonded to strip detector at SLAC
⇒ See signals from β sources

• Working on demonstrating low threshold of trigger
(not needed for test beam)

• Many small changes to KPiX4 have accumulated (e.g. some MOS capacitors replaced with metal capacitors, further improvements needed to decouple analog and digital sections)

• KPiX5 will be needed before moving to KPiX 1024.

Testing plans – including testbeam

- Test KPiX-n with 6 cm $\times$ 6 cm detectors with 1 cm $\times$ 1 cm pixels – could be tested in beam
  (Also testing KPiX-n with strip detectors)

- Bump bond a KPiX-n chip to an existing 757 pixel prototype detector, use prototype cable – test in beam

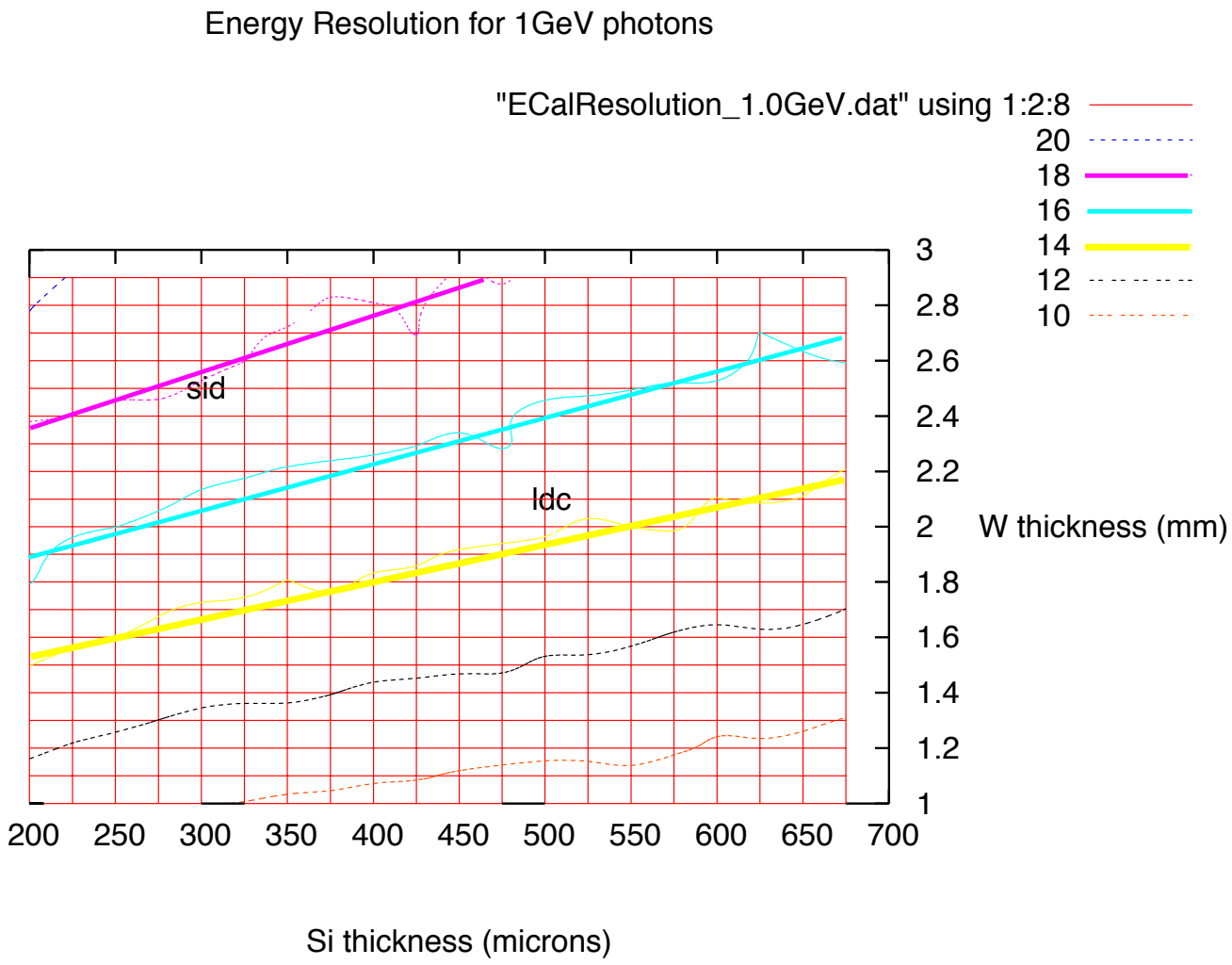
- Test single KPiX1024 and prototype II detectors – test in beam

- Build 30 $\times$ 1 wafer prototype – test in beam

Energy Resolution

Energy resolution depends on

- Tungsten thickness
- Silicon thickness
- Detector depth



Iso-resolution contours from Norman Graf

Line fit by eye (Strom)

Norman finds the resolution is given by

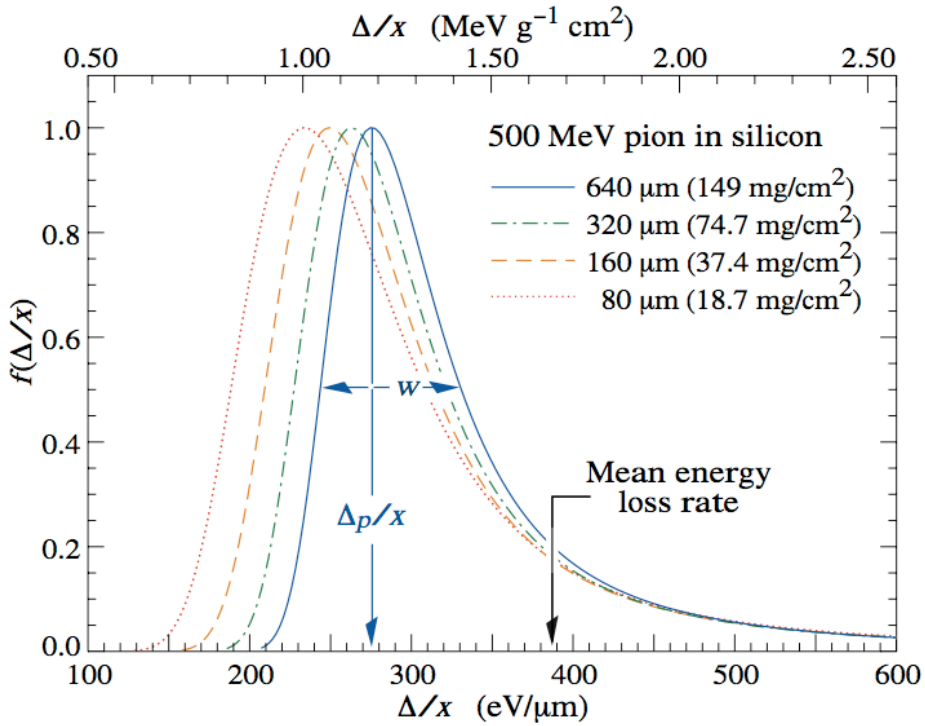
$$\frac{\sigma}{E} \simeq \left[-1.8\left(\frac{t_{Si}}{300\mu\text{m}}\right) + 11.5\left(\frac{t_W}{2.5\text{mm}}\right) + 8\right]\%$$

where t_{Si} is the silicon thickness and t_W is the tungsten thickness

- Doubling silicon thickness to 600μm would reduce resolution by 1.8%
- Decreasing tungsten thickness by 5% would reduce resolution by 1.4%

Optimization of ECAL sampling and study of digital HCAL to catch leakage not yet complete

Ray Frey found that change in resolution is consistent with the expected change in fluctuations in energy deposition with silicon thickness



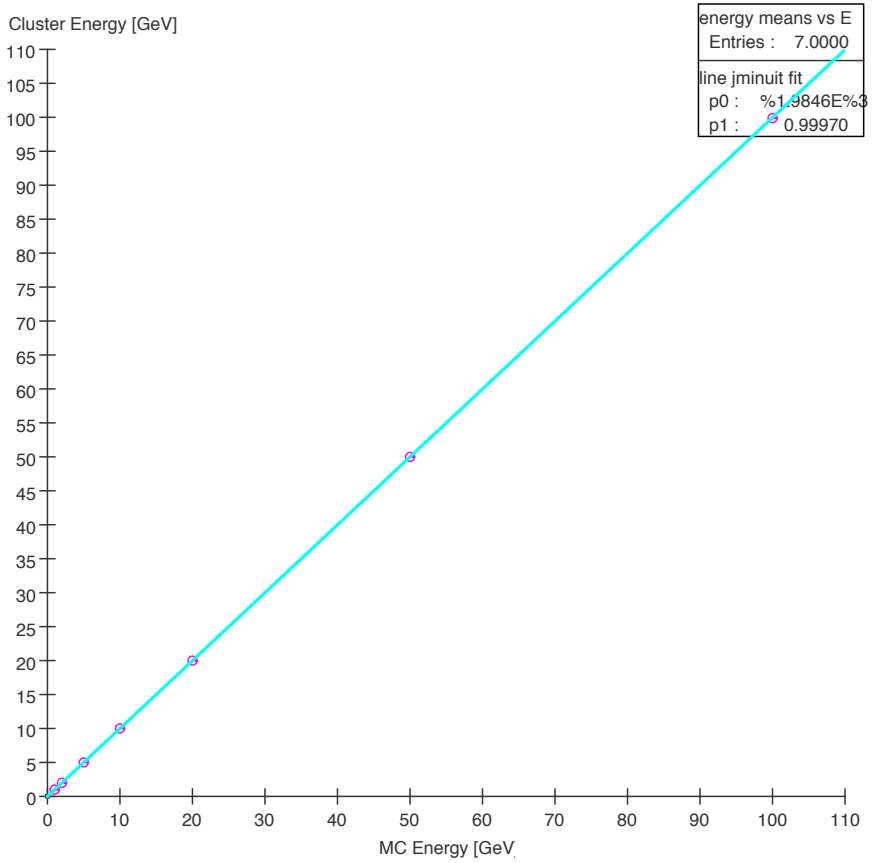
PDG, H. Bichsel, Rev. Mod. Phys. 60, 663 (1988).

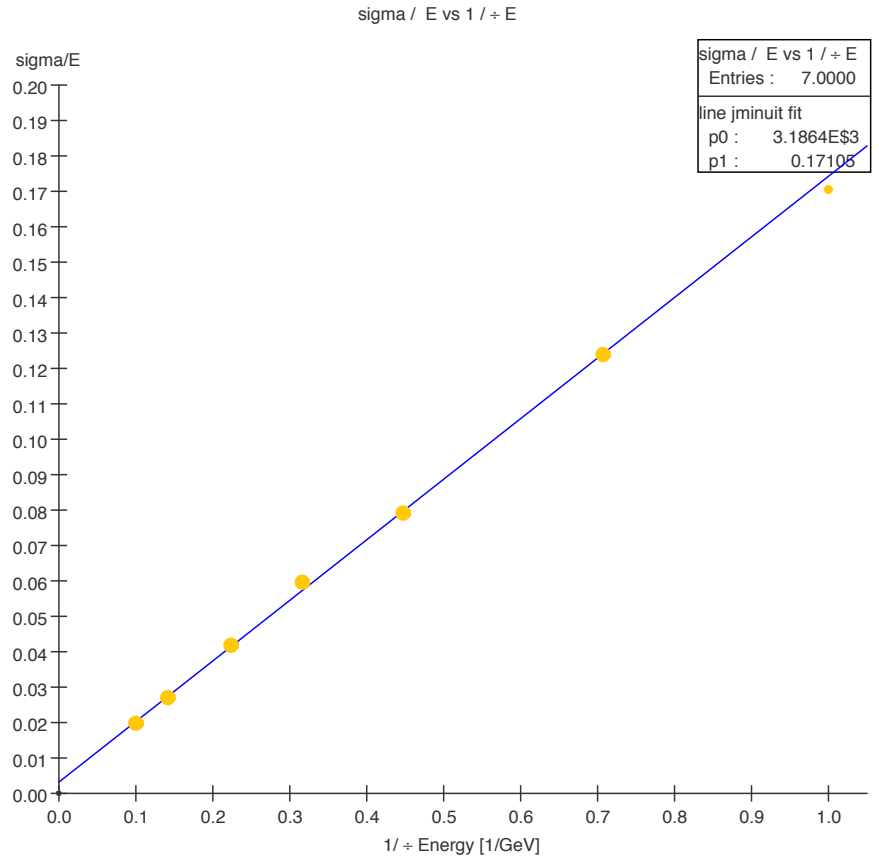
For $t = 320\mu$m $\frac{w}{\Delta} = 2.884$
For $t = 640\mu$m $\frac{w}{\Delta} = 3.883$

Here Δ is mean and w is full width at half max

Default configuration: 20 thin layers (2.5mm, dens24)
10 thick layers (5.00mm, dens24)

Norman Graf finds ideal behavior with proper weighting, energy and resolution scales ACME0605 with dens25, ecal 2.71mm, 5.43mm, 7.5mm hcal +scint





Physics case for better energy resolution unclear:

- Jet energy resolution depends mostly on few GeV photons:

  $\Rightarrow$ implies finer sampling in front of calorimeter
  $\Rightarrow$ better Molière radius of thicker sampling probably will give better jet energy resolution

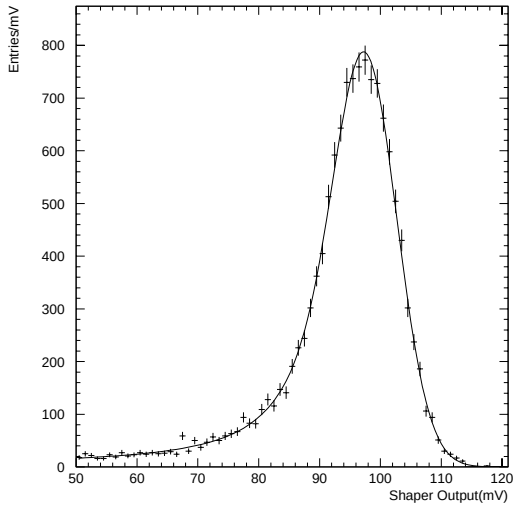
- Is there a physics case for energy resolution below 2% for high energy clusters?

  e.g. $H \rightarrow \gamma\gamma$
  see hep-ph/9610417, hep-ph/9607360
  Do we need dedicated SiD work here?

This process can be measured at the LHC. Requires measurement of $\gamma\gamma \rightarrow h$

Better resolution for high energy electromagnetic showers would require sub 1% calibration. This will be challenging.

• Use 60KeV Gamma's from Am^{241} to determine values of calibration capacitors in each channel of KPiX (we have enough bits to do this) after module assembly but before they are shielded by tungsten.



• Control external calibration voltage to better than 1%

• Perform electronics calibration often

• Some offsets in KPiXs calibration depend on transistor properties that may not be stable. Must be studied.

Needed software studies:

- Longitudinal segmentation
  - Particle flow (e.g. soft photons need more early samplings?)
  - Id of tau states (EM resolution)
  - π^0 reconstruction (G. Wilson)
  - How well does to the HCAL work for leakage
- Transverse segmentation
  - Cluster splitting algorithms
  - EM shower id

  (Good progress with H-Matrix (Norman Graf, Graham Wilson+student)
  Need 3-D studies – No PFA to-date uses available information from ECAL
- Existential studies
  - What processes require $\frac{\Delta E}{E} = 3\%$ energy PFA energy resolution?

  See benchmark talk
  - PFAs are most sensitive to HCAL – ECAL studies on back burner

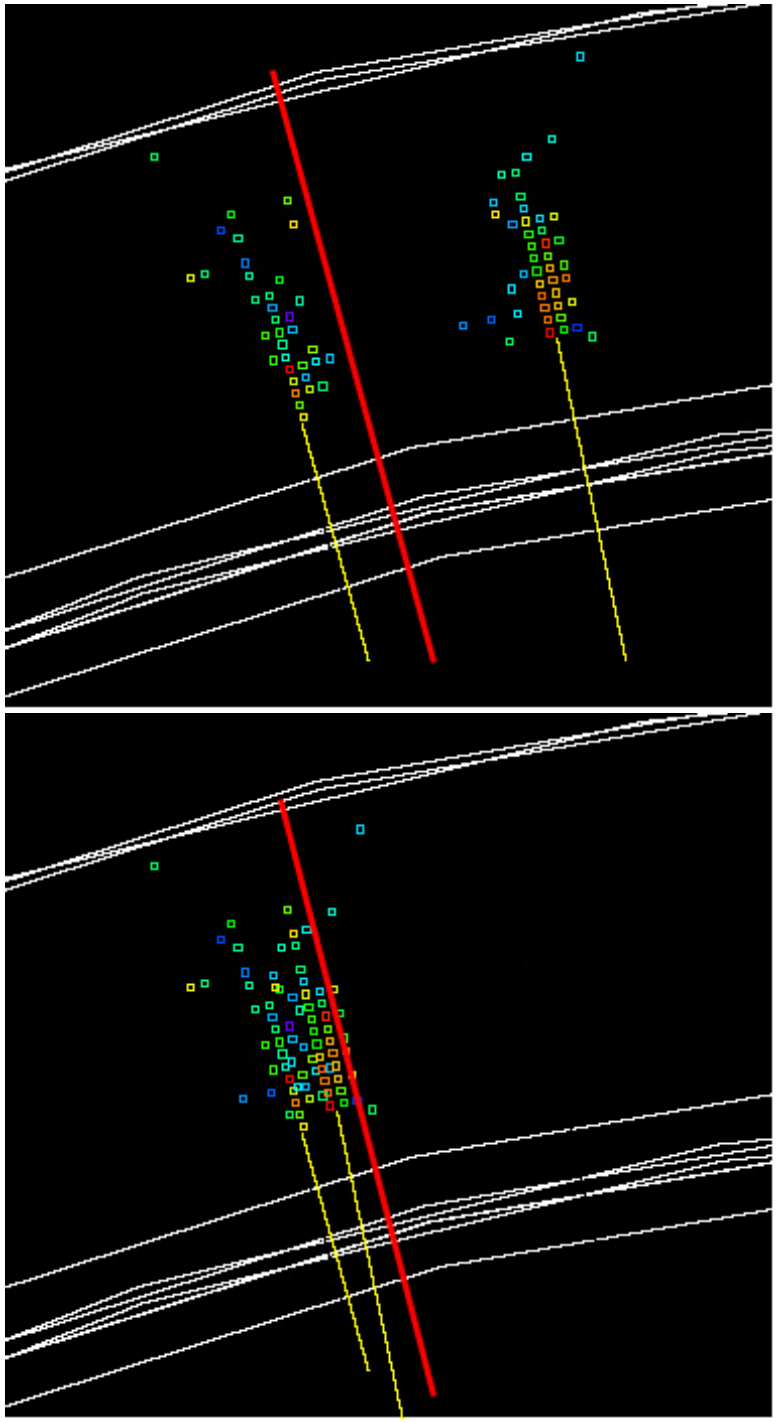
  We will be able to defend the high cost of the SiW ECAL?
  - Tau polarization from new physics, is it crucial?
  - Electrons in jets, neutrino reconstruction

For unmerged photons, it is easy to separate charged and neutral energy

The real job of the ECAL is to separate merged clusters so that charged and neutral energy can be separated

⇒ Need 3D H-matrix or similar

⇒ Important for Taus!



Summary

- New sensor design ready for fabrication
- Prototype cable fabricated, testing with wire bonded chips
- Much of KPiX functionality is demonstrated – simulation largerly agrees with measurements
- Testing schedule will depend on KPiX