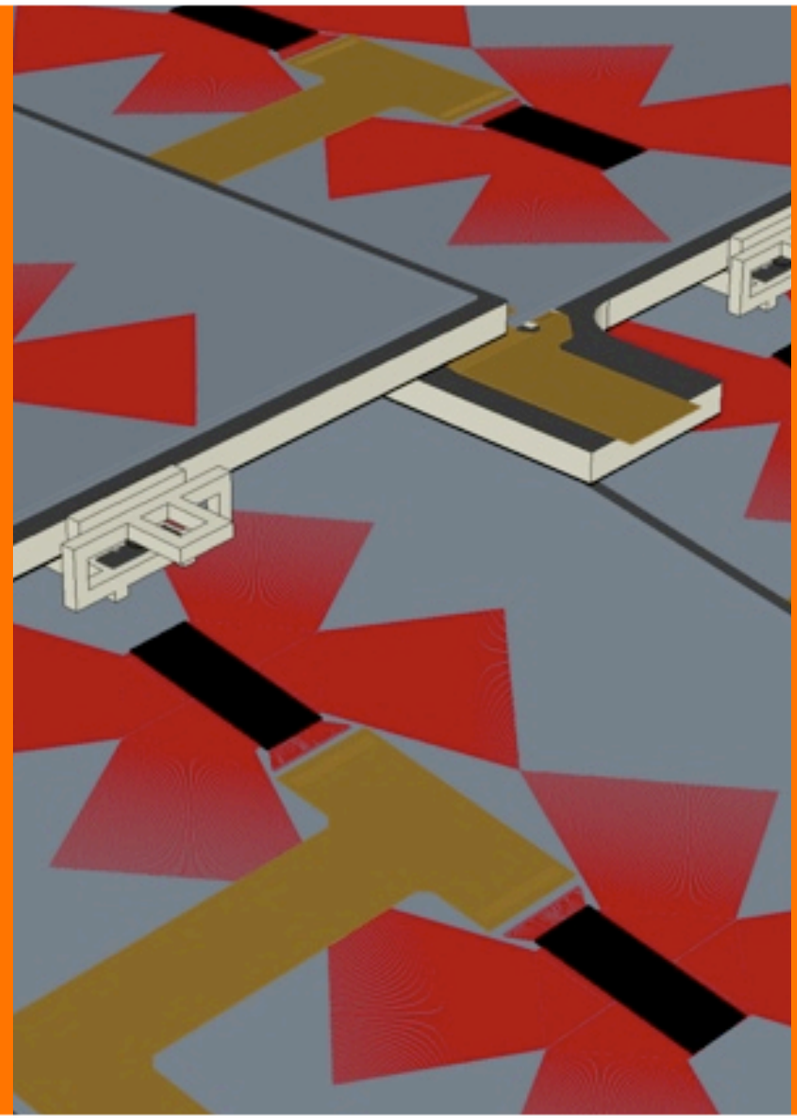
Prototype Sensor Design and Specifications



Tim Nelson

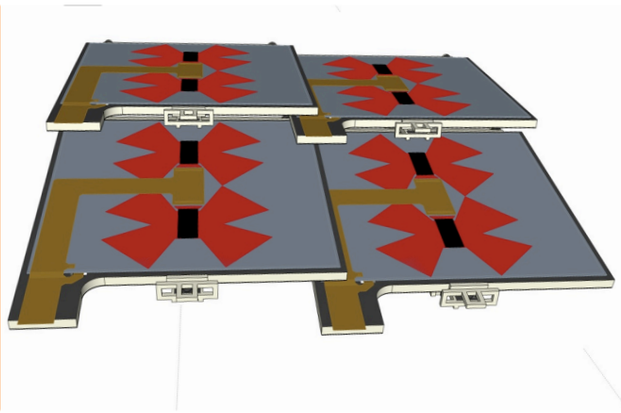
SiD

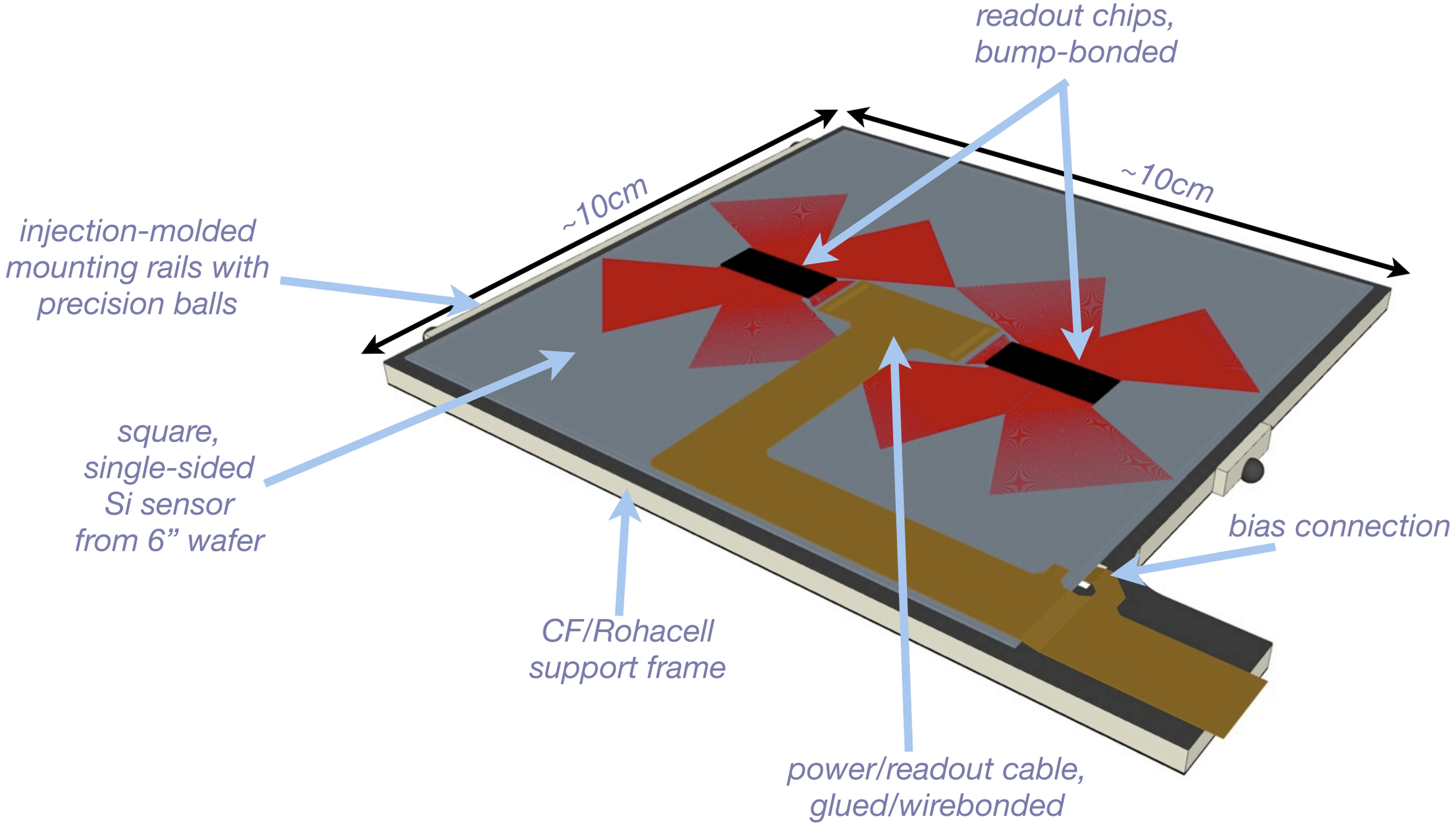
SLAC

SiD Workshop

FNAL - April 9, 2007

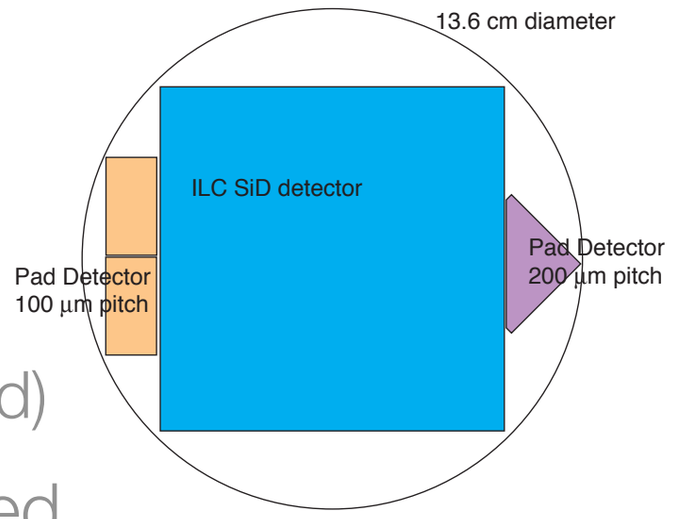
Barrel Module Concept





Status and Recent Changes

- Sensor design review 11/29/06, several constructive suggestions
  - Reworked double-metal power/readout connections
  - Capacitance calculations by Zhijing Tang (FNAL) - more changes?
  - Small changes to spec
- Proposal for additional prototypes/test structures
  - DC coupled charge-division readout sensor
  - Pixel sensors from Hiro Tajima (willing to pay for area used)
- Feedback on specs from HPK (Yamamura) and continued consideration have led to more changes to drawings and spec

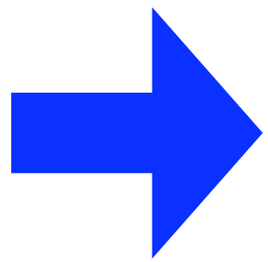


H. Tajima - SLAC

Need final agreement on design, drawings and specification so we can get HPK started for delivery this FY.

Delivery

Number of devices	20 sensors
Schedule	Delivery before 02/2007

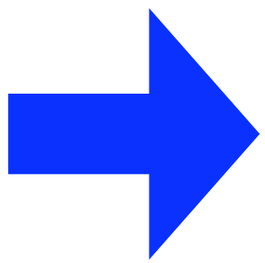


Number of devices	20 sensors, diced
Schedule	Delivery before 08/2007

Propose to change this to end of FY07

Wafer Specs

Parameter	Value
Thickness	300 μm $\pm$ 20 μm
Wafer diameter	6 inch
Wafer type (orientation)	n-type (<100>)
Resistivity	*see depletion voltage spec*
Wafer warp	<80 μm (on best-effort basis)
Polishing	mirror finish on one side



Parameter	Value
Wafer diameter	6 inch
Thickness	320 μm $\pm$ 20 μm
Wafer type (orientation)	n-type (<100>)
Resistivity	*see depletion voltage spec*
Wafer warp	<80 μm (on best-effort basis)
Polishing	mirror finish on one side

Propose no further changes

Sensor Specs (from Review)

Parameter	Value
Overall Dimensions	93.531mm×93.531mm
Active Area	92.031mm×92.031mm
Strip pitch	25 μm
Readout pitch	50 μm
Number of strips	3679
Number of readout strips	1840
Depletion voltage	60V$<V_{dep}<$100V
~~Depletion voltage uniformity~~	~~$<20\%$~~
Biasing scheme	poly resistors along both edges
Poly resistor value	4.5 ± 0.5MΩ
Implant strip width	8 μm
~~Implant depth~~	~~$>1\mu$m~~
~~Doping of Implant~~	~~$>1\times10^{14}$ ions/cm^3~~
Width of Al sense strips	7 to 8 μm
Width of Al readout traces (double-metal)	3 to 4 μm
~~Thickness of Al traces (all)~~	~~$>1\mu$m~~
Resistivity of Al sense strips	$<30\Omega$/cm
Resistivity of Al readout traces (double-metal)	$<60\Omega$/cm
Thickness of insulating layer between metal layers	3 μm
Coupling capacitor value	>10 pf/cm
Passivation	SiO_2 0.5-1.0μm thick
Width of unpassivated regions along bias ring	$\geq 200\mu$m
Junction breakdown	>200 V
Micro-discharge breakdown	>150 V
Coupling capacitor breakdown	>100 V
Total detector current at 150V	$<20\mu$ A
Interstrip capacitance	<1.2 pf/cm
Non-working strips	<20 strips detector

Parameter	Value
Overall Dimensions	93.531±0.1mm × 93.531±0.1mm
Active Area	92.031mm×92.031mm
Strip pitch	25 μm
Readout pitch	50 μm
Number of strips	3679
Number of readout strips	1840
Depletion voltage	<100V
Biasing scheme	poly resistors along both ends
Poly resistor value	20 ± 2MΩ
Implant strip width	7 to 8 μm
Width of Al sense strips	7 to 8 μm
Width of double-metal readout traces	3 to 4 μm
Resistivity of Al sense strips	$<20\Omega$/cm
Resistivity of double-metal readout traces	$<40\Omega$/cm
Insulation thickness between metal layers	0.9 μm (3 μm if possible) [1]
Coupling capacitor value	>10 pf/cm
Passivation (except bonding areas)	SiO_2 + Si_3N_4, 0.5-1.0μm thick
Width of unpassivated regions on bias ring	$\geq 200\mu$m
Junction breakdown	>200 V
Micro-discharge breakdown	>150 V
Coupling capacitor breakdown	>100 V
Total detector current at 150V	$<5\mu$ A
Interstrip capacitance	<1.2 pf/cm
Non-working strips	<20 strips detector

Sensor Specs (from Yamamura)

Parameter	Value
Overall Dimensions	93.531±0.1mm × 93.531±0.1mm
Active Area	92.031mm×92.031mm
Strip pitch	25 μm
Readout pitch	50 μm
Number of strips	3679
Number of readout strips	1840
Depletion voltage	<100V
Biasing scheme	poly resistors along both ends
Poly resistor value	20 ± 2MΩ
Implant strip width	7 to 8 μm
Width of Al sense strips	7 to 8 μm
Width of double-metal readout traces	3 to 4 μm
Resistivity of Al sense strips	$< 20\Omega$/cm
Resistivity of double-metal readout traces	$< 40\Omega$/cm
Insulation thickness between metal layers	0.9 μm (3 μm if possible) [1]
Coupling capacitor value	> 10 pf/cm
Passivation (except bonding areas)	SiO_2 + Si_3N_4, 0.5-1.0μm thick
Width of unpassivated regions on bias ring	$\geq 200\mu$m
Junction breakdown	> 200 V
Micro-discharge breakdown	> 150 V
Coupling capacitor breakdown	> 100 V
Total detector current at 150V	$< 5\mu$ A
Interstrip capacitance	< 1.2 pf/cm
Non-working strips	< 20 strips detector

Parameter	Value
Overall Dimensions	93.531±0.1mm × 93.531±0.1mm
Active Area	92.031mm×92.031mm
Strip pitch	25 μm
Readout pitch	50 μm
Number of strips	3679
Number of readout strips	1840
Depletion voltage	<100V
Biasing scheme	poly resistors along both ends
Poly resistor value	20-40MΩ
Implant strip width	8 to 9 μm
Width of Al sense strips	8 to 9 μm
Width of double-metal readout traces	3 to 4 μm
Resistivity of Al sense strips	$< 25\Omega$/cm
Resistivity of double-metal readout traces	$< 60\Omega$/cm
Insulation thickness between metal layers	0.9 μm (3 μm if possible) [1]
Coupling capacitor value	> 10 pf/cm
Passivation (except bonding areas)	SiO_2, 0.5-1.0μm thick
Width of unpassivated regions on bias ring	$\geq 200\mu$m
Junction breakdown	> 200 V
Micro-discharge breakdown	> 150 V
Coupling capacitor breakdown	> 100 V
Total detector current at 150V	$< 4\mu$A
Interstrip capacitance	< 1.2 pf/cm
Non-working strips	< 20 readout strips/detector

Need to correct or remove dimensions tolerance (now on drawing)

Thicker Oxide?

[1]For this application, it would be very desirable to achieve the thickest oxide possible between the metal layers. If necessary, loosening other specifications (e.g. wafer warp) to allow this processing is a possibility. The manufacturer is encouraged to make a proposal for modified specifications to allow for a thicker oxide layer.

Test and Measurement (from review)

5 Definition of Bad Channels

Parameter	Value	Defect
Coupling capacitor value	>1.1 × typical[1]	short
Coupling capacitor value	<0.9 × typical[1]	open
Coupling capacitor value	>1.1 × typical[1]/ normal neighbors	pinhole
Current through coupling capacitor	>1 nA	pinhole

6 Measurements by Manufacturer

1. Visual inspection of each sensor to ensure that there are no significant scratches, blemishes or edge chipping
2. Depletion voltage, measured on test structures of each wafer
3. Value of polysilicon resistor, measured on test structures of each wafer
4. Total leakage current up to 250V or until breakdown occurs
5. Probing of all strips to produce a list of bad (broken, shorted or open) strips on each sensor according to above definitions

5 Testing and Measurements by Manufacturer

All strips shall be tested for defects by measuring the capacitance value of the coupling capacitor and the current through the coupling capacitor to identify shorts, opens and pinholes. A channel with any of these three defects shall be considered a bad channel. Because of variations in the double-metal readout, it should be anticipated during testing that readout capacitances will vary across the sensor. For this reason, the expected capacitance for a strip will need to be defined by an average over some number of similar, neighboring strips.

In addition to providing a list of bad channels according to the above criteria, the vendor shall perform the following inspections and tests:

- A visual inspection of each sensor to ensure that there are no significant scratches, blemishes or edge chipping
- A measurement of the depletion voltage on test structures of each wafer
- A measurement of the interstrip capacitance on test structures of each wafer
- A measurement of the value of the polysilicon resistor on test structures of each wafer
- Total leakage current up to 250V or until breakdown occurs at intervals of 5V or less.

The bad channel lists and results of these tests shall be supplied in a .pdf file. In addition, the I-V data shall be supplied in spreadsheet format.

Propose no further changes

Test and Measurement (from Yamamura)

5 Testing and Measurements by Manufacturer

All strips shall be tested for defects by measuring the capacitance value of the coupling capacitor and the current through the coupling capacitor to identify shorts, opens and pinholes. A channel with any of these three defects shall be considered a bad channel. Because of variations in the double-metal readout, it should be anticipated during testing that readout capacitances will vary across the sensor. For this reason, the expected capacitance for a strip will need to be defined by an average over some number of similar, neighboring strips.

In addition to providing a list of bad channels according to the above criteria, the vendor shall perform the following inspections and tests:

- A visual inspection of each sensor to ensure that there are no significant scratches, blemishes or edge chipping
- A measurement of the depletion voltage on test structures of each wafer
- A measurement of the interstrip capacitance on test structures of each wafer
- A measurement of the value of the polysilicon resistor on test structures of each wafer
- Total leakage current up to 250V or until breakdown occurs at intervals of 5V or less.

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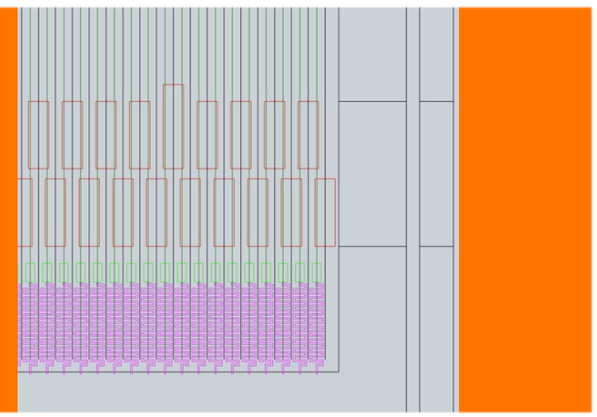
In addition to providing a list of bad channels according to the above criteria, the vendor shall perform the following inspections and tests:

- A visual inspection of each sensor to ensure that there are no significant scratches, blemishes or edge chipping
- A measurement of the depletion voltage on test structures of each wafer
- A measurement of the interstrip capacitance for each lot
- A measurement of the value of the polysilicon resistor on test structures of each lot
- Total leakage current up to 250V or until breakdown occurs at intervals of 5V or less.

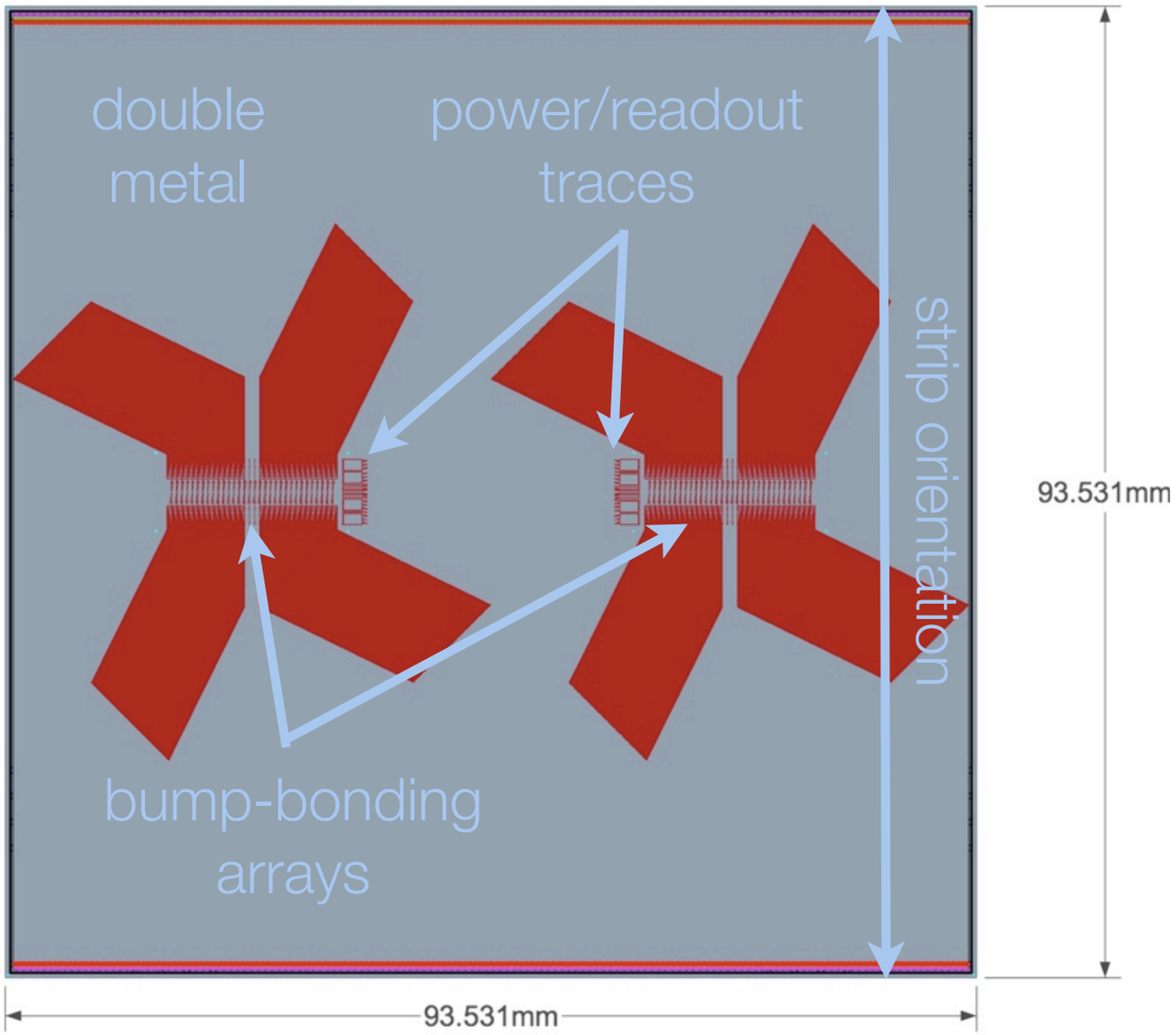
The bad channel lists and results of these tests shall be supplied in a .pdf file. In addition, the I-V data shall be supplied in spreadsheet format.

Propose no further changes

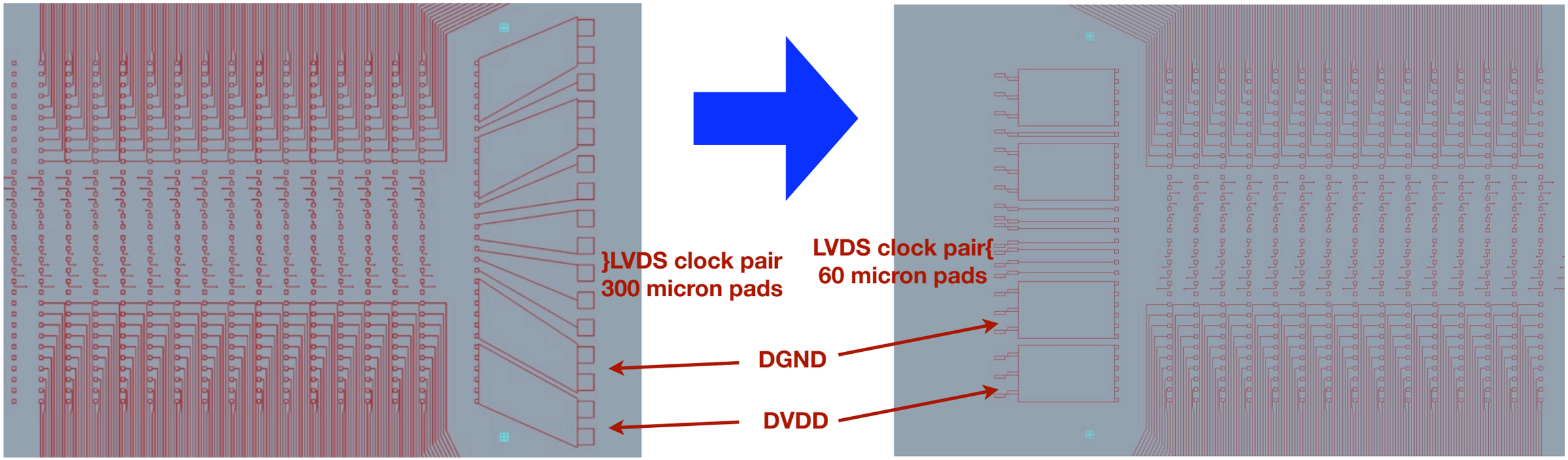
Silicon Sensor Design



wirebonding pads both ends



Silicon Sensors - Status



Re-optimize cable connections for wirebonding-only:

- Changes to clock traces/pads reduce worst-case pedestal shift from capacitive coupling to ~3500e^-
- simulation of power/ground traces give effect similar in nature and magnitude to clock effects
  - ➡ Arrange power traces ⊥ underlying readout traces

Drawing changes

- Tolerances removed except:
  - cut edges +/-10 microns and
  - 50 microradians with masks
- Many small corrections and changes, some still need decisions...
  - Numbering scheme
  - Outer guard
  - Small problems in I-DEAS drawings?

1. ALL SENSOR FEATURES TO BE INTERPRETED AS BEING REFERENCED TO THE X-Y AX
2. NECESSARY/REQUIRED FEATURES AND DIMENSIONS ARE SHOWN WITHIN A BORDERED AREA ——— — — ——— WITH ADJACENT NOTATION: "FEATURE REQUIRED". OTHER FEATURES MAY BE CHANGED SUBJECT TO SID PROJECT REVIEW.
3. ALL FEATURE LOCATIONS ARE IDEAL LOCATIONS.
4. SUGGESTED SENSING TRACE NUMBERING SCHEME: CONSISTS OF ARABIC NUMERALS EVERY TENTH SENSING TRACE WITH THE NUMERAL INDICATING THE TENTHS DIGIT. DOTS/SQUARES ARE USED TO INDICATE THE HUNDRETHS DIGIT.
5. ALL TRACE LINES SHOWN INDICATE THE CENTER OF THE STRIPS.
6. UNPASSIVATED BOND/CONTACT/BOND PAD AREAS ARE DESCRIBED AND REQUIRED. CHANGES ARE SUBJECT TO SID PROJECT REVIEW.
7. THE SILICON CUT DIMENSIONS ARE FIXED AND REQUIRED. THE ANGLE OF THE CUT EDGES WITH RESPECT TO THE READOUT STRIPS = ±50 MICRO-RADIANS.
8. THE EXPECTED ACTIVE LENGTH, ACTIVE AND CUT WIDTH AND DISTANCE FROM CUT END TO A.C. BOND PADS ARE BASED UPON HPK'S RECOMMENDATIONS. CHANGES ARE SUBJECT TO SID PROJECT REVIEW.
9. VENDOR IS RESPONSIBLE FOR DETERMINING GUARD RING AND BIAS RING STRUCTURE DESIGNS, ALBEIT SUBJECT TO SID PROJECT REVIEW.
10. FIDUCIAL DESIGN/DETAILS MAY BE CHANGED, SUBJECT TO SID PROJECT REVIEW.

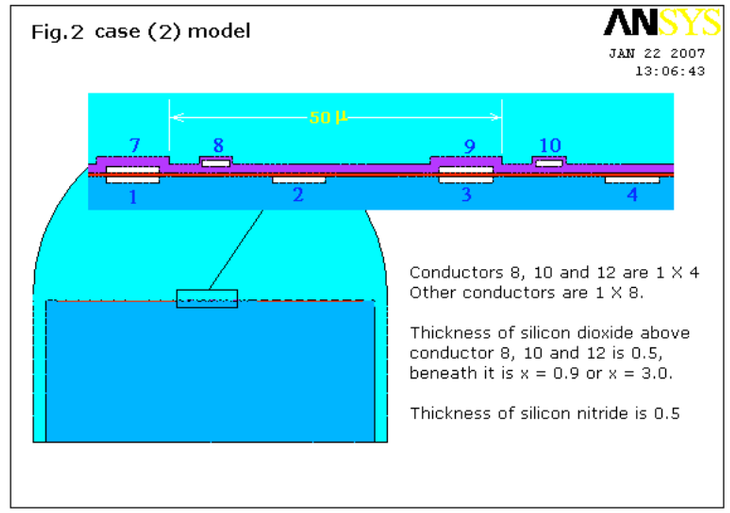
3 2

Capacitance Calculations

- Zhijing Tang (FNAL) created a series of ANSYS capacitance models for the sensors
- Most results as anticipated, but some interesting lessons
  - Penalty for crossing in double-metal somewhat larger than expected (5.5pF vs. 3pF)
  - Penalty for fine-pitch double-metal fanout smaller than expected (3pF vs. 6pF)

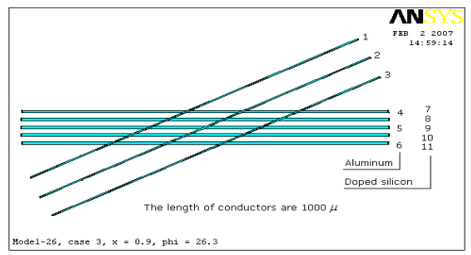
Is there a better design?

The model for case 2 is plotted in Fig.2. There are 12 conductors. The capacitance matrices are listed on next page.



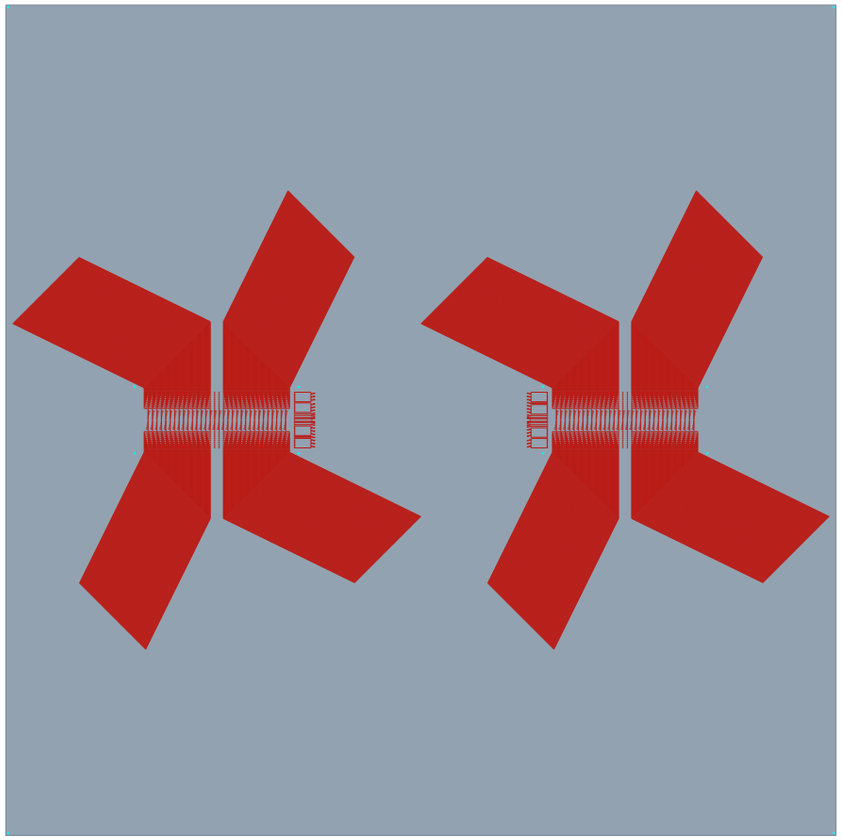
Capacitance matrix for case (3)
x= 0.9 micron phi = 26.3 degree
2/5/07
conductor length is 1000 micron, the unit of capacitance is pF

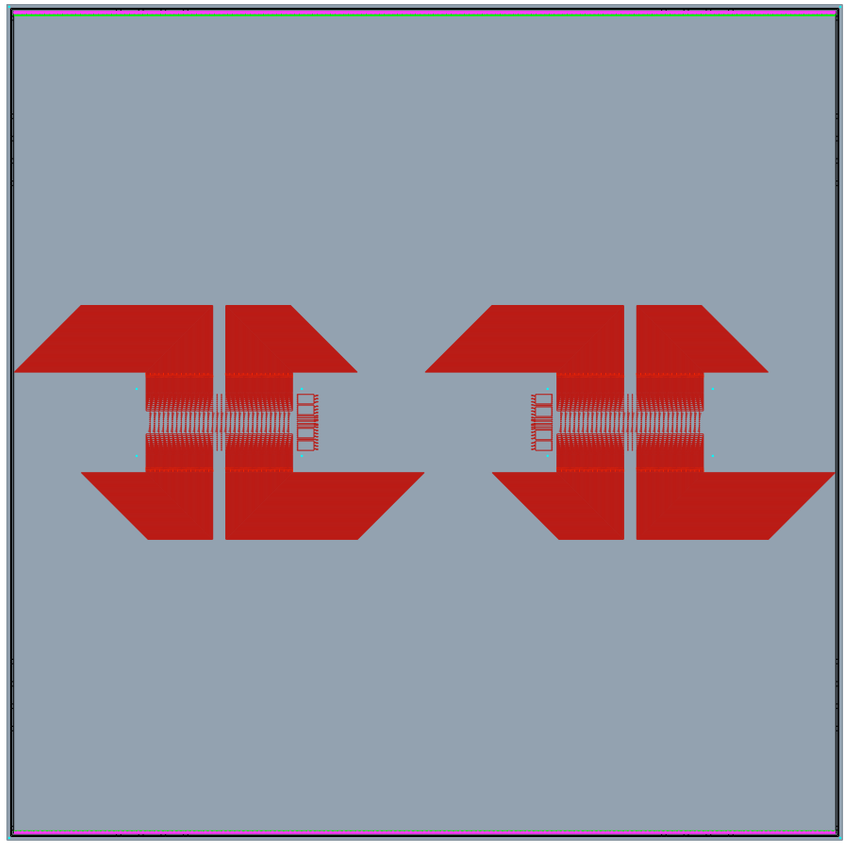
0.023018										
7.49E-03	2.02E-02									
2.32E-03	7.48E-03	2.30E-02								
8.88E-03	8.75E-03	8.68E-03	4.79E-03							
8.11E-03	8.01E-03	8.14E-03	4.34E-04	2.66E-03						
8.74E-03	8.79E-03	8.87E-03	1.44E-04	4.33E-04	4.74E-03					
8.69E-03	8.16E-03	7.84E-03	1.29E+00	1.39E-03	5.57E-04	2.57E-02				
1.17E-02	1.15E-02	1.14E-02	9.36E-03	8.57E-03	8.67E-04	4.39E-02	1.91E-02			
5.18E-03	5.11E-03	5.19E-03	1.44E-03	1.29E+00	1.43E-03	8.64E-03	4.02E-02	1.54E-02		
1.15E-02	1.15E-02	1.17E-02	8.70E-04	8.57E-03	9.33E-03	4.73E-03	9.64E-03	4.02E-02	1.91E-02	
7.82E-03	8.14E-03	8.68E-03	5.60E-04	1.39E-03	1.30E+00	3.20E-03	4.73E-03	8.64E-03	4.39E-02	2.57E-02

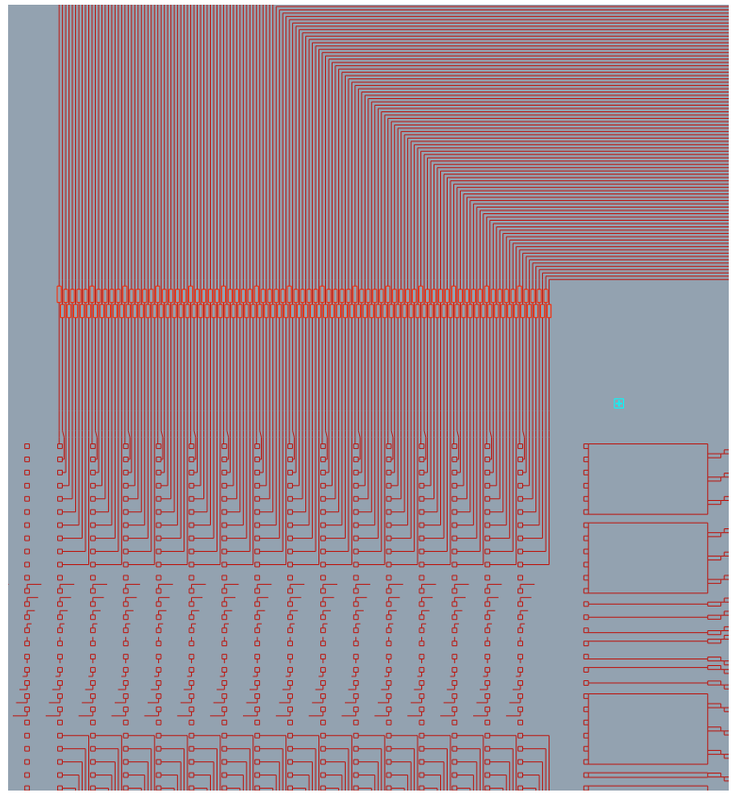


5.44E+00

Double-metal Proposal

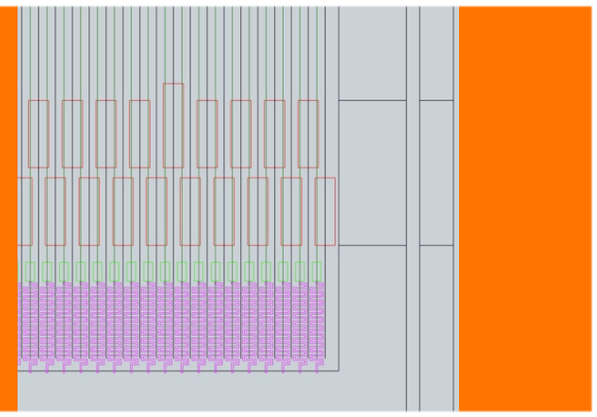






- Reduces max/average capacitance slightly and spread significantly
  - From 12-21pF to 14-18 pF for 95% of channels (max goes from 22 to 20 pF)
  - Provides pads for testing a wirebonded KPiX (or other centrally-mounted chip)

Silicon Sensors - Plans



- Would like to leave here with final agreed-upon changes
- Would like to keep changes to those we are able to implement in coming week
- Submit to HPK USA and follow up through Hiro Aihara at U. Tokyo
- Must keep up good progress on on KPiX, bump-bonding and cable so we are ready to work with sensors when they arrive.