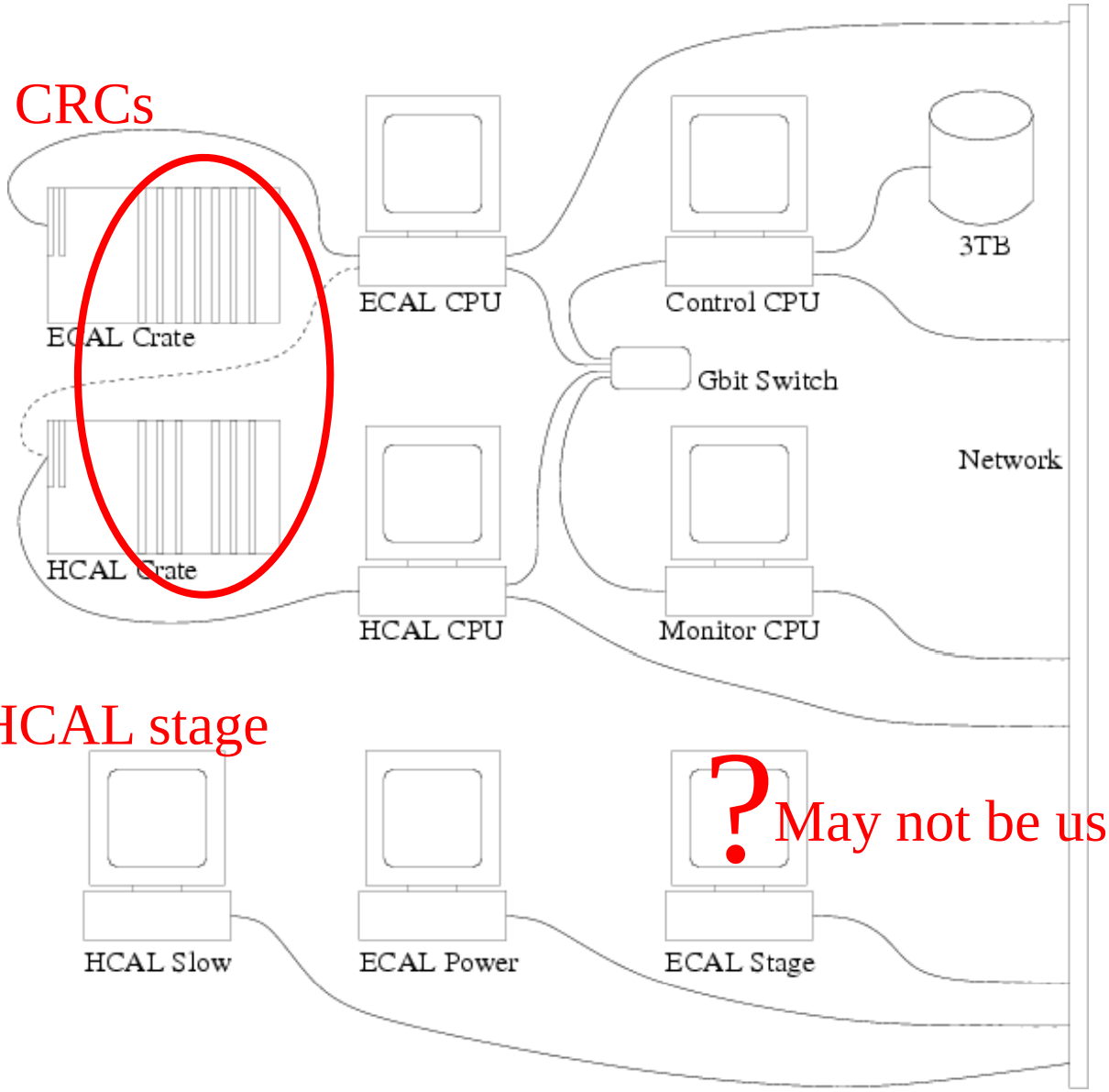
DAQ Readiness

Paul Dauncey

DAQ hardware layout

More CRCs

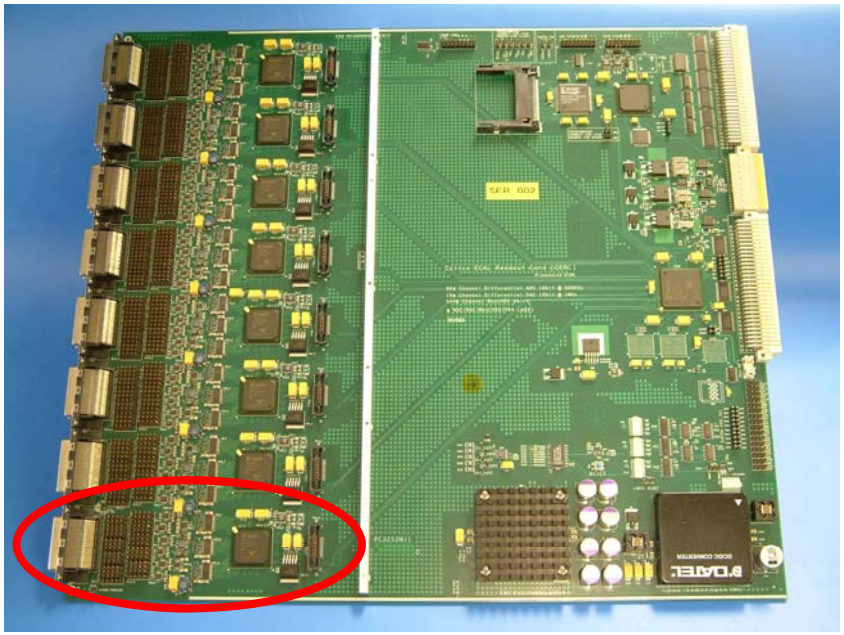


New HCAL stage

? May not be used

CRC requirements

- Need 13 CRCs total
  - ECAL crate requires 6 CRCs
  - AHCAL crate requires 7 CRCs
  - 8 Front Ends/CRC (FE = connector)
  - FE count is critical
- ECAL has (up to) 60 PCBs
  - 30 full PCBs; one CRC FE each
  - 30 half PCBs; one CRC FE per pair
  - 45 FEs total out of 6×8 = 48 in crate
- AHCAL, TCMT and trigger in other crate
  - AHCAL has 38 layers, one CRC FE each, via two cables
  - TCMT needs 2 FEs
  - Trigger data occupy 2 FEs (equivalent; can be non-functional)
  - Veto scintillator, PIN diode monitoring need 3 FEs
  - 45 FEs total out of 7×8 = 56 in crate



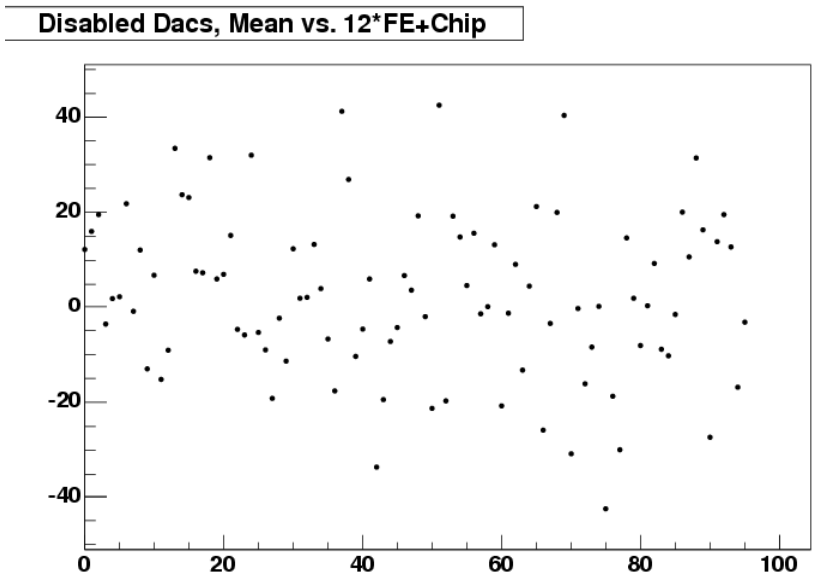
One FE

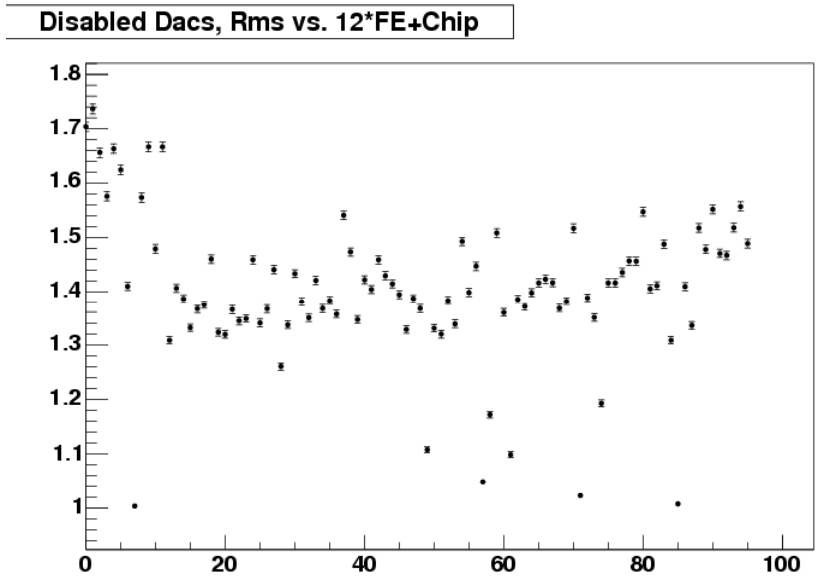
CRC hardware repairs

- Several FEs found to have faults during CERN run
  - Enough fully functional FEs to read everything in 2006, but not in 2007
- Matt Warren (UCL) gone through repair program; two main tests
  - "Battery pack" test
    - Constant 1.5V input to all channels on one FE in parallel
    - Pack moved by hand to other FEs in turn during run
    - Done for link array at both full (ECAL) and half-full (ECAL/HCAL) PCB settings
  - Internal DAC scan test
    - Internally loop back on-CRC DAC into ADCs
    - Scan over full DAC range, measure electronics calibration
    - Turn off DACs for pedestals and noise
- 14 out of 16 CRCs were tested; repairs made to 11 of these
  - Other 2 CRCs were not available
- Faults found were very varied
  - Several components missing; possible broken off from mishandling
  - Some bad solder joints on front connectors; again possibly due to mishandling
  - Several bad vias on PCB; required adding wires to bridge broken traces

CRC pedestals and noise

- CRC has 8 FEs, each with 12 ADC channels = 96 channels total
  - Most of following plots have channel number on x axis
- Pedestal and noise are most basic properties of CRC
  - Bad channels usually show up as deviations from average value
- Plots following are e.g. SER013, which is fully functional

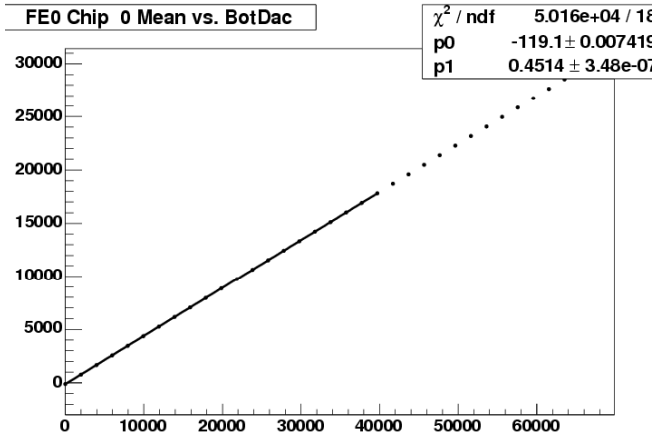


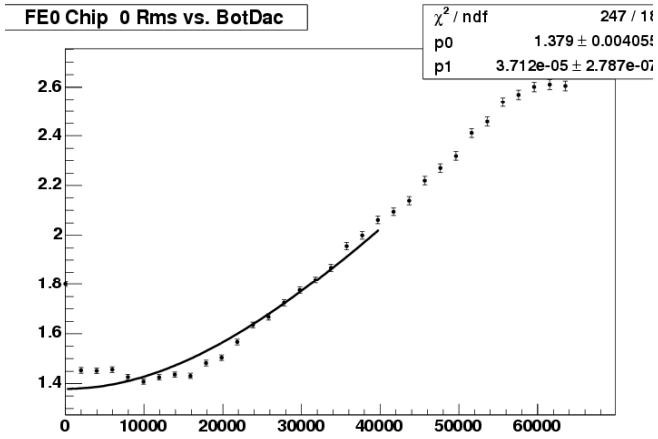


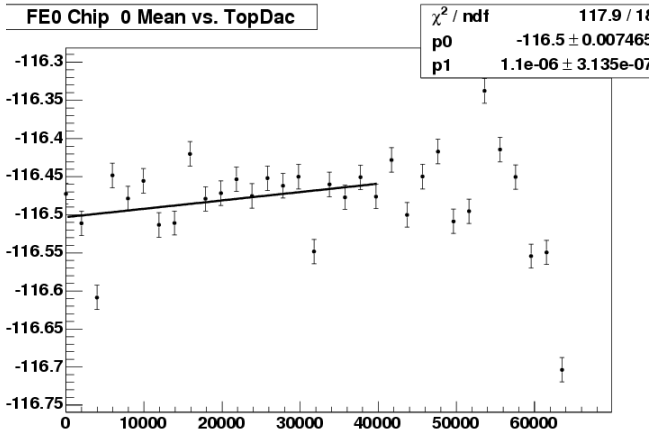
- Pedestals all within ±50 ADC counts of zero (full scale ±32k)
- Noise: all with 1–2 ADC counts; ECAL noise ~6 ADC counts

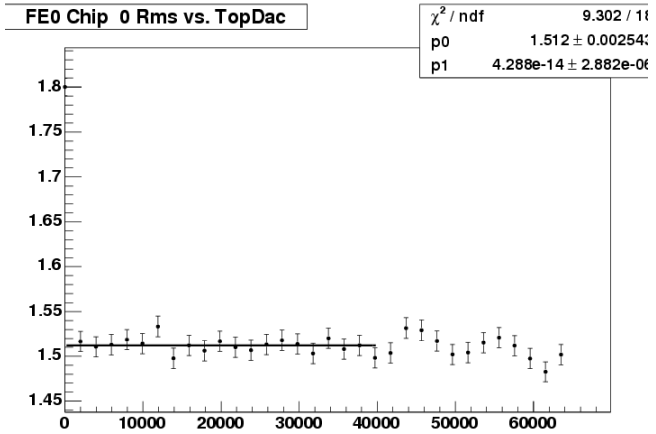
CRC internal DAC test

- CRCs have two on-board DACs going to alternating ADC channels
  - Can measure response and cross-talk of each channel to neighbour
  - Measure signal and noise vs DAC value for every channel; here e.g. FE0, Ch0



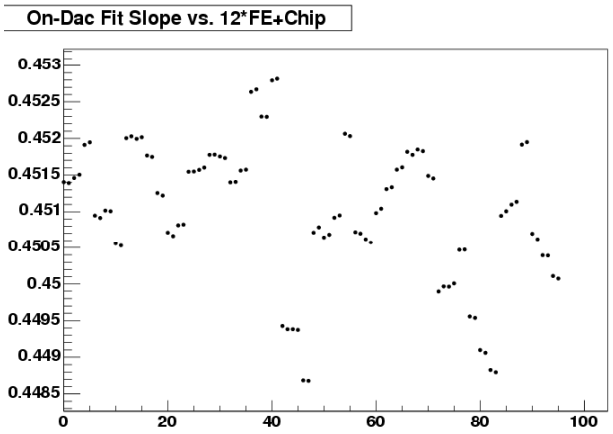


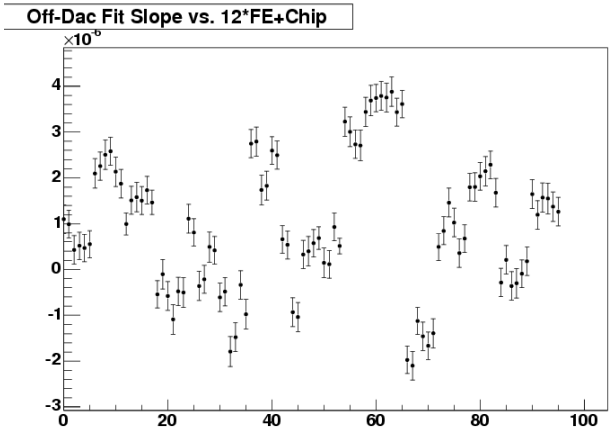


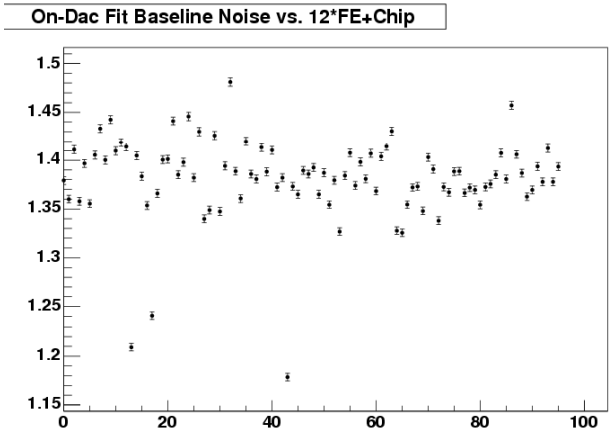


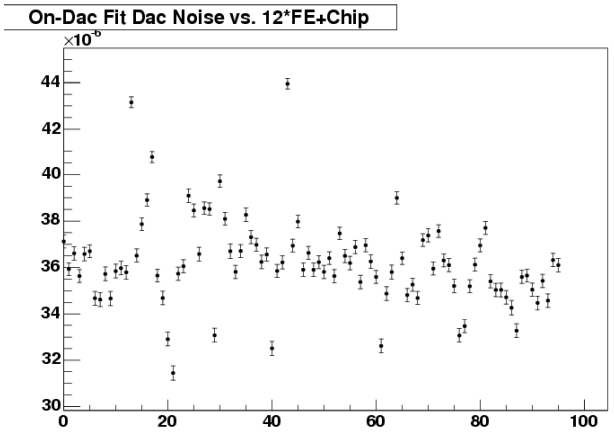
CRC internal DAC test (cont)

- Summary of DAC responses for each channel









- Gain is uniform to better than 1%, cross-talk down by 10^{-5}
- Signal-related noise is uniform to within 10%

CRC good FE status

CRC	Post-CERN	Post-Matt
SER003	0	8
SER004	3	Dead
SER005	7	8
SER006	8	8
SER007	5	8
SER008	3	7
SER009	???	???
SER010	6	6
SER011	5	8
SER012	6	8
SER013	8	8
SER014	7	8
SER015	6	8
SER016	5	8
SER017	7	8
SER018	8	8

- SER004 destroyed by manufacturers (!) while trying to replace static-damaged FPGAs
  - Will make a new CRC but timescale unknown
- SER009 in NIU/FNAL since early 2006
  - Not tested; status unknown
- Example of use; “best” CRCs in ECAL
  - ECAL crate
    - SER003, SER005, SER006, SER007, SER0011, SER012
    - 48 functional FEs (need 45)
  - AHCAL crate
    - SER008, SER010, SER013, SER014, SER015, SER016, SER017
    - SER008 or SER010 used for trigger CRC
    - 53 functional FEs (need 44, plus 1 non-functional for trigger CRC)
  - SER018 spare; usable in any slot

CRC firmware status

- Firmware (almost) unchanged since CERN
- One modification to revive SER003
  - Bad connection between BE and 8MByte memory
  - Interface is 18 parallel I/O tracks; one broken
  - Bit 10 of every other channel stuck to zero
  - Affects every FE so whole CRC unusable
  - Only 16 of the 18 lines used
- Reorder in firmware so bit 10 uses one of spare lines
  - New firmware used for all other board tests; no problems
- Should consistently use new firmware throughout
  - Or might accidentally load wrong firmware into SER003
- Matt still trying “remote” (VME) boot and firmware downloads
  - SER010 will remain at UCL until nearer CERN start

Other hardware items

- TDCs: Will want to use same ones as last year
  - Significant DAQ software investment in getting them running
  - Borrowed two from CERN electronics loan pool; should not be a problem but should be sure to get them out well in time
  - Last year, soldered (!) cables to TDC board; better to use connectors this year; who will provide these?
- Cables: Checked at DESY
  - Sufficient number with no errors and available (AFAIK)
- 3TByte DAQ disk: Saw some problems related to temperature
  - Should be rack mounted this year with fans
  - But needs to be close to DAQ PCs; need rack in control room
  - Also ensure air-conditioning in control room is left on
  - Must also be cleared before start of run; are we sure all files (slw, log) are copied?
- ECAL additional PCs:
  - Stage PC was stolen; will it be needed/replaced?
  - Power PC; will it be integrated into DAQ? Must be made more reliable if so as USB failures could crash DAQ

Software status

- No significant changes to core software since CERN
  - If it ain't broke…
- Main work has been on ScECAL and DHCAL
  - ScECAL now effectively complete but DHCAL developments ongoing
  - Need to ensure code is kept coherent and prevent multiple branches
  - Issue is that DHCAL will be running at same time as CERN
- HCAL stage is a new item
  - Communication to DAQ will have same structure
  - Actual data themselves may be different (relevant for LCIO converter also)
- Some other items to do (none time-critical)
  - Allow DAQ to use cvs code repository directly
  - Upgrade HAL ("Hardware Access Library" = VME interface) to newer version as required for DHCAL readout

FNAL issues

- Main work will be integration of new systems
  - DHCAL, although slice test will be critical to prepare for this in advance
  - Beam line components; trigger, PID, tracking: could be a large effort needed so any experience beforehand would be useful
  - HOLD timing will need to be remeasured
  - May be extra issues with DHCAL/ECAL synchronisation?
- Code tuning may be useful to optimise for change to beam timing
  - Do we want to make more use of 2min out-of-spill period; e.g. pedestals or calibration?
  - If so, substantially more work would be needed
- DAQ needs to work on US power
  - Crates are spec'ed for US power
  - PCs should be OK
  - Disk is probably OK but not confirmed
  - Note; none of these have been tested in the US

Summary

- CERN 2007 likely to be very similar to 2006 for DAQ
  - No major changes needed in h/w, f/w or s/w
- CRC faults significantly reduced
  - Great work from Matt Warren over last few months
  - Now confident that all channels can be read with fully functional FEs
- Firmware and software changes minimal
  - Coordinating parallel software developments are main issue
- FNAL will be a major change
  - Should not underestimate time needed to integrate there
  - Should not expect to plug'n'play
  - Any preparations which can be done in advance should be given priority