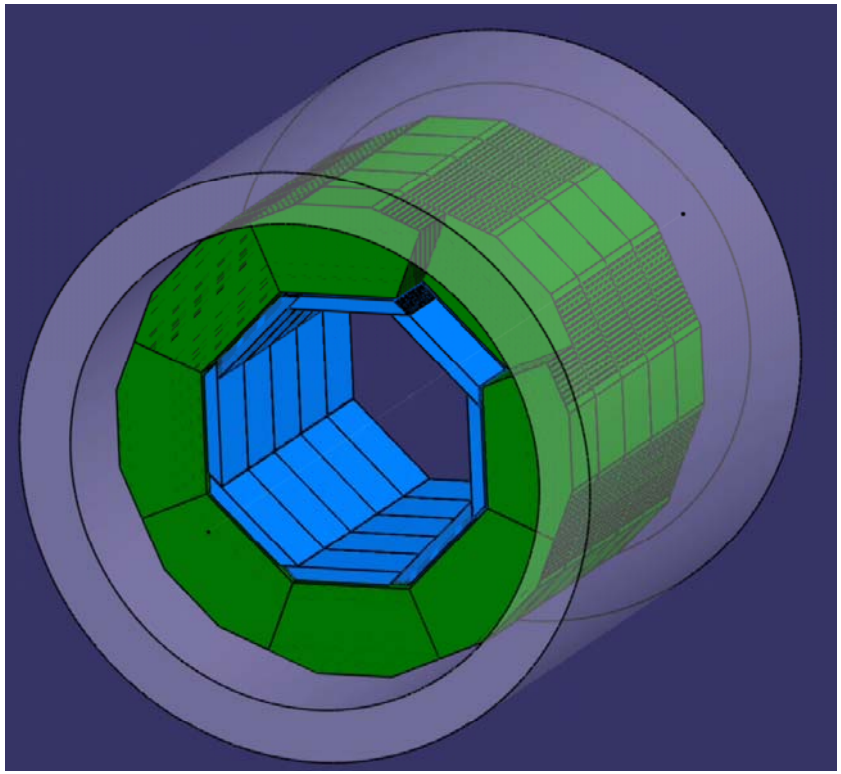


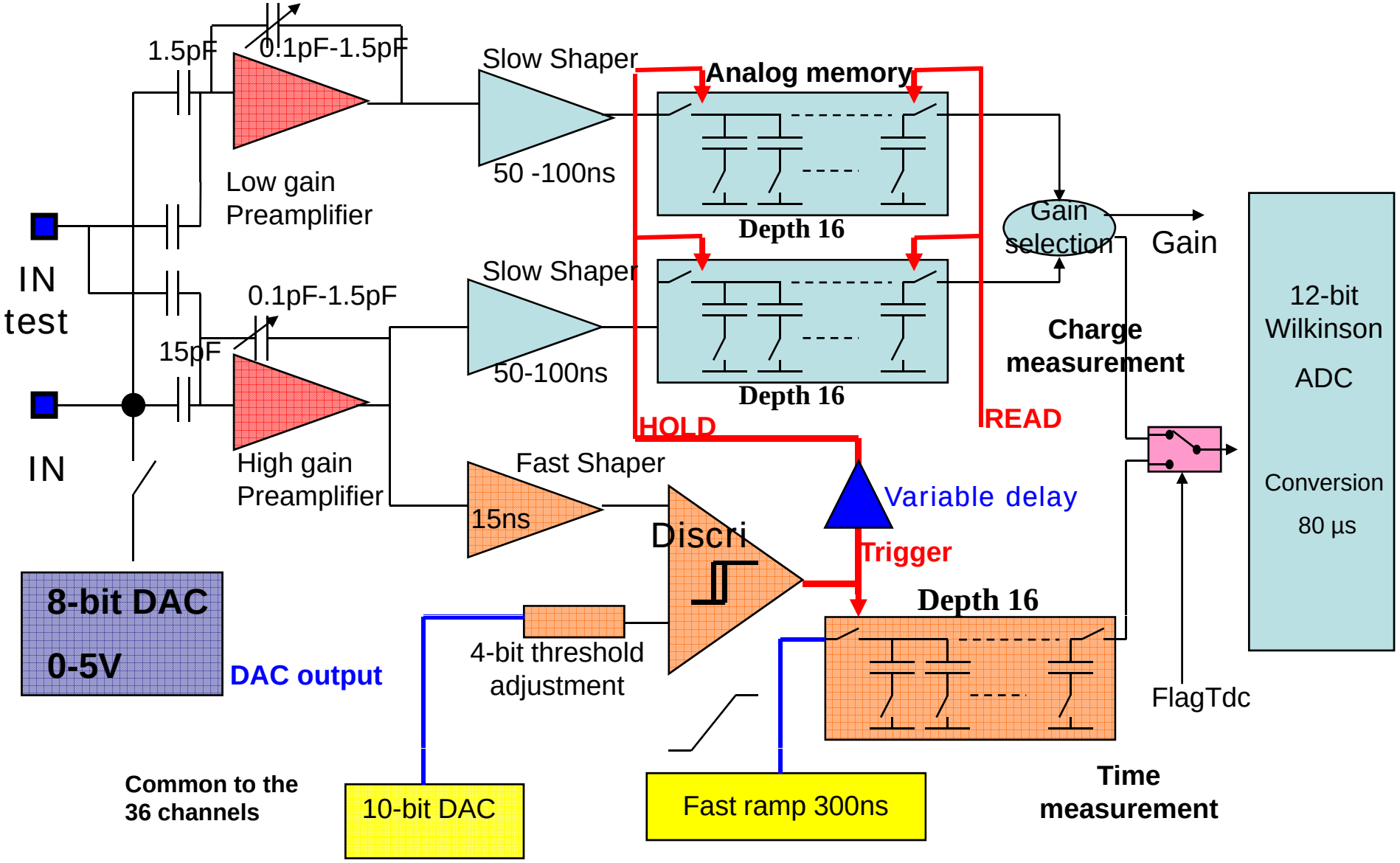
SPIROC update

Felix Sefkow
Most slides from
Ludovic Raux

HCAL main meeting
April 18, 2007

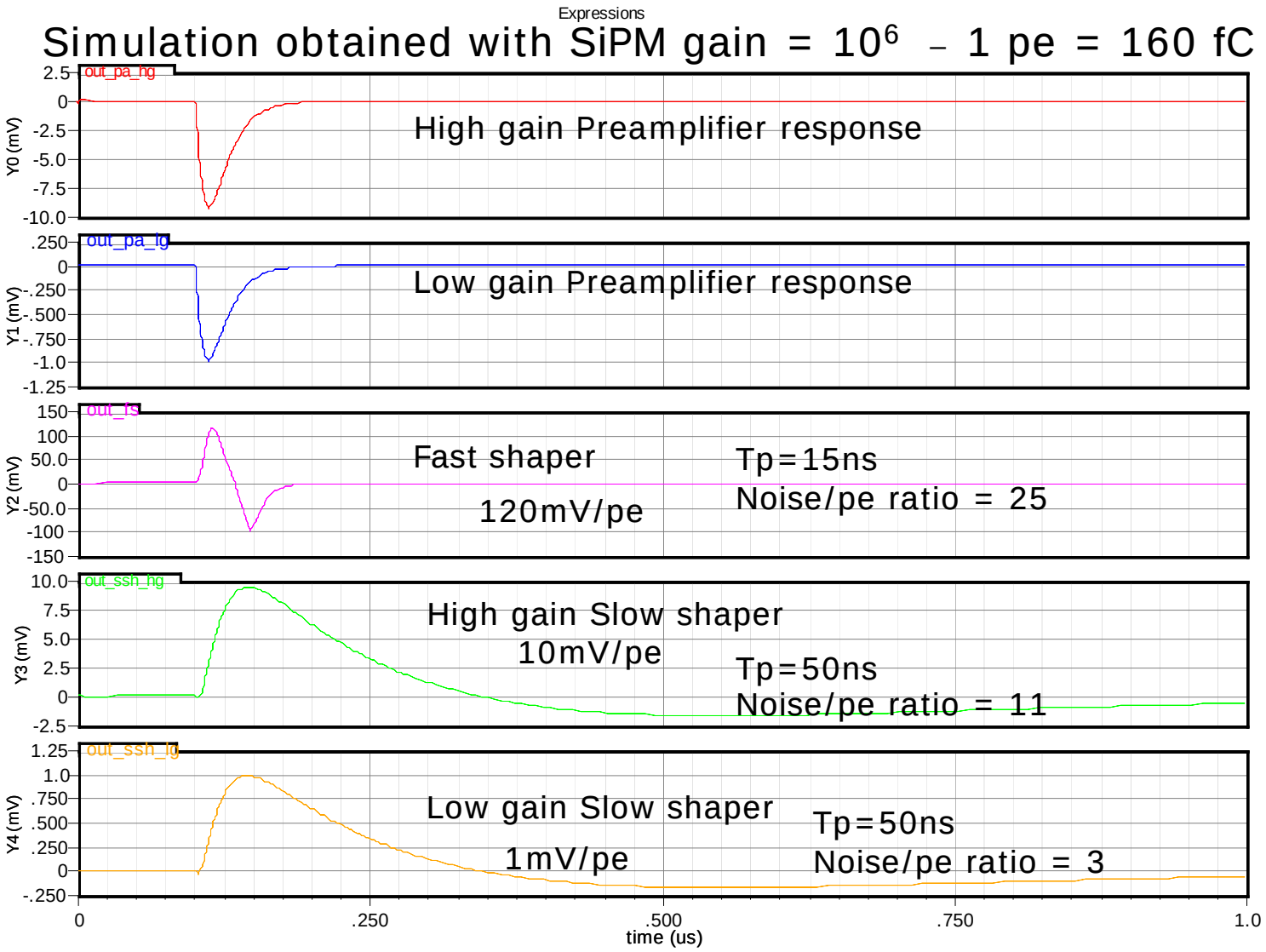
Topics:

- ASIC overview
- Noise level requirements
- Trigger schemes
- Readout options

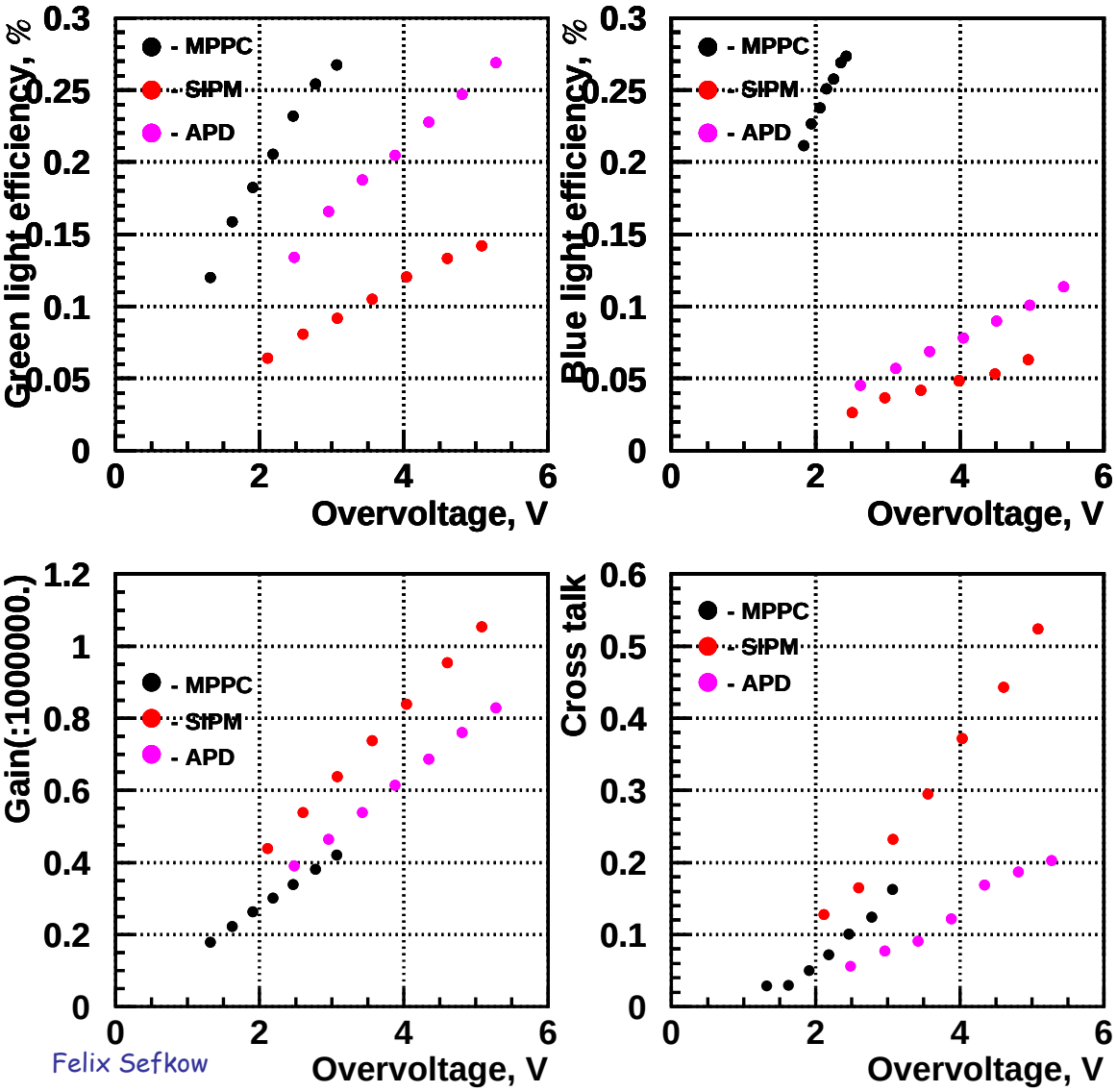

1.5pF
0.1pF-1.5pF
Slow Shaper
Analog memory
Low gain
Preamplifier
50 -100ns
Depth 16
IN
test
Slow Shaper
0.1pF-1.5pF
Gain
selection
Gain
12-bit
Wilkinson
ADC
15pF
50-100ns
Depth 16
Charge
measurement
HOLD
READ
IN
High gain
Preamplifier
Fast Shaper
Variable delay
15ns
Discri
Trigger
Conversion
80 µs
8-bit DAC
0-5V
DAC output
Depth 16
4-bit threshold
adjustment
FlagTdc
Common to the
36 channels
10-bit DAC
Fast ramp 300ns
Time
measurement

SPIROC : Photoelectron response simulation

Ludovic Raux

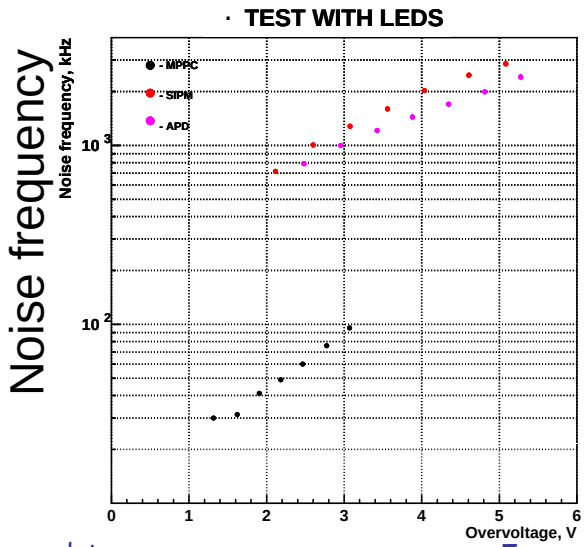


Comparison of different Multipixel Geiger Photo Diods (MGPD)



MGPD were illuminated with Y11 (green) and scintillator (blue) light

Efficiency was normalized to MPPC one

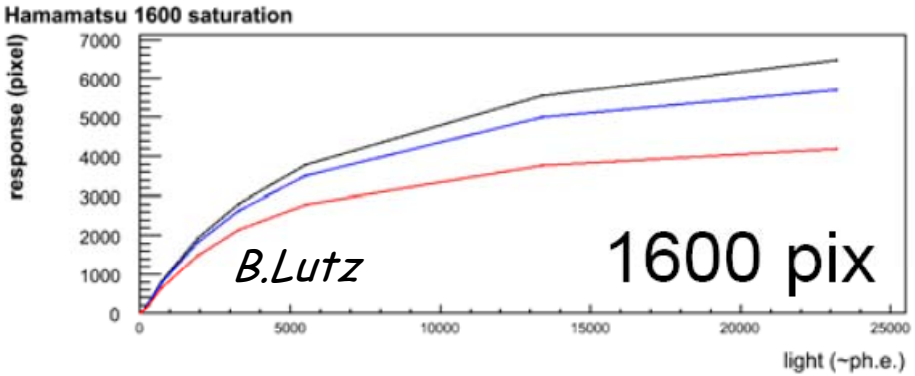


Noise limits

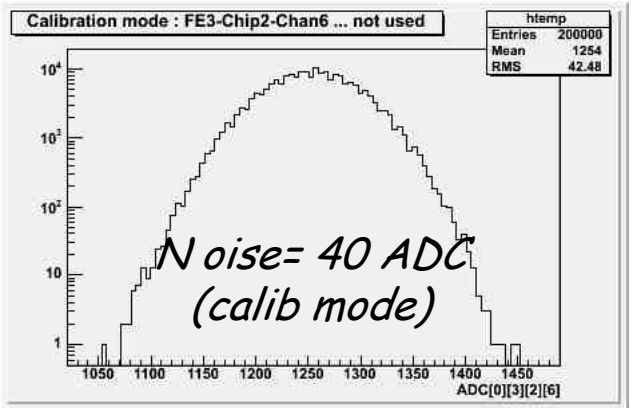
- Gain can be as small as $0.2*10^6$
- Noise can be so low that threshold at 1.5 p.e is possible
- Trigger mode:
  - limit given by occupancy: 10^{-4} ➔ T > 4-5 σ(Noise)
  - Noise must be below $1/5 * 1.5 * 0.2 * 10^6$ e ➔ N/p.e.> 17 ☺
- High gain mode:
  - Limit given by separation of single p.e. peaks ➔ G > 3-4 σ (Noise)
  - Noise must be below $1/4 * 0.2 * 10^6$ e ➔ N / p.e. > 20 ☹
- Low gain mode:
  - Limit given by MIP resolution dominated by Poisson statistics: σ(Noise) < 1/3 σ(Poisson)
  - Noise must be below $0.2 * 10^6$ e ➔ N / p.e > 5 😐
- High gain ("calibration") mode most challenging
  - Gain some factor with higher impedance of r/o lines

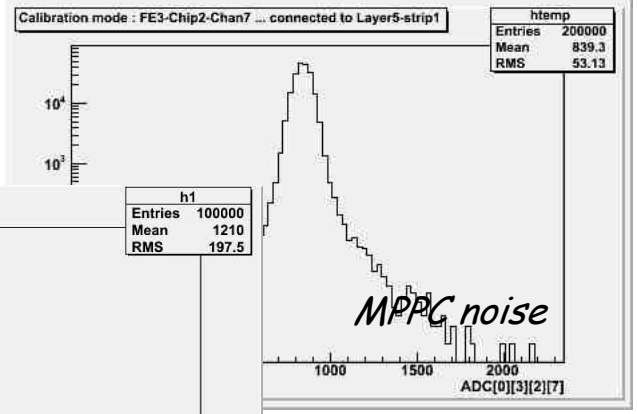
Experience with MPPCs

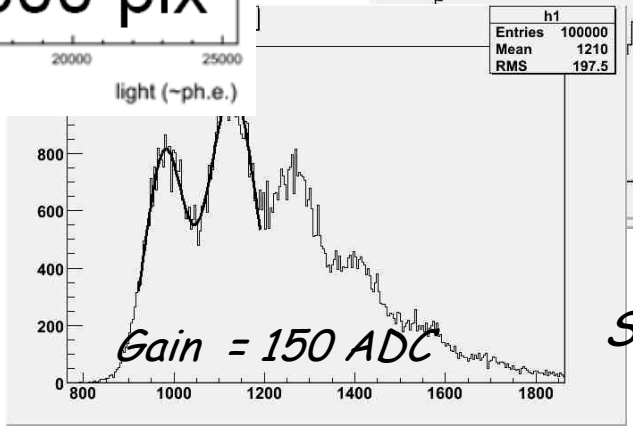
- Operated at 2.something V ➔ gain 0.3-0.4 * 10^6 (~ SiPM)
  - *Just* works
- Keep an eye on dynamic range



- Actually no saturation seen far in DESY 6 GeV e beam







Satoru Uozumi

SiPM readout

- SPIROC: Data volume:
  - 36 channels, ADC + TDC + time stamp = 948 bits / event
  - 16 time slices: 15 kbit
- Readout speed:
  - 5 MHz: 3-4 ms / chip if RAM full
  - 1 MHz: 14-20 ms / chip
- ILC: 200 ms max readout time
  - 5 MHz: max 50 VFE / FE, 1 MHz: max 10 VFE / FE
  - HCAL layer 2000 channels / 36/chip = 60 chips ➔ < 5 MHz: > 1 FE
  - Faster with parallel readout or faster clock
- Test beam:
  - Asymptotic rate: 16 / 100-200 ms = 80-160 Hz
    - Test beam layer: 1 m^2 ➔ only 2x faster

SiPM buffer depth: ILC case

- ILC mode: 3 MHz bunch crossing rate for 1 ms (3000 bx/train)
  - 300 Hz – 3 kHz noise from SiPM above ½ MIP threshold
    - : 0.3 to 3 hits per train
    - Buffer depth of 16 ok for individual trigger
  - .OR. of 36 channels: trigger rate of 10 – 100 kHz
    - Buffer of 16 slices fills up in 0.16 – 1.6 ms
    - Not sufficient for ILC cycle
    - Independent of physics topology, because noise and not physics induced
  - Full channel-by-channel zero suppression only in 3rd generation ASICs (like ECAL)

SiPM buffer depth: test beam

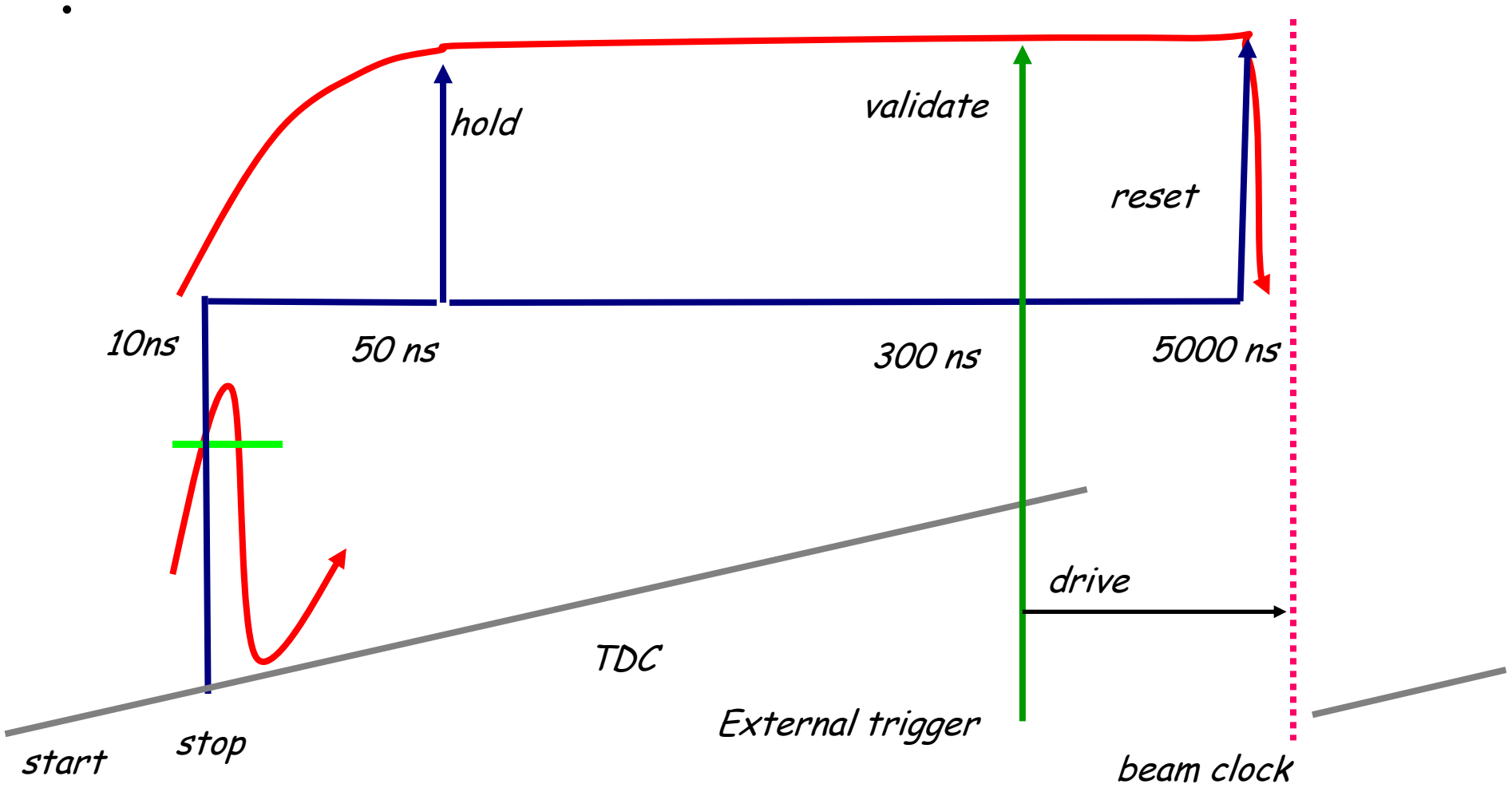
- Testbeam mode
  - Need to adjust readout cycle to noise rate and buffer depth
  - Shorten r/o cycle to 0.1 ms?
  - Asymptotic rate stays the same: 80 Hz for 200 ms r/o
  - BUT:
  - Without external trigger read mainly noise
    - Physics fraction = beam rate / noise rate ~ 1/10 … 1/100
    - Effective rate for 1 kHz beam
      - only 1 or few Hz for .OR.ed auto-trigger
      - Order of 50 Hz for individual trigger

Fast timing 1

- In present system shaping acts as latency – and is too short
  - Would like to go from 200 ns to, say, 400 ns
- SiPM shaping in physics mode is shorter (50-100 ns)
- ➔ need to decouple shaping and latency, store charge in-between

See next slide

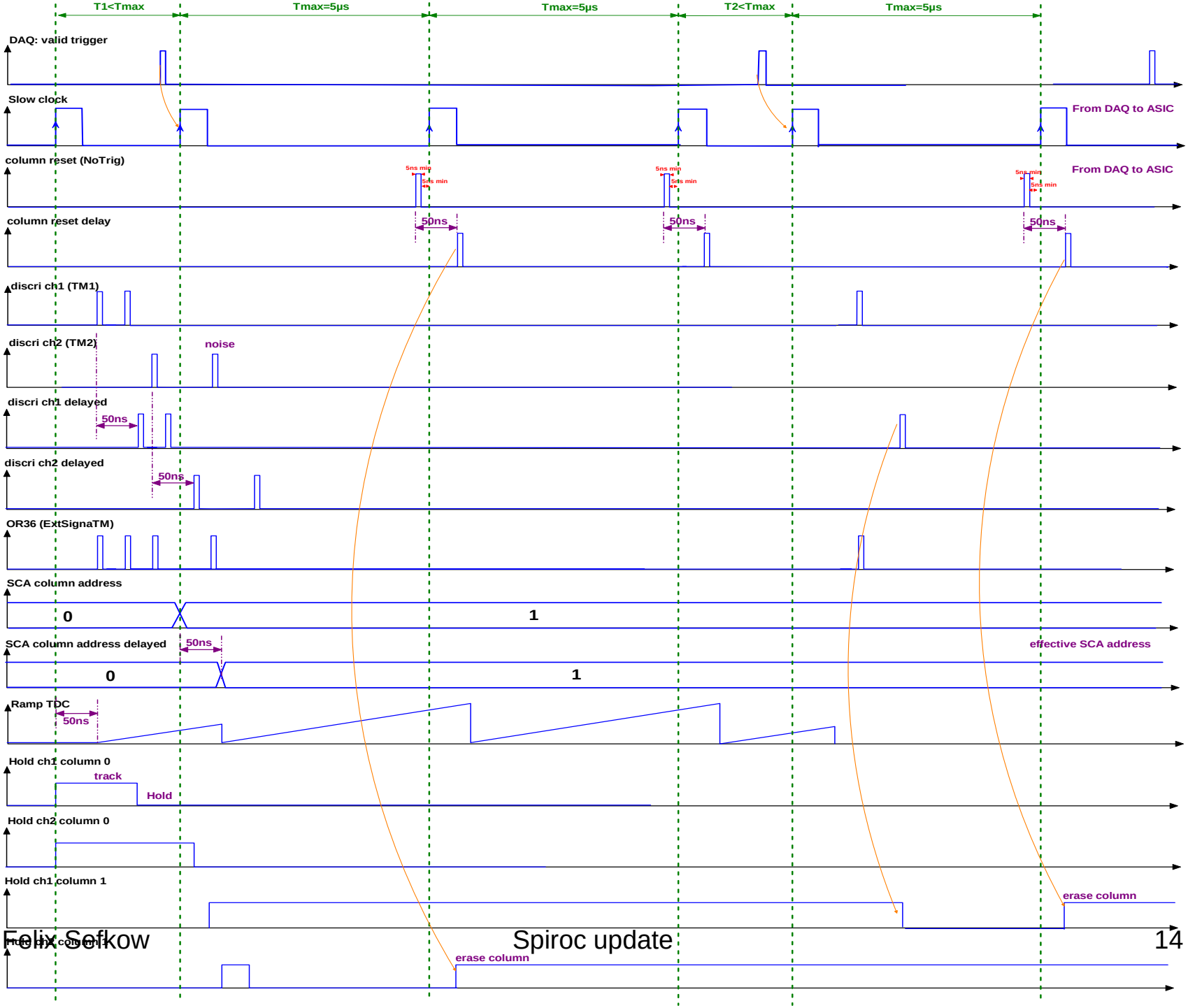
Timing


hold
validate
reset
10ns
50 ns
300 ns
5000 ns
drive
TDC
External trigger
start
stop
beam clock

Fast timing 2

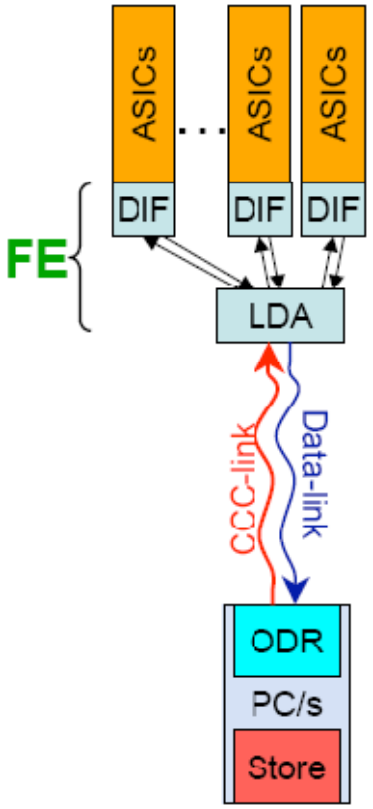
- Timing scheme takes care of difference between shaping time = hold delay and latency for validation

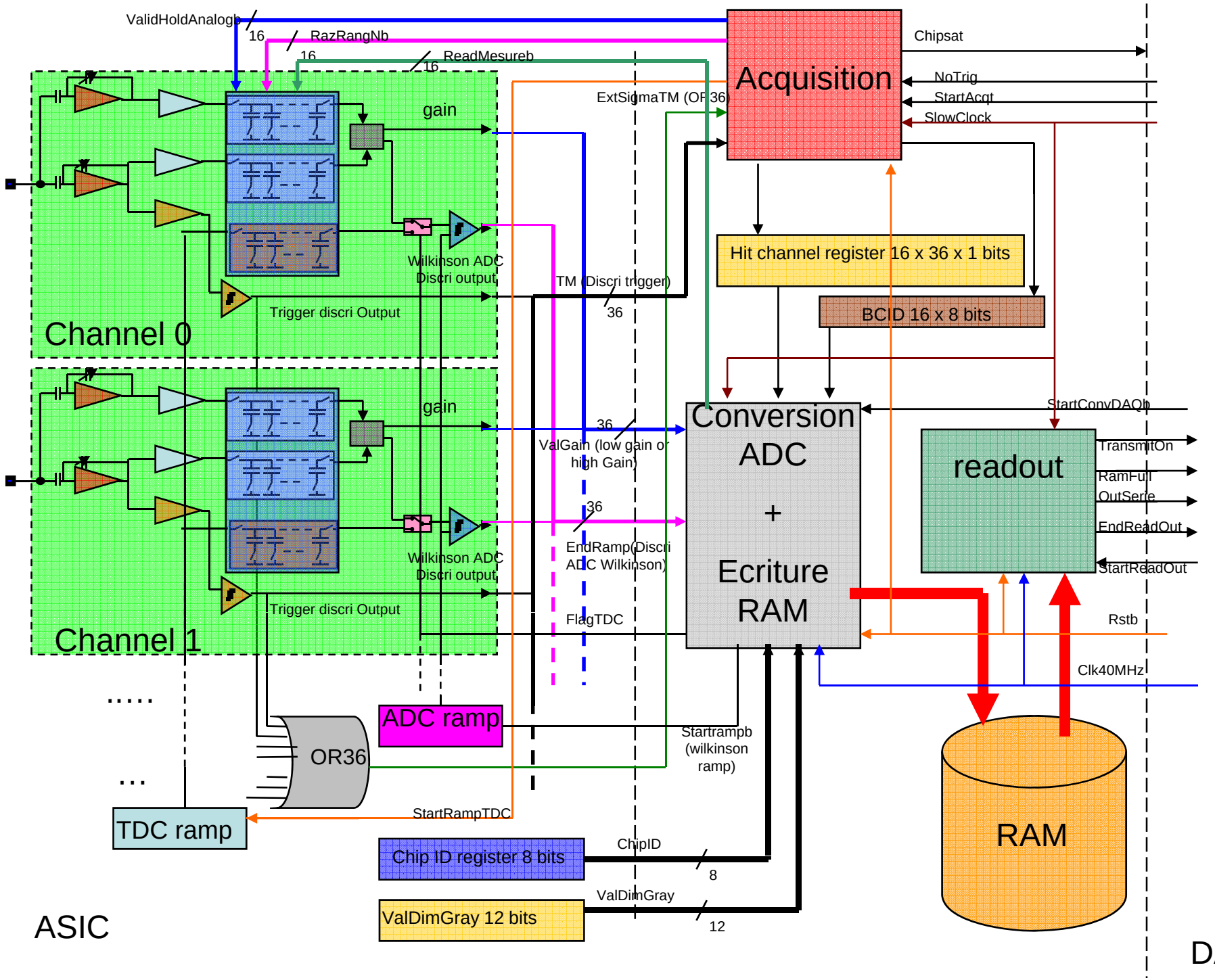
- If validation in next clock cycle, loose data
  - Dead-time = latency / clock (in test beam only)
  - Long cycle (50000 ns): < 10%, no problem

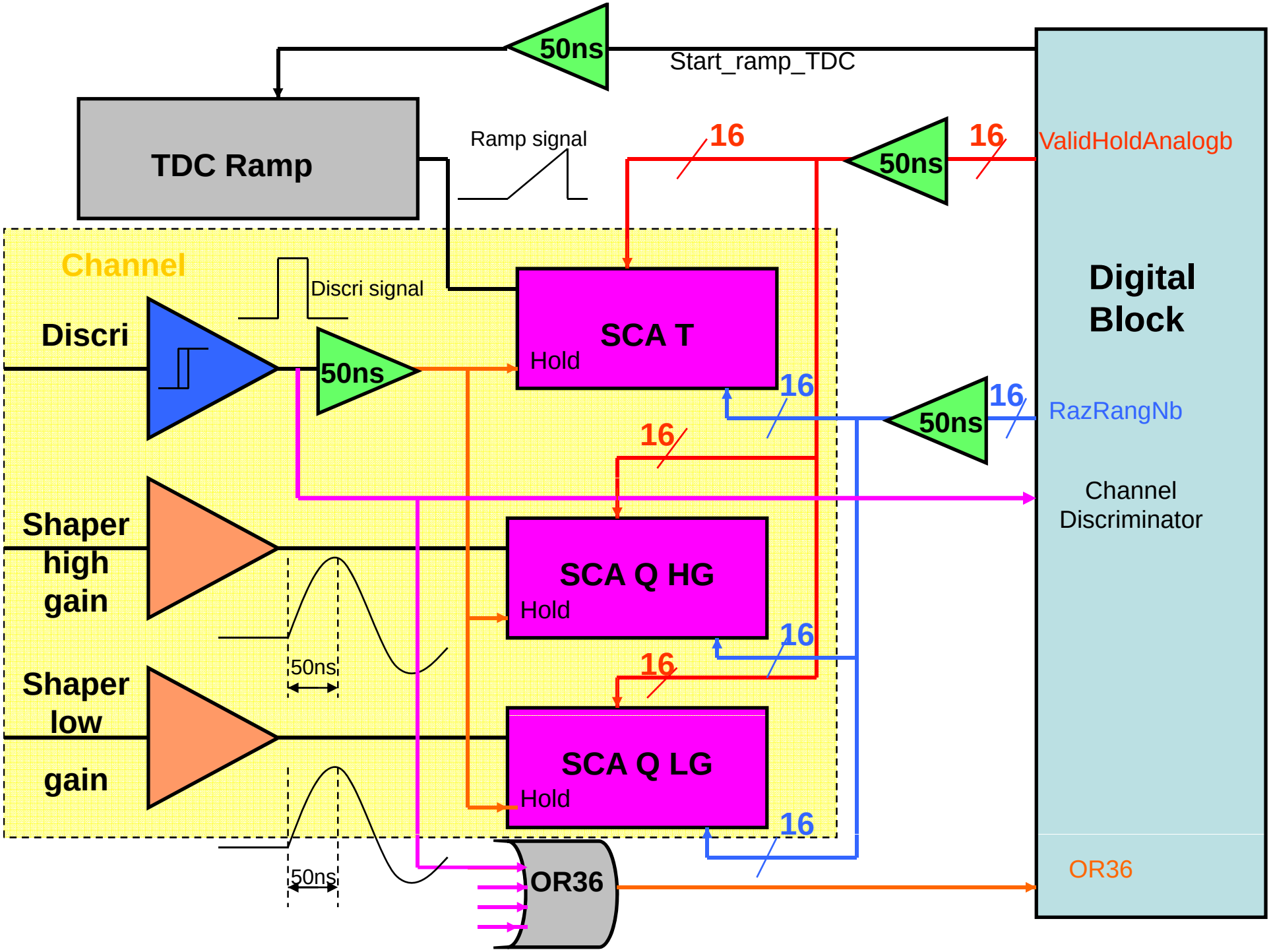

T1<Tmax
Tmax=5µs
Tmax=5µs
T2<Tmax
Tmax=5µs
DAQ: valid trigger
Slow clock
From DAQ to ASIC
column reset (NoTrig)
5ns min
From DAQ to ASIC
column reset delay
50ns
discri ch1 (TM1)
discri ch2 (TM2)
noise
discri ch1 delayed
50ns
discri ch2 delayed
50ns
OR36 (ExtSignaTM)
SCA column address
0
1
SCA column address delayed
50ns
effective SCA address
0
1
Ramp TDC
50ns
Hold ch1 column 0
track
Hold
Hold ch2 column 0
Hold ch1 column 1
erase column
Hold ch2 column 1
erase column

Readout options

- New DAQ
- A prototype DIF
  - Hopefully using the same protocols and software standards
- The old CRCs?
  - In principle possible
  - But only for amplitudes (Charge)
  - Possibility to read TDC being invastifgated, but adds complication and risk
- Need better understanding of schedules to make most practical choice




ValidHoldAnalogb
16
RazRangNb
16
ReadMesureb
16
Acquisition
Chipsat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR 36)
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 0
TM (Discri trigger)
36
Hit channel register 16 x 36 x 1 bits
BCID 16 x 8 bits
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 1
36
ValGain (low gain or high Gain)
36
EndRamp(Discri ADC Wilkinson)
FlagTDC
Conversion ADC + Ecriture RAM
StartConvDAQb
readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
Rstb
Clk40MHz
.....
...
OR36
ADC ramp
Startrampb (wilkinson ramp)
TDC ramp
StartRampTDC
Chip ID register 8 bits
ChipID
8
ValDimGray
ValDimGray 12 bits
12
RAM
ASIC
DAQ


50ns
Start_ramp_TDC
TDC Ramp
Ramp signal
16
50ns
16
ValidHoldAnalogb
Digital Block
Channel
Discri signal
Discri
50ns
SCA T
Hold
16
50ns
16
RazRangNb
16
Channel Discriminator
Shaper high gain
SCA Q HG
Hold
16
50ns
16
Shaper low gain
SCA Q LG
Hold
16
50ns
OR36
OR36

Summary

- ASIC design in full swing, presently working on simulation and analysis
- Signal over noise levels nominally OK even for lower MPPC gain
- ILC mode of operation can be tested
- External trigger scheme for test beam implemented, to protect against SiPM noise
- Functionality with old DAQ possibly restricted (no TDC?)
- Submission in June