# HCAL – Integration Plans

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1. Introduction
2. HCAL Base Unit (HBU) - Update
3. Testboards
4. Light Calibration System (LCS) – Constraints


# HCAL Base Unit (HBU) – first idea

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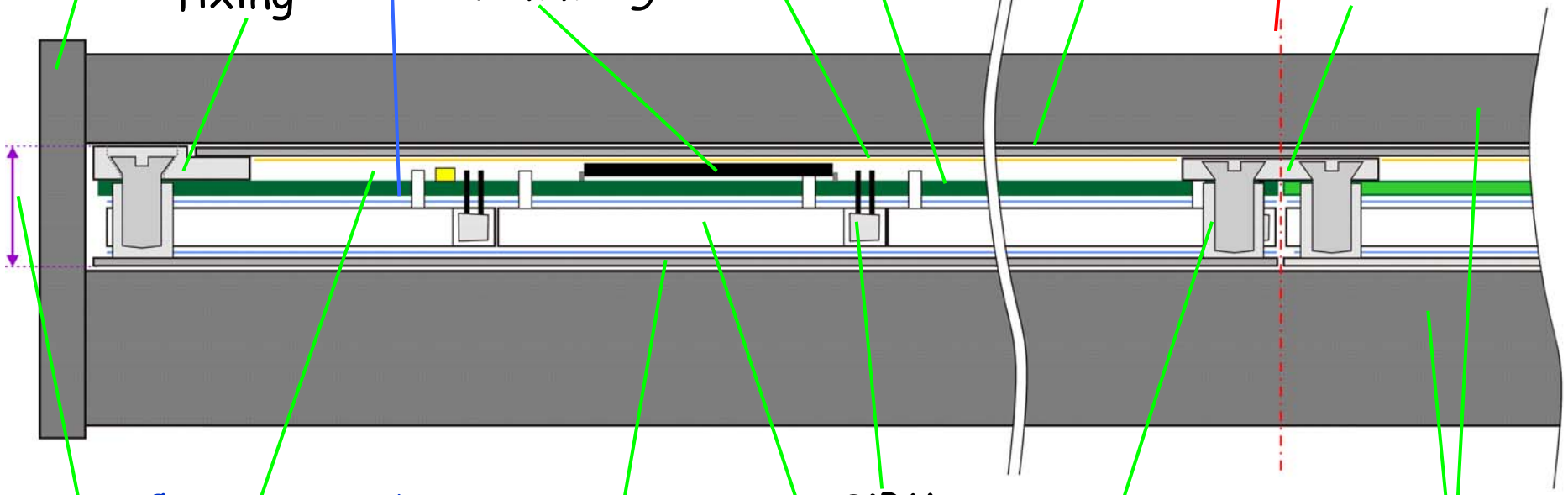

# HBU – Constraints

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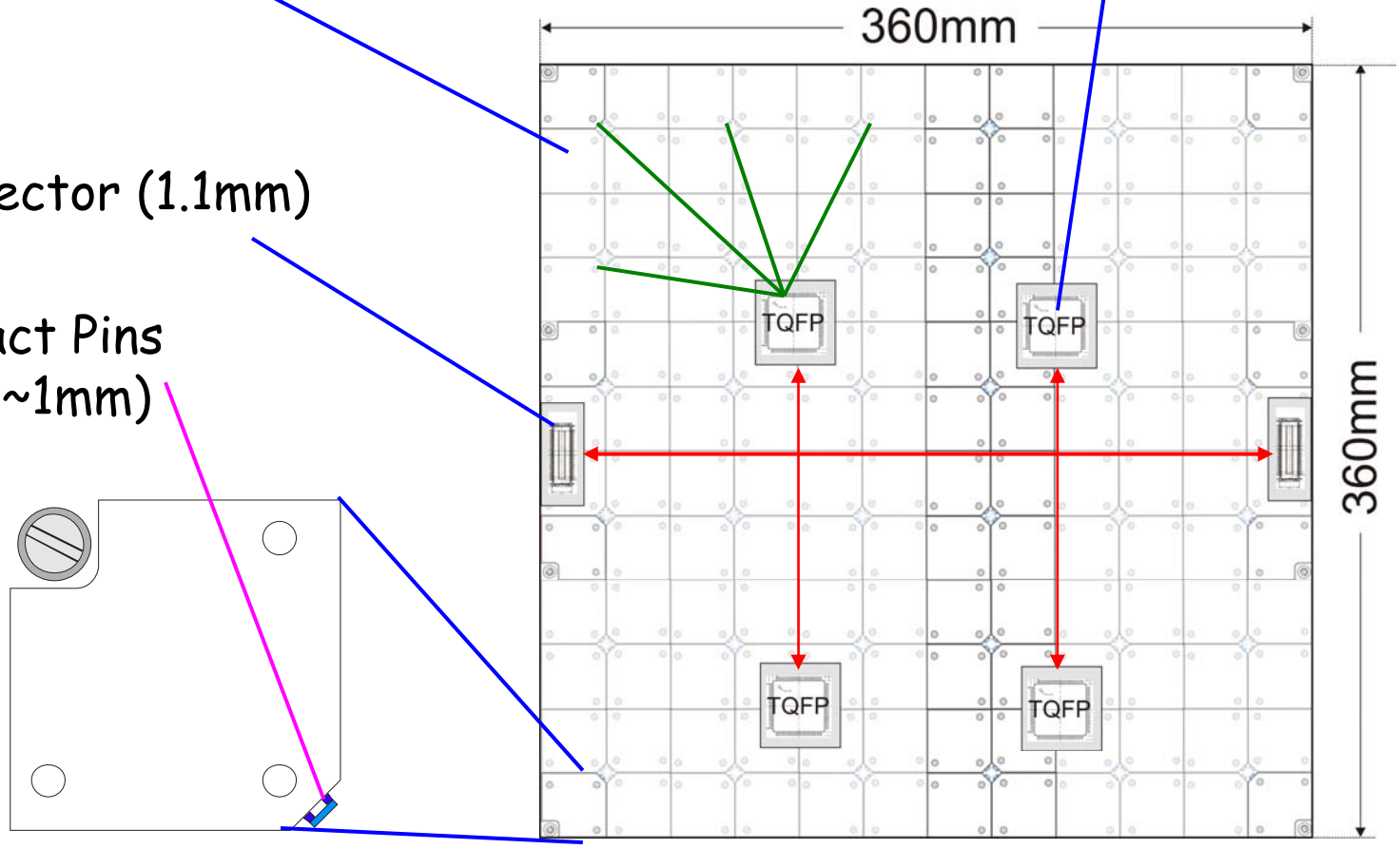
**PCB (*shown transparent*):**
Two signal layers (50Ω):
- CLK, Control, Data, LED
- SiPM Readout, HV

ASIC - TQFP100
36 inputs (1mm)

Connector (1.1mm)

SiPM Contact Pins
(soldering, ~1mm)



# HBU - PCB layer structure I

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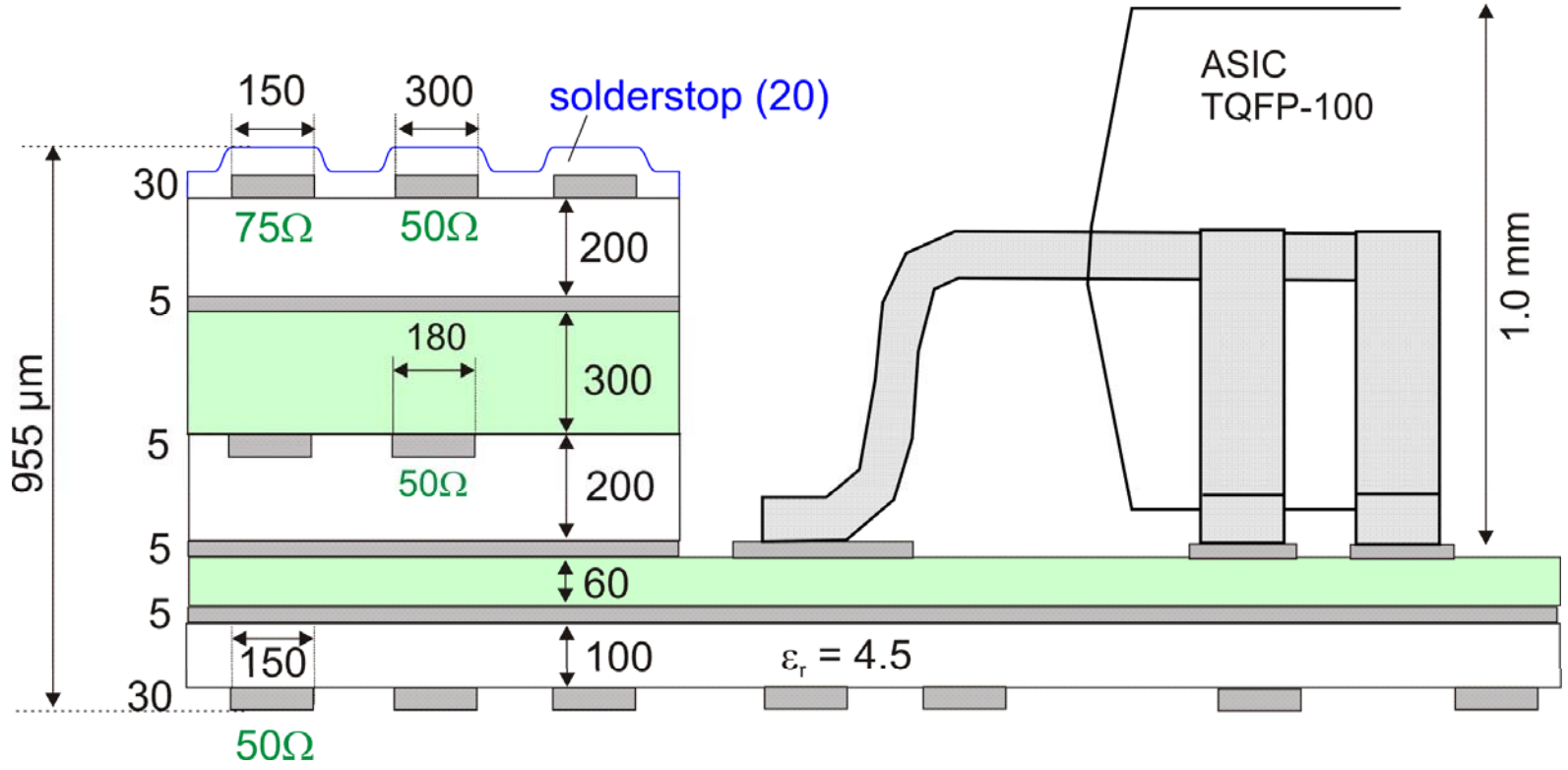
-6 layer design with cut-outs for ASICS and connectors
-75Ω Lines for high-gain SiPM setup
-Three signal layers for impedance-controlled routing
-**Total height (PCB + components): 1.32mm**
- Feasibility / Cost-factor under investigation



# HBU – PCB Layer Structure II

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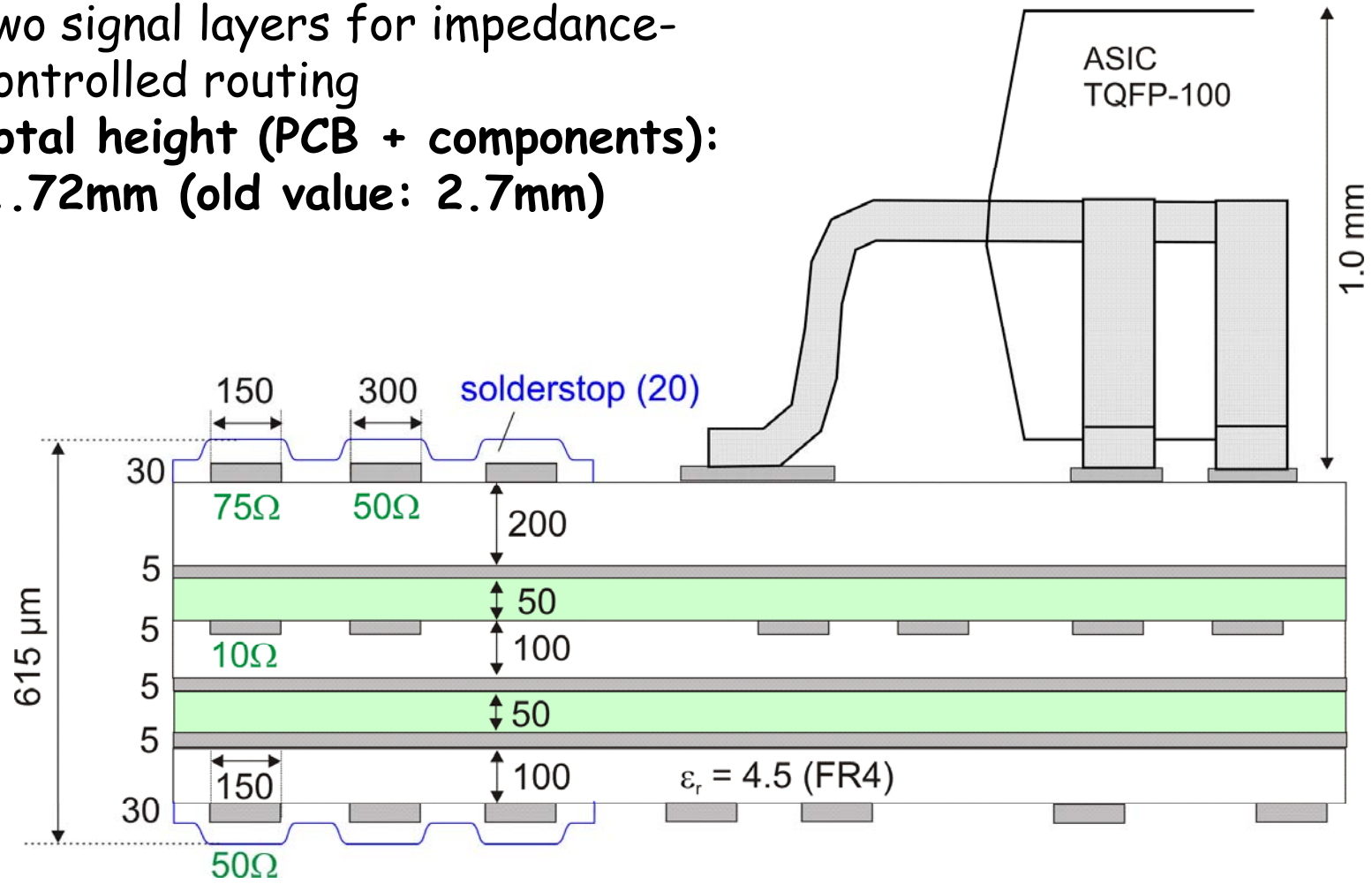
-6 layer design with standard setup
-75Ω Lines for high-gain SiPM setup
-Two signal layers for impedance-controlled routing
-**Total height (PCB + components): 1.72mm (old value: 2.7mm)**



# Testboard I : LED

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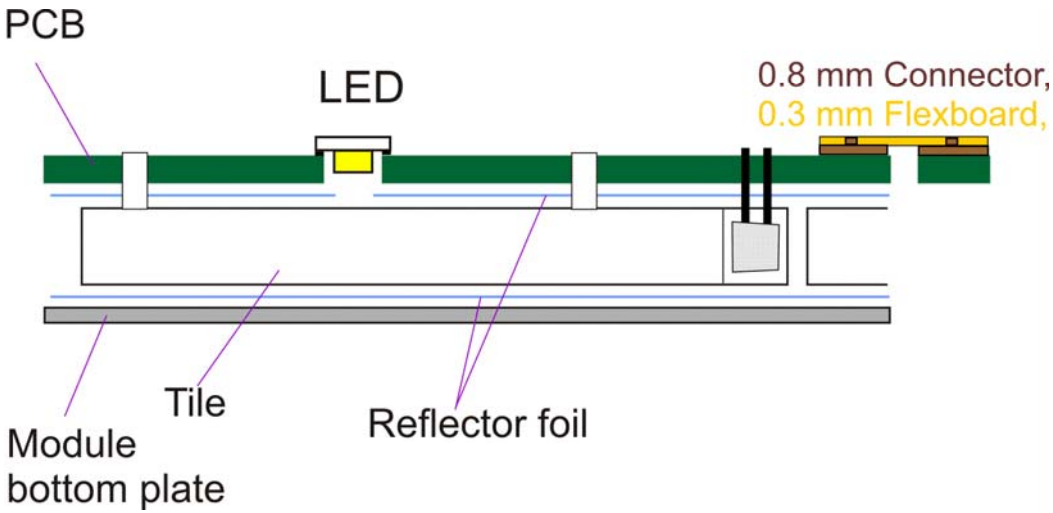
Test LED integration into HBU (LCS):
Proof of principle together with our colleagues from Prague

-Crosstalk of driving circuit to SiPM?

-Integration to PCB / coupling to tile?

-Connector test: stability, number of connection-cycles?




**Features:**
- SMD LEDs (two types)
  LED size 1.6 x 0.8 x 0.6 mm³
- Several LED driving circuits
- >2 Tiles with analog output
- proposed HBU Connector
- Multilayer PCB needed!!
  (crosstalk test)
- No ASIC…

# Testboard II : SPIROC

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SPIROC (ASIC) Testboard **IS** HBU prototype!

Test of:

-Cassette (=HBU) assembly (tiles, electronics, cover)

-Performance of SPIROC in the dense HBU setup
(noise, crosstalk, power, gain, …)

-LCS with LEDs on board

-Signal Integrity (see Testboard III),
Communication with DAQ

-Analog AND digital outputs / interfaces (next slide)

# Testboard II : Integration

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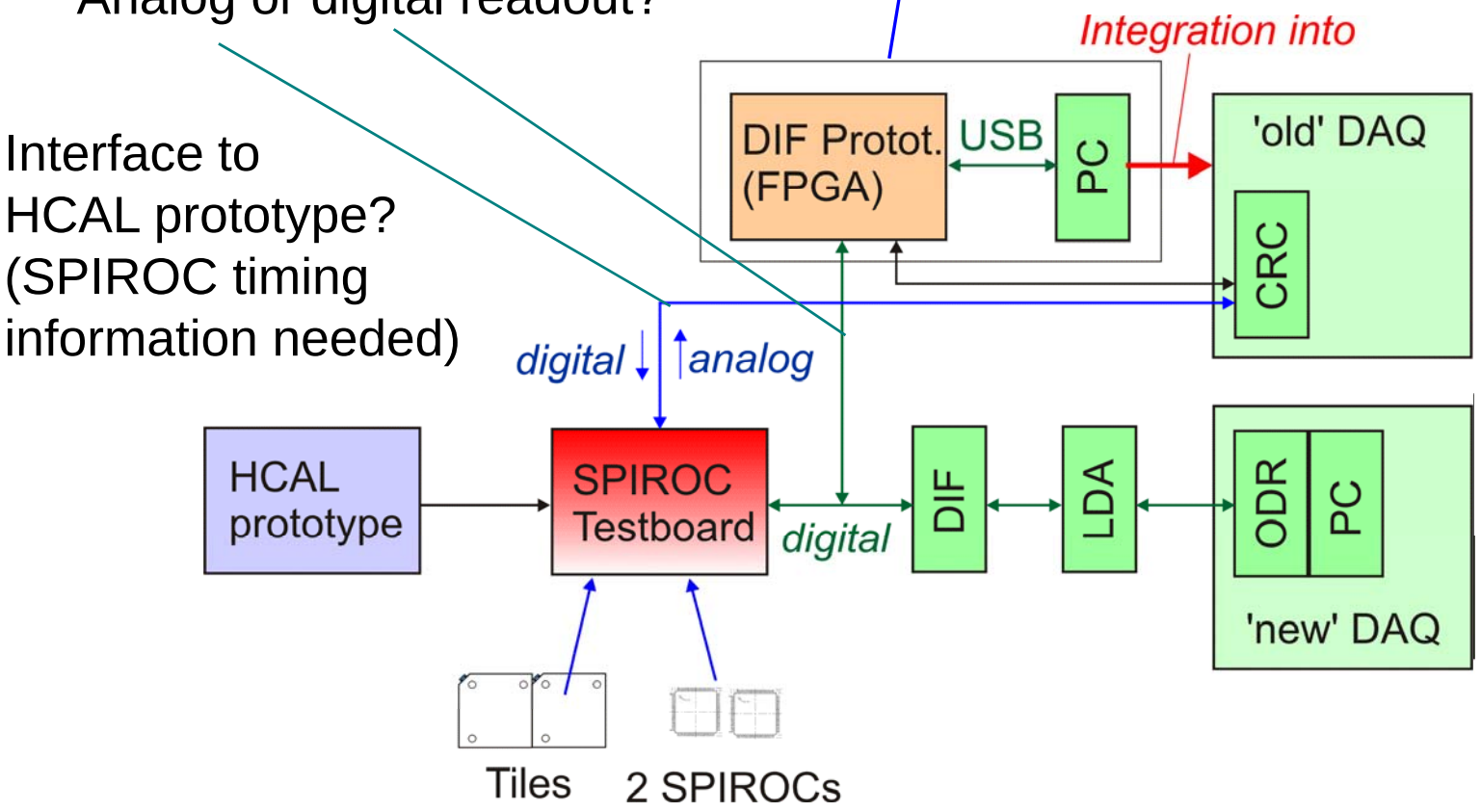
## Environment of the SPIROC Testboard:

Stand-alone, or Integration into old DAQ?
(Menpower problem …)

When using CRC:
Analog or digital readout?

Interface to
HCAL prototype?
(SPIROC timing
information needed)



# Testboard III : Power-System

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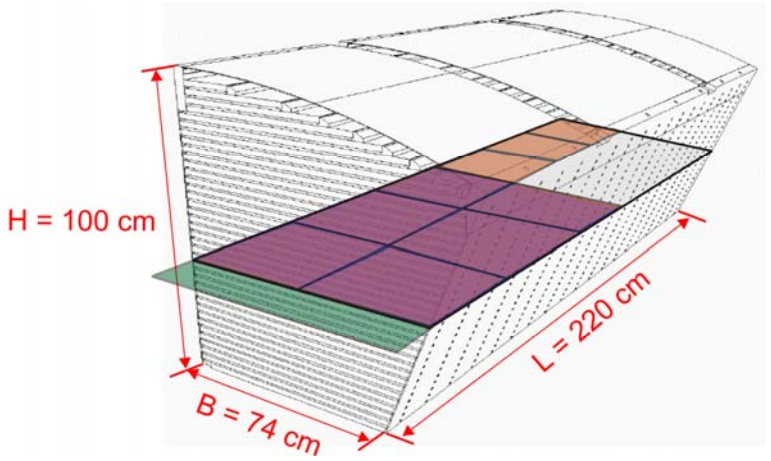
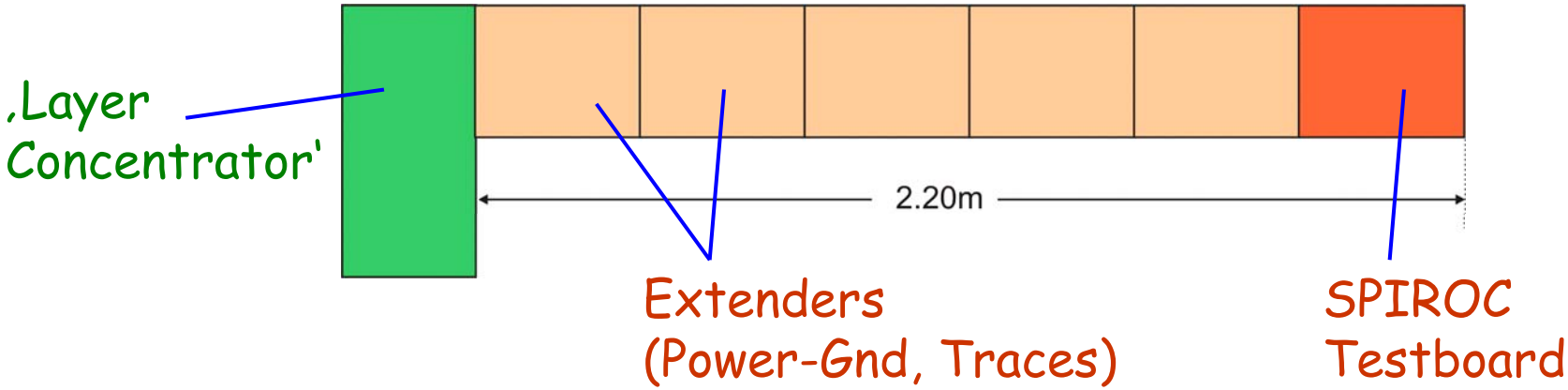
Test Power-Ground System (2.20m):

-Oscillations when switching?

-Voltage drop, signal integrity
(traces, connectors)?

-SPIROC performance @ far end
(blocking caps sufficient)?



# Light Cal.-System - Constraints

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Tile: For 1 MIP ≈ 15 pixels ↔ 12 photons * 5 * 1.75 ≈ 100 photons

Crosstalk (1.25px)

Losses

SiPM efficiency (20%)

1. Photons per second into tile:

$$n_{PH} = \frac{N_{PH}}{t} = \frac{100}{5ns} = 20 \cdot 10^9 \frac{1}{s}$$

2. Optical output power (LED):

$$P_{opt} = n_{PH} \frac{hc}{\lambda} = 10nW$$

$$h = 6.626 \cdot 10^{-34}\ Js$$

$$c = 3 \cdot 10^8 \frac{m}{s}$$

$$\lambda = \lambda_{UV\_LED} = 400nm$$

# Light Cal.-System - Constraints

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3. From LED data sheet:

$$P_{opt} = 1.1mW \;\; @ \;\; 20mA \;\; \& \;\; 3.5V$$

$$\Rightarrow \;\; 10nW: \quad I_{drive} = 181\,nA$$

4. Charge in single pulse:

$$Q = I_{drive} \cdot t = 181nA \cdot 5ns = 0.91\;fC$$

Current/Charge is dominated
by LED capacitance and/or parasitics

# Light Cal.-System - Constraints

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5. LED Input Power (Heat, only when active)

$$P_{in} = I_{drive} \cdot V_{diode} = 0.633\,\mu W$$

$$P_{heat} = P_{in} - P_{opt} = 623\,nW$$

LED driver has to be added (not yet clear)

Promising parameters for a low-crosstalk LED implementation!
Verification together with our colleagues from Prague.

# LED Drive Circuits

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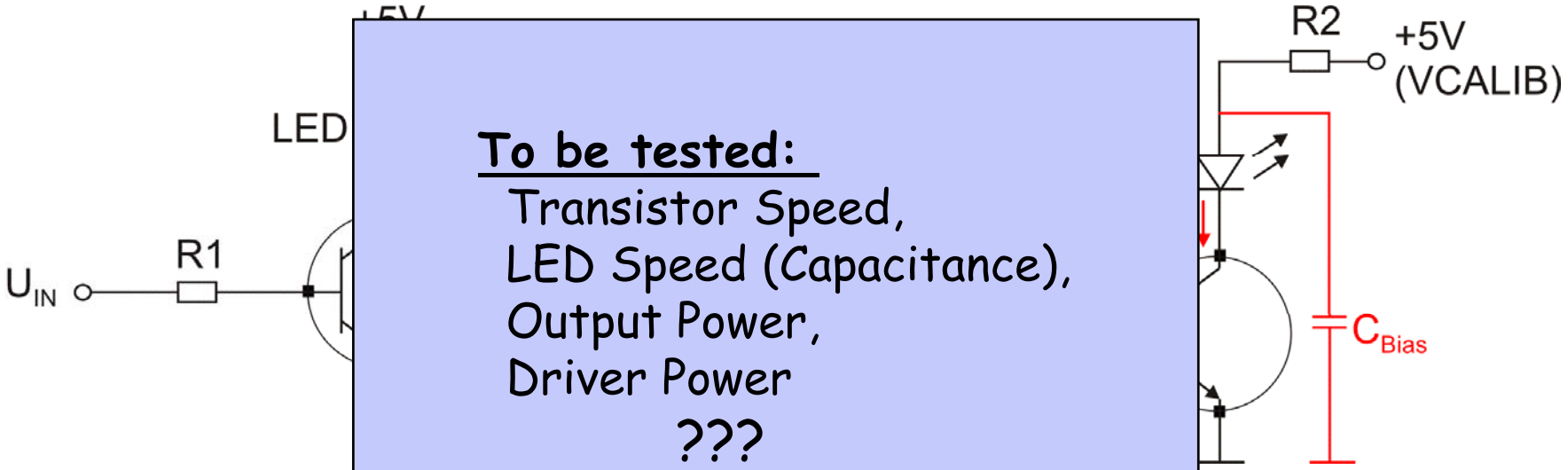
## Analog Driver

## Digital Driver

Transistor is ‚on' or ‚off'




**To be tested:**

Transistor Speed,
LED Speed (Capacitance),
Output Power,
Driver Power
???

$$I_{LED} = \left(\frac{U_{in} - 0.6V}{R2}\right) \cdot \left(\frac{\beta}{\beta+1}\right)$$

$$181nA = \left(\frac{5mV}{25k\Omega}\right) \cdot \left(\frac{10}{10+1}\right)$$

$$I_{LED} = \frac{V_{Calib} - V_{LED} - V_{T,sat}}{R2}$$

$$200nA = \frac{3.8V - 3.5V - 0.25V}{250k\Omega}$$

# Conclusion

FEB

-LED Testboard design starts now.

-HBU PCB structure in discussion with companies.

-SPIROC Testboard (HBU protot.) design started summer/autumn 2007 (ASIC Pinout and loading sequence is not fixed).

- Time schedule for DAQ (possibly prototype) should be discussed.