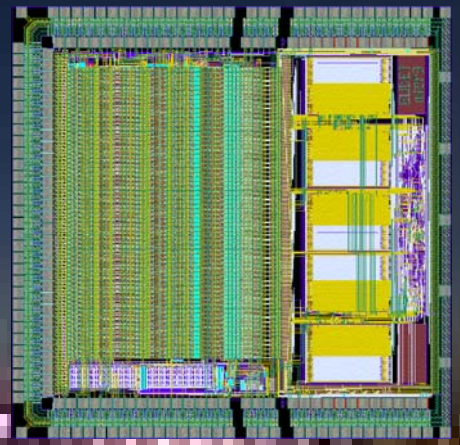
# HaRDROC performance

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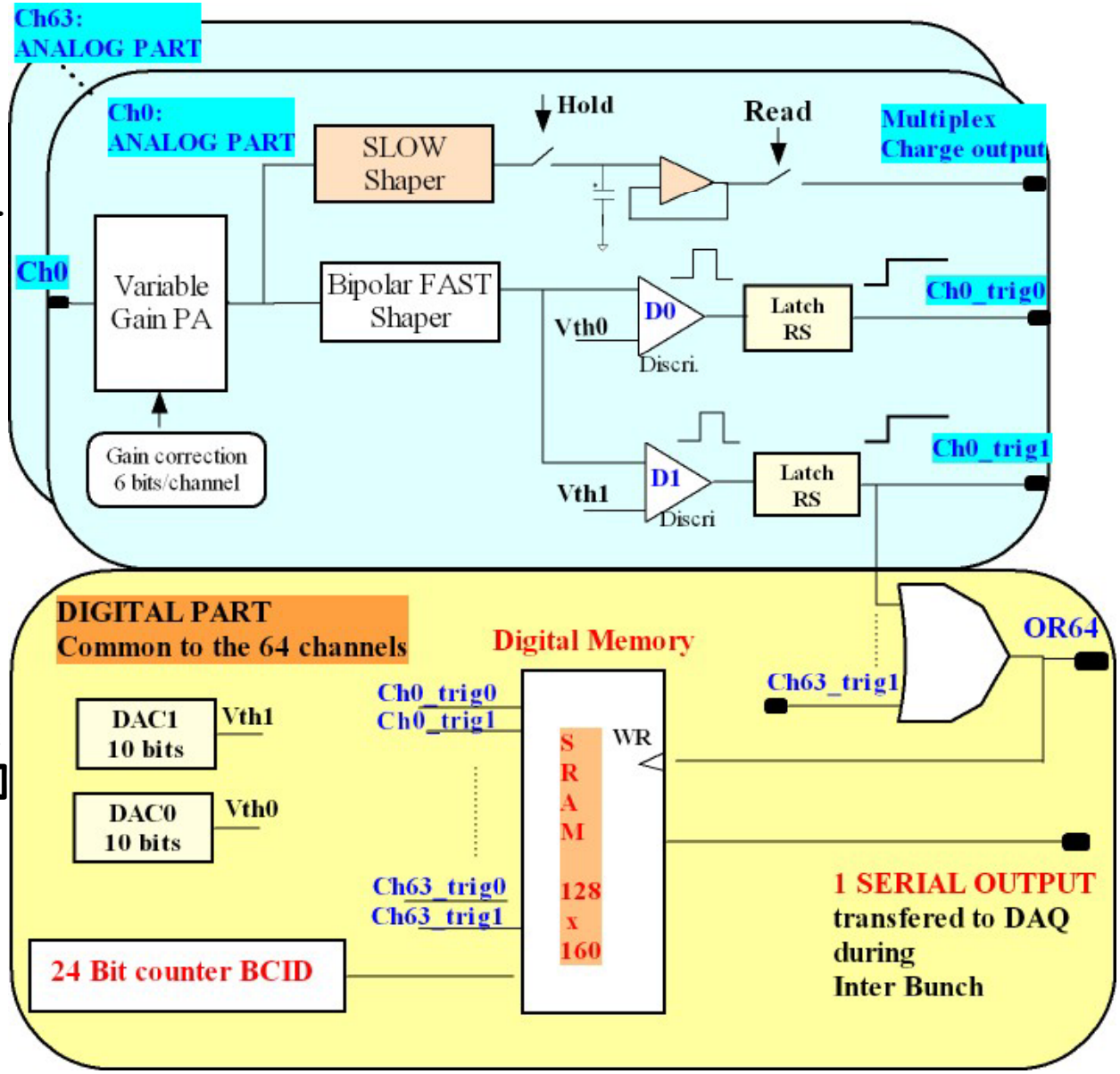
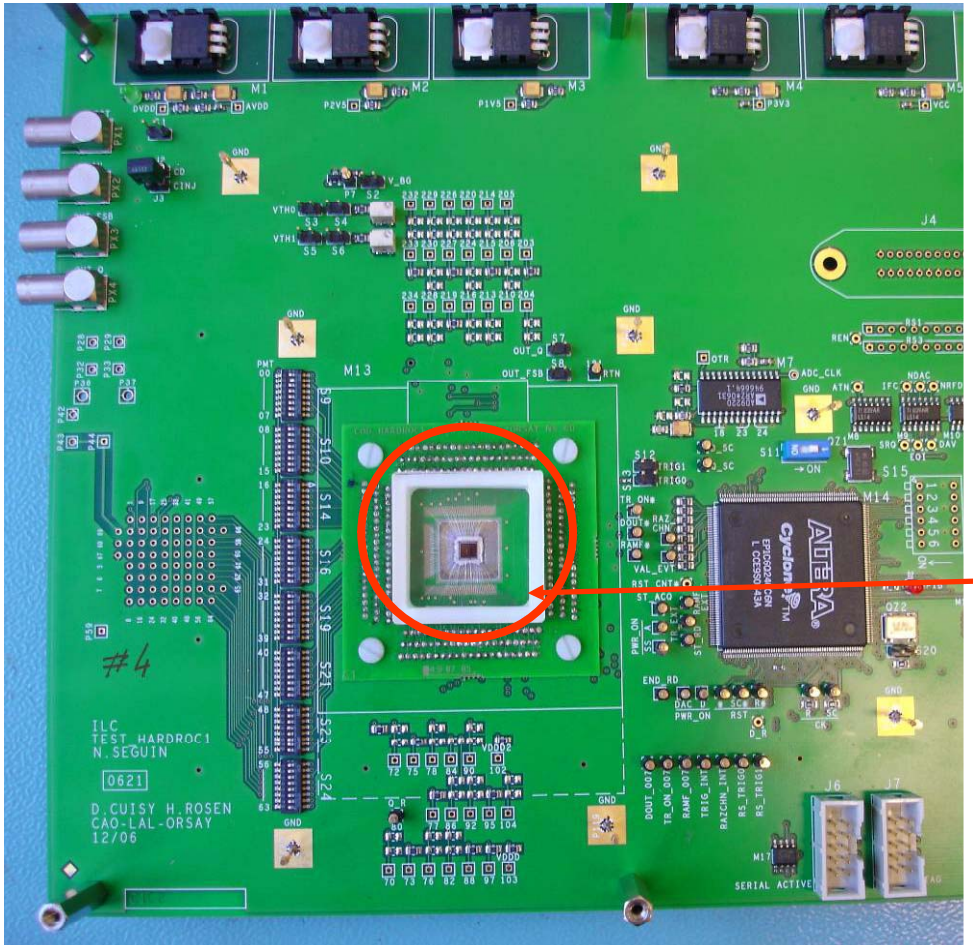
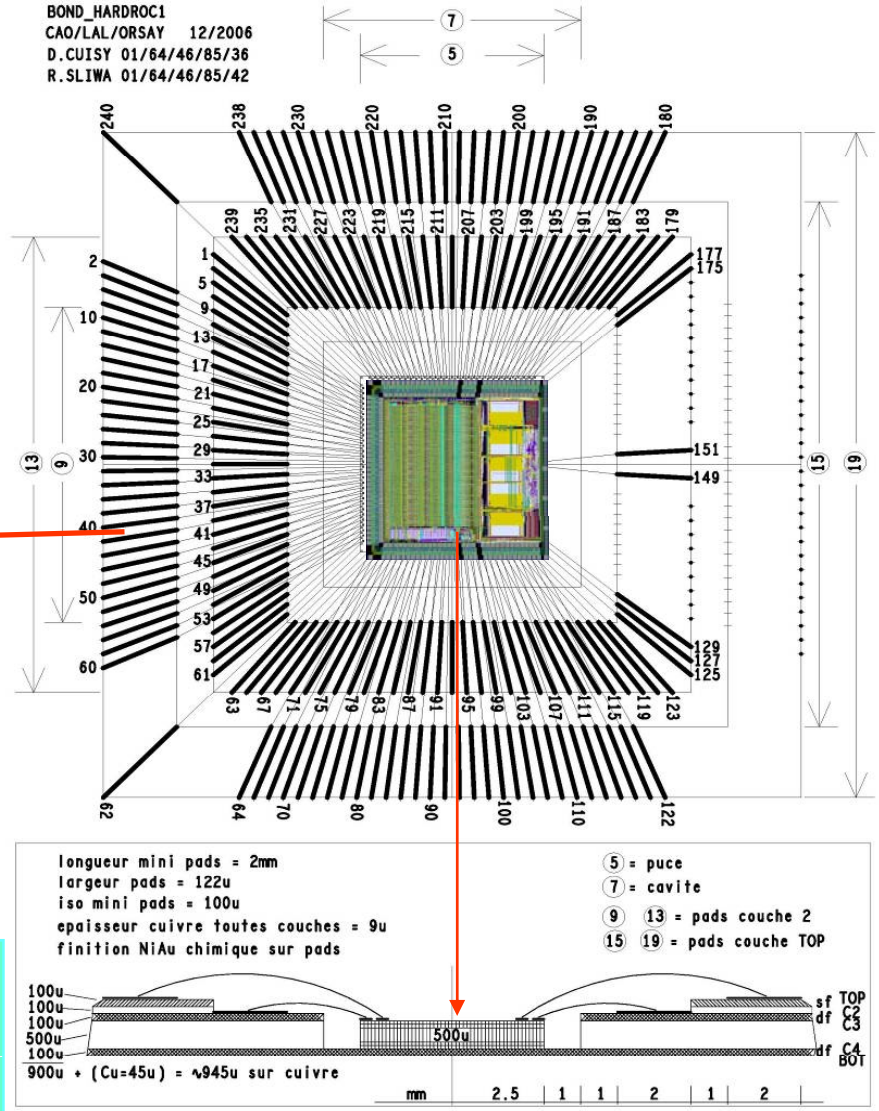
# HaRDROC architecture

- Full power pulsing
- Digital memory: Data saved during bunch train.
- Only one serial output @ 1 or 5MHz or more
- Store all channels and BCID for every hit. Depth = 128 bits
- Data format : 128(depth)*[2bit*64ch+24bit(BCID)+8bit(Header)] = 20kbits
- Based on MAROC ASIC, but several design changes



# HARDROC1: TESTBOARD with Chip On Board

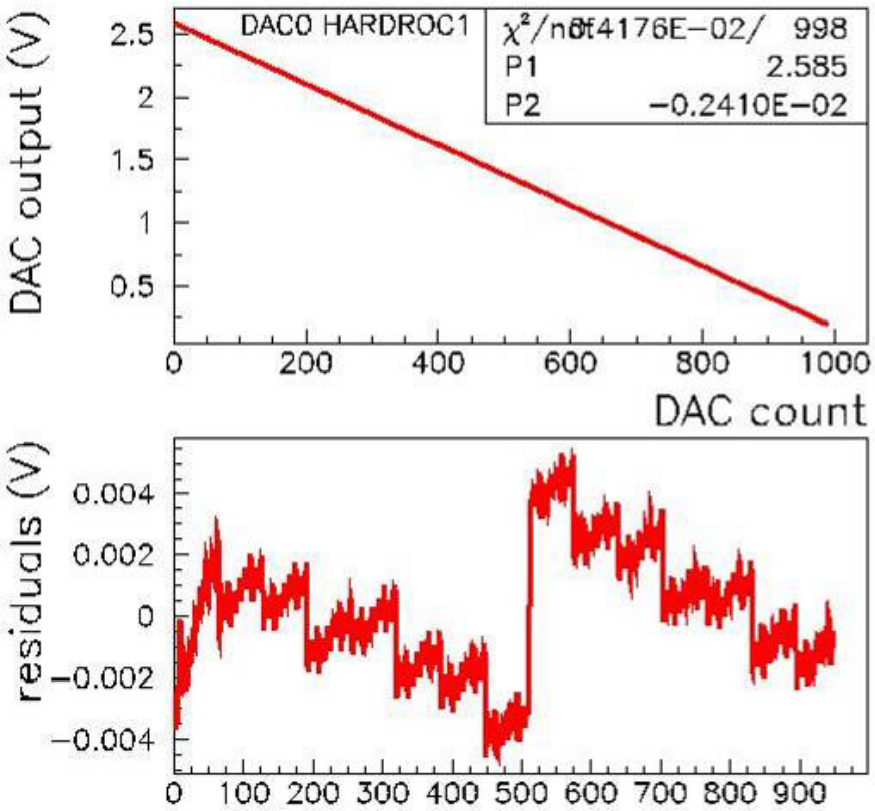


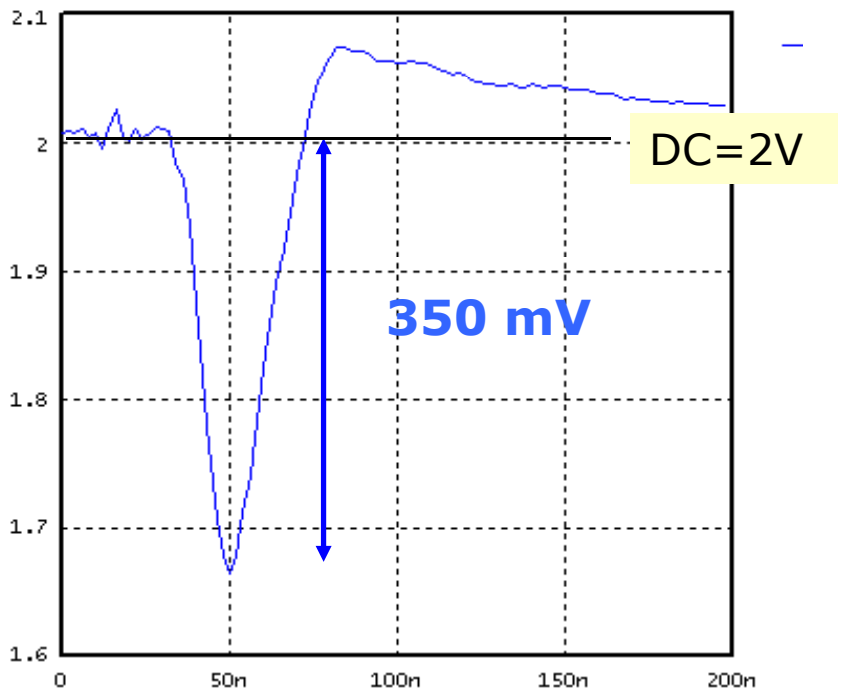

**PCB for COB:** to estimate feasability (ECAL)
6 layers, COB on Layer 5
2 steps to facilitate the bonding

# Trigger efficiency: Scurves

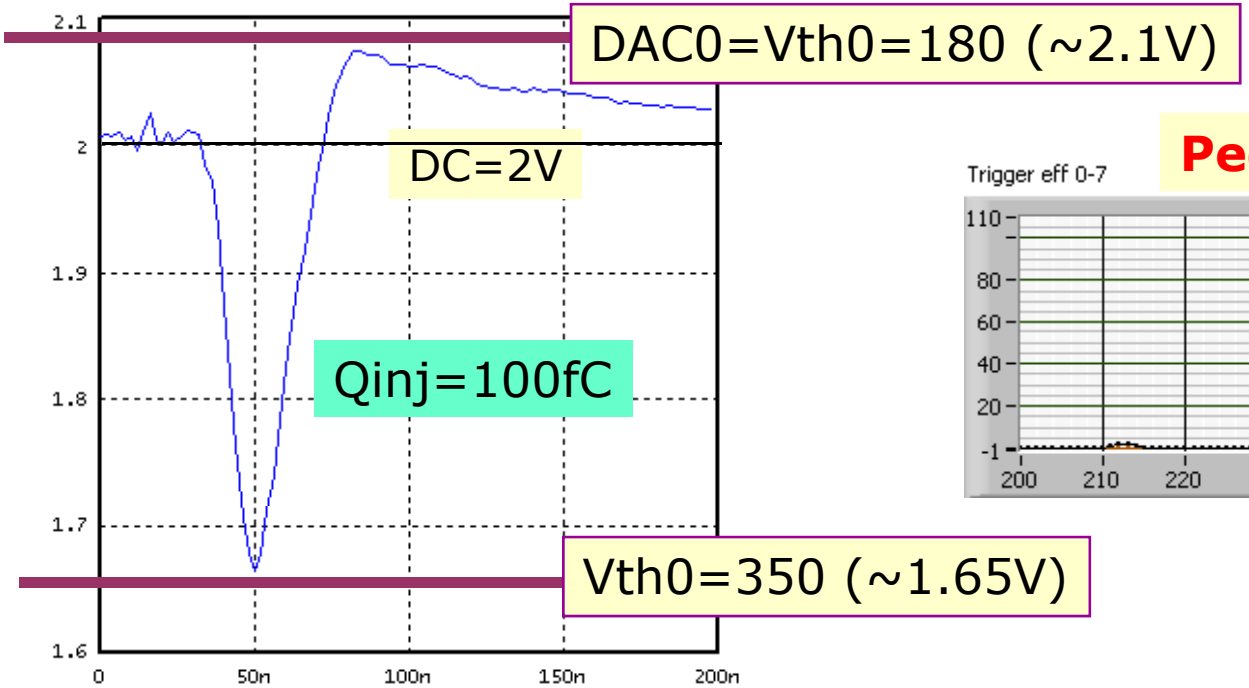
- **Charge injected in one channel: 100fC**
  - **Typically 3.5mV/fC**
- **Scurves performed by varying the DAC value (Threshold)**
  - 2 integrated DACs to deliver Threshold voltages
  - Residuals within ±5 mV / 2.6V dynamic range. INL= 0.2% (2LSB)
  - **2.5 mV/DAC Unit ie 0.7 fC/UADC**

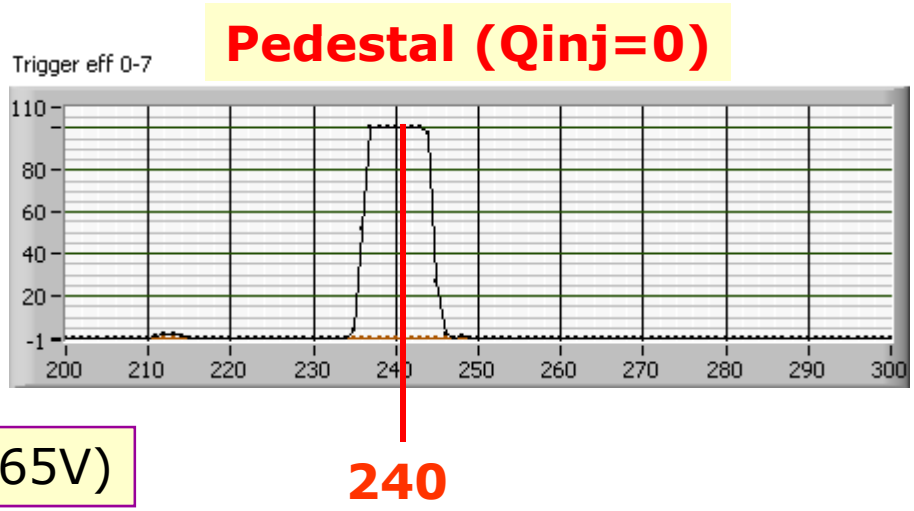


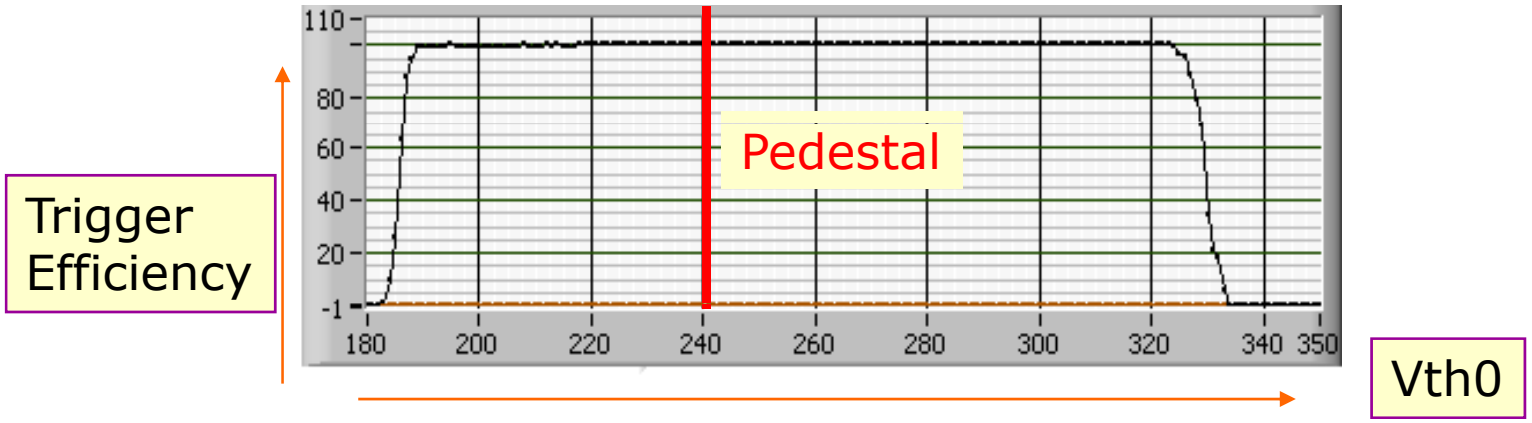

**Out FSB @Qinj=100fC**



# Trigger efficiency: Scurves

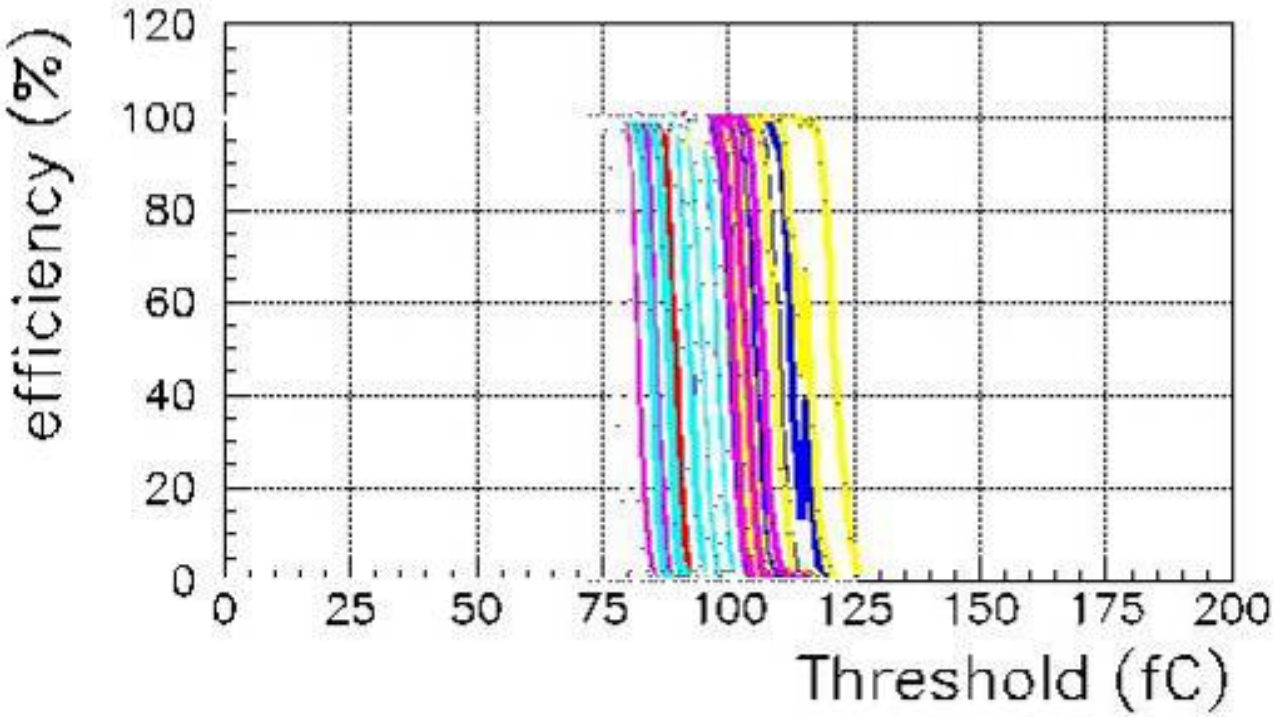


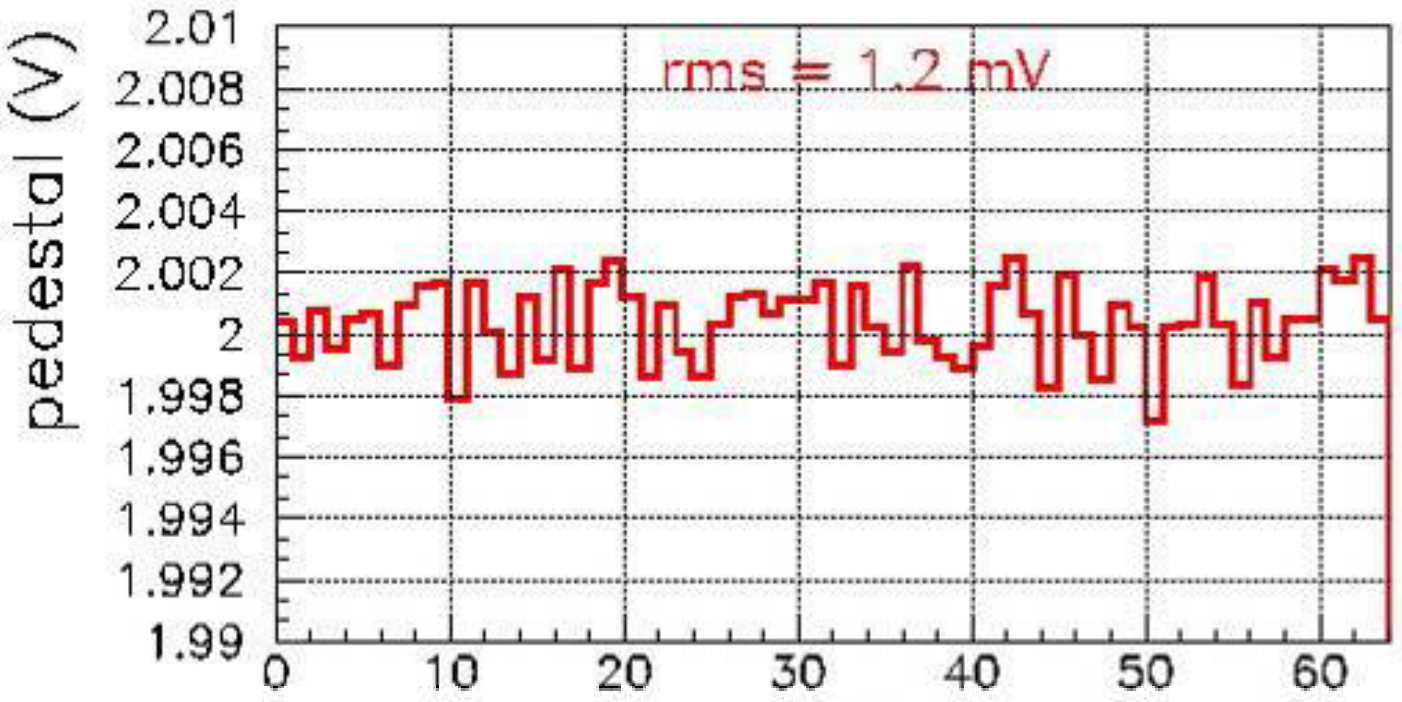



# Scurves of the 64 channels, Gain PA=1

- Charge injected in each channel: 100fC
- Non uniformity quite large (±25%) due to current mirror mismatch (small transistors to optimise speed)
- Can be compensated by tuning the gain of each channel

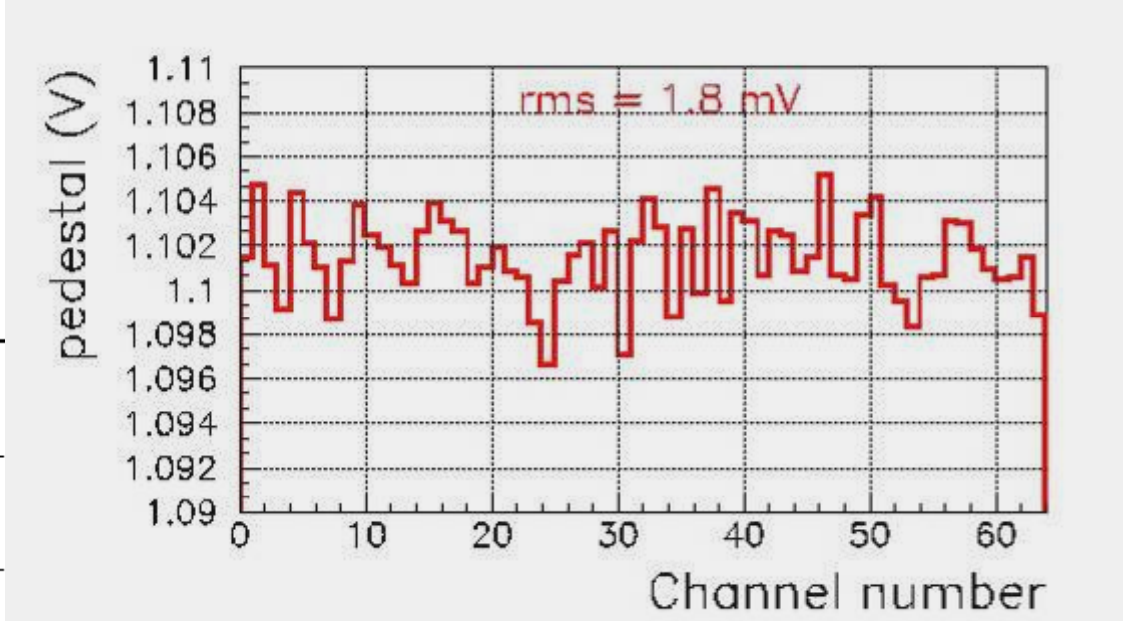


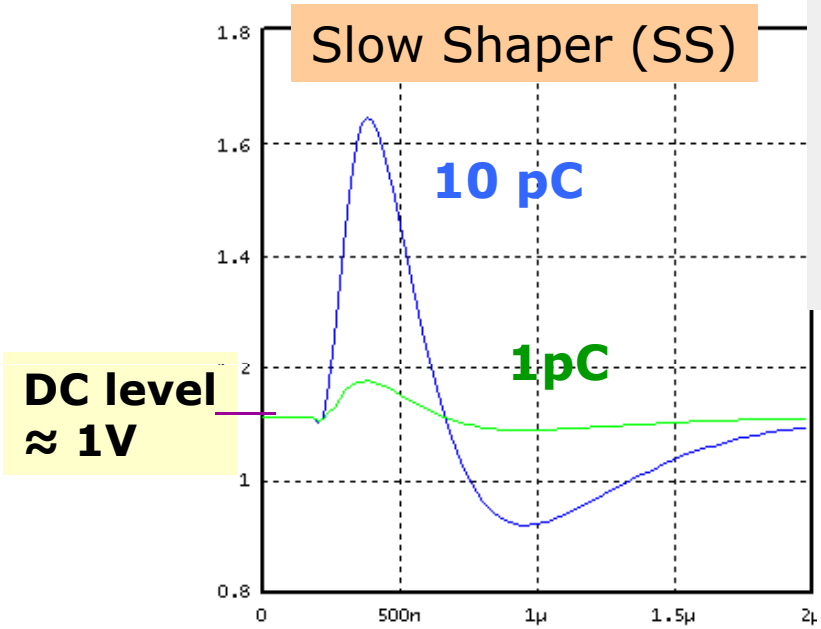
# FSB DC measurement: Uniformity



# SS waveforms (scope measurements)

- Out Q: Very usefull for detector characterisation
- DAQ0
- SS: 10 pC => 535mV, slowest peaking time:tp=150 ns



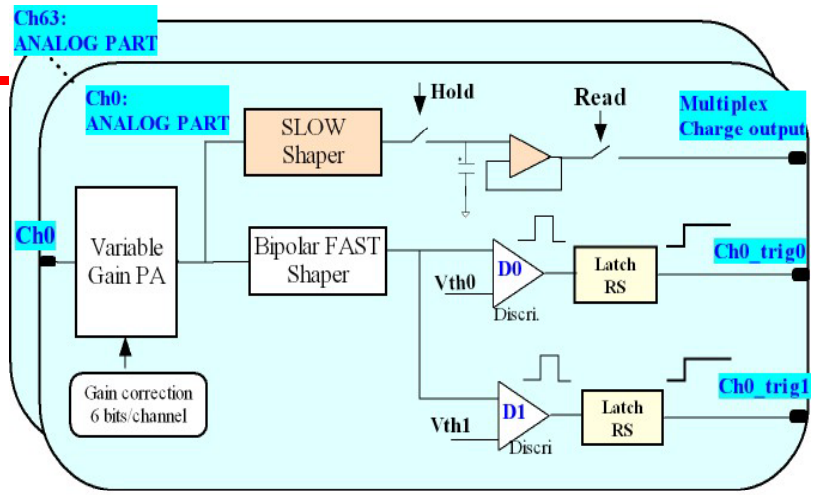
# Zin and Xtk

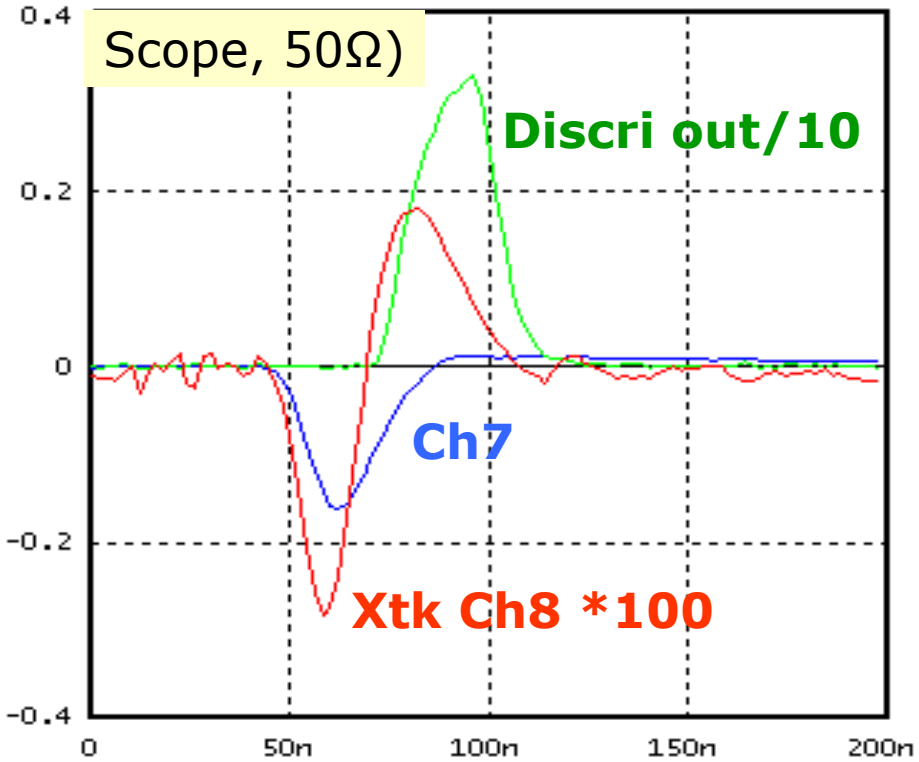
- **Zin (PA)=50Ω with Vgain=3V,**
- **Zin (PA)=70Ω with Vgain=3.5V**

- **Qinj=100fC on Ch7**
  - out_fsb=160mV (on 50Ω), tp=15ns

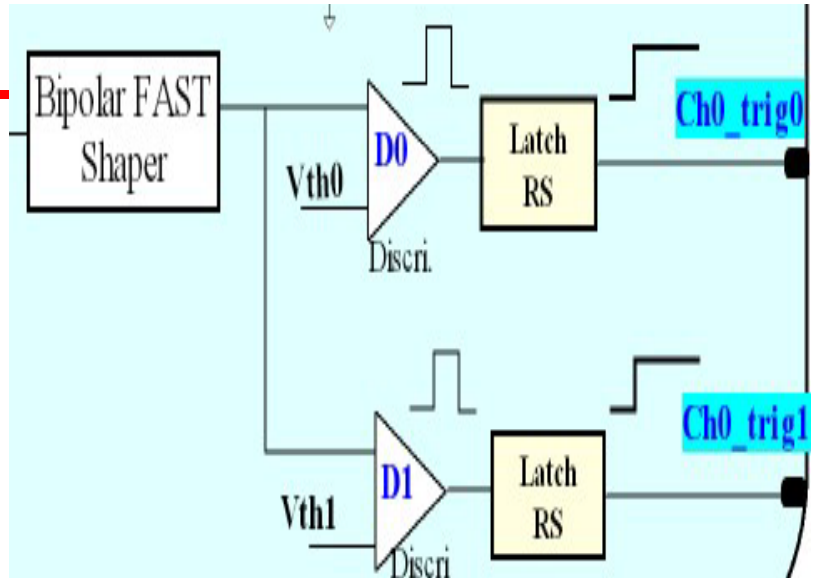
- **Xtk: well differentiated**
  - Ch6: ± 3mV
  - Ch8: ± 3mV (± 2%)
  - Ch9: ± 0.5mV

- **Xtk: on the input**
  - Gain=1 on Ch7 and Gain=0 on Ch8,
    - => Xth (ch8)=0

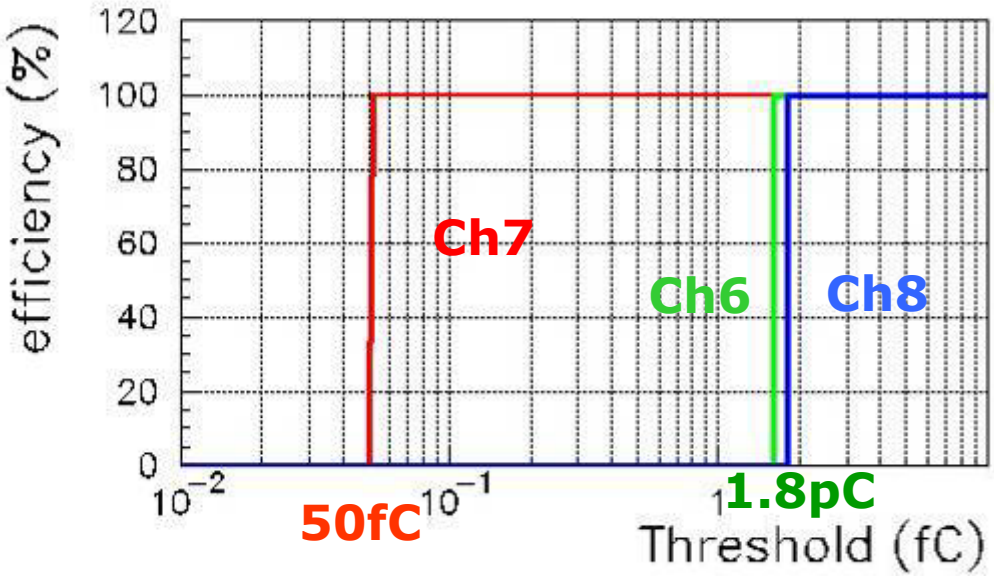


# Trigger Xtk:




- **DAC0 and DAC1 = 300**
  - (=> Vth0 =Vth1~50fC)
- **Qinj in Ch7**
  - Up to 1.6 pC: triggers on CH7 only, nothing on the neighbors
  - 1.8 pC: Triggers on Ch7 and CH6, no trig on other channels
  - 2 pC up to 5,6pC: Triggers on CH7, CH6 an 8
  - 10pC Triggers on Ch7 anc on the 4 direct neighbors



# Power dissipation

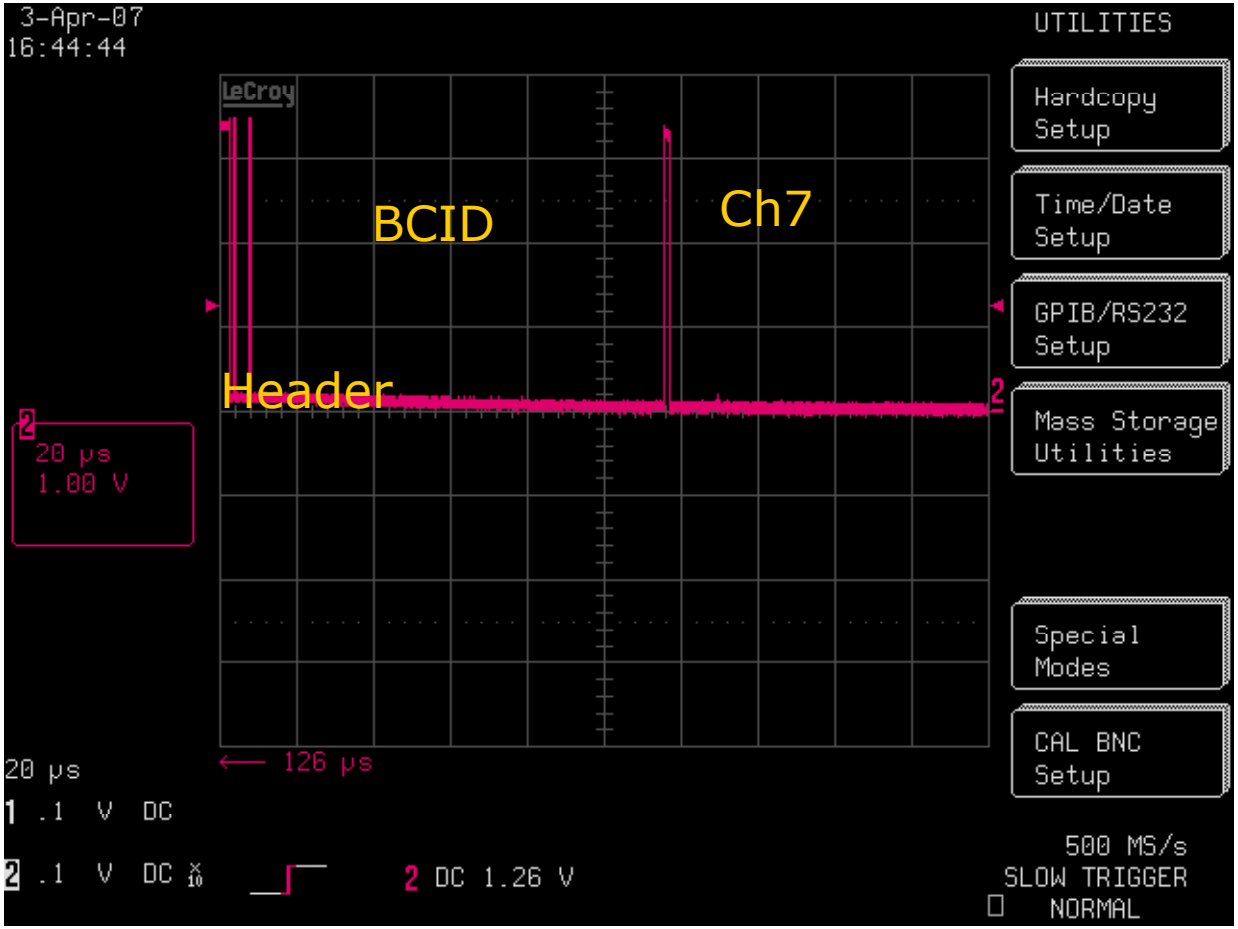
- **Measured power dissipation (no power pulsing)**
  - Preamp : 6 mA = 100 µA/ch
  - Fast shaper : 5,3 mA
  - Discriminators (2) :  5.9 mA
  - Slow shaper (used only for backup) : 14.5 mA
  - DAC : 0.8 mA
  - Bandgap reference : 5 mA
  - Digital part : 3 mA

- **Total : : 26 mA*3.5V = 90 mW/64ch = 1.4 mW/channel**
  - 140 mW if slow shaper (analog readout) is used

- **Need to test power pulsing (0.5 to 1% duty cycle) -> 8-15 µW/ch**

# MEMORY FRAMES: Auto trigger mode

**Auto trigger with 10fC:**
Qinj=10fC in Ch7
DAC0 and DAC1=255 (~5fC)



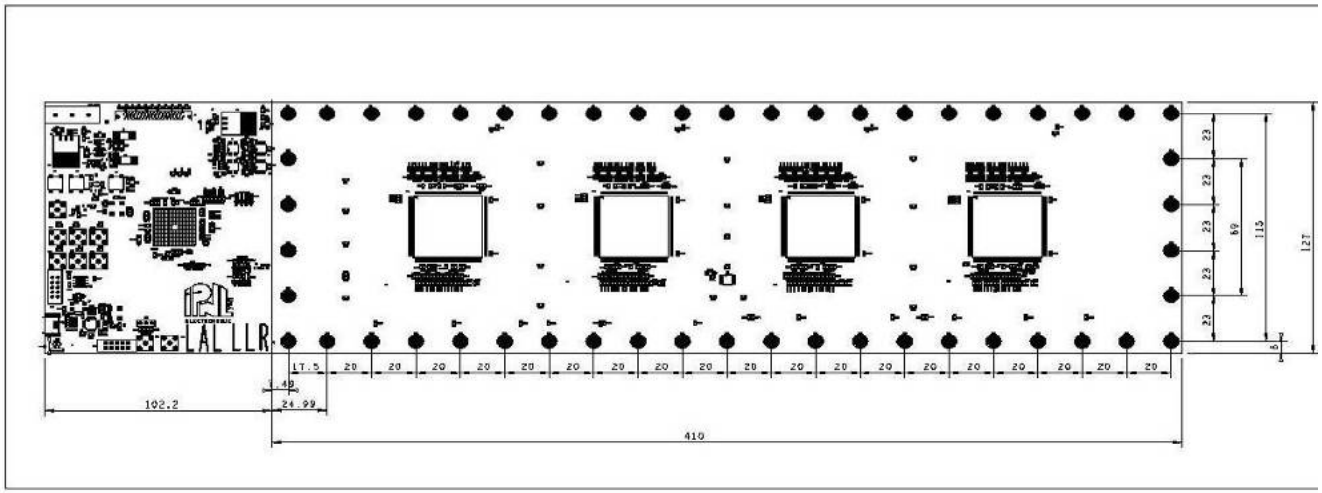
# HARDROC1 PERFORMANCE SUMMARY

| | |
|---|---|
| Number of inputs/outputs | 64 inputs, 1 serial output |
| | |
| Input Impedance | 50-70Ω |
| Gain Adjustment | 0 to 4, 6bits, accuracy 6% |
| Bipolar Fast Shaper | ≈3.5 mV/fC tp=15ns |
| 10 bit-DAC | 2.5 mV/fC, INL=0.2% |
| Trigger sensitivity | Down to 10fC |
| | |
| Slow Shaper (analog readout) | ≈50 mV/pC, 1fC to 10pC , tp= 100ns to 150ns |
| Analog Xtk | 2% |
| Analog Readout speed | 5 MHz |
| | |
| Memory depth | 128 (20kbits) |
| Digital readout speed | 5MHz or more |
| | |
| Power dissipation (not pulsed) | 100 mW (64 channels) |

# CONCLUSION

- **Permormance of hardroc1: so far so good**
  - **Autotrigger down to 10fC**
  - Digital part: OK for one chip

- **Lot of work to be done for the readout of several chips with DAQ0 and DAQ2**
  - 15 chips measured before being mounted on DHCAL PCB (4 chips /PCB), which were received at the beginning of May.

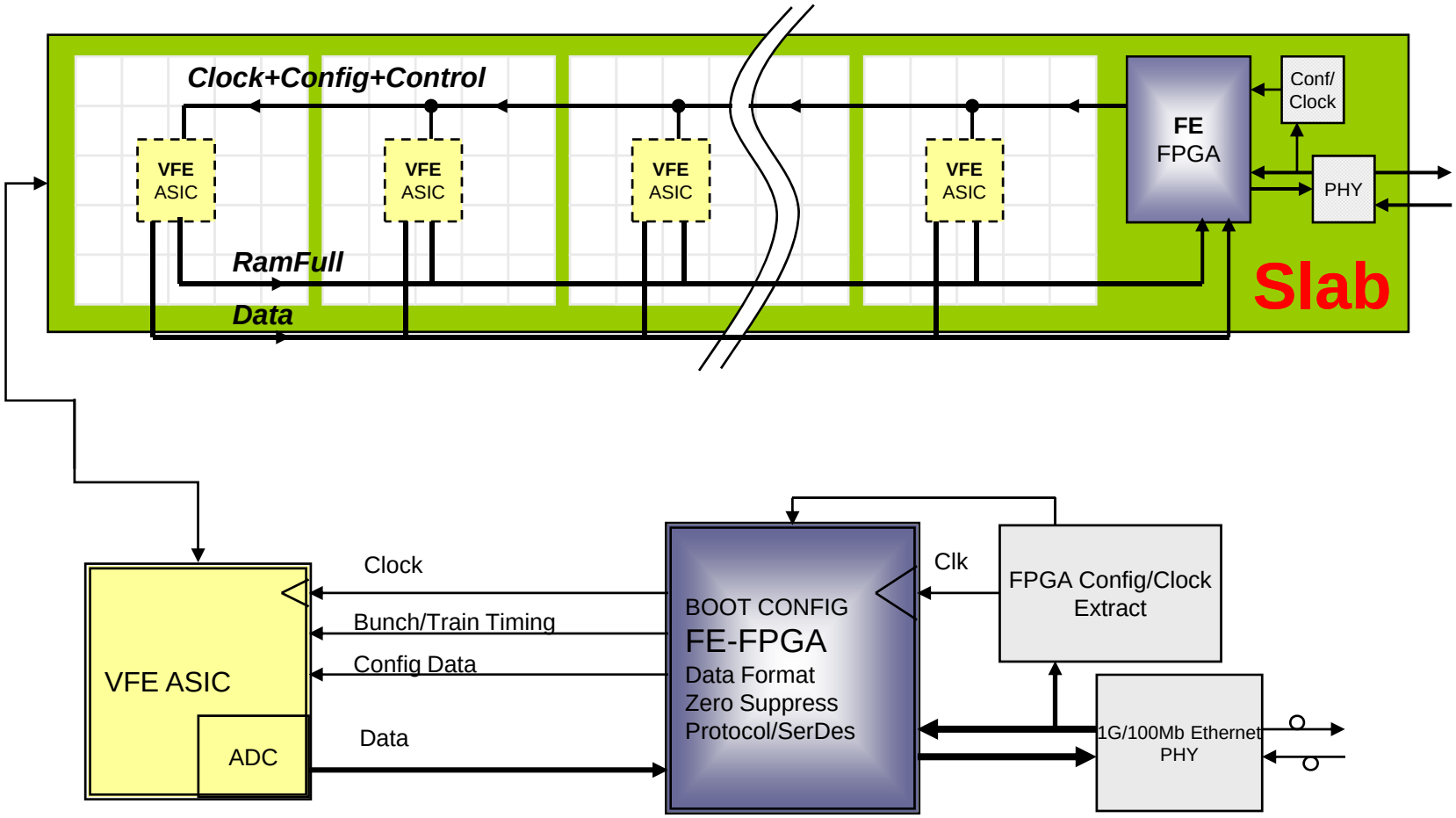


# ANNEXE

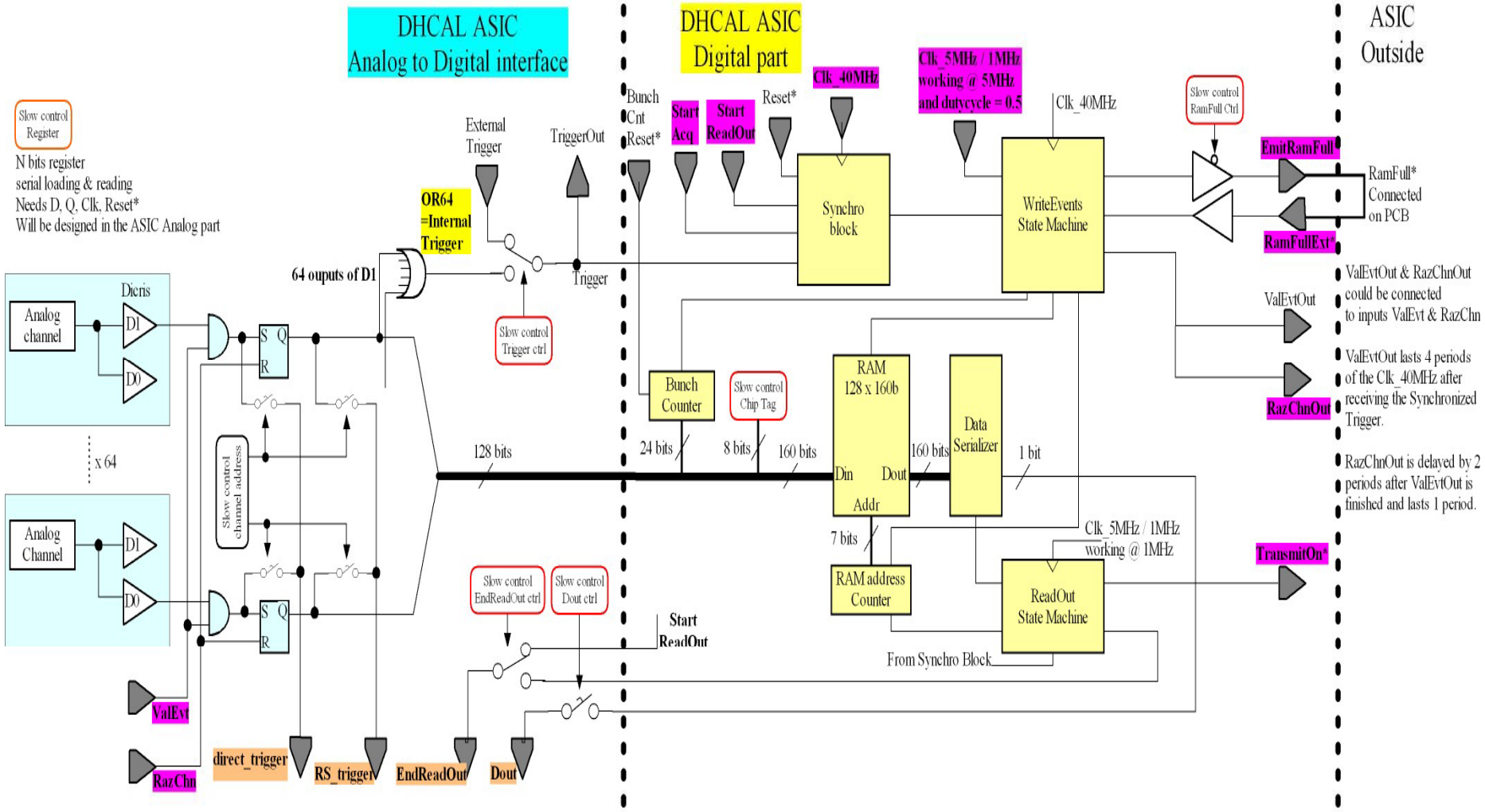
# Digital architecture towards 2nd generation DAQ

ECAL, AHCAL, DHCAL

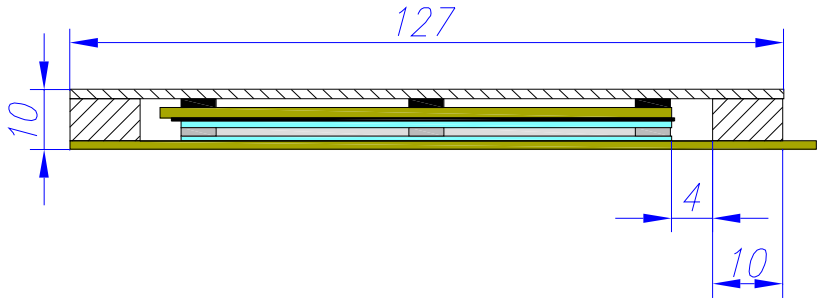
## detector readout

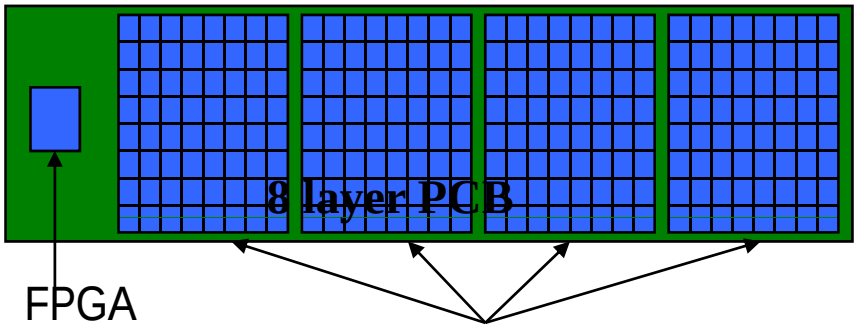


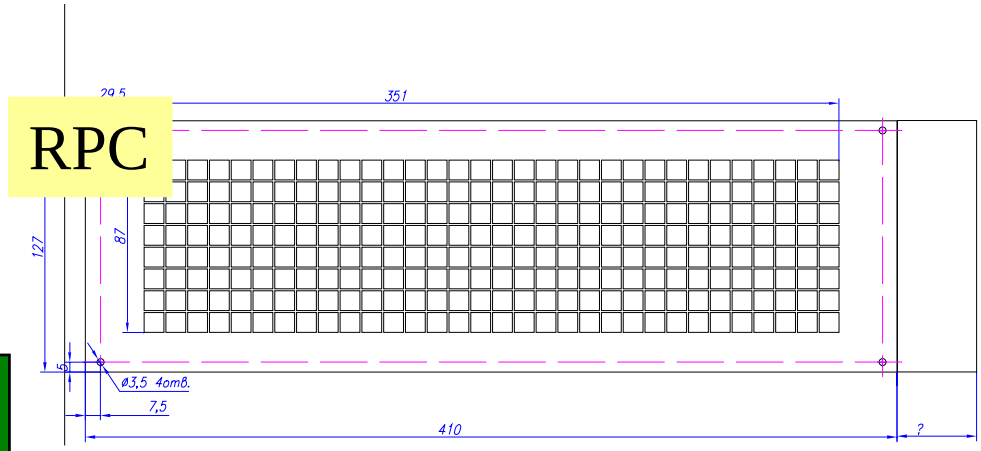
# HARDROC1: digital part



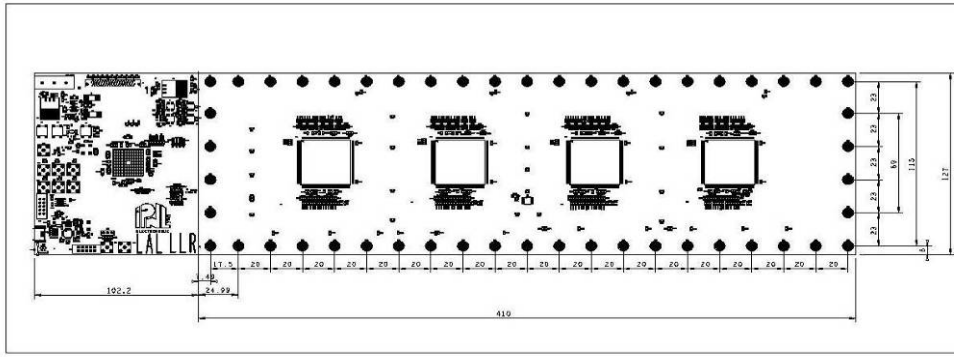
# 8x32 pads: RPC and μMegas




4 areas of 64 pads of 1 sq cm : bottom layer
Hardroc external components : top layer



-6 PCBs (4chips): received beginning of MAy

-Tests with cosmics (standalone USB DAQ) in LLR +IPNL in June

-

-Tests in July07 with test beam at DESY and CERN with DAQ0

-Can be used for DAQ2 tests (UK)