DHCAL Acquisition with HaRDROC VFE

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Preliminary remarks

- *My current understanding...*

- First detector with 2nd generation ASICs and 2nd generation DAQ
  - Integration of HaRDROC VFE chip in the PCB
- $1m^3 \equiv$ (here!) $70 \times 70 \times 100\ cm^3$
- $1 \times 1\ cm^2$ cells (plus margins)
  - ➔ 4096 channels / layer
    $\times$ 40 planes = 163 840 channels
- Occupancy: ~1000 channels/layer after zero suppression

HaRDROC
(Hadronic RPC Detector Read Out Chip)

- 64 channels → **2560 Chips in 1m³**
- 2 thr. with integrated DAC
- External or internal trigger
- power pulsing + full storage (depth: 128)
- Data format :
  - Energy: 2 bits / ch
  - 2bit × 64ch+24bit(BCID)+8bit(Header)
    = 160 bits per ASIC and per event
  - × 128 (full depth) = 20kbits per ASIC
- 1 serial link @ 1 Mhz for readout
- One additional seried analog output

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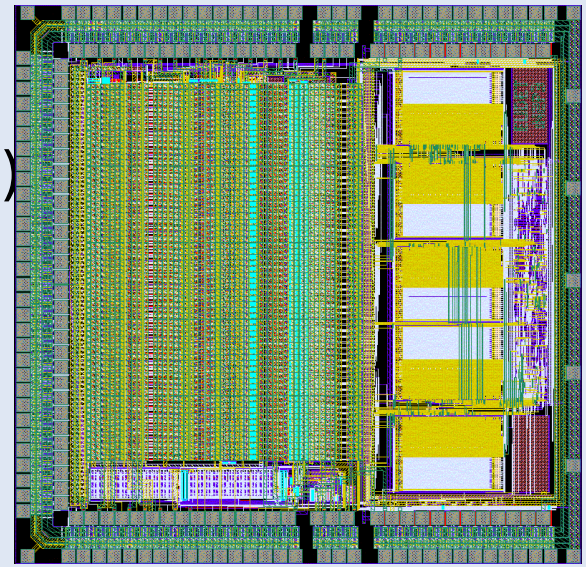
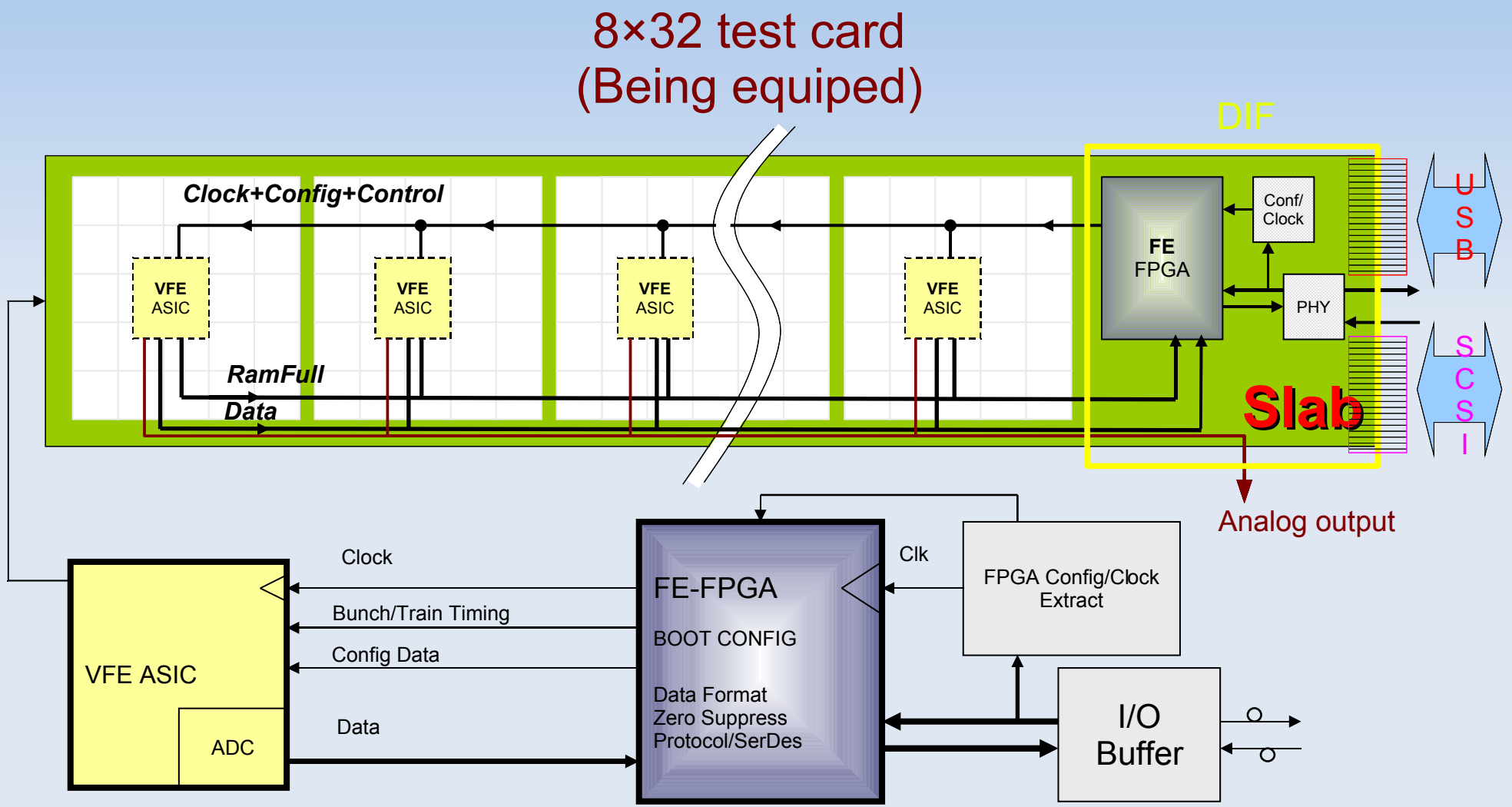


DAQ with VFE


8×32 test card
(Being equiped)
DIF
Clock+Config+Control
VFE
ASIC
VFE
ASIC
VFE
ASIC
VFE
ASIC
FE
FPGA
Conf/
Clock
PHY
USB
SCSI
RamFull
Data
Slab
Analog output
Clock
Bunch/Train Timing
Config Data
Data
VFE ASIC
ADC
FE-FPGA
BOOT CONFIG
Data Format
Zero Suppress
Protocol/SerDes
Clk
FPGA Config/Clock
Extract
I/O
Buffer

Timeline (reminder)

- Test assembly of RPC on PCB in may-june 07
  - ➔ Load parameters
  - ➔ Analog readout (cosmics)
- Beam test in Jul/Aug 07:
  - ➔ a single slab in beam @ DESY
  - ➔ Needs a Single Slab DAQ (Digi & Analog readouts) on 4 ASICs (256 ch.)
- End '07 – Beg '08: a full layer (8×8 ASICs, 4096 ch.)
  - ➔ DAQ0 Digital & Analog readout for at least one PCB
- End of 2008: full 1 m³ module
  - ➔ Full DAQ2 (digital readout of ~160k channels)

Single Slab DAQ (SSD): Digital

- For test of single 8x32 slab
  - ➔ Debug of digi readout; Assembly test
- Loading of parameters
- USB based
- Readout of digital part through the daisy link
- 2 implementations being developped
  - LabView based [*R. Dellanegra* – IPNL]
    - LAL Code for HaRDROC test card
    - To be extended for 4 ASICs
    - Work just started ➔ fast working setup
  - C based [*C. Jauffret* – LLR]
    - Firmware + software being written and tested on HaRDROC testcards (1 ASIC)
    - ➔ 8x32 cards (4 ASICs) next week
    - Aims higher perf & developpement ➔ DIF card & Analog readout

SSD (Analogue)

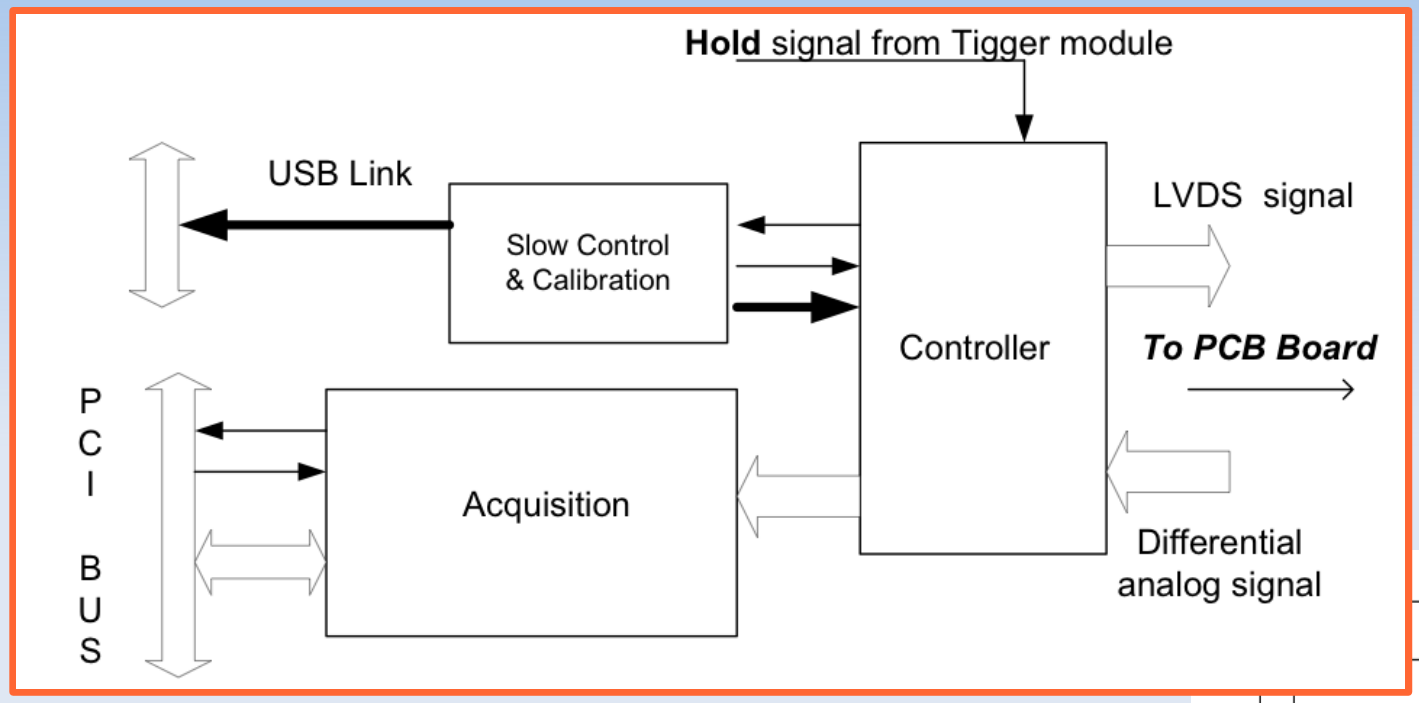
Initial plan:

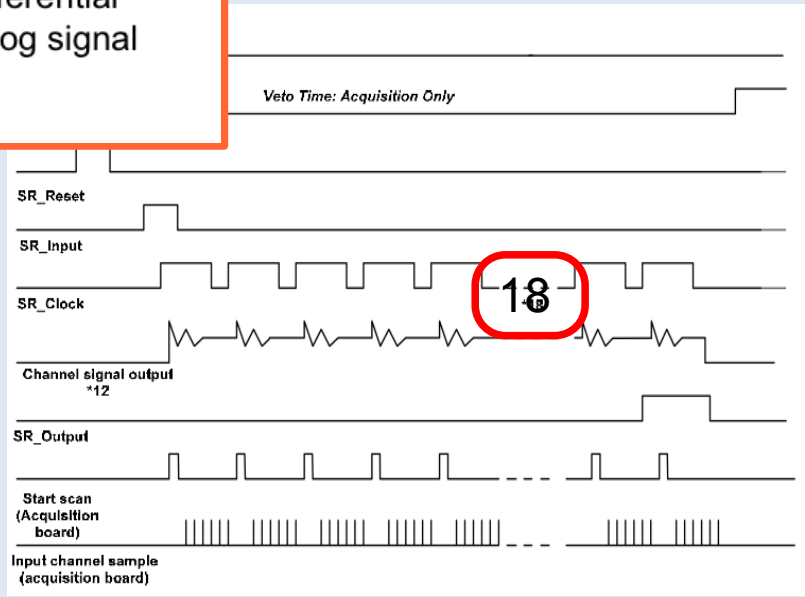
- Readout of analog part by a CRC card
- To do [...?]
  - Write DIF firmware (cycling readout)
  - Modified software (data integration) & CRC firmware
- Pbm:
  - availability of CRC (in DESY ?)
  - manpower ?

Backup (local) plan

- Use the LLR ECAL cosmic test DAQ for analog readout
  - was used for ECAL cosmic test
  - full Compatibility with CRC
    ➜ minimal adaptation needed
  - Nat. Instr. commercial *acq. card* & CPLD based *controller card*
  - All HW elements avail. in double
- To do [*C. Jauffret*]
  - modify PCB firmware from C based DAQ (cycling readout / delays)
  - Small modif software / firmware (written for ECAL)

Cosmic test bench DAQ





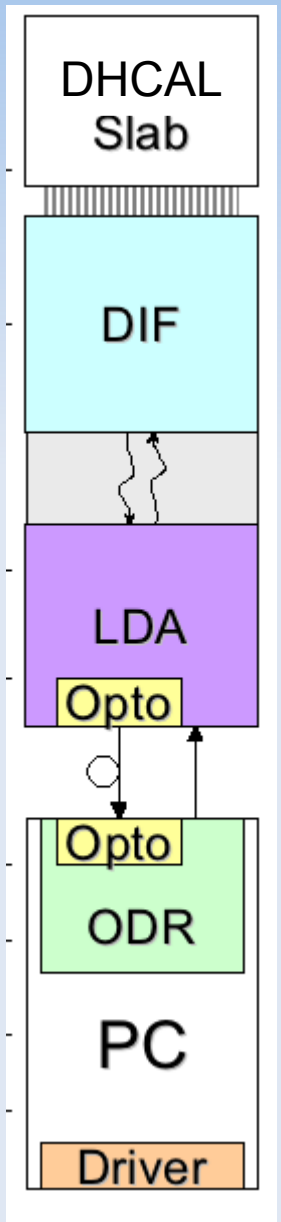
- Designed to be compat. with the CRC
- 24 diff. Channels
- Multiplexed readout at 1.25Mb/s (total)
- 12bit dynamics
- DAC output for calibration

- Minimal changes in readout sequences

DAQ2 (needed for the m³)

- DIF: Det. Specific. FE
  - To be defined next...

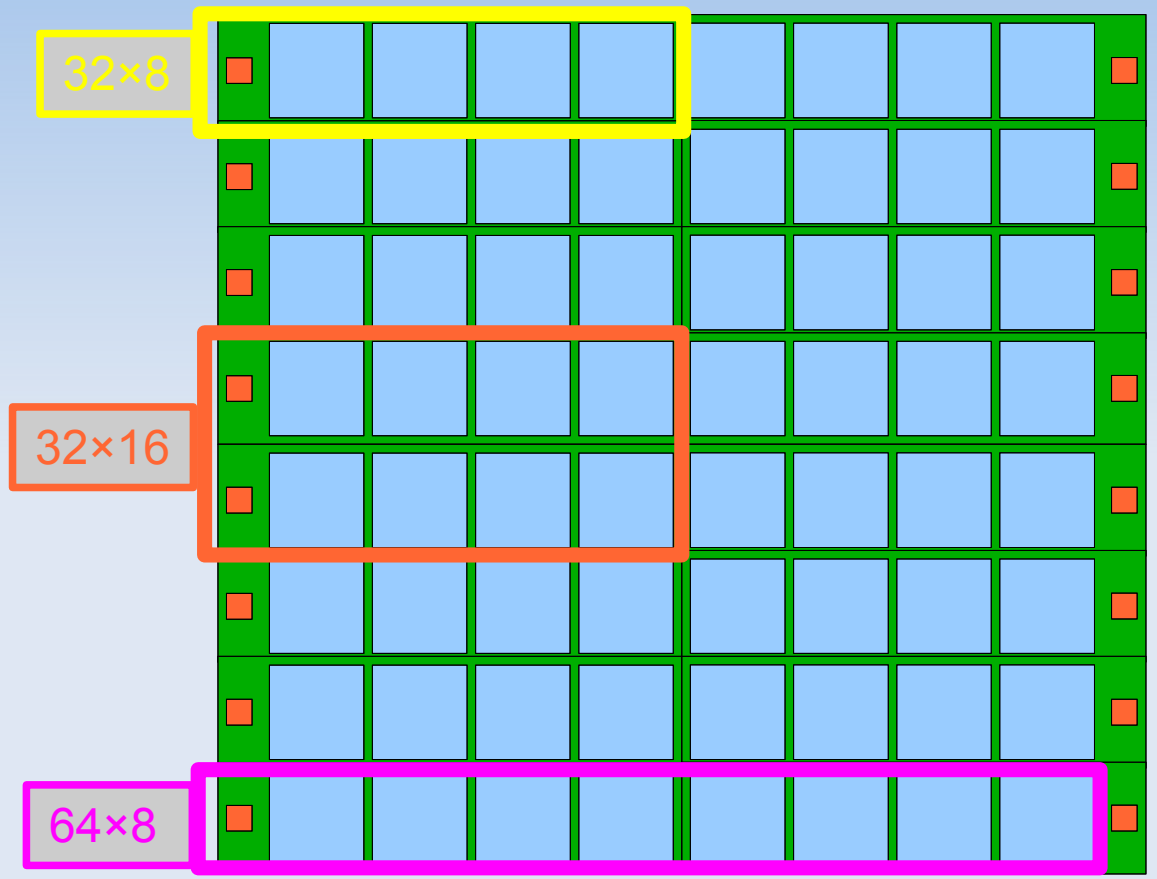
  Constraints (M. Wing):
- LDA: concentrator card
  - 1 Gbits/s output
  - Up to 50 DIF input (#pins of the FPGA)
    ➜ 20 Mbits/s per DIF
- ODR: readout card
  - Can reads 2 LDA @ 1 GB/s
  - Links are expensive



DIF card

- Reads out a complete Slab
- Load and control HaRDROC's
- Zero suppression (& compression ?)
- Reads serially HaRDROC's (serial link @ 1 Mhz)
  - ➔ 160bits per ASIC × number of BC (<128) ≤ 20480 bits/ASIC
  - ➔ Readout time ≤ 20 ms/ASIC
    - Event^{ly} a problematic for testbeams, not for final det.
- Optimal number of ASIC / DIF ?
  - ➔ Ideally (for TB): 20 ASIC *lines* per DIF read in parallel
  - ➔ But:
    - Size of PCB (1 ASIC ➔ 8×8 cm²) ➔ price, ...
    - Serial lines on PCB += 8 cm / ASIC, non terminated (to lower power cons.)
- Interface with LDA
  - Data, Clock & Control

DIF/PCB configurations



Separated DIF

- 8 lines of 4 ASICs readout in //
- 2 DIF / layer
  → 2×8 Mb/s
- 2 LDA / Module

On PCB DIF

- 1 line of 4 ASICs
- 16 DIF / layer
  → 16×1 Mb/s
- Intermediate concentrator

- 4 lines of 8 ASICs readout in //
- 2 DIF / layer
  → 8×2 Mb/s
- 2 LDA / Module

Option
2 lines of 4 interleaved ASICs
→ reduces
- readout time
- occupancy / line

+++
- 8 (16) ASICs readout in //
- 1 DIF / layer
  → 16 Mb/s
- 1 LDA / Module

- Bigger FPGA
- Length of lines

LDA & ODR cards

- PPARC programme (October 2005-March 2009)
  - Tests of ASICs in 2007 and 2008
  - Test results on model slab (2007)
  - Prototype ODR (March 2007) ✔
  - Initial ODR (December 2007)
  - Full-scale DAQ system (2008/9)
  - Much more which you don't (necessarily) know about - networks, c&c&c
- EUDET programme (January 2006-December 2009)
  - PCI prototype available (June 2007)
  - DAQ system prototype available (September 2008)
  - DAQ system available (June 2009)

OK for 1 layer

Challenging for 1 m³ ???

➔ Need 1 LDA (prototype ?) for end 2007…

➔ Q? integration with data flux of other det.

Conclusion

- Schedule is tight
- 2 solutions for digi readout of a ”8×32” SLAB
- 2 possible solutions for a analog Single Slab DAQ for july test
  - Using 1 DESY CRC if avail.
  - LLR Cosmics Test bench for backup/local solution
- Full layer beg. '08 needs functionnal
  - DIF proto(s) (being defined)
  - ODR + LDAs protos
- Good training field for the DAQ2 preparation

VFE DAQ code (C. Jauffret)