

# European DHCAL development

CIEMAT, IPNL, LAL, LAPP, LLR, PROTVINO, SACLAY

- Status : detectors, electronics
- Future projects

Imad Laktineh  
IPNL

# Detector Study

**GRPC** : Protvino, IPNL,...

8X8 pads, 8X32 pads, 1m<sup>2</sup>

*(advanced state)*

**μMEGAS** : LAPP, IPNL,....

8X8 pads, 6X16 pads, 50X50 pads...

*(need more efforts ⇒ Saclay)*



Efficiency, cross-talk, homogeneity studies,  
new gas mixtures... : ongoing

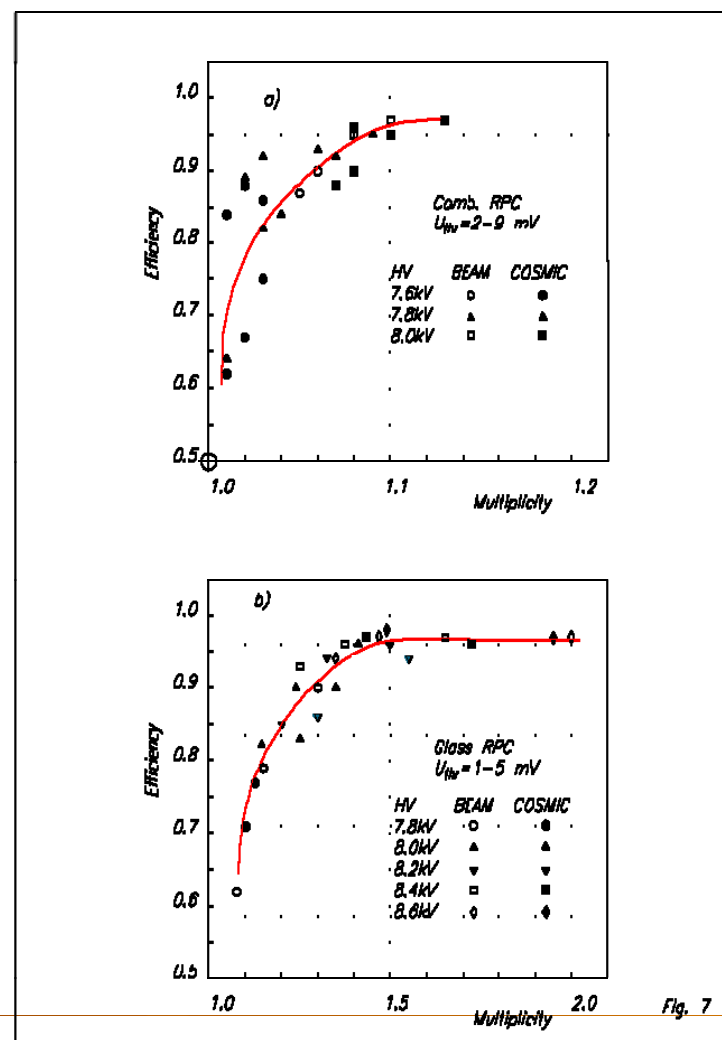
# Protvino activities

## Combined RPC

Protvino results confirm first observation of ANL group about combined RPC – low hit multiplicity,  $\langle m \rangle \sim 1.1$  at 95% With 400 V plateau.

It seems that the combined RPC is promising option for the DHCAL.

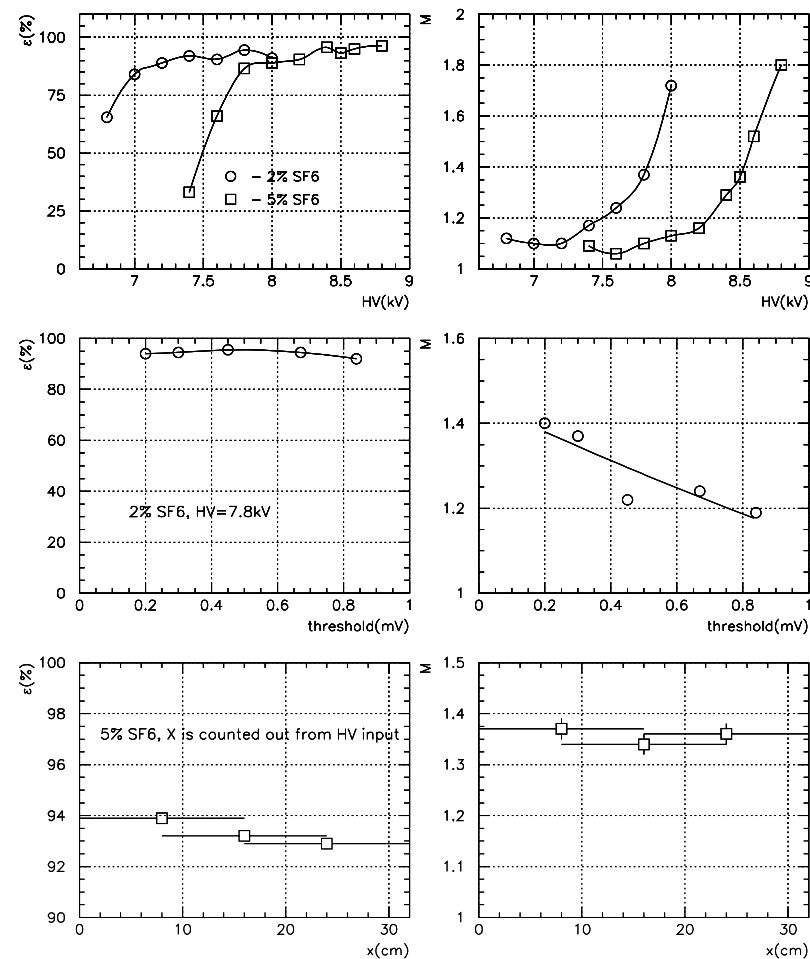
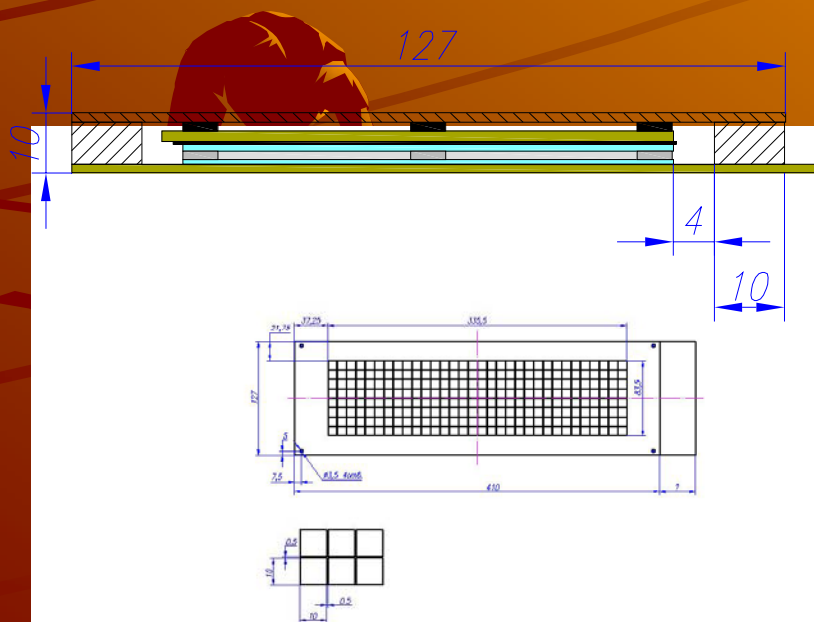
Long term stability study of combined RPC is underway.



# Protvino activities

## 8X32 pads RPC

4 RPCs for 8x32 pad read out were produced. One chamber was sent to Lyon. Chambers are waiting for anode PCBs with hardroc chips



# Protvino activities

**Long term stability of combined RPC**

**8x32 pads RPC**

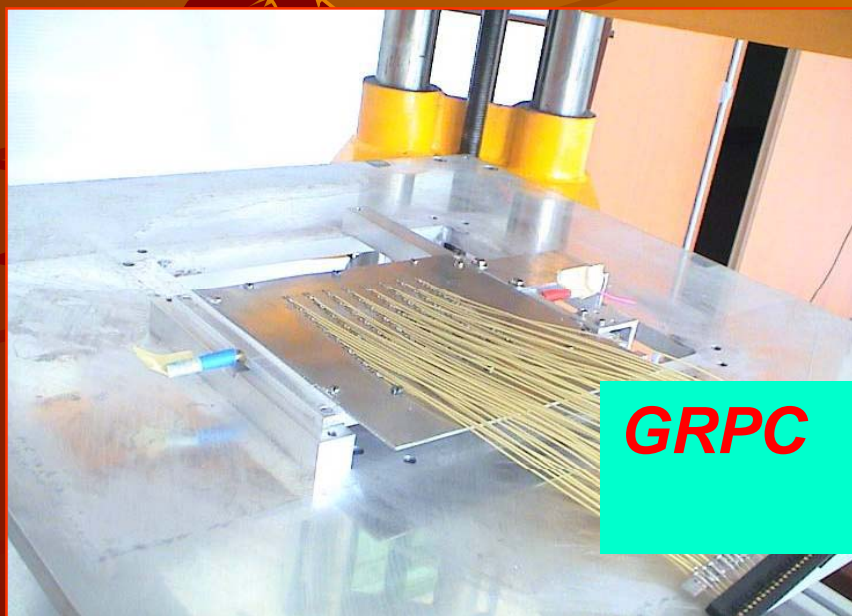
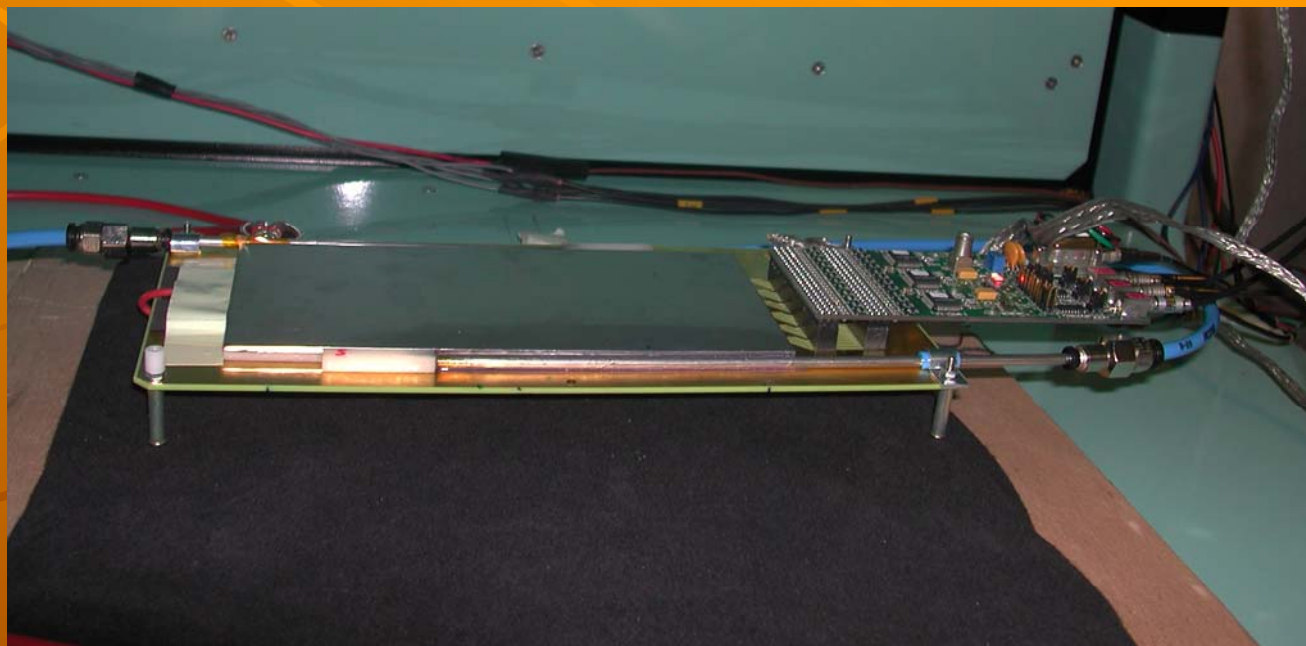
**Preparation for the 1m<sup>2</sup> RPC production**

- Facility preparation
- Cosmic stand construction with 1m<sup>2</sup> sc. counters and DC
- Decision of technological questions ( HV coverage, production of spacers)

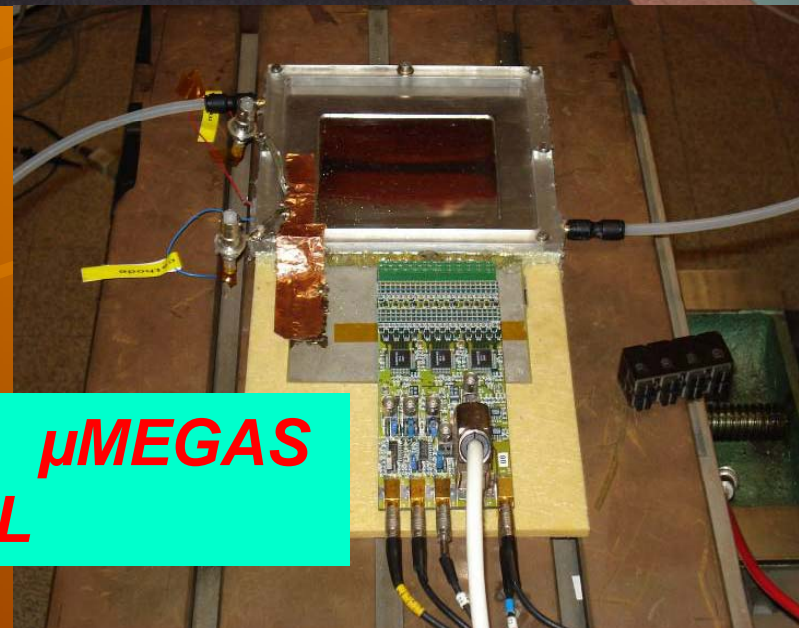
**4. Ready to participate in 1m<sup>2</sup> RPC assembly, DHCAL installation, beam tests**

# France activities

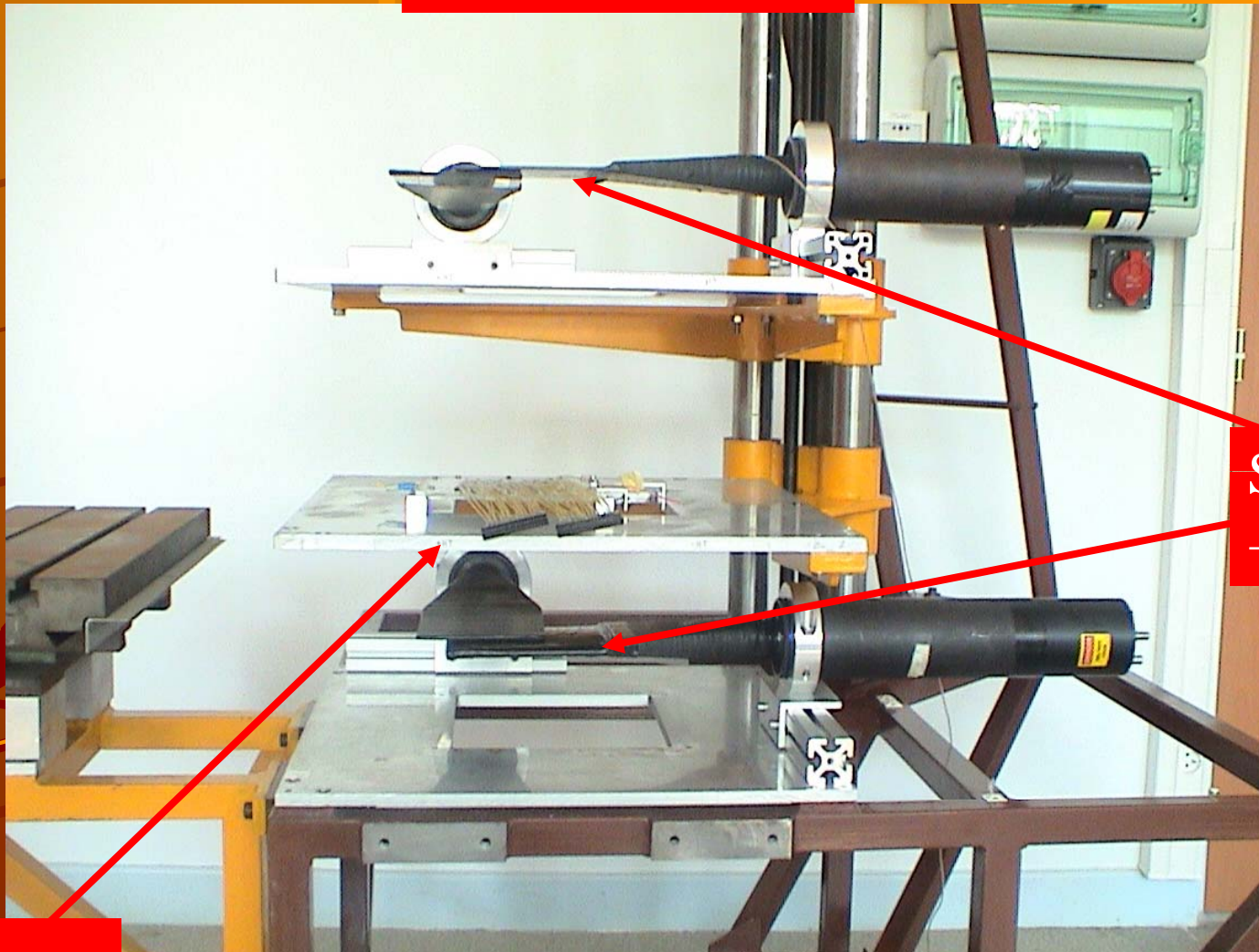
**$\mu$ MEGAS  
LAPP**



**GRPC +  $\mu$ MEGAS  
IPNL**



# Test Bench IPNL

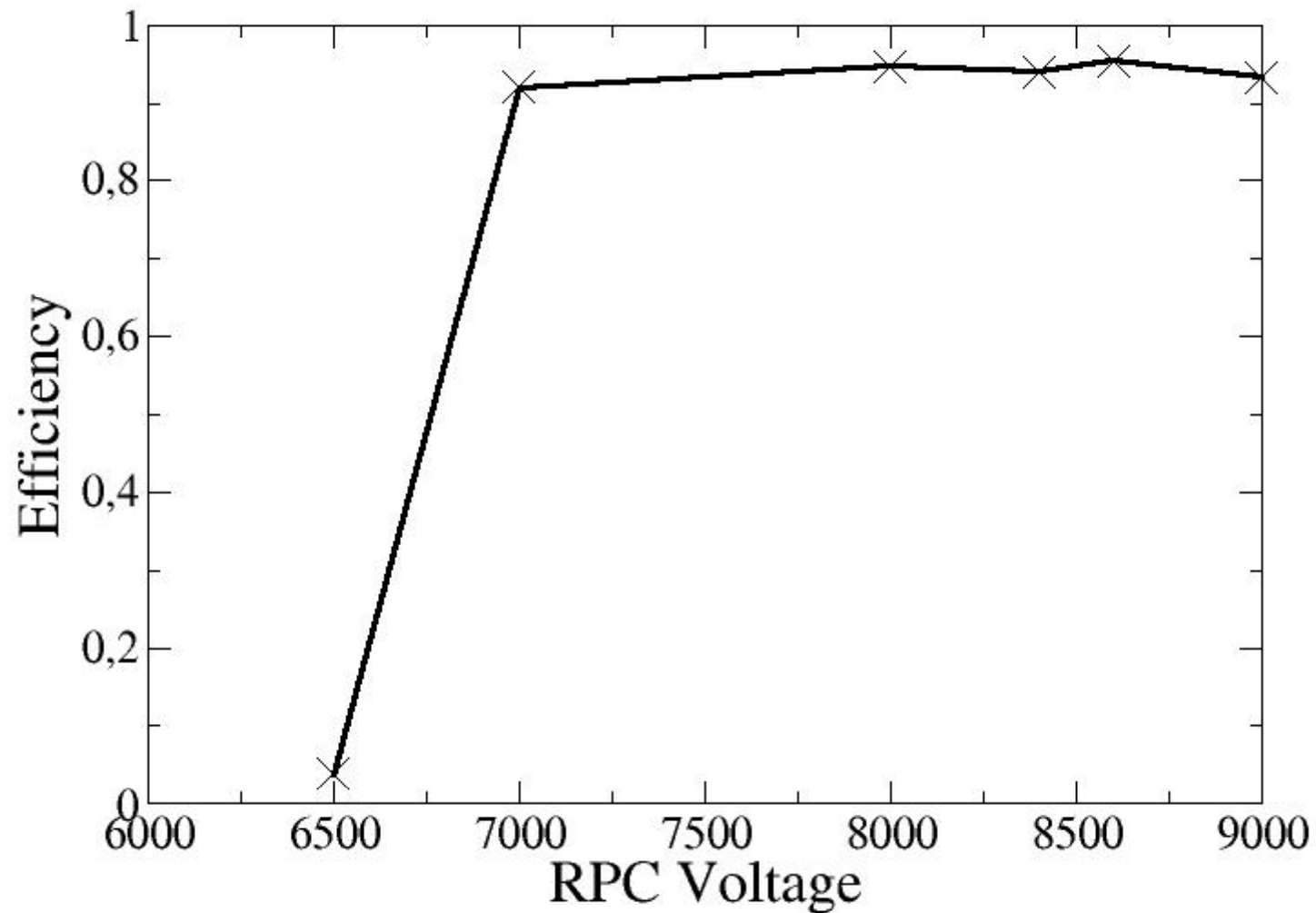


Scintillators  
+PM's

GRPC

Acquisition : ADC (V 792)

# RPC Efficiency



Preliminary results obtained for one of the two 8X8 pads protvino  
RPC's tested at IPNL.

# Detector Study

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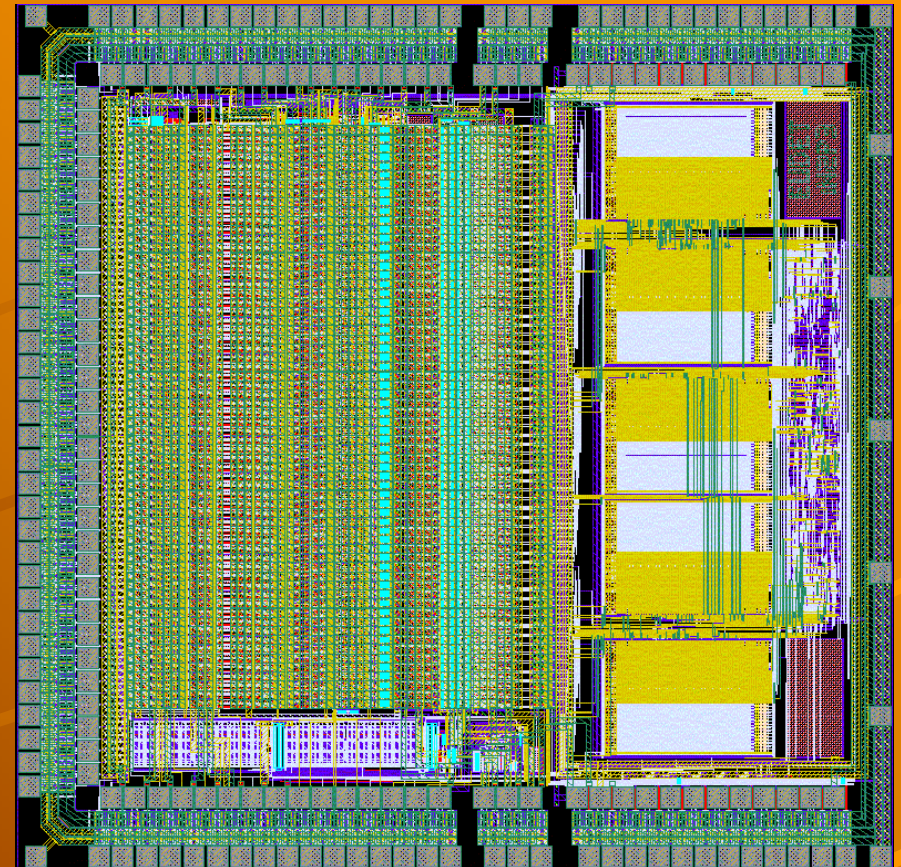
Efficiency, cross-talk, homogeneity studies,  
new gas mixtures... : ongoing

# Electronics

LAL, IPNL, LLR

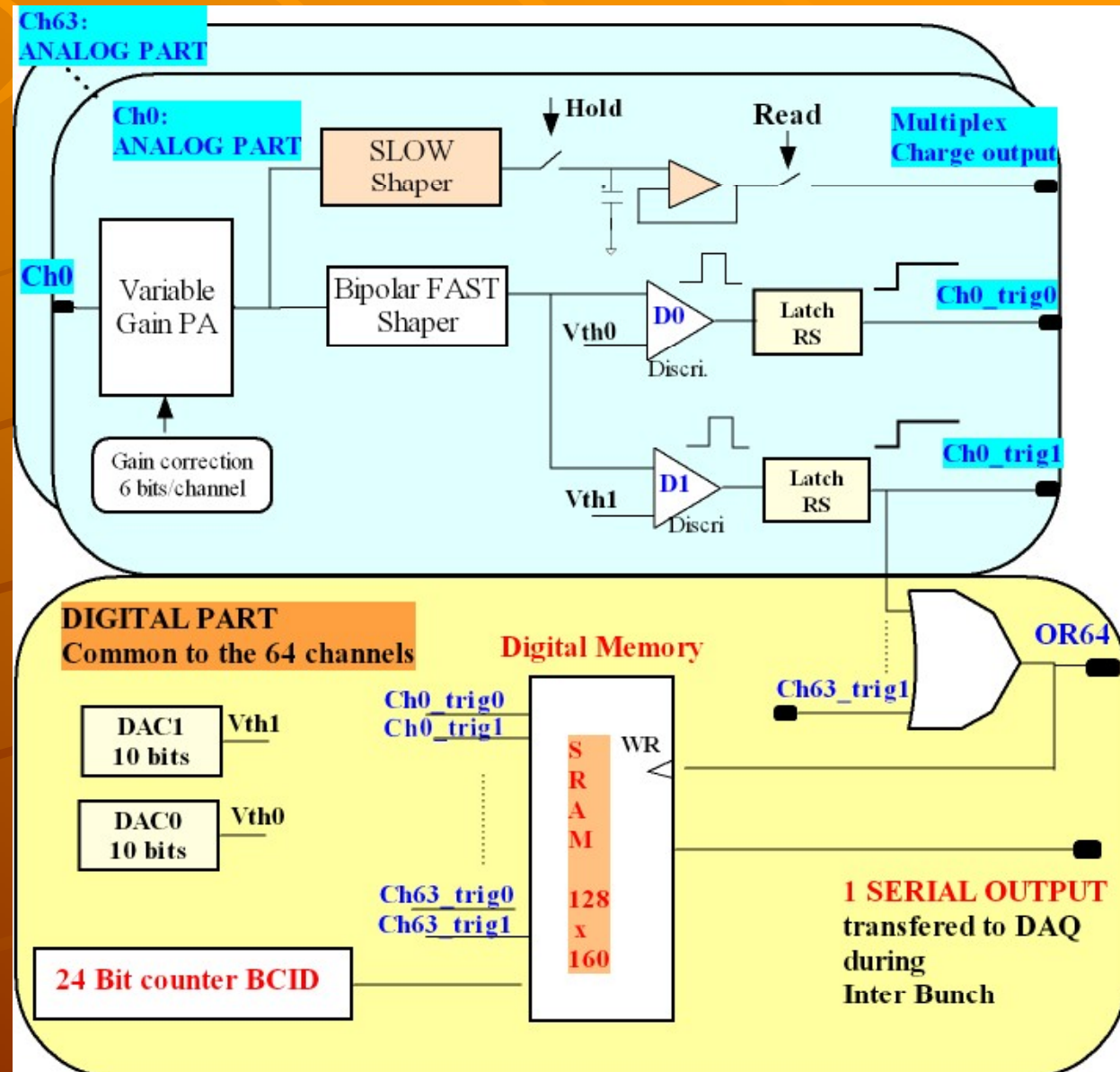
## HARDROC

- 64 channels chip
- Semi-digital output, readout conceived to be compatible With the 2d generation DAQ
- Low consumption, full power pulsing

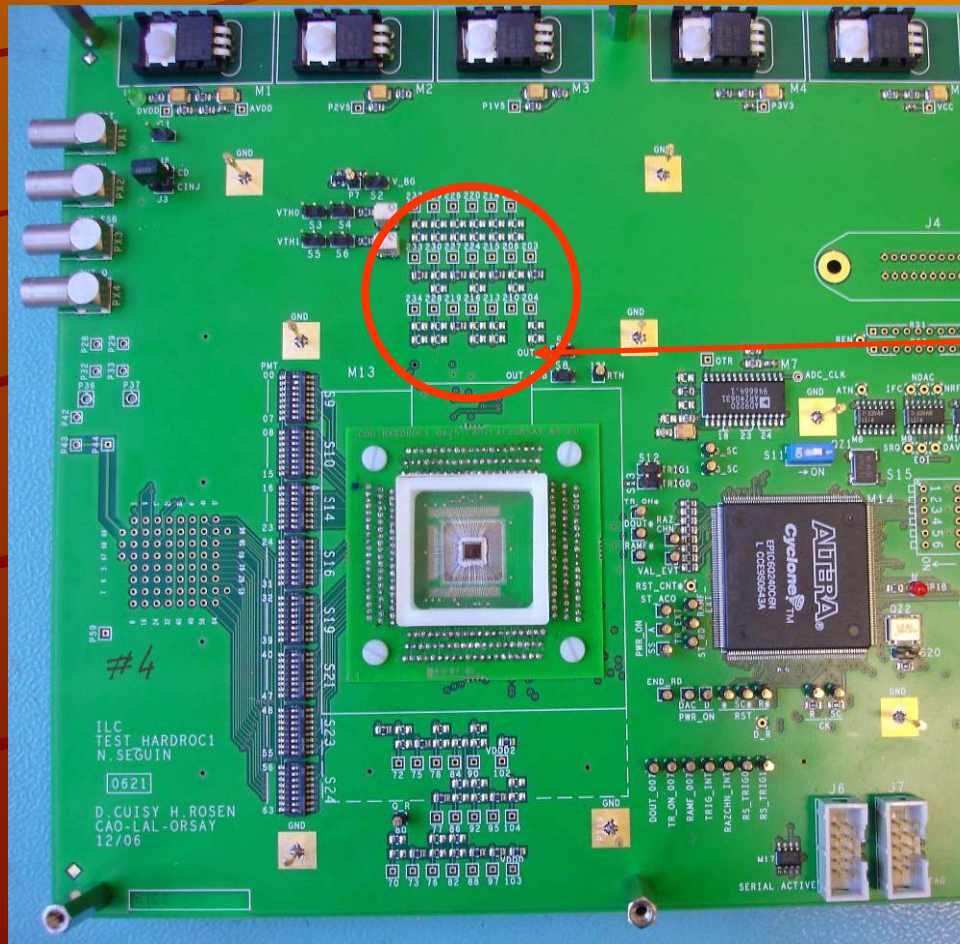


# HARDROC1 Architecture

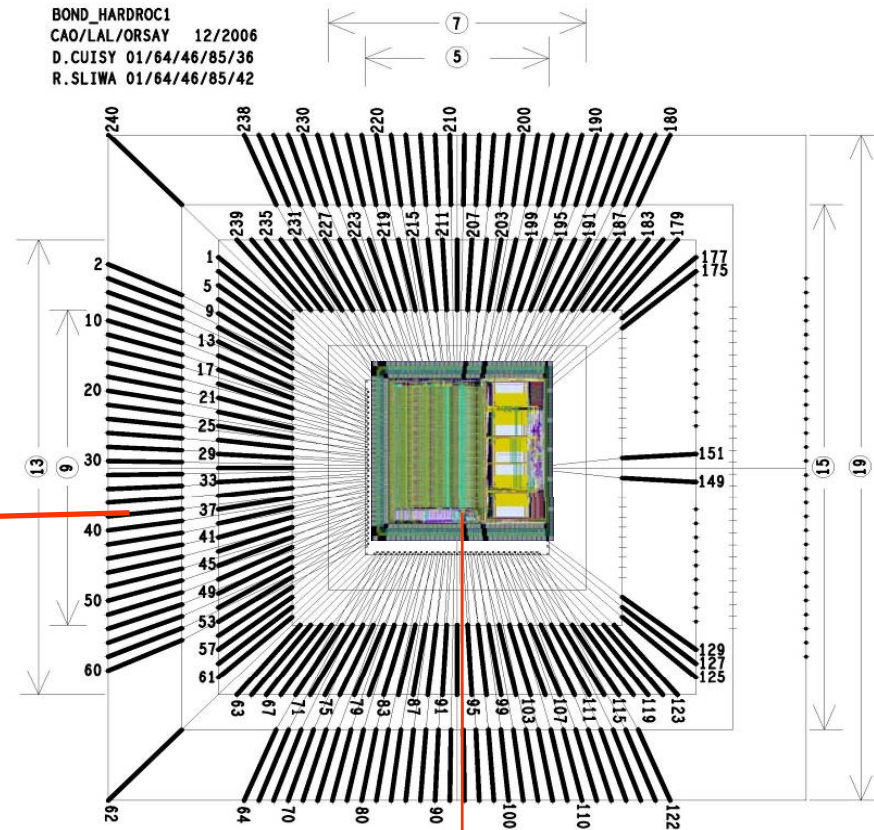
- Full power pulsing
- Digital memory:  
Data saved during bunch train.
- Only one serial output @ 5MHz
- Store all channels and BCID for every hit. Depth = 128 bits
- Data format :  
 $128(\text{depth}) * [2\text{bit} * 64\text{ch} + 24\text{bit}(\text{BCID}) + 8\text{bit}(\text{Header})] = 20\text{kbits}$
- Based on MAROC ASIC, but several design changes



# HARDROC1: TESTBOARD with Chip On Board

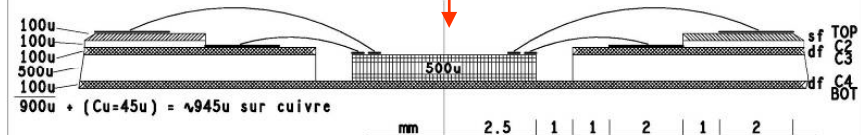


BOND\_HARDROC1  
CAO/LAL/ORSAY 12/2006  
D.CUISY 01/64/46/85/36  
R.SLIWA 01/64/46/85/42

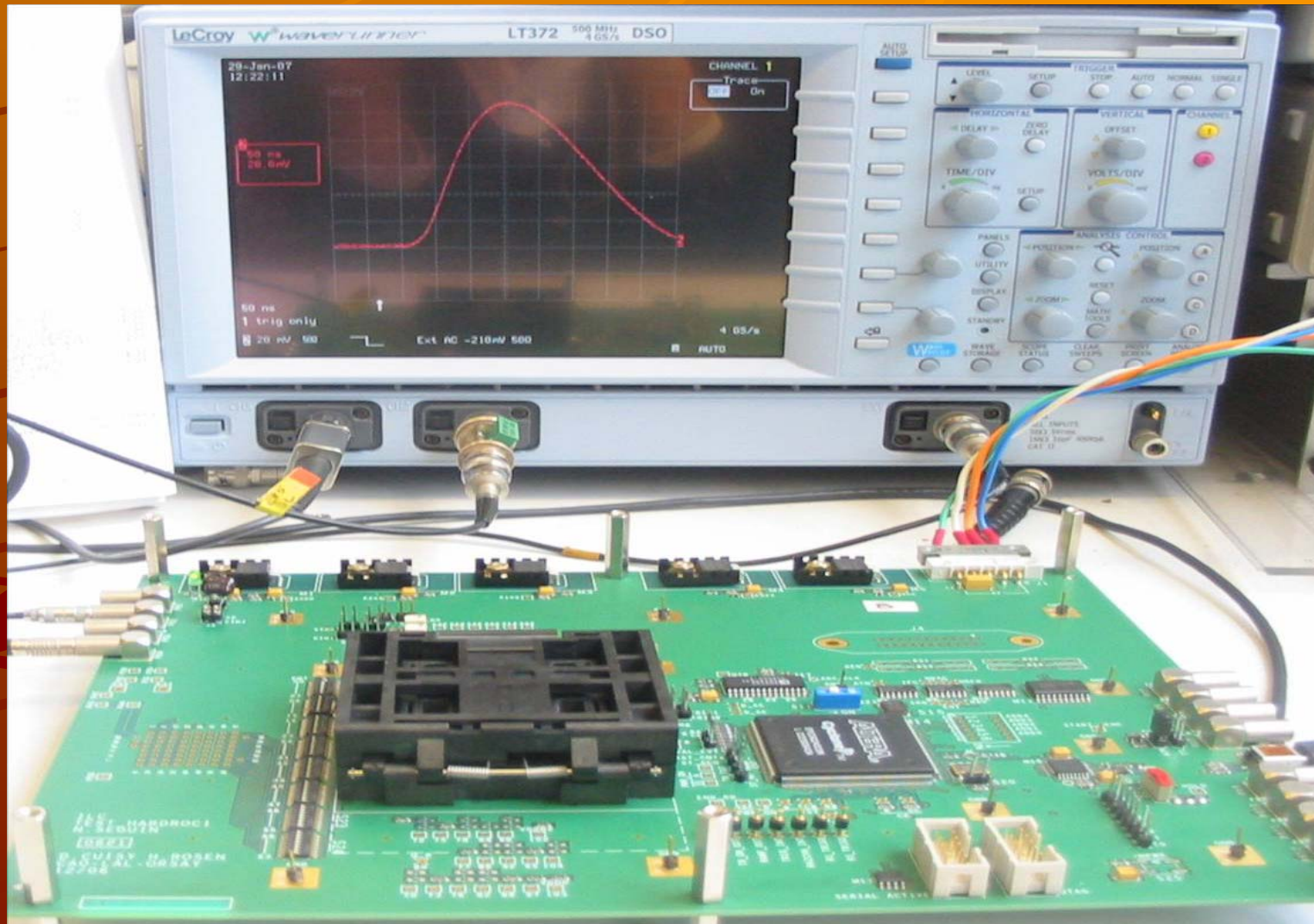


longueur mini pads = 2mm  
largeur pads = 122u  
iso mini pads = 100u  
epaisseur cuivre toutes couches = 9u  
finition NiAu chimique sur pads

⑤ = puce  
⑦ = cavite  
⑨ ⑬ = pads couche 2  
⑮ ⑰ = pads couche TOP



# HARDROC1: TESTBOARD with a packaged chip LAL,IPNL...

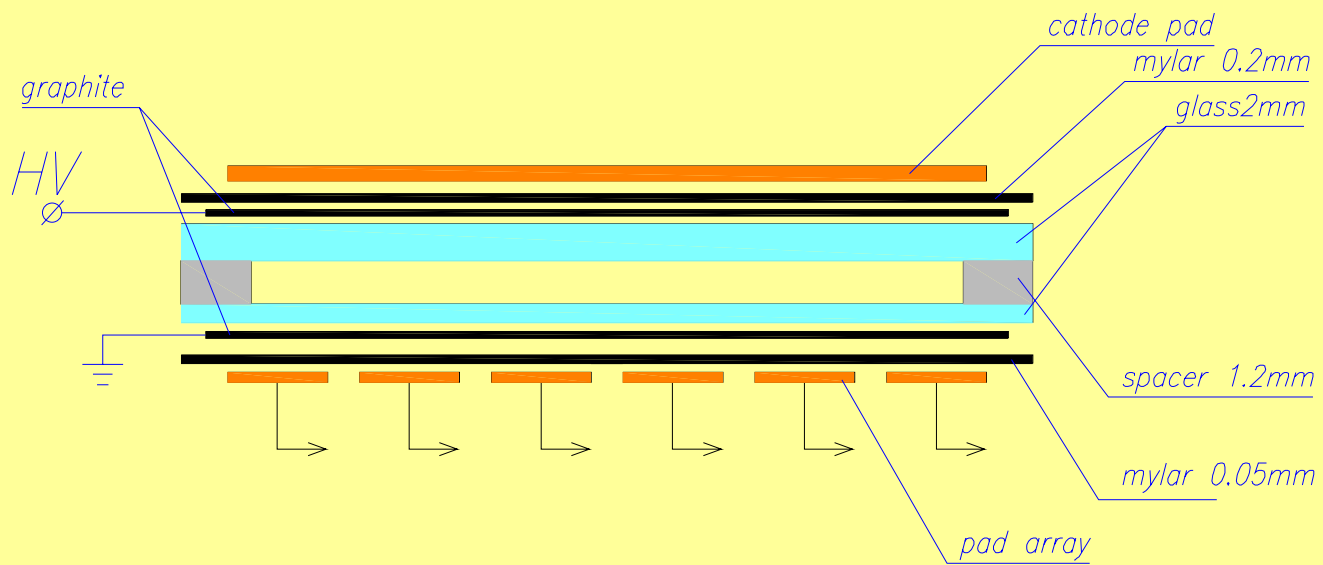


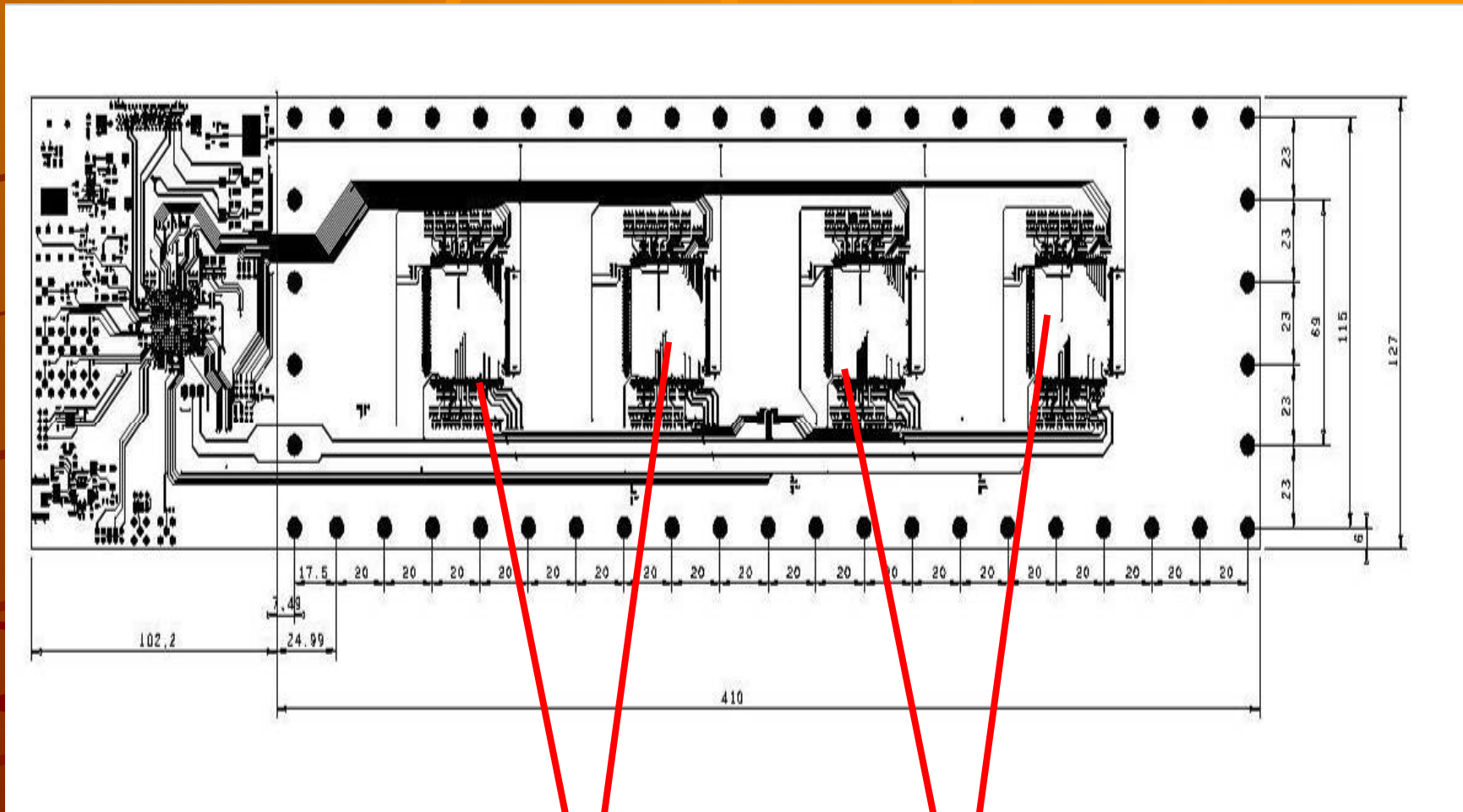
# 2007 Project

**Realization of 8X32 pads detectors fully instrumented:**

- **8X32 pads detector RPC:** already built
- **4 HARDROC:** already produced and tested
- **8-layers PCB** designed and optimized to reduce cross-talk with two schemes on the same pcb. Now realized
- **Readout** USB + FPGA realized

# 8X32 pads RPC

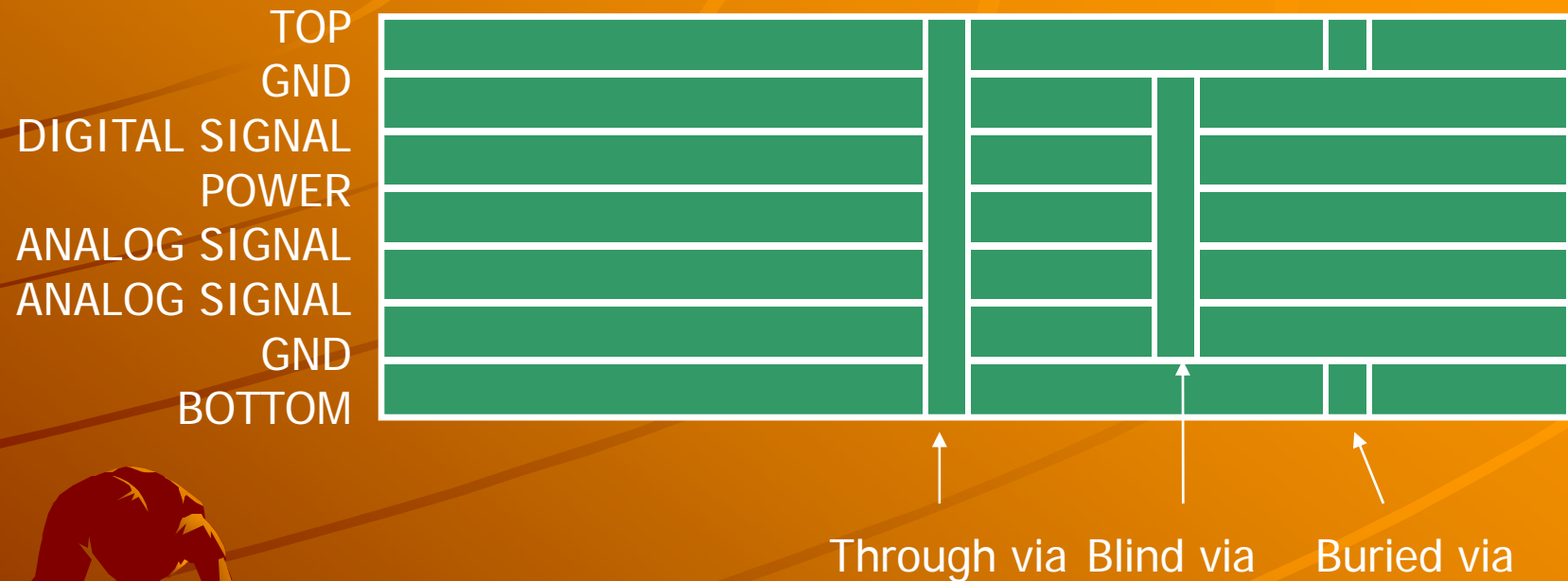




6-Layers scheme

8-Layers scheme

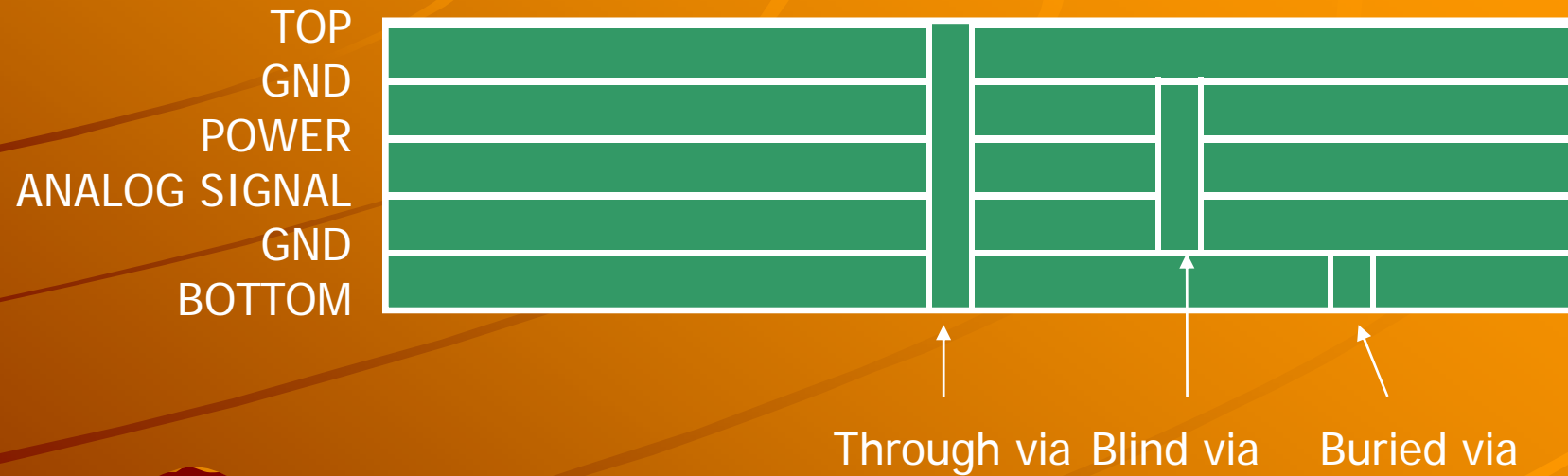
## Layout in 8 layers (solution1)



Layer definition ( except FPGA area )

- TOP LAYER : Component layer
- GND : Ground layer and access to internal layers
- DIGITAL SIGNAL : Layer to interconnect between hardroc and FPGA
- POWER : Power to hardroc
- ANALOG SIGNAL : Layer to interconnect pad signals
- BOTTOM : RPC pads layer

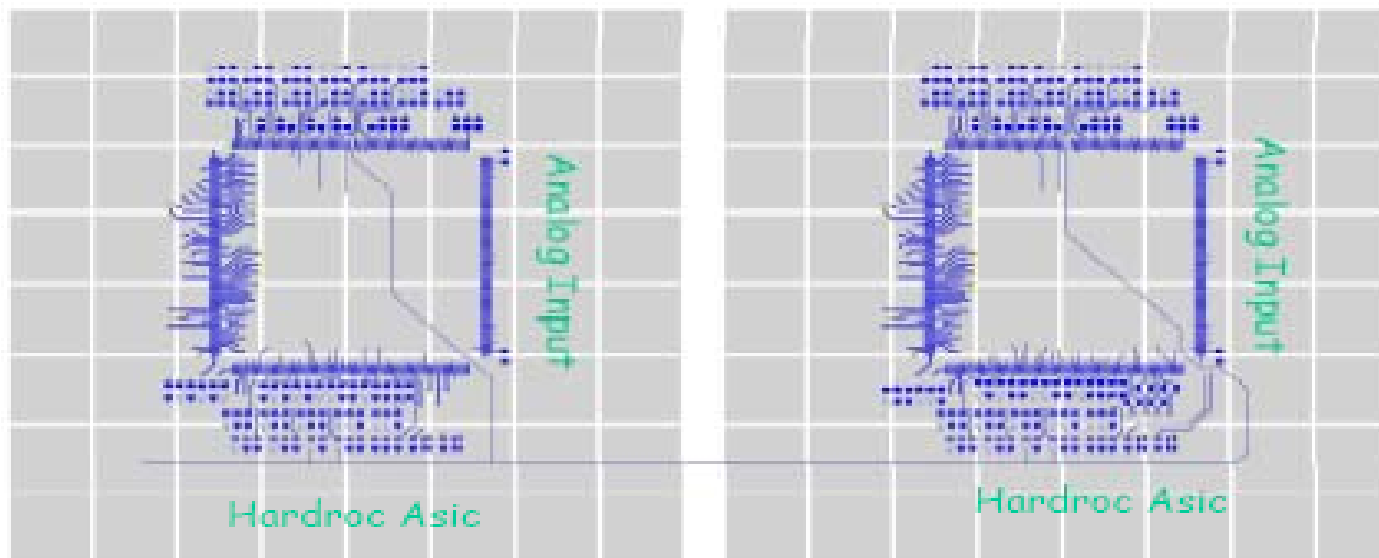
## Layout in 6 layers (solution2)

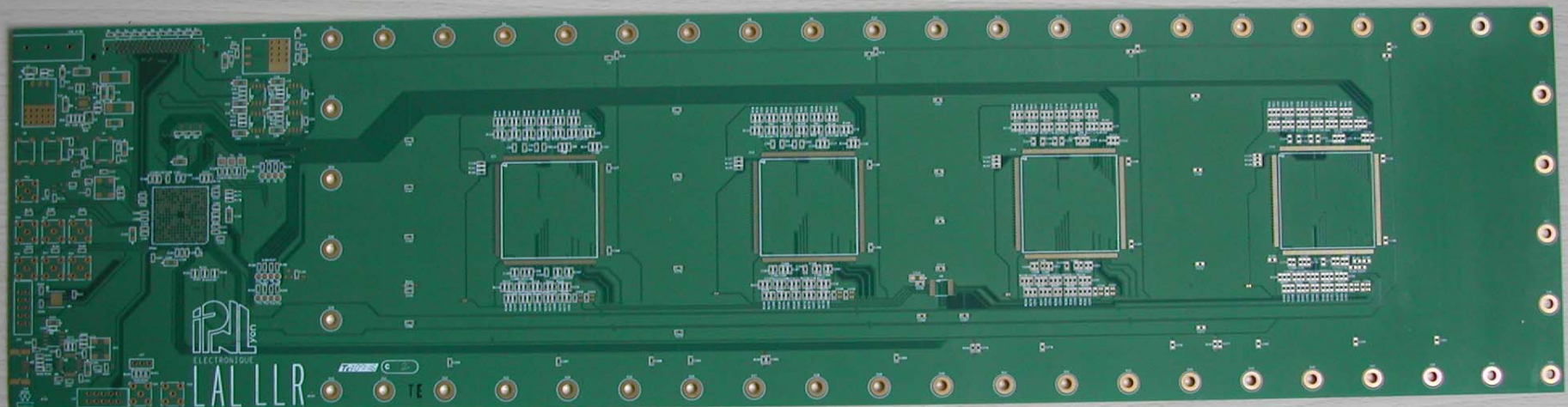


Layer definition ( except FPGA area )

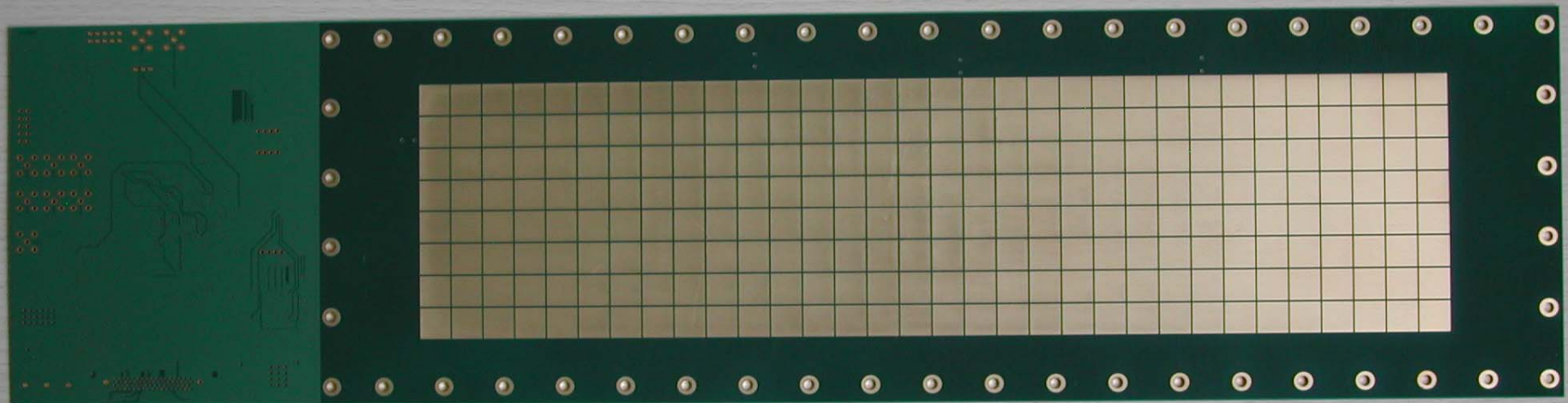
TOP LAYER	: Component layer+interconnect between hardroc and FPGA
GND	: Ground layer and access to internal layers
POWER	: Power to hardroc
ANALOG SIGNAL	: Layer to interconnect pad signals
BOTTOM	: RPC pads layer

## Top layer and Pads (8 layers)





Thickness =  $800\ \mu$



1 cm<sup>2</sup> pads  
500  $\mu$  separation

# Next steps

- ✦ Test the pcb performance : cross-talk **Ongoing**
- ✦ Assembly the different electronics components **MAY**
- ✦ Check the whole system without the detector **MAY**
- ✦ Develop/adapt a DAQ for both digital and analog output (see Vincent talk) **Ongoing**
- ✦ Put the electronics on the RPC detector **June**
- ✦ Cosmics data **June**
- ✦ Test beam at DESY > **July**

**N.B :** The pcb was conceived to be compatible with  $\mu$ MEGAS detector as well.

# Future project

## First step (2007-2008):

- 70X70 cm<sup>2</sup> GRPC plane fully equipped
- 70X70 cm<sup>2</sup>  $\mu$ MEGAS plane fully equipped

### Using

- 1) Calice acquisition for the analog output
- 2) Standalone acquisition for digital output

### Using

The desy mechanical structure

*Extensive study and comparison between the two detectors*

## Second step(2008-2009) :

A prototype of 40 of 70X70 cm<sup>2</sup> planes with steel planes and mechanical structure (ciemat)

# Future project

- **Budget**

300 K euros were requested for the 2007-2009 period (ANR).

Equivalent demand for the same period will be submitted to IN2P3.

This to fund the electronics and detectors of the prototype

The mechanical structure can be funded by CIEMAT ?

- **Acquisition**

By 2009 the second generation DAQ should be ready otherwise a solution should be found (Vincent talk)



# Conclusions

- ✦ Many efforts on DHCAL are going on in Europe
- ✦ European DHCAL project has the ambition to be as close as possible to ILC detector.
- ✦ European project is complementary to the American one
- ✦ The two projects should become one in the future.

# POSSIBLE LAYOUT DESIGN for 1 m<sup>2</sup> detector

1 m

