SOI, 3D and Thinned Detectors

Ronald Lipton, Fermilab

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- ILC Vertex Constraints and Goals
- Introduction to Silicon-on-Insulator devices
- 3D Driving Technologies
- Thinned, edgeless sensors
- Laser annealing
- SOI X-ray sensor circuit in the OKI process
- SOI ILC Development in the American Semiconductor FLEXFET process
- 3D Circuits
- 3D Circuit for ILC
- Power considerations

Contributers – Fermilab, Bergamo, Cornell, Purdue

ILC Vertex Detector

Designed for *precision* physics. Minimize luminosity cost by optimizing the detector

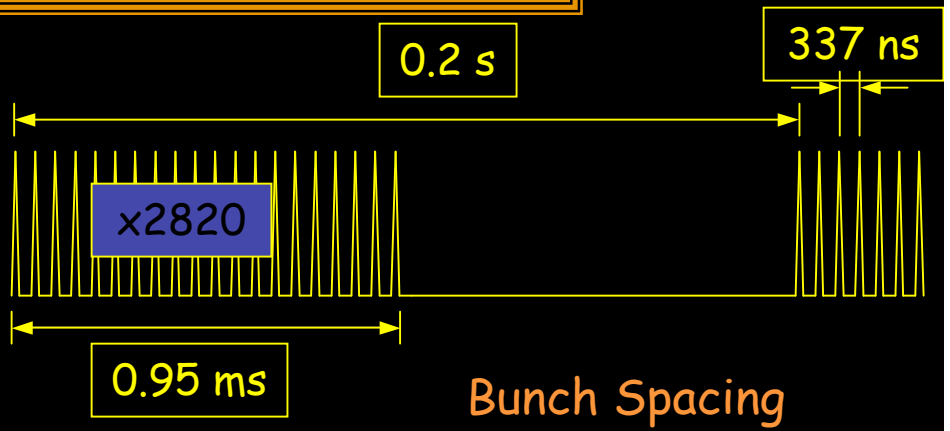
- Higgs branching ratios
  - Requires excellent separation of b/c/light quark vertices
- Higgs self coupling:

$$e^+e^- \rightarrow ZHH \rightarrow qqbbbb$$
$$backgrounds: tt \rightarrow bb\,\mathrm{csc}\,s, ZZZ, ZZH$$

  - B quark ID within jets
- Higgs recoil mass

Vertex Detector Design Goals

- Low mass ~0.1% RL/layer
  - Directly effects physics reach
  - Coupled to power, signal/noise
  - Limited by mechanical supports, cables
- Time resolution
  - Requirements dependent on beam background
    - Studies have found ~50 μs sufficient
    - Single bunch resolution optimal
- Spatial resolution
  - <5 microns appears achievable
- Power
  - <50(?)W average to allow air cooling
  - Pulsed/serial power



These challenges have inspired a host of R&D initiatives to adapt existing technologies and have driven our work on 3D and SOI

SOI and Thinned Detectors

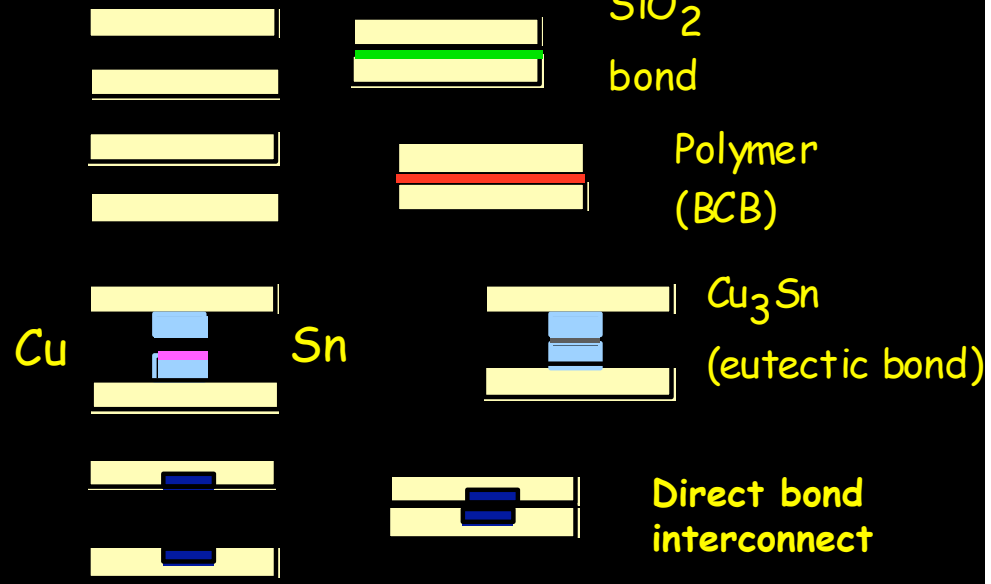
New semiconductor technologies are becoming available from commercial IC and focal plane sensor development work which are applicable to HEP detectors, especially ILC vertex technologies.

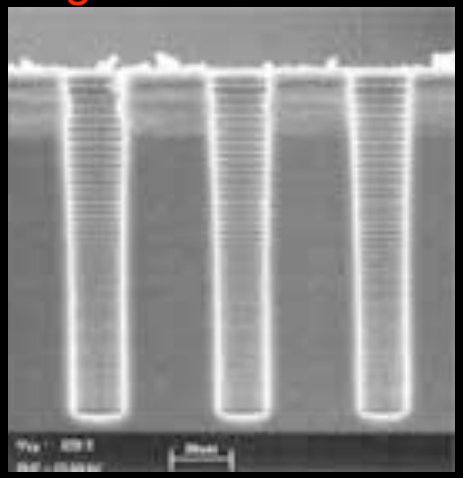
- Thinned devices - developed for a variety of commercial applications
- Deep trench etching and doping – “Edgeless sensors”, vertical integration
- SOI - handle wafer engineering
- Access to process steps in CMOS wafer fabrication

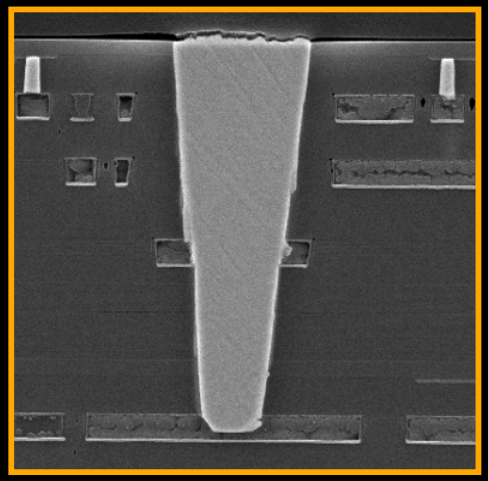
Three dimensional integration of electronics and sensors

Key Technologies for SOI/3D

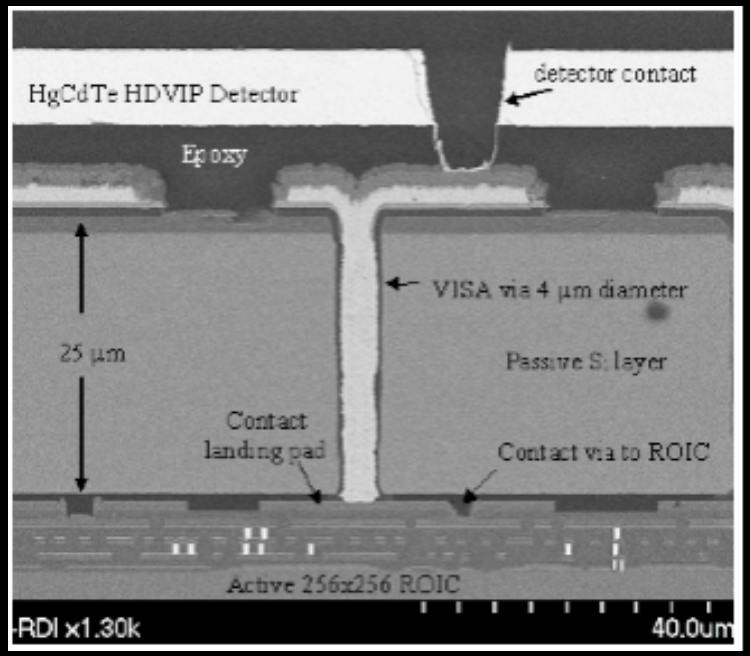
1) Bonding between layers
   - Oxide to oxide fusion
   - Copper/tin bonding
   - Polymer/adhesive bonding
2) Wafer thinning
   - Grinding, lapping, etching, CMP
3) Through wafer via formation and metalization
   - With isolation
   - Without isolation
4) High precision alignment



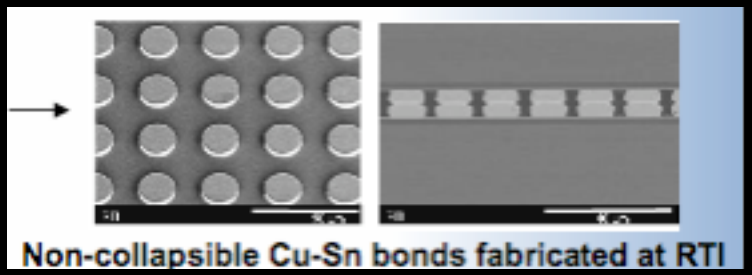


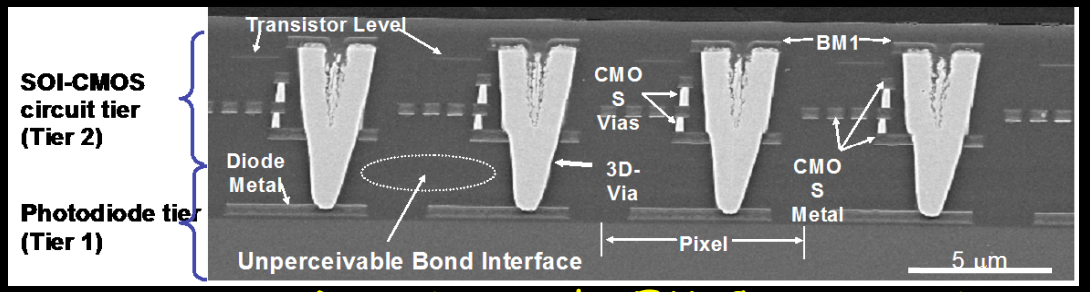


3D Sensor Integration Examples



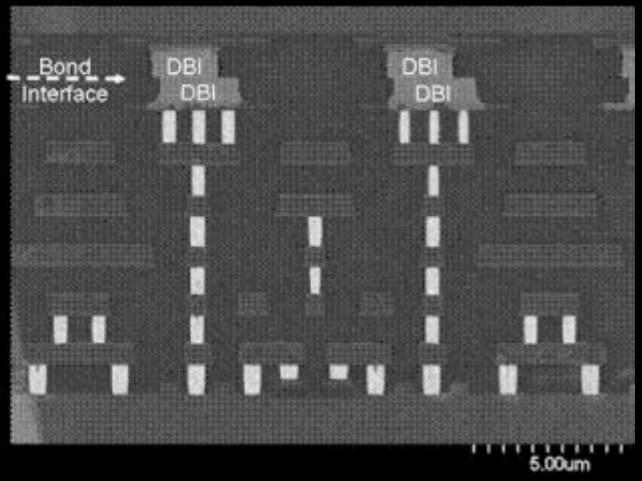
Epoxy bonded 3D connected imager (RTI/DRS)





Drawing and SEM Cross section

8 micron pitch, 50 micron thick oxide bonded imager (Lincoln Labs)



8 micron pitch DBI (oxide-metal) bonded PIN imager (Ziptronix)

Group Initiatives

- Thinned, edgeless sensors
- Chip being designed in American Semiconductor 0.18 um SOI process (SBIR)
  - With pixel sensor layer and one or more electronics layers for ILC vertex detector
- 3D chip being fabricated in MIT LL 0.18 um SOI multi-project run.
  - 3 tier demonstrator chip for ILC vertex detector
- Chip being fabricated in OKI 0.15 micron SOI process
  - Includes sensor and one layer of electronics for electron microscope.
- Bonding Technologies (being explored)
  - Cu-sn bonding of FPIX chips/sensors
  - DBI bonding of 3D chips to MIT sensors
- Laser annealing (Cornell)

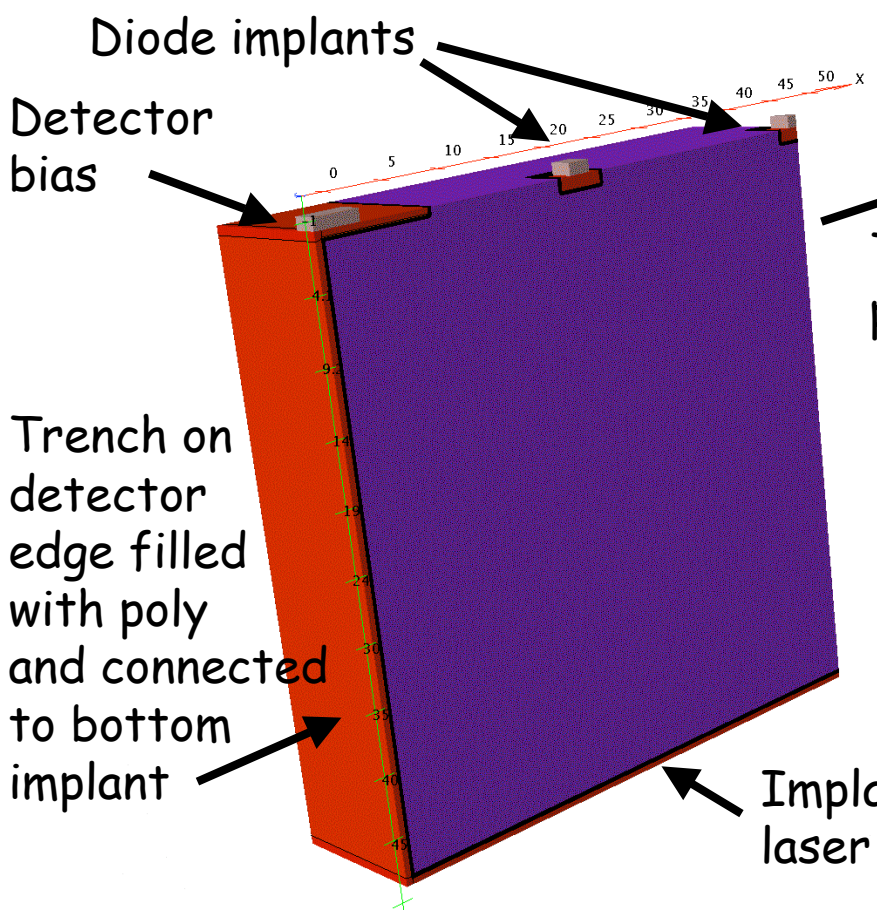
Sensor Studies

We are producing a set of thinned, “edgeless” sensors at MIT-LL as a initial test of these concepts

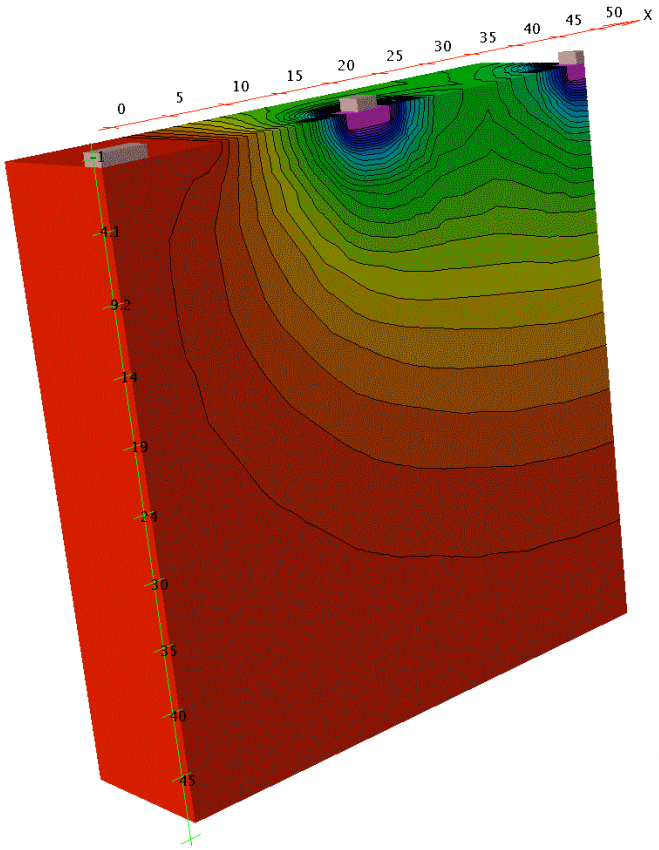
Derived from back illuminated focal plane process

- Produce a set of detectors thinned to 50-100 microns for beam and probe tests.
  - Validate process
  - Understand performance
- Explore and validate the technologies which provide detectors sensitive to the edge
  - Measure the actual dead region in a test beam
- Parts available for prototype vertex structures
- Masks designed at FNAL
  - Test structures
  - Strip detectors (12.5 cm and ~2 cm)
  - FPiX2 pixel detectors (beam tests)
  - Detectors to mate to 3D chip
- Wafers due in September

Edgeless Detector Concept



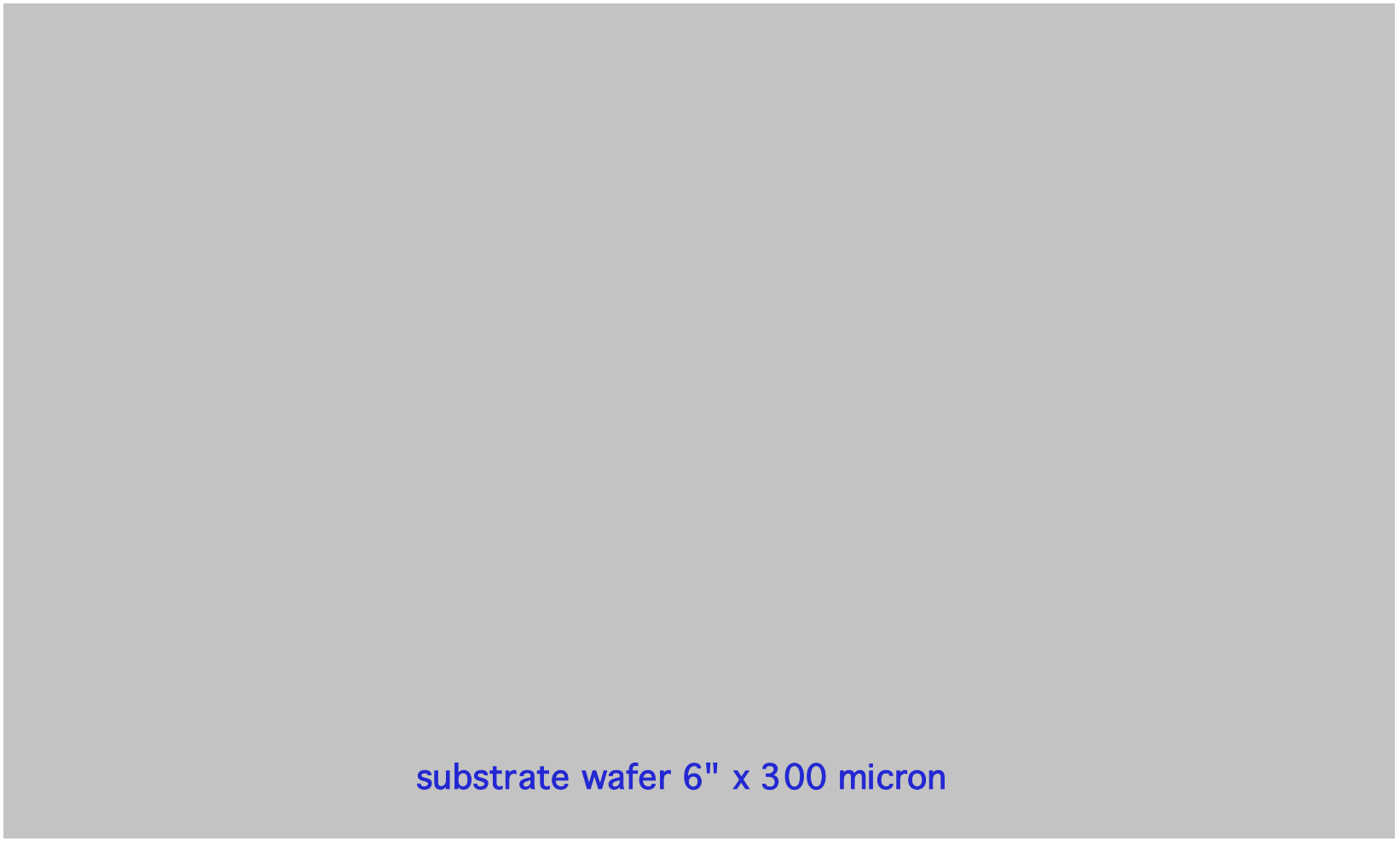
Detector Cross section near one detector edge



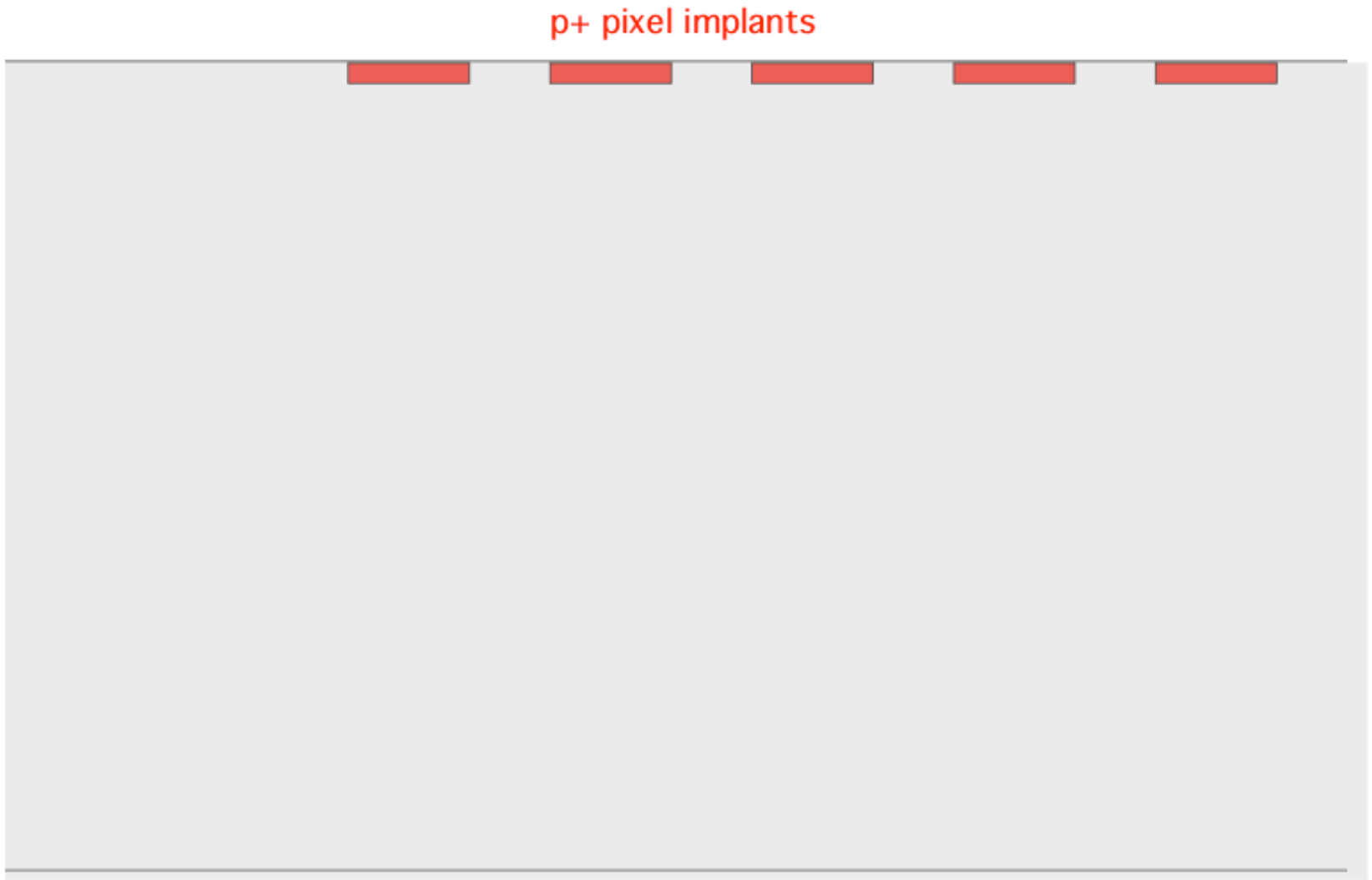
Equipotential lines in detector near one detector edge

Sensor-only fabrication sequence

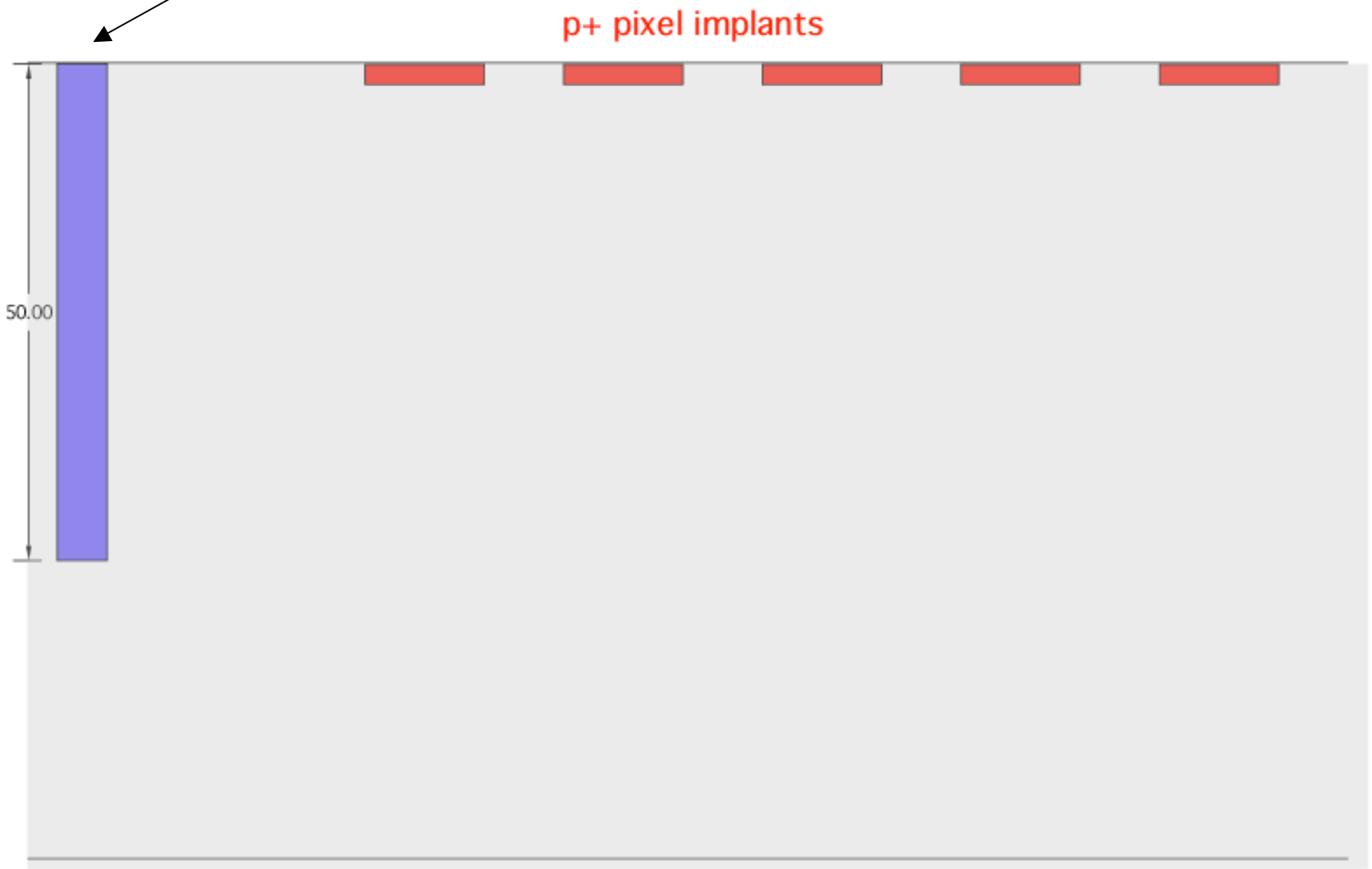
Start with standard float zone silicon wafer



p+ pixel implant

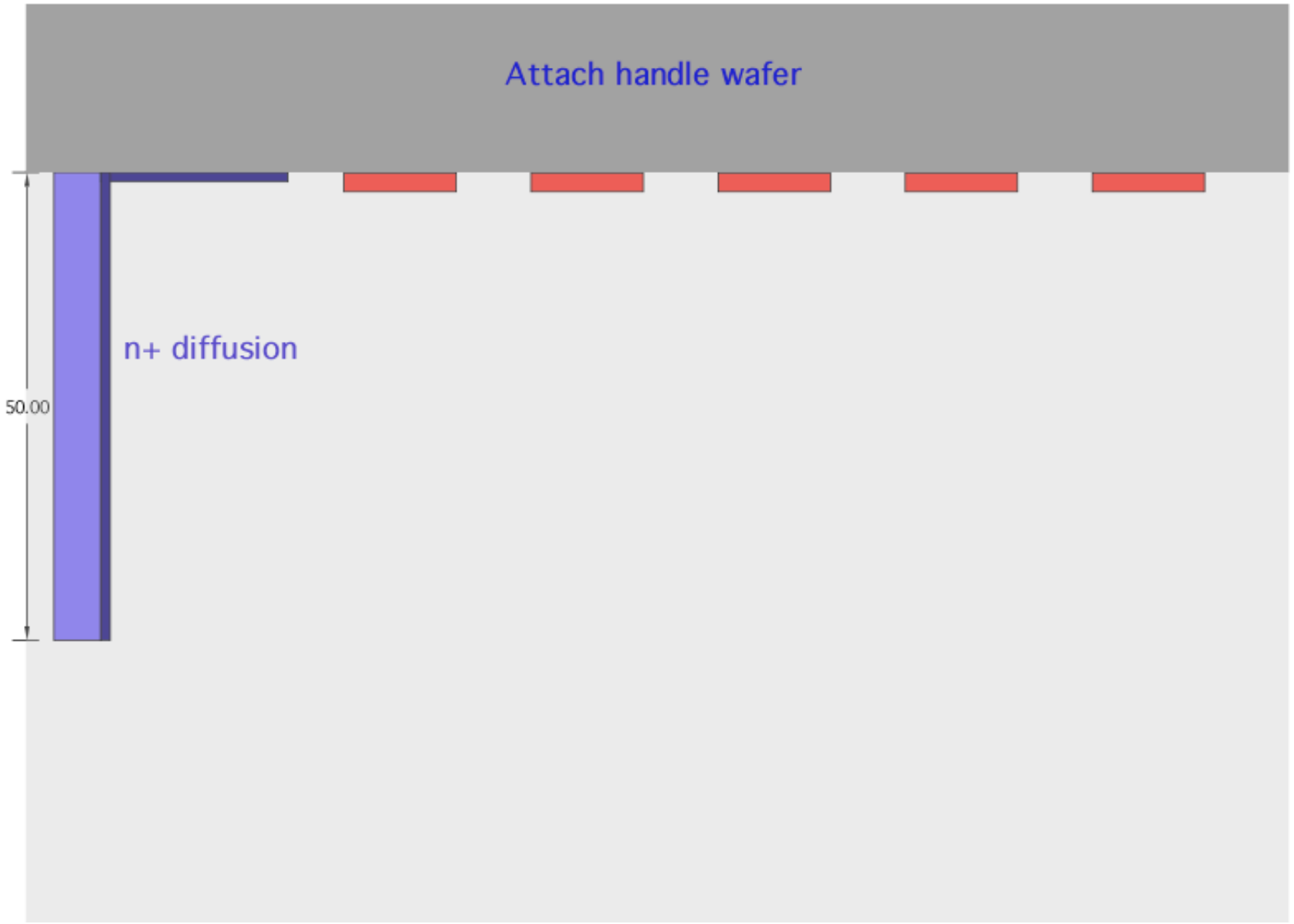


Deep trench etch using Bosch process

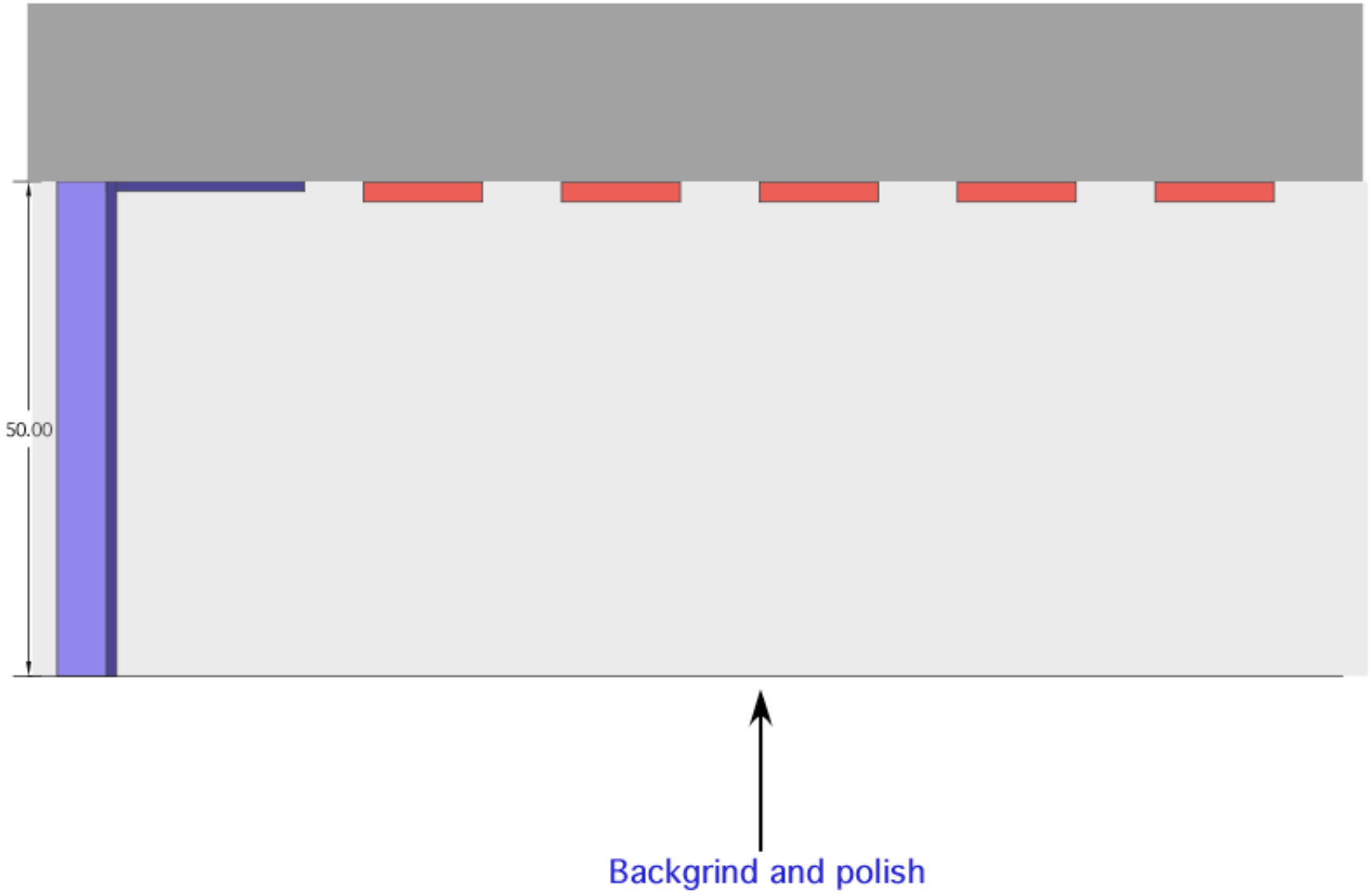


Fill trench with doped polysilicon,
implant edge contact,thermal anneal
Doped polysilicon provides the sidewall doping

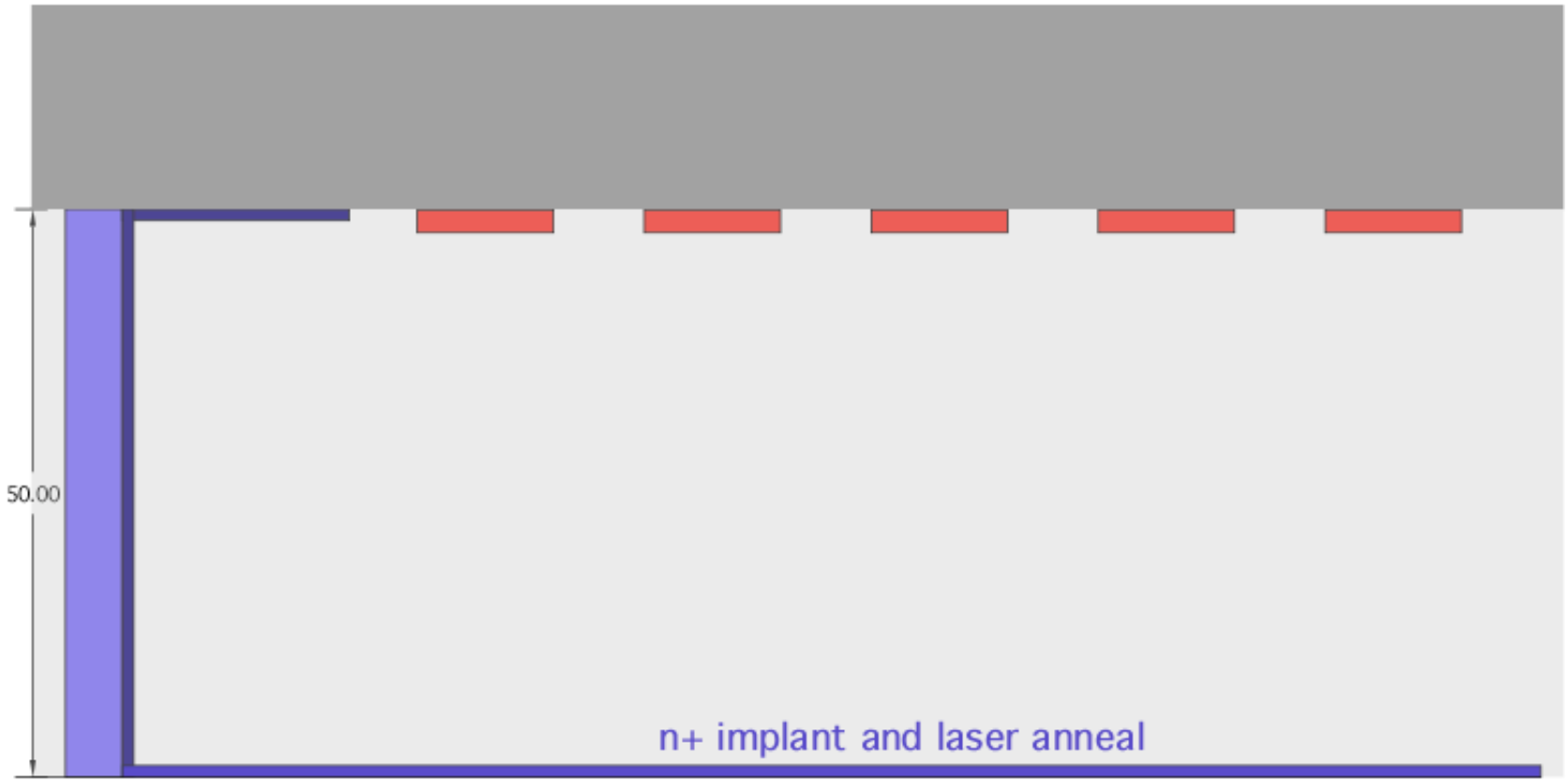
- Handle wafer is attached using oxide bonding



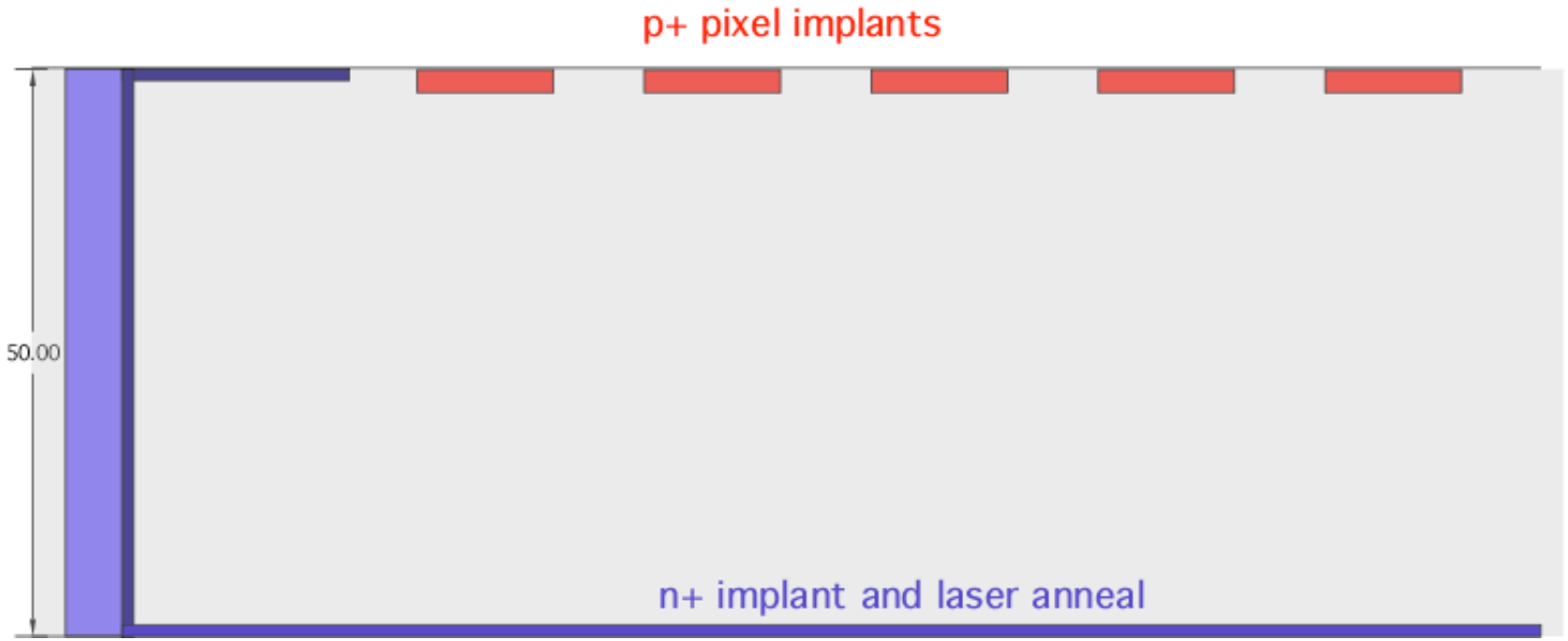
Wafer is ground to desired thickness



Implant and anneal the backside ohmic contact

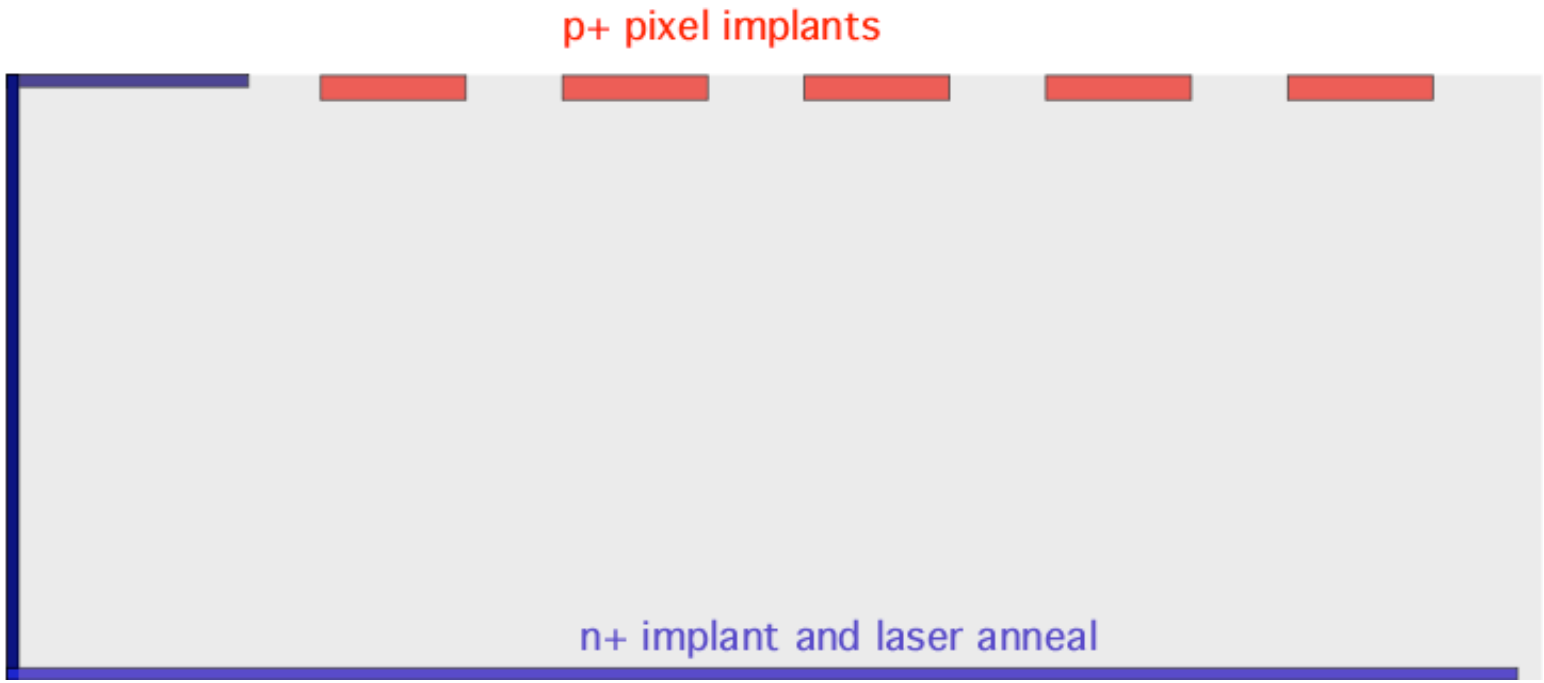


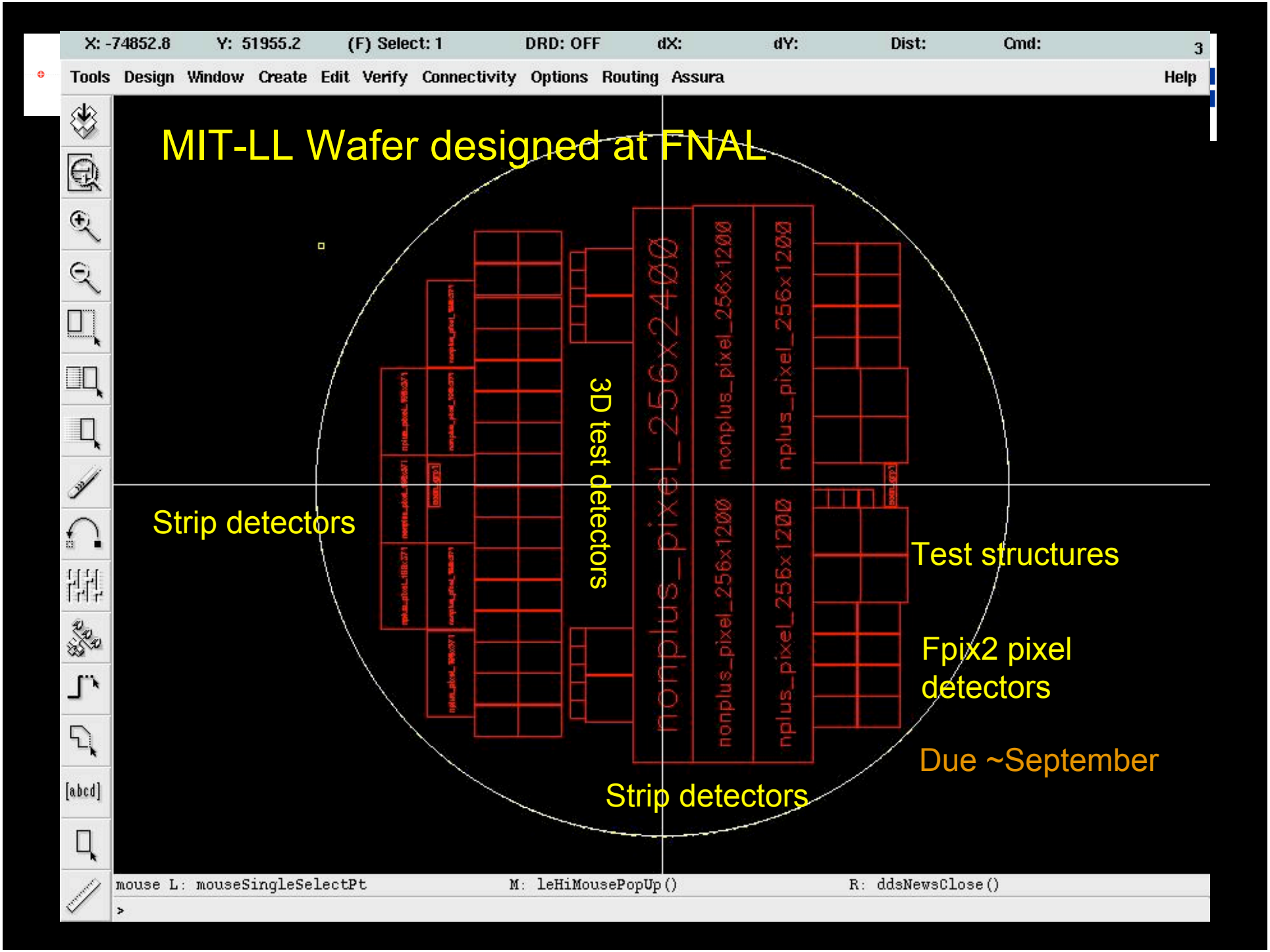
Remove the handle



Add back side quartz handle

Dice and etch away trench polysilicon

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MIT-LL Wafer designed at FNAL
Strip detectors
3D test detectors
Test structures
Fpix2 pixel detectors
Due ~September
Strip detectors
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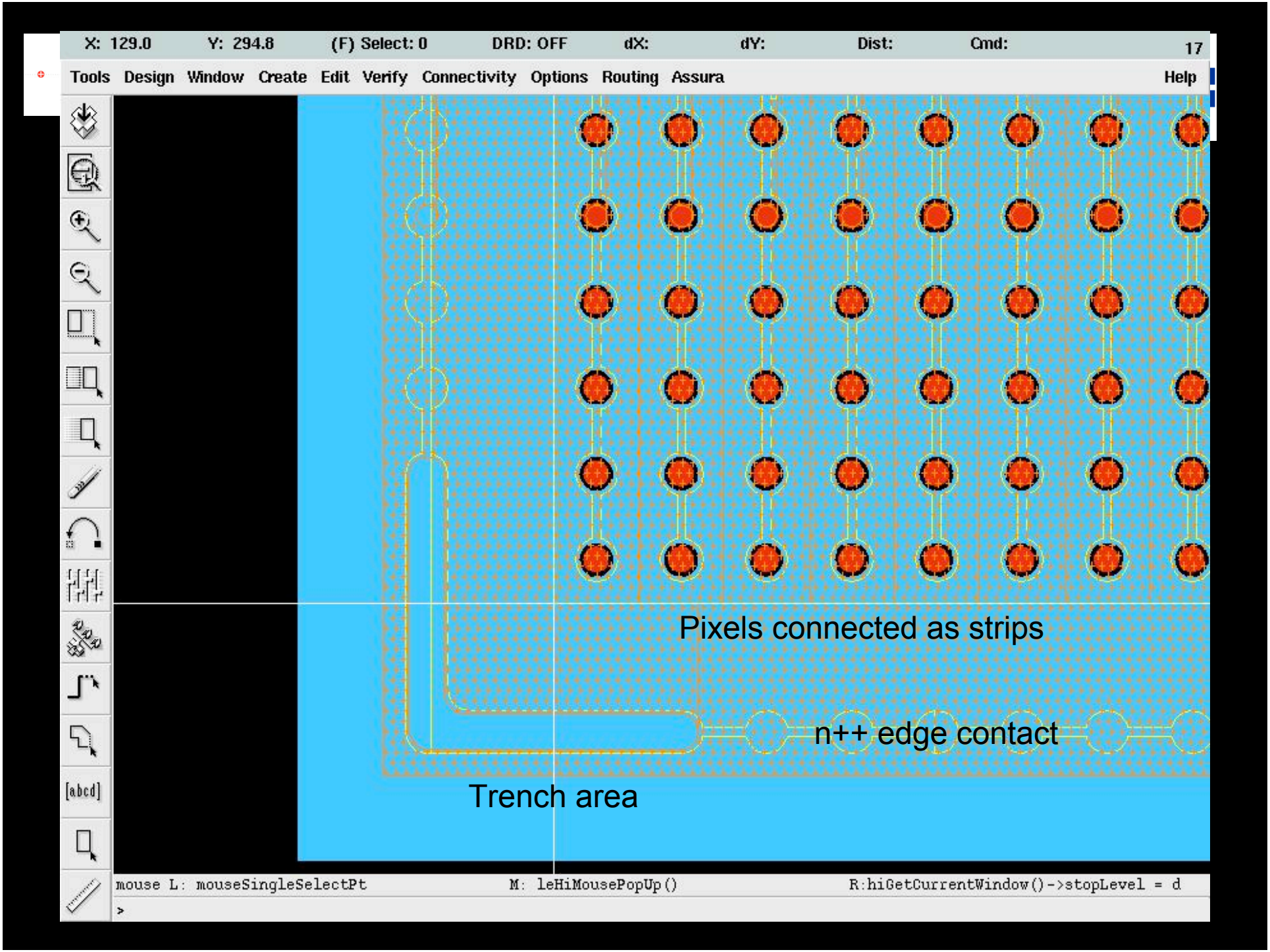
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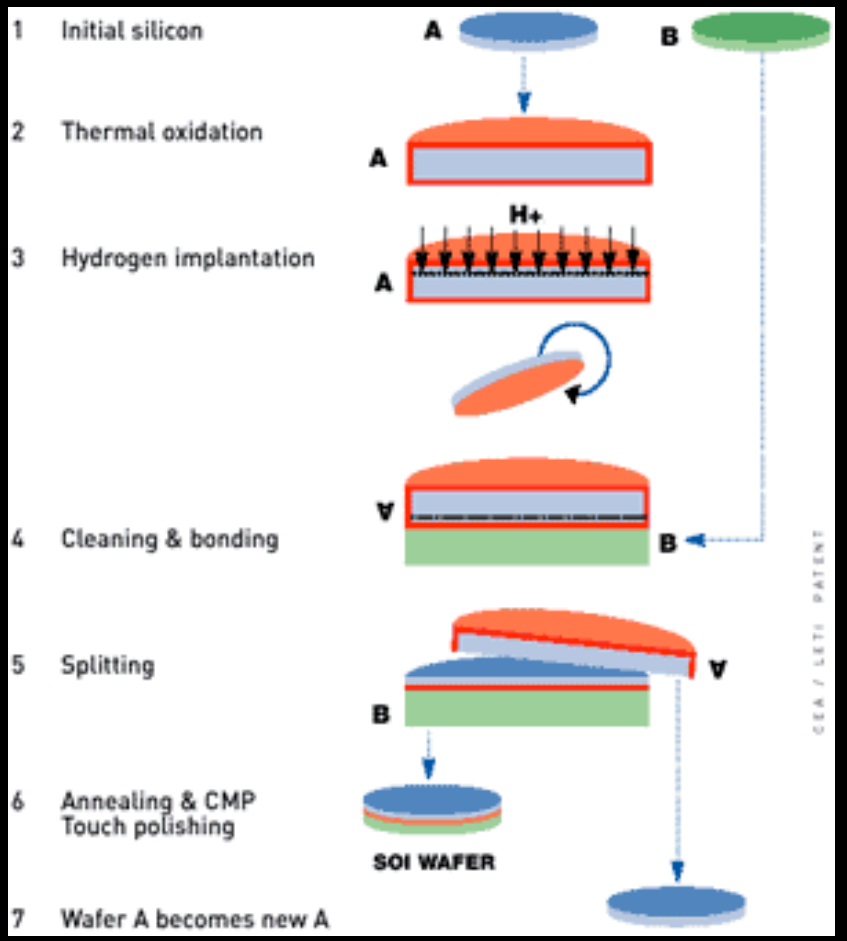
Silicon-on-Insulator

- SOI is based on a thin active circuit layer on an insulating substrate. Modern technology utilizes ~200 nm of silicon on a “buried” oxide (BOX) which is carried on a “handle” wafer.
- The handle wafer can be high quality, detector grade silicon, which opens the possibility of integration of electronics and fully depleted detectors in a single wafer with very fine pitch and little additional processing.
- Used for high speed, circuits, immune to SEU
- Important for 3D integration



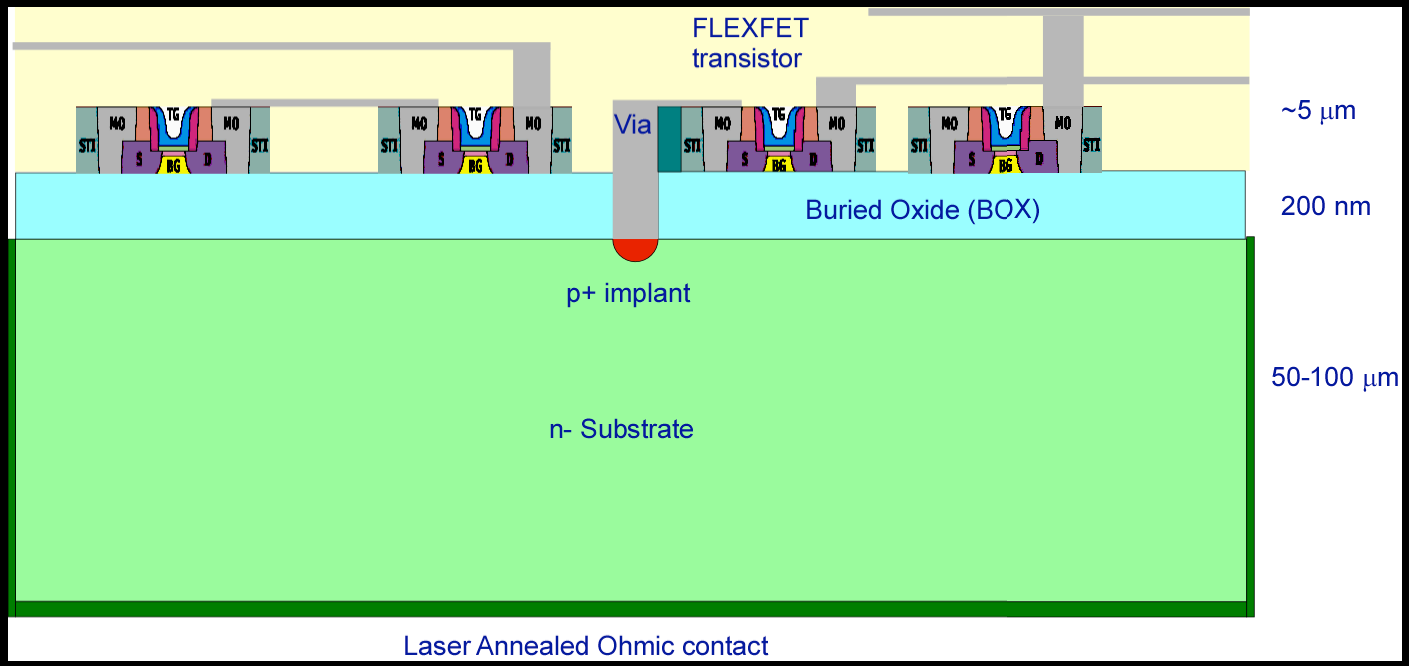
Formation of an SOI wafer

(Soitech illustration)

SOI Concept for HEP

not to scale

Minimal interconnects,
low node capacitance



High resistivity
Silicon wafer,
Thinned to 50-
100 microns

Active edge
processing

Backside implanted after thinning
Before frontside wafer processing
Or laser annealed after processing

SOI Advantages

- Advantages of SOI
  - High resistivity substrate available for fully depleted diodes - large signal
  - No limitation on PMOS transistor usage as in CMOS MAPs
    - Full low power CMOS, integration of digital and analog in pixel
    - No parasitic charge collection
  - Sense nodes can have very low capacitance – crucial for low power signal/noise
  - SOI Radiation hard to >1 Mrad, low SEU sensitivity
  - SOI is a low power technology
  - Sensor thinning to 50 microns demonstrated
  - Minimum charge spreading with fully depleted substrate
  - No bump bonds
  - 100% diode fill factor

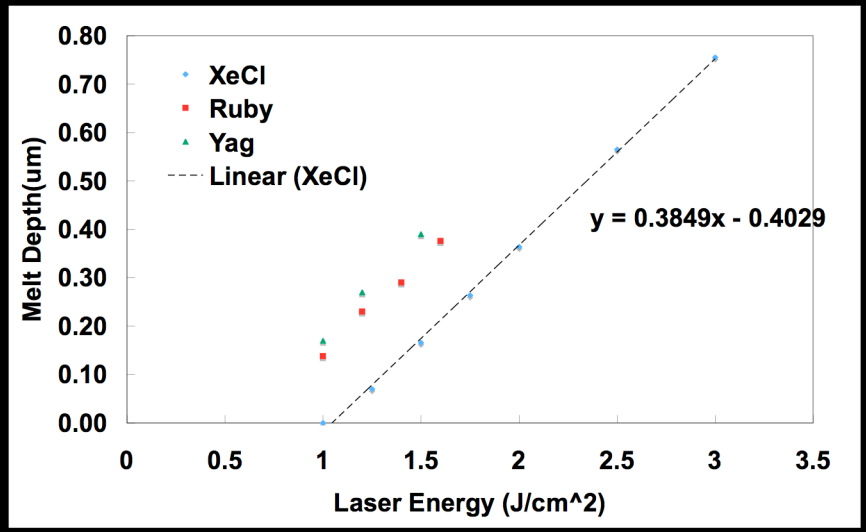
How to Make this Work?

- Explore commercial processes which include processing of the handle wafer as part of the fabrication process (OKI, American Semiconductor).
- What is the optimal process for forming the detector diodes?
  - Model charge collection, shielding
- After thinning a backside contact must be formed. This is usually done by implantation and high temperature furnace annealing - which will destroy the front side CMOS SOI circuitry. An alternative is laser annealing of the backside implantation, which limits the frontside temperature.
- Can we retain good, low leakage current, detector performance through the CMOS topside processing?
- How does the charge in the BOX due to radiation and potential of the handle wafer affect the operation of the top circuitry?
- How does topside digital circuitry affect the pixel amplifier?

Laser annealing

Problem: provide backside contact to thinned wafer while keeping topside below ~500 deg C

- Use a raster scanned eximer laser to melt the silicon locally – this activates the implant and repairs the implantation damage by recrystallizing the silicon
- Diffusion time of phosphorus in molten silicon is much less than cooling time therefore we expect ~uniform distribution in melt region

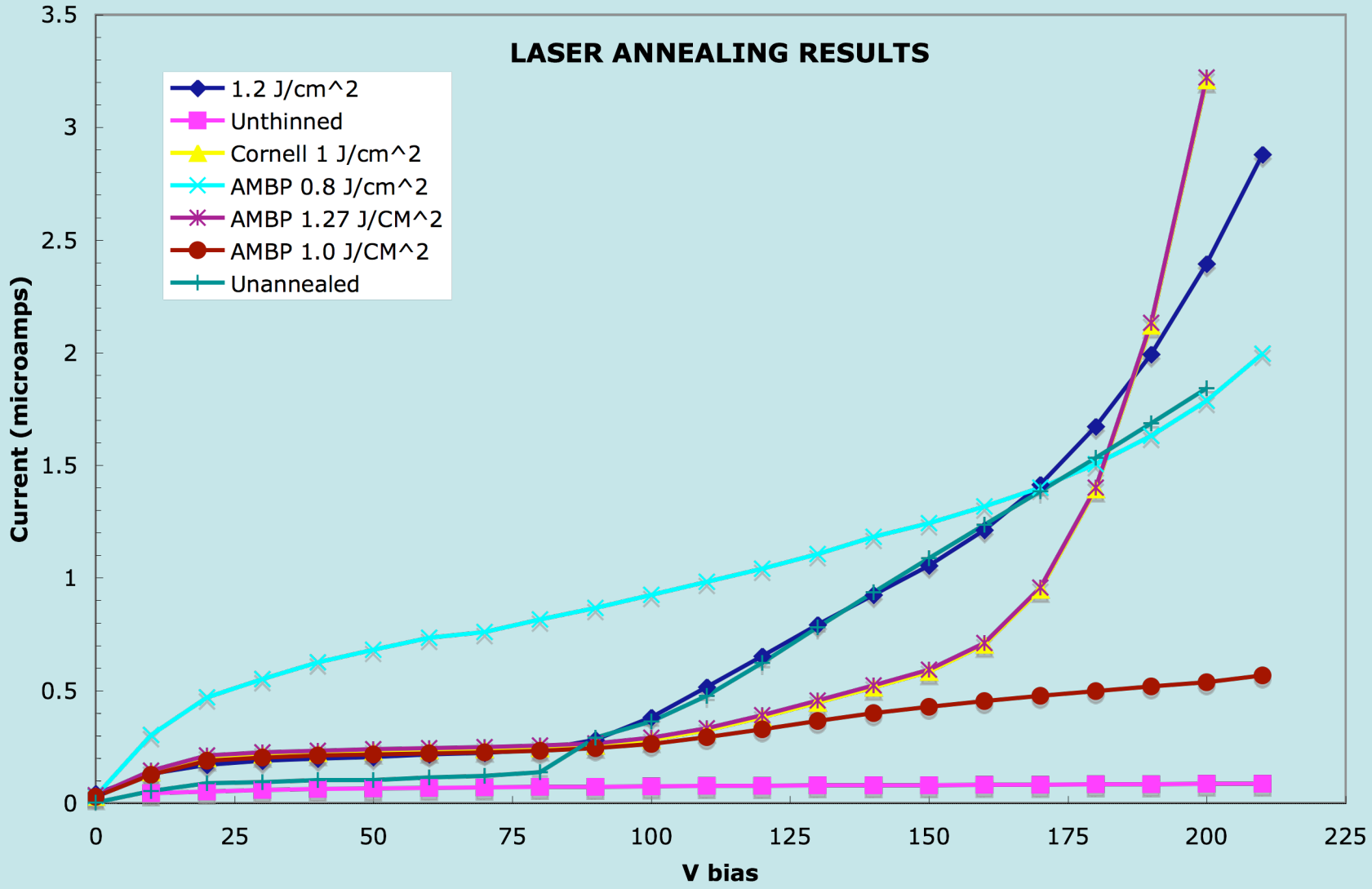


To study and qualify this process we took a sample of Run2b HPK, low leakage 4x10 cm, strip detectors and reprocessed them

- Backgrind by ~50 microns to remove back implant and aluminization, polish
- Re-implant detector using 10 KeV phosphorus at 0.5 and 1.0x10^{15}/cm^2
- Laser anneal and measure CV and IV characteristics
  - AMBP - 0.8, 1.0, 1.2 J/cm^2, 248 nm laser
  - Cornell - 1.0 J/cm^2 34x nm laser

Laser Annealing Results (Cornell)

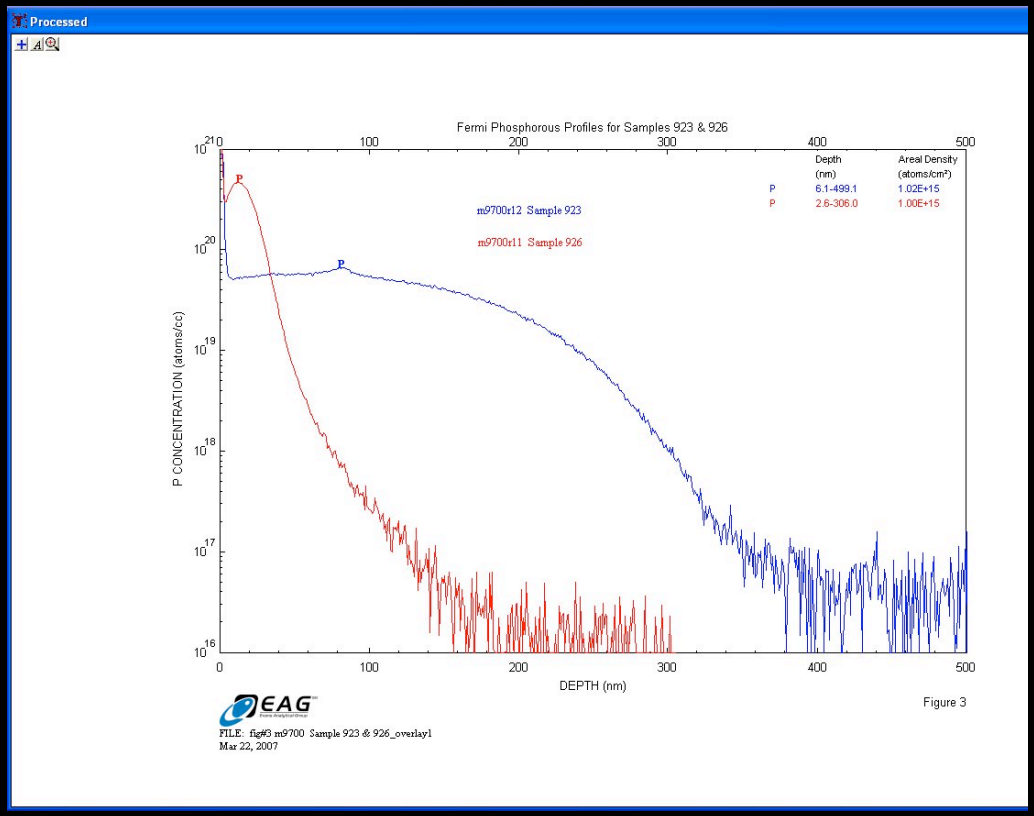
preliminary



SIMS Measurements

Secondary Ion Mass Spectroscopy provides implant depth profiles by analysis of ions ejected from the surface upon ion bombardment:

- Two samples, before and after 1.2 J/cm^2 248 nm laser anneal
- Goal was ~>2x10^{19} concentration
- Melt depth ~300 nm



Laser melt depth is close to expectation, phosphorus concentration close to expectation

- Additional sintering at 400 deg should improve leakage
- Explore leakage current as a function of dose.

Fermilab SOI Detector Activities

SOI detector development is being pursued by Fermilab at two different foundries :OKI in Japan, and American Semiconductor Inc. (ASI) in US . The two processes have different characteristics as seen below

Process	**0.15μm Fully-Depleted SOI CMOS process, 1 Poly, 5 Metal layers (OKI Electric Industry Co. Ltd.).**
SOI wafer	**Wafer Diameter: 150 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、>1k Ω-cm (*No type assignment)*, 650 μm thick (SOITEC)**
Backside	**Thinned to 350 μm, no contact processing, plated with Al (200 nm).**

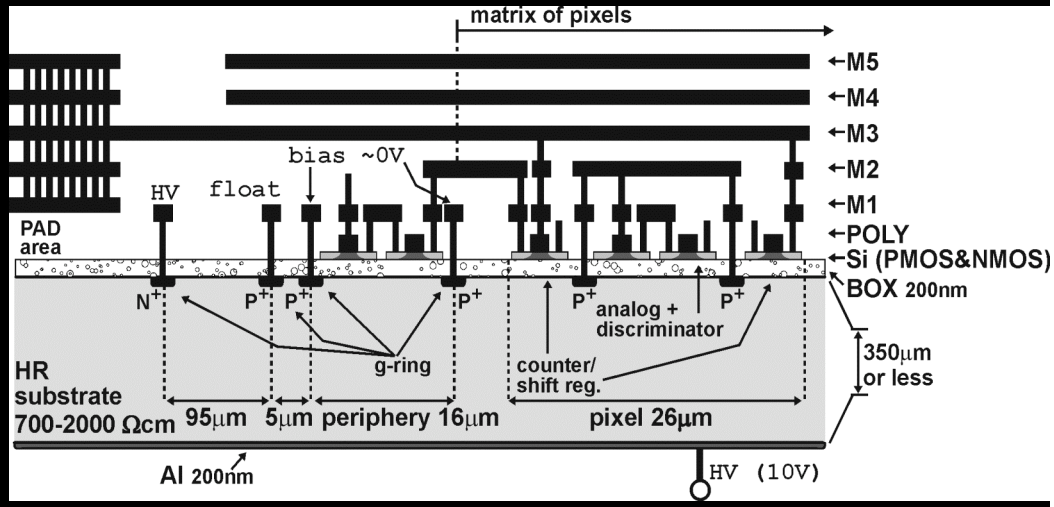
OKI Process

Process	**0.18μm partially-Depleted dual gate SOI CMOS process, Dual gate transistor (Flexfet), No poly, 5 metal (American Semicondutor / Cypress Semiconductor.)**
SOI wafer	**Wafer Diameter: 200 mmϕ, Handle wafer: FZ>1k Ω-cm (*n type)***
Backside	**Thinned to 50-100 μm, polished, laser annealed and plated with Al.**

ASI Process

"Mambo" SOI X-Ray Chip

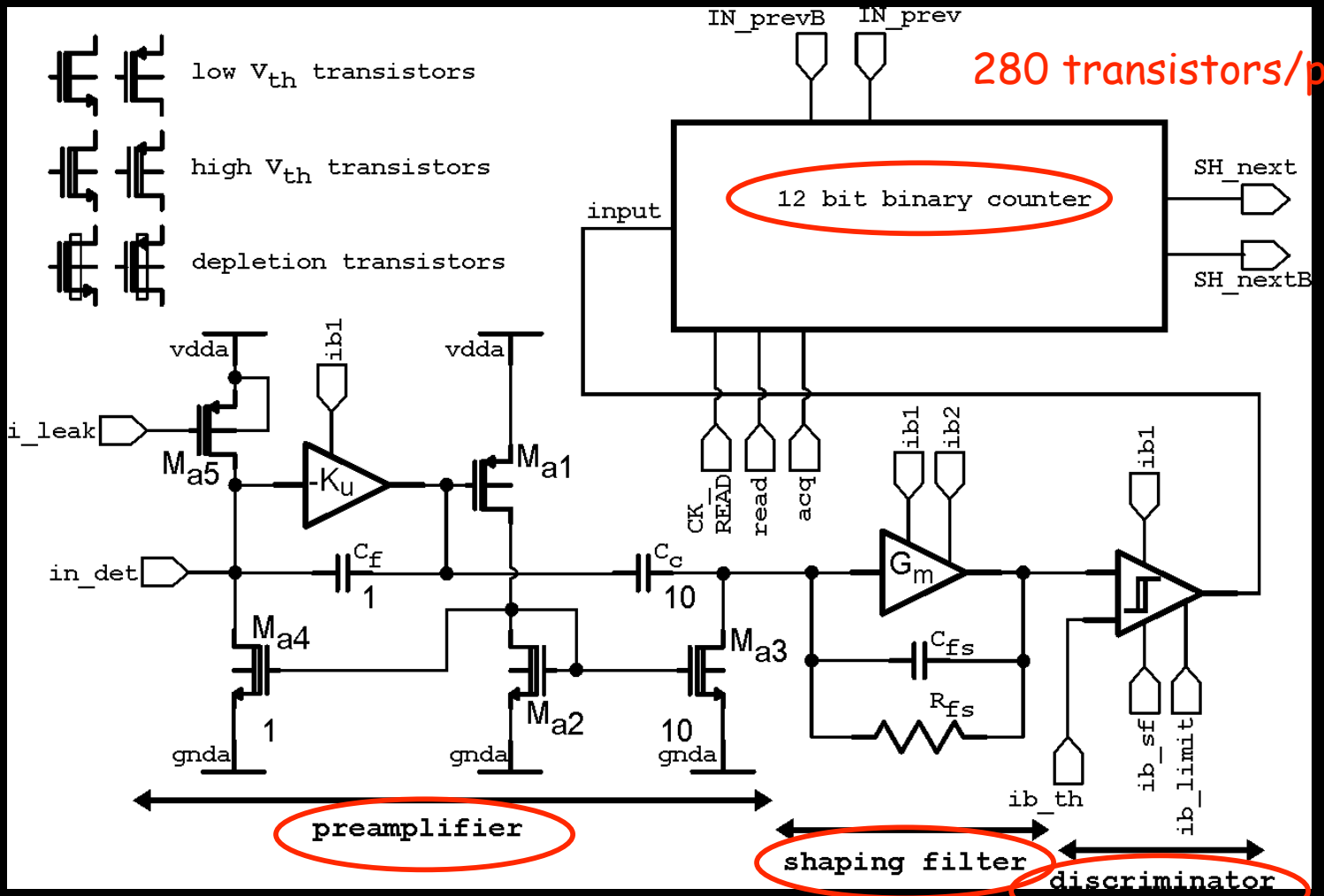
- Fermilab has submitted a design to a KEK sponsored multiproject run at OKI which incorporates diode formation by implantation through the BOX. The chip incorporates a 64 x 64 26 micron pitch 12 bit counter array for a high dynamic range x-ray or electron microscope imaging.
- Max 13 μm implant pitch is determined by the "back gate" effect where the topside transistors thresholds are shifted by handle potential
- Should come to FNAL this month.



Counting pixel detector plus readout circuit

- Maximum counting rate ~ 1 MHz.
- Reconfigurable counter/shift register
- 12 bit dynamic range
- Limited peripheral circuitry
- Drivers and bias generator
- Array size 64x64 pixels
- 350 micron detector thickness

Mambo Chip Schematic



280 transistors/pixel cell

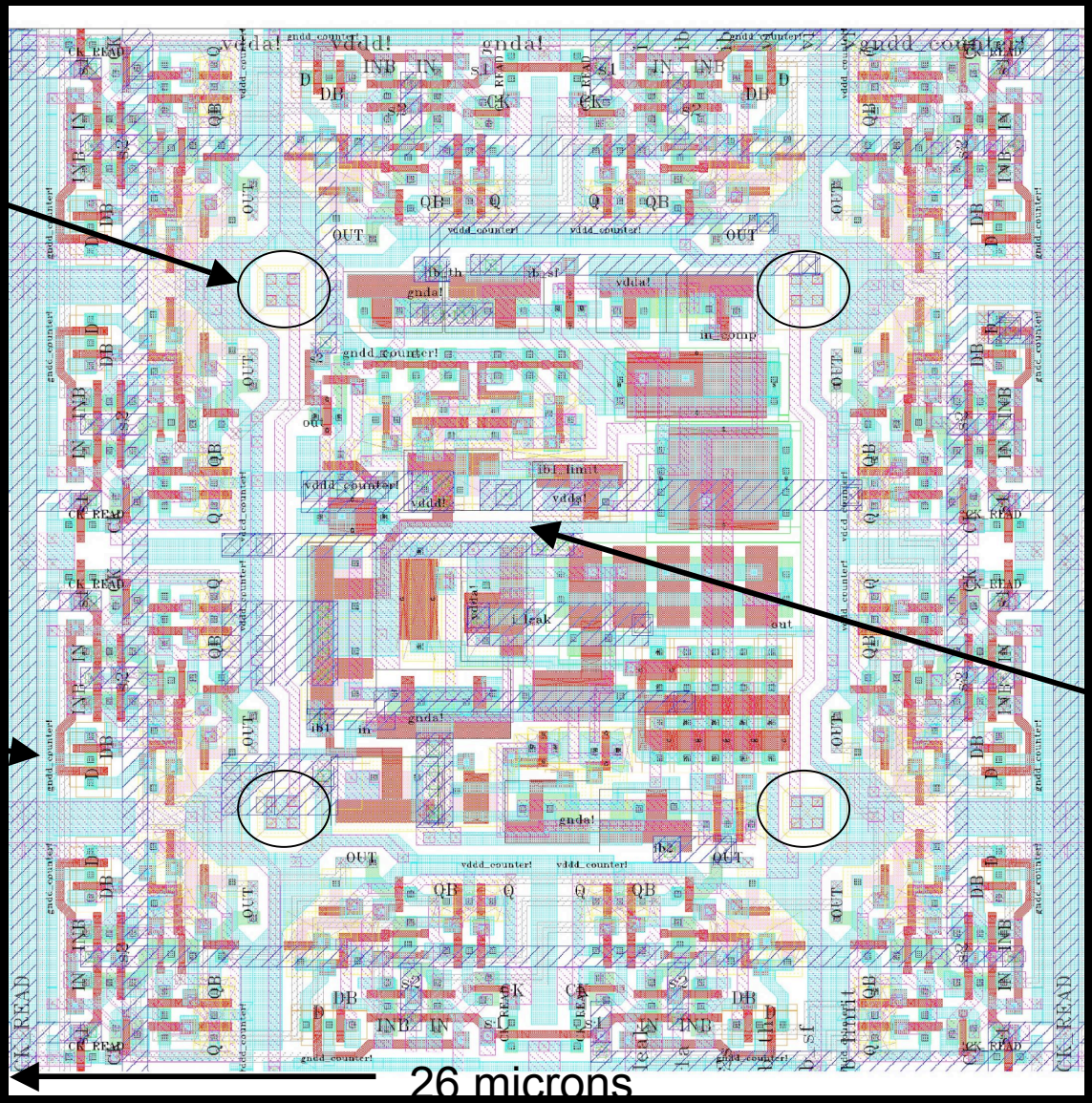
Common Threshold For all discrimina tors

Charge Sensitive Preamplifier with CRRC shaper:
~ 150 mV/1000 e-,
150 ns peaking time

Mambo Pixel Cell Layout

One of four detector diodes

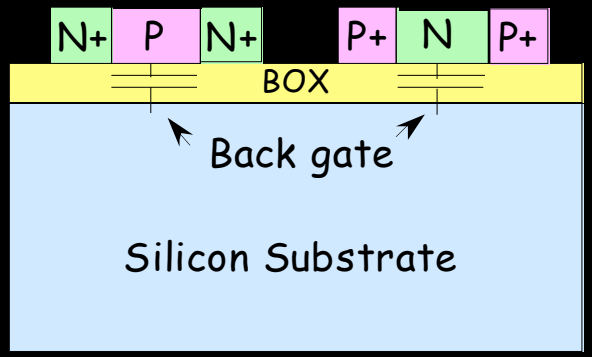
One of twelve D flip-flops arranged around perimeter of pixel cell

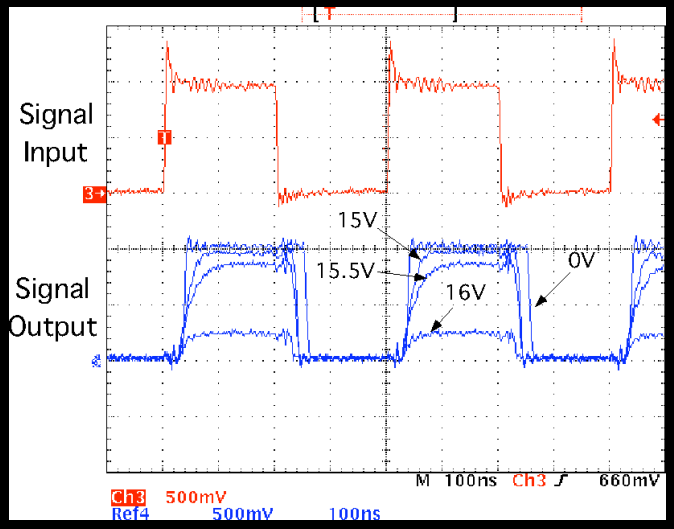


All analog circuits are located in center of pixel cell between diodes and surrounded by guard ring

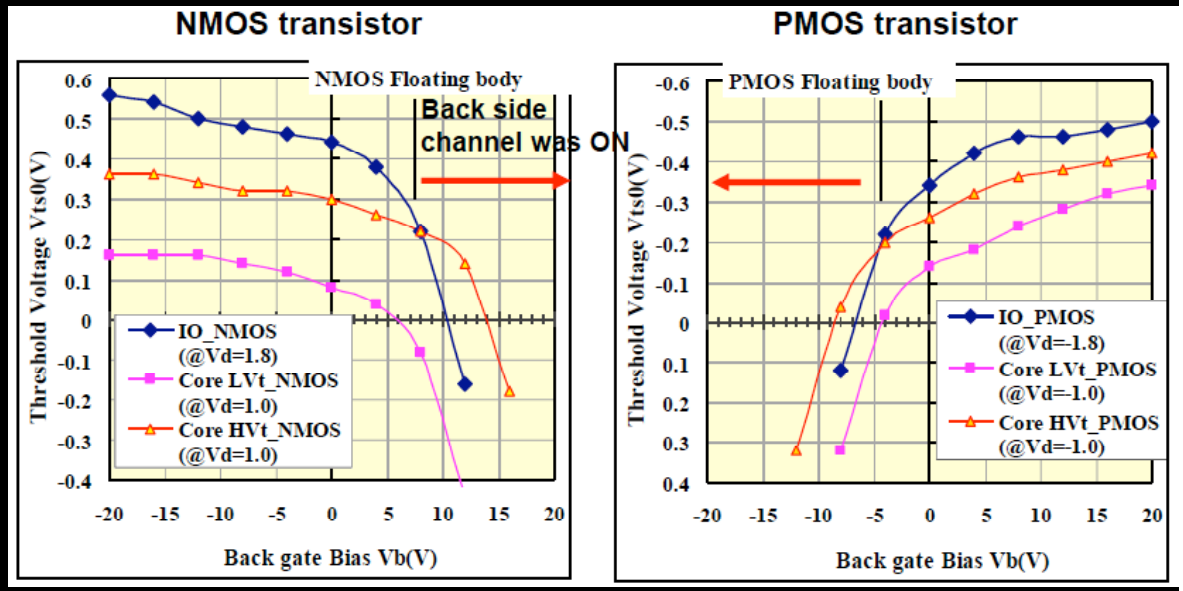
Back gate Effect

Inverter





Signal diappears at Vb~16V



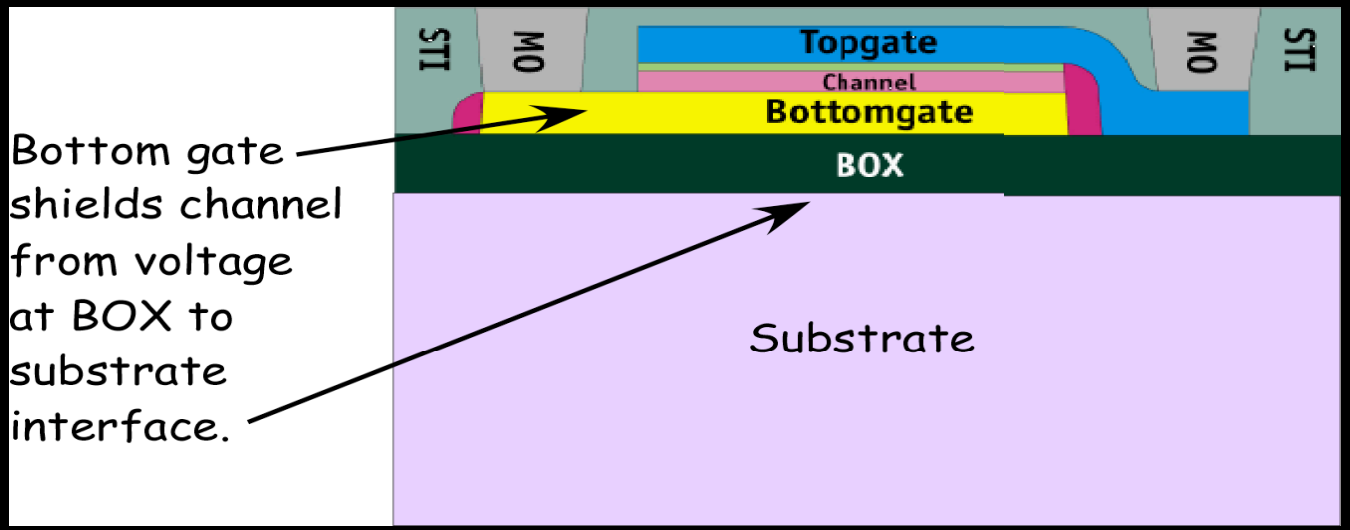
Substrate voltage acts as a back gate bias and changes the transistor threshold - like another gate

- Requires minimum ~15 micron diode spacing to control surface potential

(from Y. Arai (KEK))

American Semiconductor FLEXFET Process

- ASI process based on dual gate transistor called a Flexfet.
- Flexfet has a top and bottom gate.
- Bottom gate shields the transistor channel from charge build up in the BOX caused by radiation.
- Bottom gate also shields the transistor channel from voltage on the substrate and thus *removes the back gate voltage problem*.
- The process can include a “pinning layer” which can be used to shield the analog pixel from digital activity

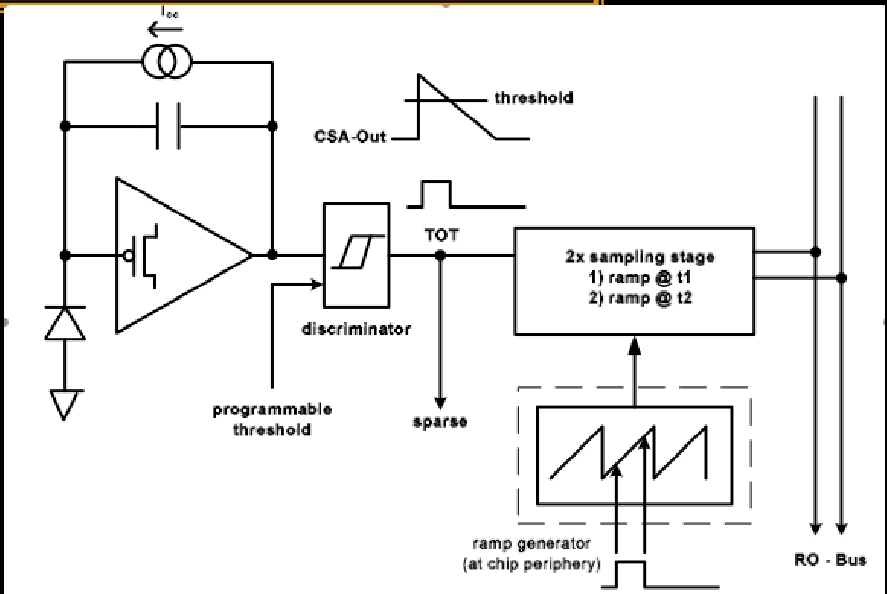


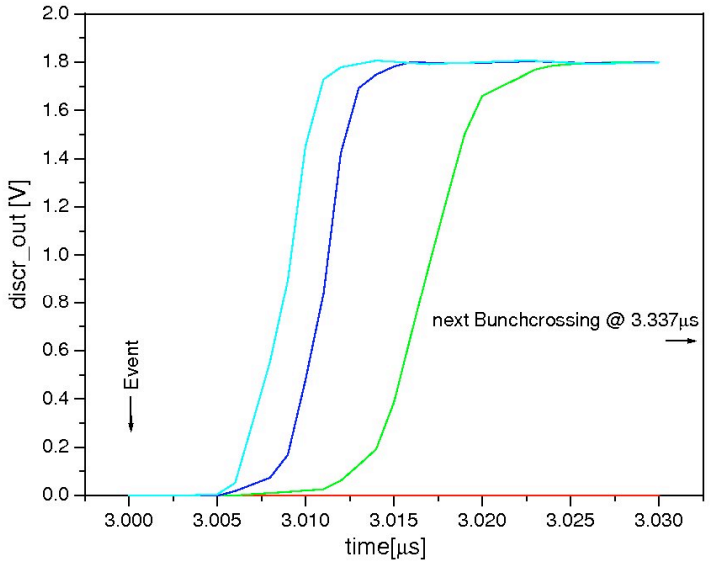
Pixel Design in ASI 0.18μm

As part of a phase I SBIR with ASI FNAL designed a demonstration SOI Pixel cell

- Voltage ramp for time marker
- ~20 micron analog pixel
  - Folded cascode amp
  - Current feedback
  - Discriminator
  - Two time ramp sampling stages
- Sample 1 - crossing time
- Sample 2 - time over threshold for analog pulse height information
- Additional 3-5 bit counter for coarse time stamp

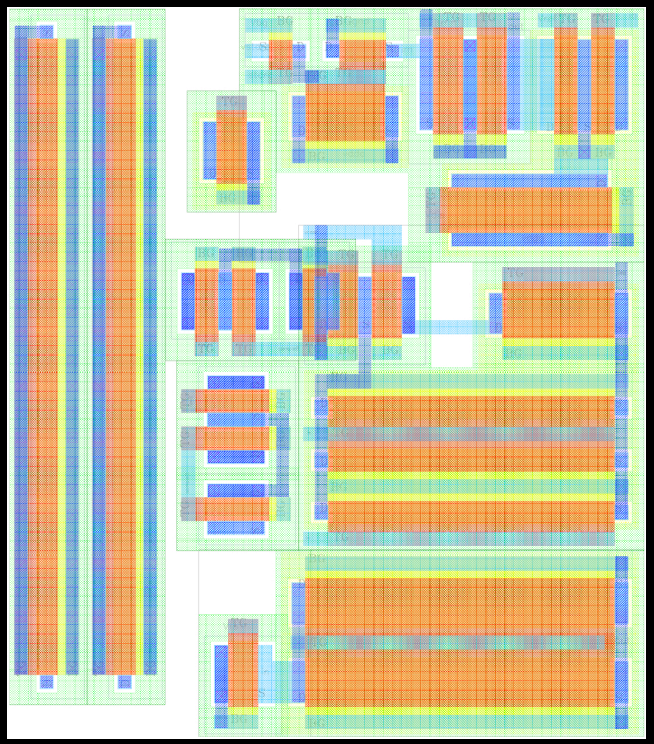
This technique can be tested with the 3D chip

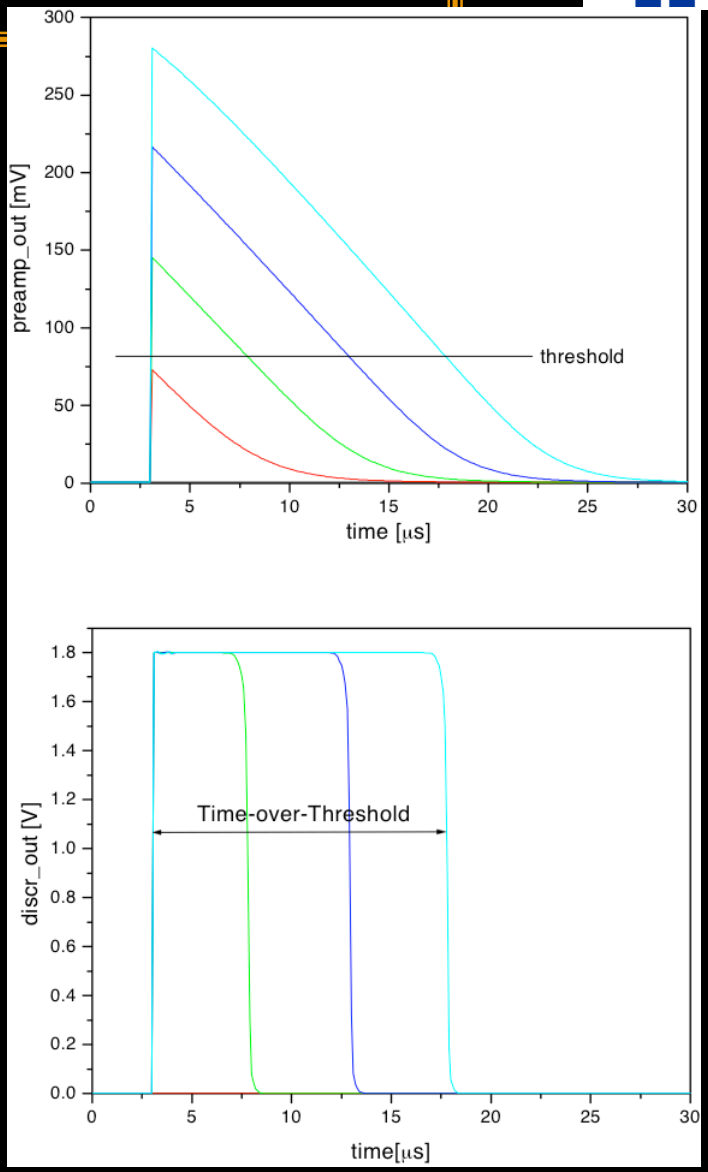




ASI Pixel Simulations

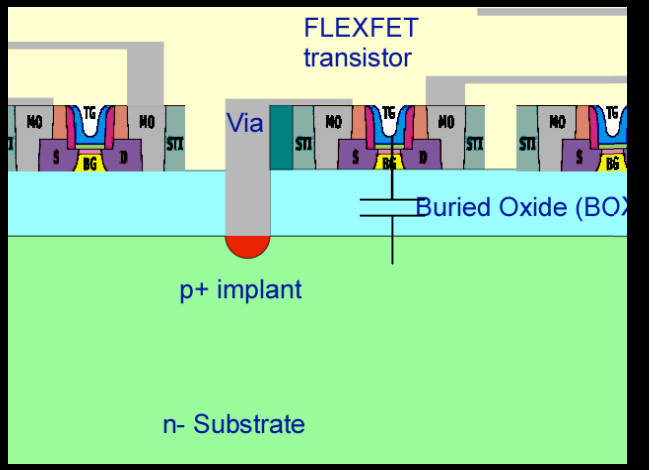
- Analog section layout ~19 x 22 microns
- Simulation of preamp/discriminator system for time over threshold



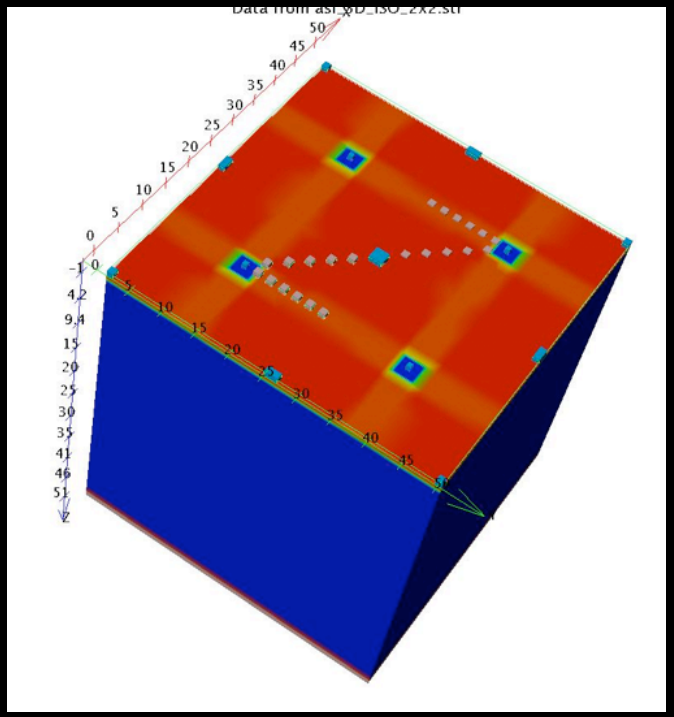


Analog/Digital Coupling

- SOI is sensitive to capacitive coupling of digital signals to pixel
  - Add a “pinning” layer at the surface of the substrate between pixels tied to a fixed potential
  - Layer must be designed to limit back to pinning current (punchthrough)
  - Available in ASI Process
  - Simulate 1.8V digital coupling to pixel
- 2D / 3D Silvaco device simulations confirm effectiveness of pinning layer



Condition	Q injected (e)
Unipolar, no pinning	2300
Bipolar, no pinning	~1/3
Unipolar pinned	23
Bipolar, pinned	~0



3D model of SOI pixel with injection electrodes

3D Pixel Design for ILC Vertex

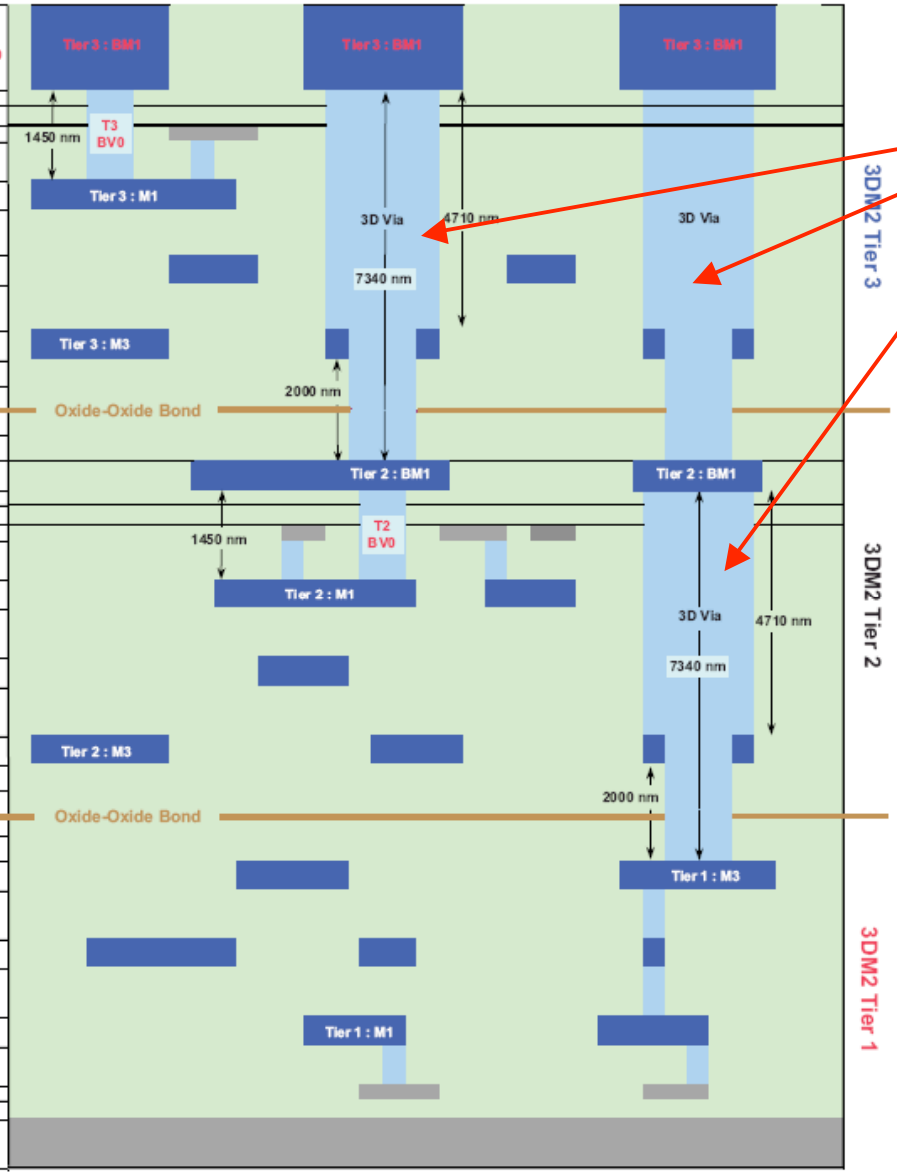
Goal - demonstrate ability to implement a complex pixel design with all required ILC properties in a 20 micron square pixel

Previous technologies limited to very simple circuitry or large pixels

- 3D chip design in MIT Lincoln Labs 0.18 um SOI process.
- Key features: Analog pulse height, sparse readout, high resolution time stamps.
- Time stamping and sparse readout occur in the pixel, Hit address found on array perimeter.
- 64 x 64 pixel demonstrator version of 1k x 1K array.
- Submitted to 3 tier multi project run. Sensor to be added later.

MIT LL 3D Multiproject Run Chip Cross Section

Tier 3	Back Metal 1 (RF)	2000
Tier 3	Cap oxide	200
Tier 3	BOX	400
Tier 3	SOI island	50
Tier 3	LTO over island	800
Tier 3	Metal 1	630
Tier 3	ILD 1-2 PECVD TEOS	1000
Tier 3	Metal 2	630
Tier 3	ILD 2-3 PECVD TEOS	1000
Tier 3	Metal 3	630
Tier 3	M3 overglass PECVD TEOS	500
Tier 3	BSG cap oxide	500
Tier 2	BSG cap oxide	500
Tier 2	PECVD TEOS	500
Tier 2	Back metal 1	630
Tier 2	Cap oxide	200
Tier 2	BOX	400
Tier 2	SOI island	50
Tier 2	LTO over island	800
Tier 2	Metal 1	630
Tier 2	ILD 1-2 PECVD TEOS	1000
Tier 2	Metal 2	630
Tier 2	ILD 2-3 PECVD TEOS	1000
Tier 2	Metal 3	630
Tier 2	M3 overglass PECVD TEOS	500
Tier 2	BSG cap oxide	500
Tier 1	BSG cap oxide	500
Tier 1	M3 overglass PECVD TEOS	500
Tier 1	Metal 3	630
Tier 1	ILD 2-3 PECVD TEOS	1000
Tier 1	Metal 2	630
Tier 1	ILD 1-2 PECVD TEOS	1000
Tier 1	Metal 1	630
Tier 1	LTO over island	800
Tier 1	SOI island	50
Tier 1	BOX	400
Tier 1	Silicon substrate	



3D vias

8.2 μm

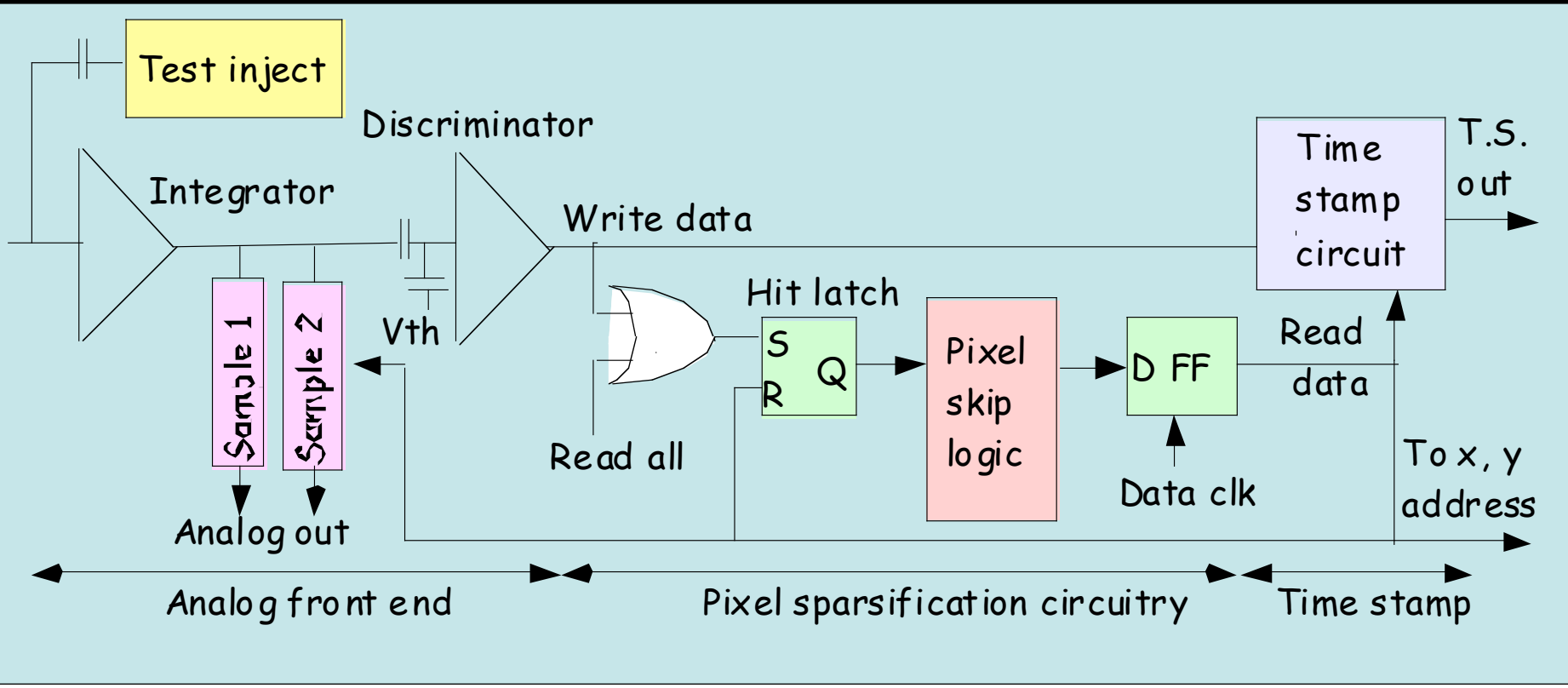
7.8 μm

6.0 μm

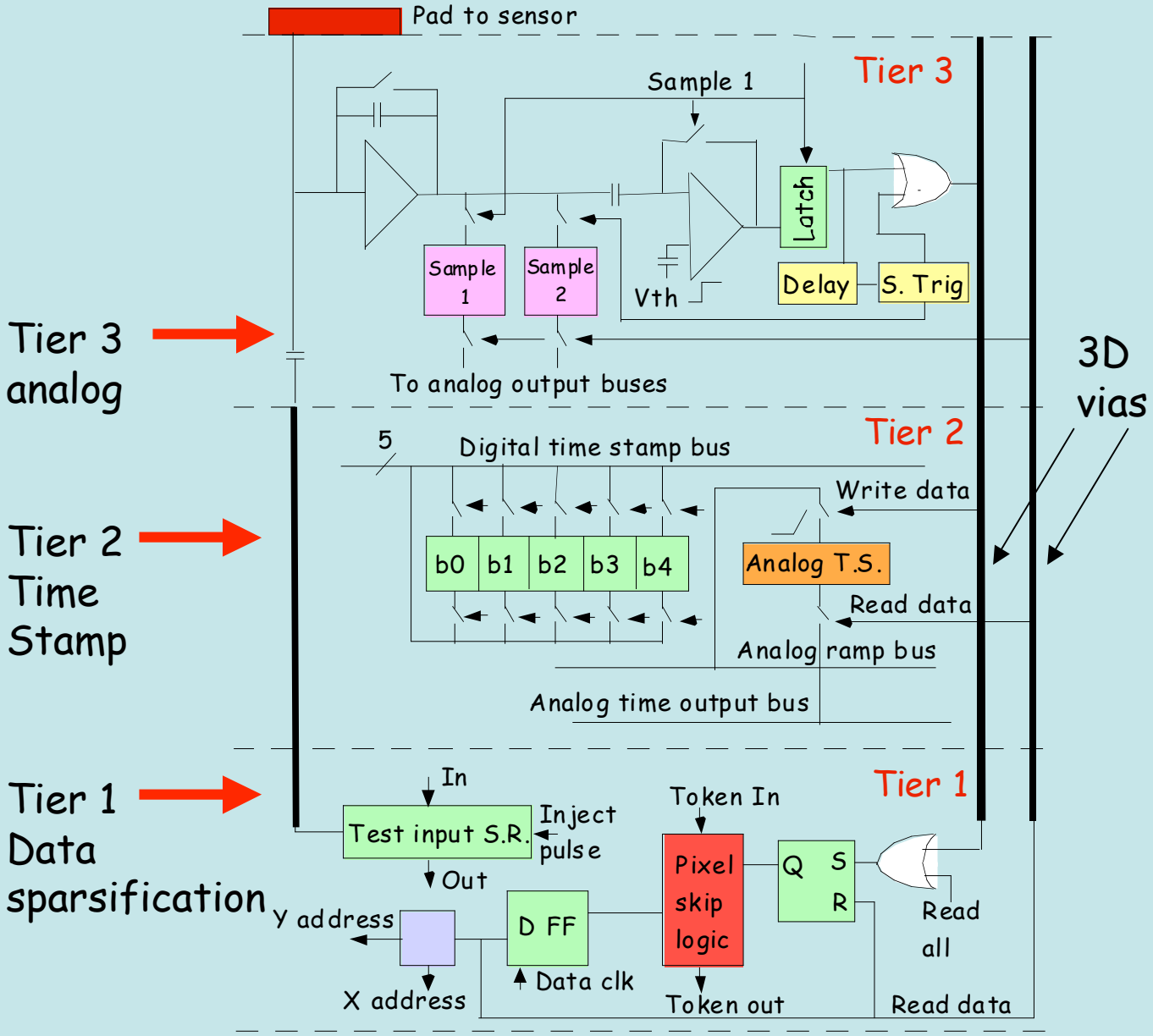
Three levels of transistors, 11 levels of metal in a total vertical height of only 22 um.

Simplified Pixel Cell Block Diagram

- When a Hit occurs, the Hit pixel stores Sample 1 & 2 and the Time Stamp, and sets the Hit Latch in sparse readout circuit.
- During readout, when the read out token arrives, the time stamp and analog values are read out, and pixel points to hit address found on perimeter of chip.
- While outputting data from one pixel, the readout token is passed ahead looking for next pixel that has been hit.

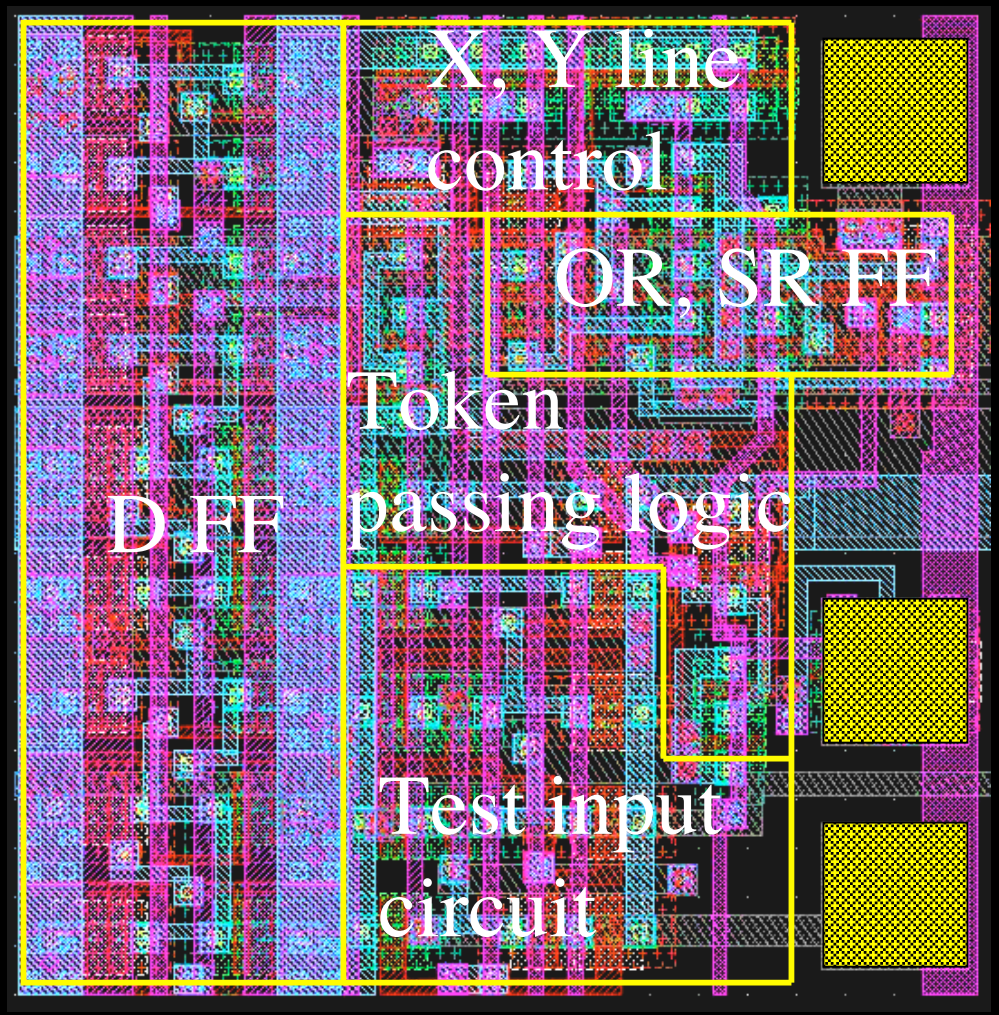


Chip designers:
Tom Zimmerman
Gregory Deptuch
Jim Hoff



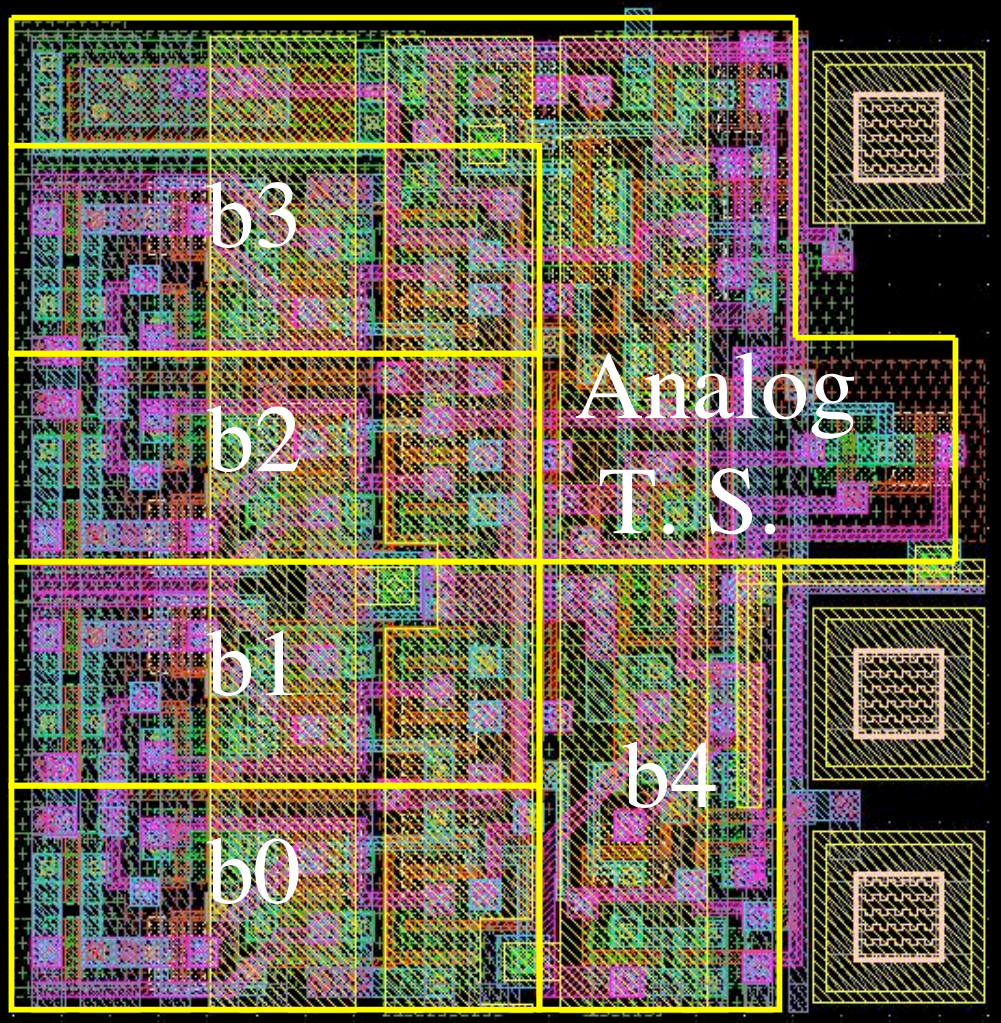
Tier 1 - Sparsification

- OR for READ ALL cells
- Hit latch (SR FF)
- Pixel skip logic for token passing
- D flip flop (static), conservative design
- X, Y line pull down
- Register for programmable test input.
- Could probably add disable pixel feature with little extra space
- 65 transistors
- 3 via pads



Tier 2 - Time Stamp

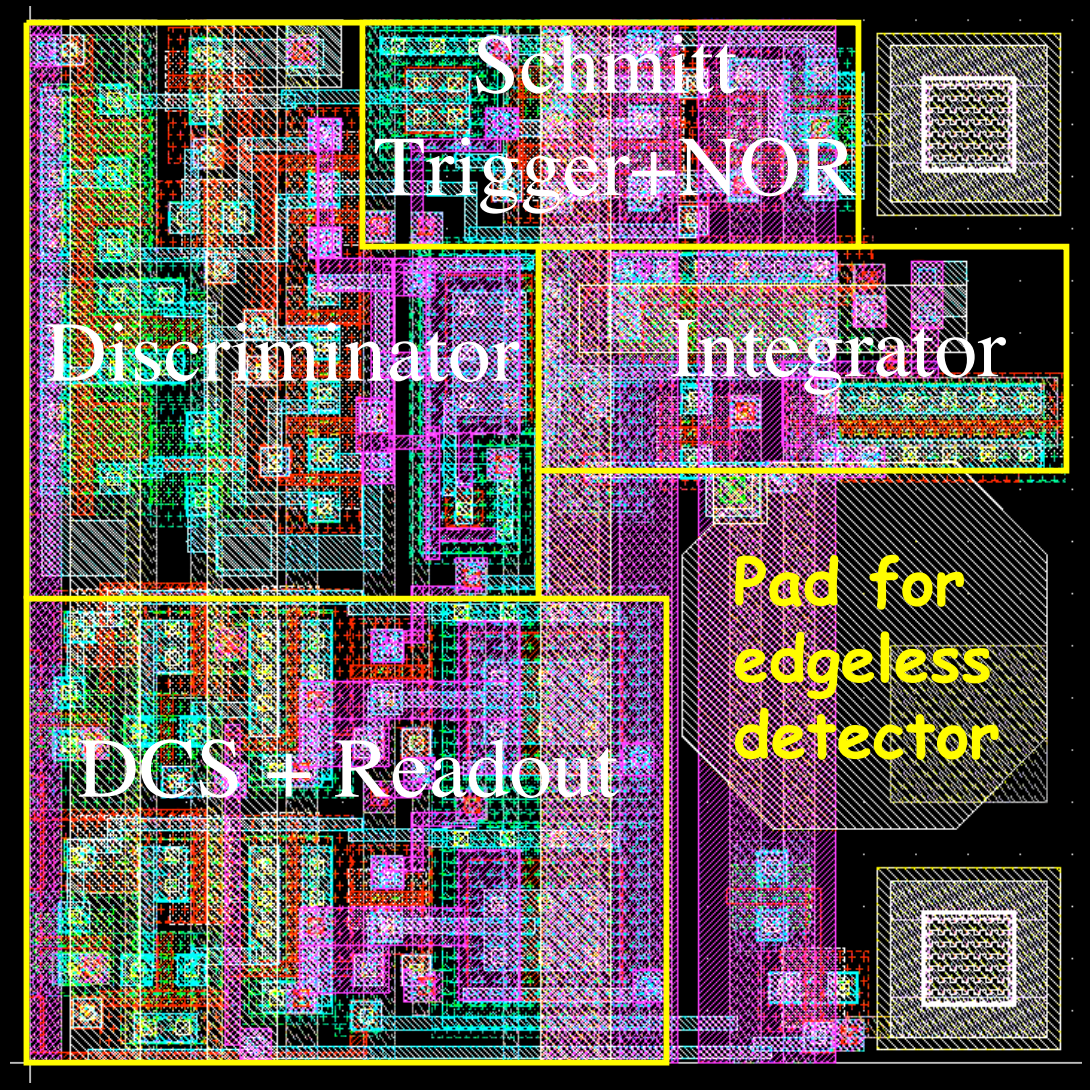
- 5 bit digital time stamp
- Analog time stamp – resolution to be determined by analog offsets and off chip ADC
- Gray code counter on periphery
- 72 transistors
- 3 vias



Tier 3 - Analog

- Integrator
- Double correlated sample plus readout
- Discriminator
- Chip scale programmable threshold input
- Capacitive test input
- 38 transistors
- 2 vias1.5 μm dia by 7.3 μm long
- Expected power ~

Chip is due back in August. Issues to be studied include analog performance, yield, and radiation tolerance.

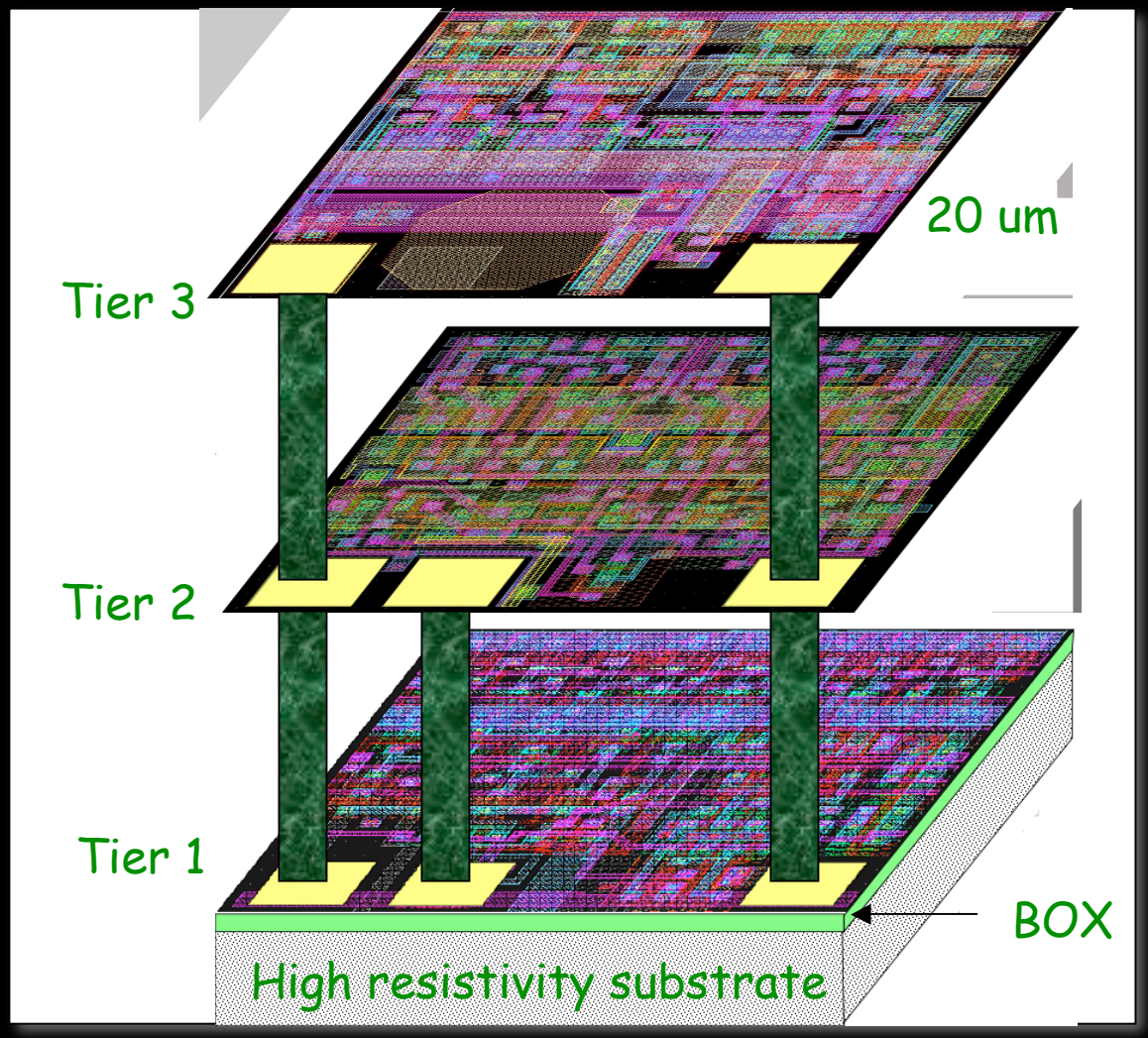


Full Pixel Circuit

Pixel cell:

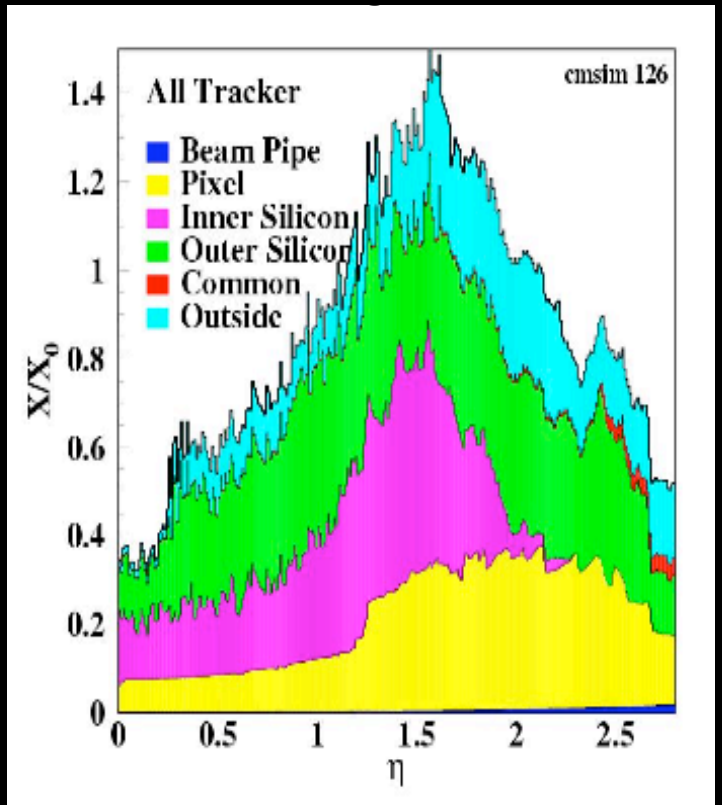
- 175 transistors in 20 μm pixel.
- Unlimited use of PMOS and NMOS.
- Allows 100 % diode fill factor.

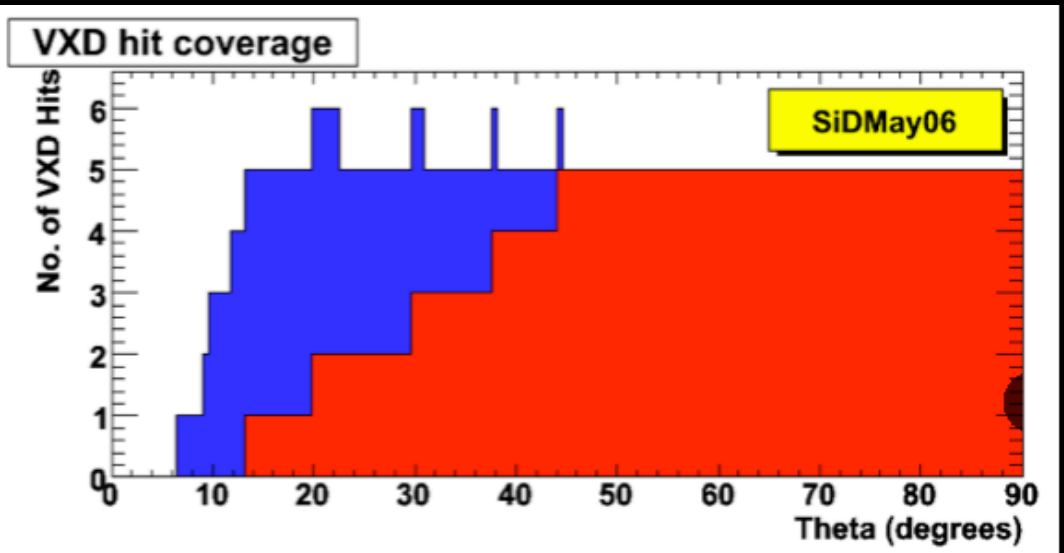
If it functions properly we will try to bond the chip to the 50 micron thick “edgeless” sensors utilizing CuSn or DBI bonding technology. (requires full wafers for pre-processing)



Material and Power

- Can this be improved for SLHC?





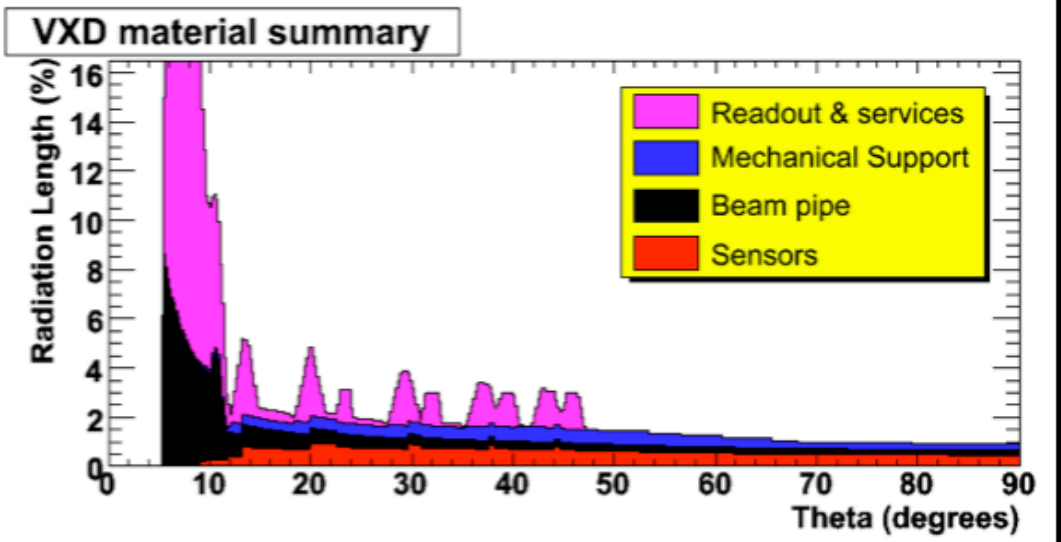


Figure 33 VXD hit pattern and material summary as a function of polar angle.

Noise and Power

Series white noise:

$$ENC^2 = (C_{\det} + C_{gate})^2 \frac{a_1 \gamma 2kT}{g_m t_s}$$

- Power scales as C^2 and 1/transductance (g_m)
- Pixel front end transistors will operate in weak inversion - where g_m is independent of device geometry and ~($I_d q/kT$).
- Acceptable low current operation (<1 μA) requires long shaping and/or low node capacitance
  - For 50e noise, t_s = 100ns, Id=0.5 μA *Cd < 135 ff*
  - ~10 ff should be achievable in SOI devices

Power Distribution

- Power is a crucial issue for the vertex detector
  - CP CCD 20 amps x 200 modules = *4000 amps* of clock
  - MAPS or SOI 20-100W x 100(DF)@1V = *2000 - 10,000 amps*
- LHC detectors are seriously compromised because power was not a driver from the start
- Vertex detector technology is sexy - but power engineering is just as important
  - Serial powering (think Xmas lights) can lower instantaneous current
    - Understand noise, engineer regulators, understand interconnects
  - Lower CCD capacitance
  - Routing within SiD
    - Include something capable of providing 2-10kW during train in simulation

Serial Power

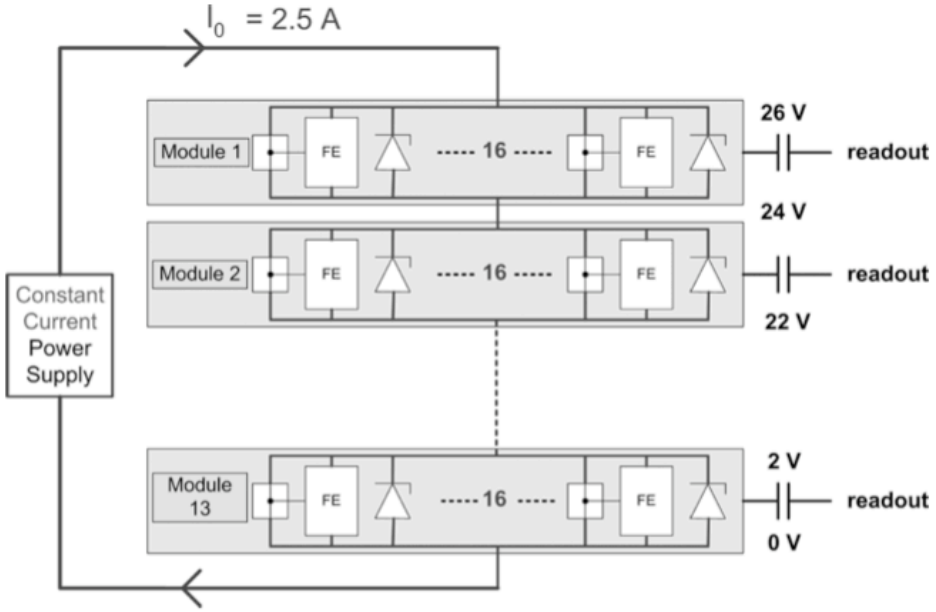


Fig. 1. Basic scheme of serial powering. A power supply provides a constant current which is fed into a chain of modules. In each module a shunt regulator generates a constant voltage from the constant current. Additional linear regulators are used if more than one supply voltage is needed.

Atlas SLHC design

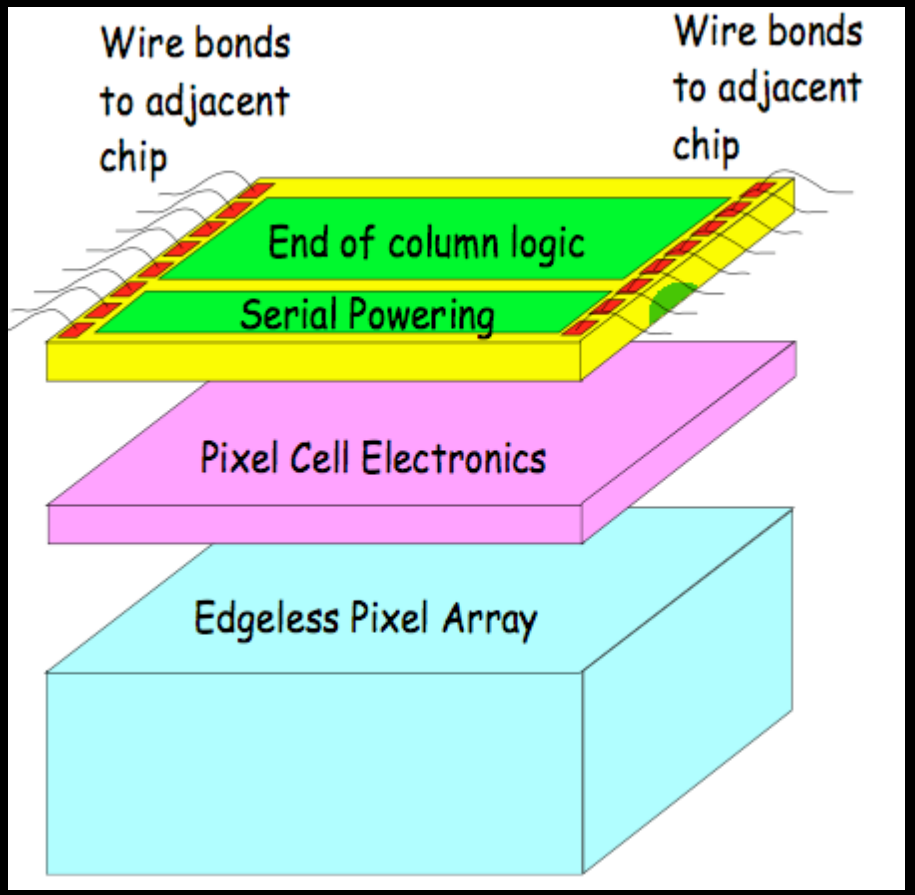
Initial tests indicate good noise performance

- instantaneous power = average power x 50-100) (achievable rise/fall times). 20W=>2kW
- At 1.5 V peak current ~666 A, 3 cm diam. of copper/side needed for 50mV drop

- Serial powering can reduce peak currents
  - –Individual ladder regulators
  - –V*n, I/n, ΔV tolerances relaxed with local regulation
  - –Being pursued for SLHC, primarily by ATLAS

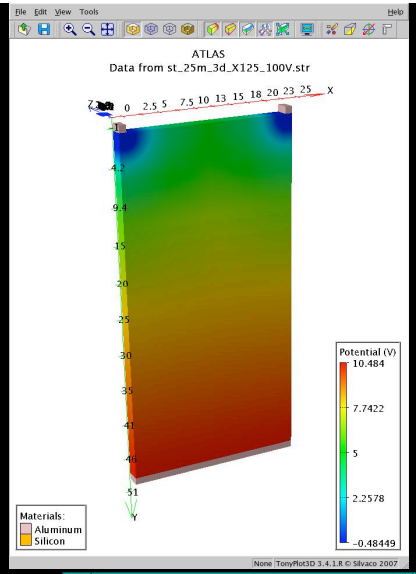
Possible Application to SLHC Pixels

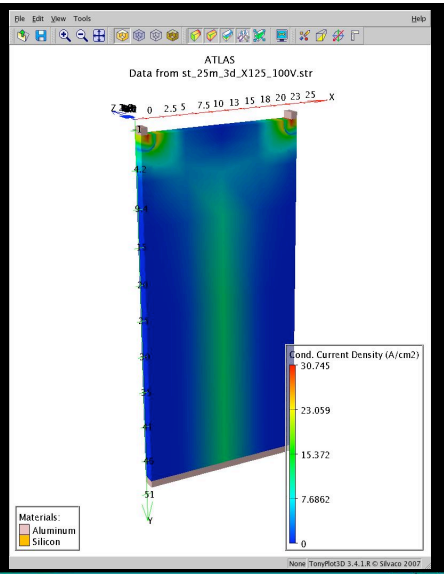
- Future pixel upgrades will look for
  - Less mass
    - Thinner sensors (lower V)
    - Less copper
  - More complexity
    - Higher readout speed
    - More functionality
  - May want smaller pixels for reduced noise to go along with smaller detector signal.
- Use serial powering for pixel Read Out chip.
- 3D allows for creative solutions, e.g.
  - Accommodates serial powering
  - Higher functionality/area
  - Thinner assemblies
  - Allows use of edgeless detectors

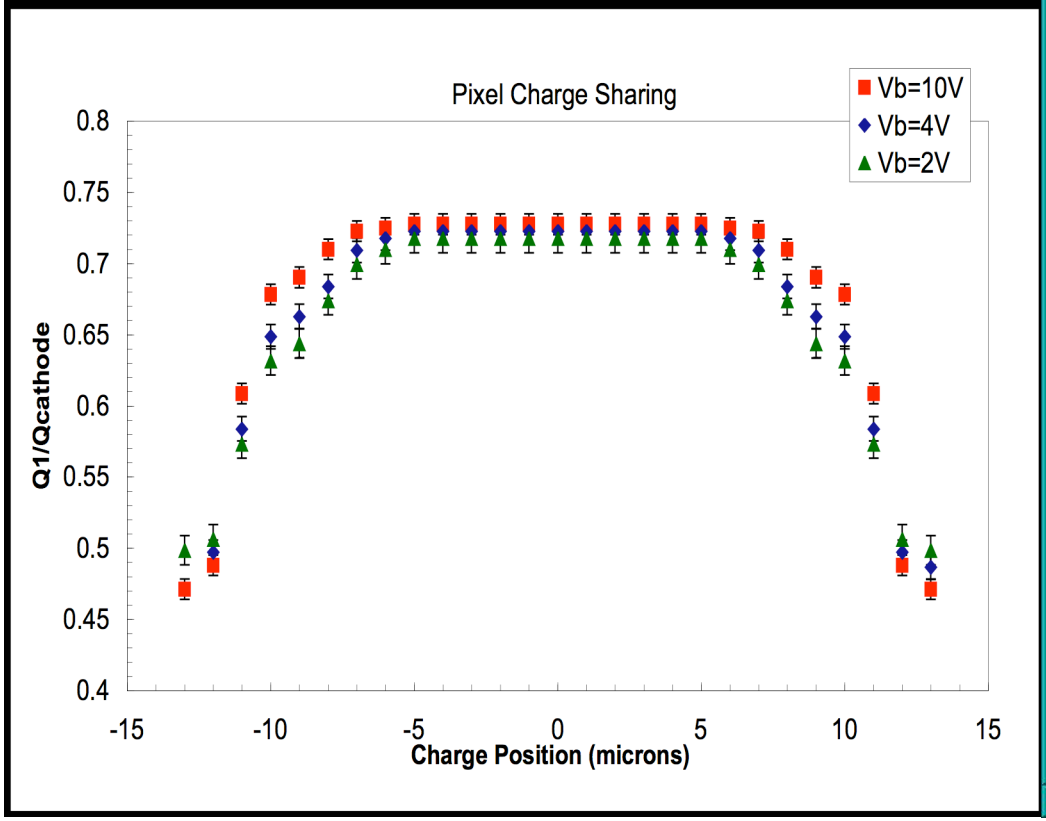


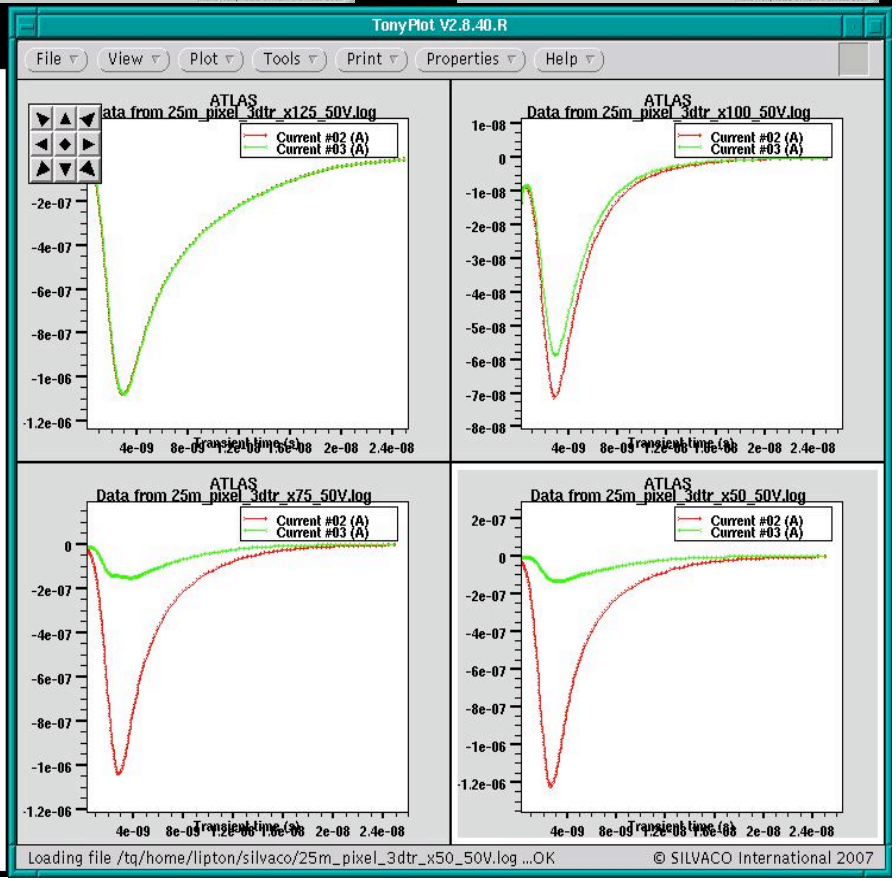
Simulation Tools

- We recently purchased Silvaco 3D device simulation tools - extremely useful to understand charge collection, back gate, and digital/analog coupling effects.









Conclusions

Vertically integrated (3D) electronics are becoming available

- Much of this technology is ideally suited to HEP vertex detectors
- Fermilab is exploring
  - Monolithic 3D Circuitry
  - SOI sensors
  - Wafer bonding technologies

  With focus on ILC, but also looking at applications in LHC, x-ray imaging, …
- The technology also has promise for X-ray detectors, electron microscope focal planes, imaging, and astronomy.