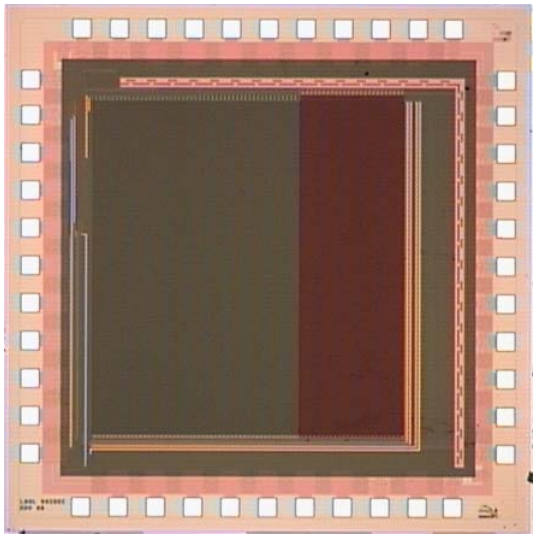
ALCPG07, Fermilab, October 22 - 25, 2007



SOI Sensor Development at LBNL

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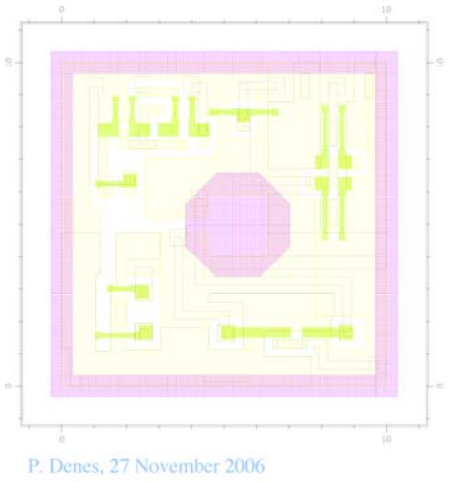
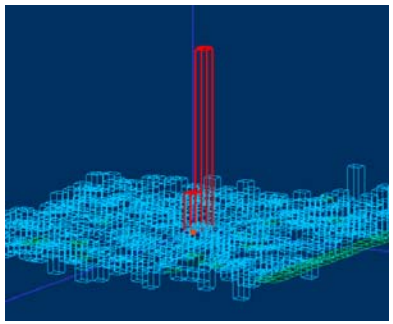
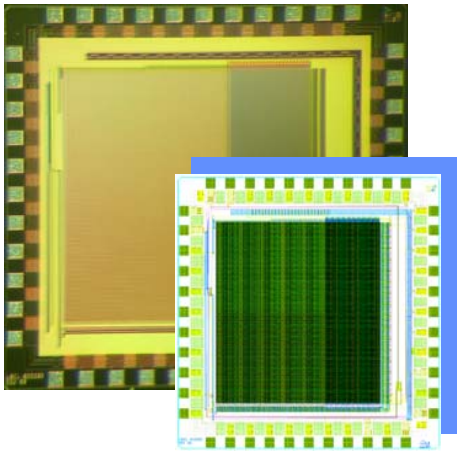
Outline

- Introduction: Description of the SOI sensor prototype
- Single transistor tests
  - Back-gating effect
  - Irradiation studies
- Analog pixel tests
  - Laser studies: charge collection properties
  - Leakage current
  - Depletion region
  - Beam test with 1.35 GeV electrons
- Digital pixel tests: Electron beam test results

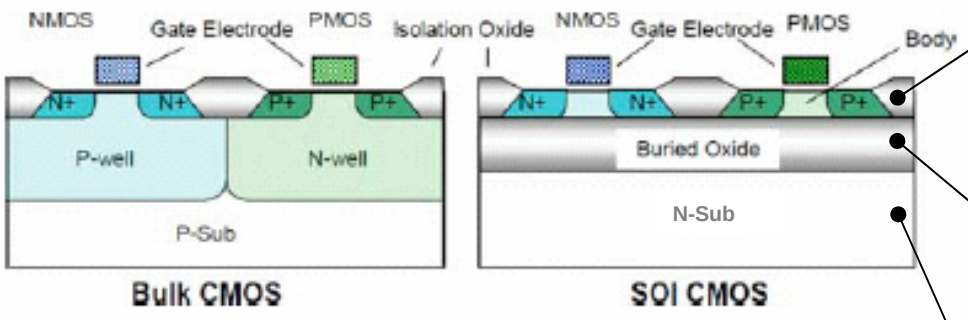






0.15 μm OKI FD-SOI process

Traditional CMOS vs. SOI structure



(courtesy Arai/KEK)

CMOS transistor layer: 40 nm

- n-type and p-type
- Can be fully depleted

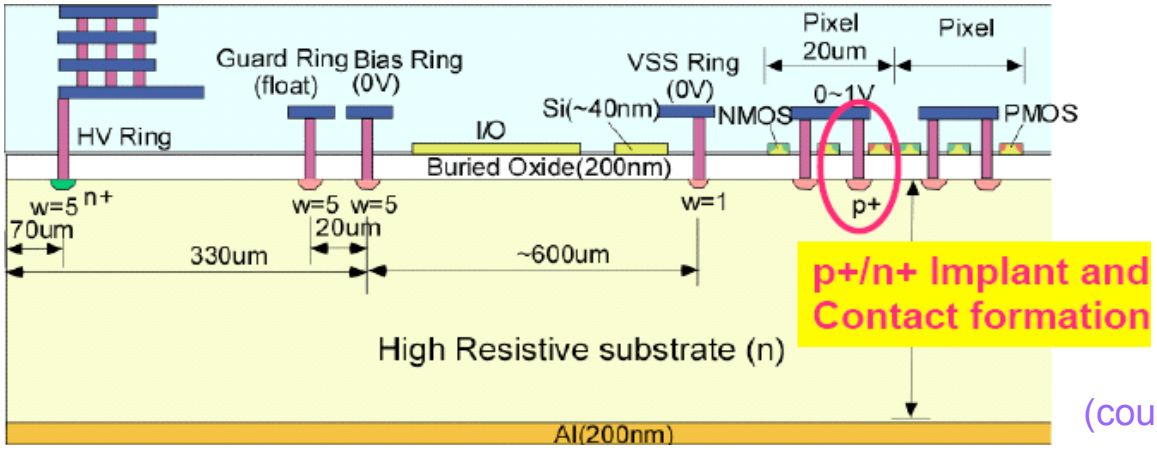
Buried oxide (BOX) 200 nm

- Isolates transistors from substrate

n-type silicon substrate: 350 μm

- Depletion voltage can be applied across substrate.

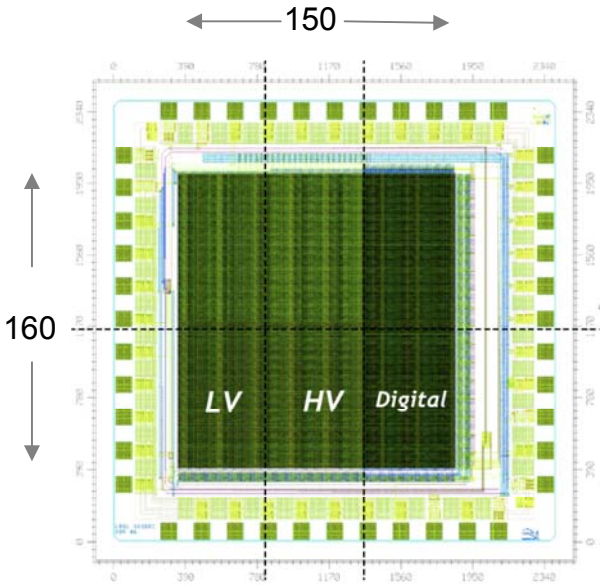
Example of an SOI sensor



(courtesy Arai/KEK)

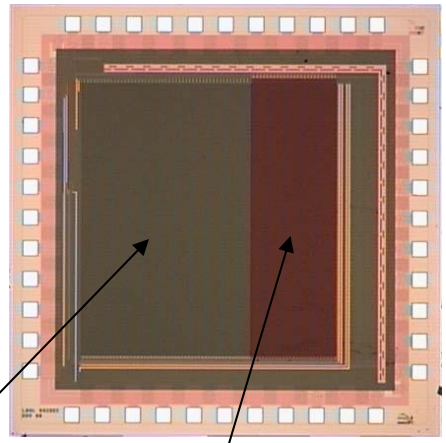
LDRD-SOI at LBNL

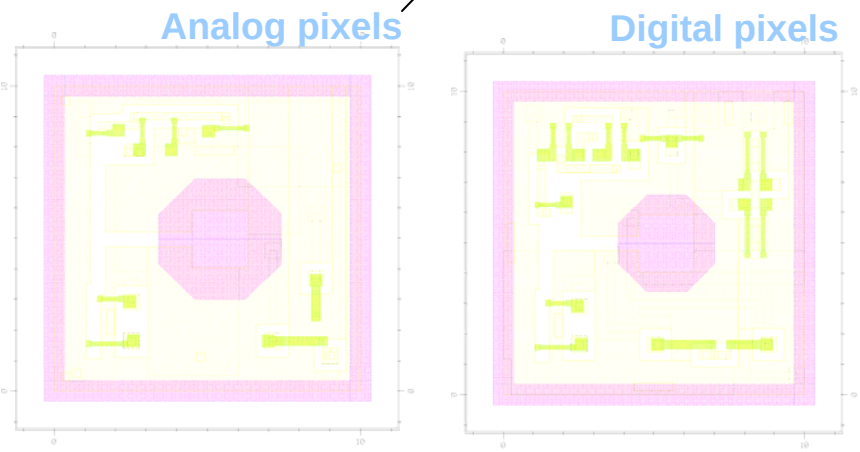
- Pixels:
  - –10 μm pitch
  - –160 x 150 matrix
  - –Diodes: 1μm to 4μm diameter
  - –Floating p-type guard-ring around each pixel



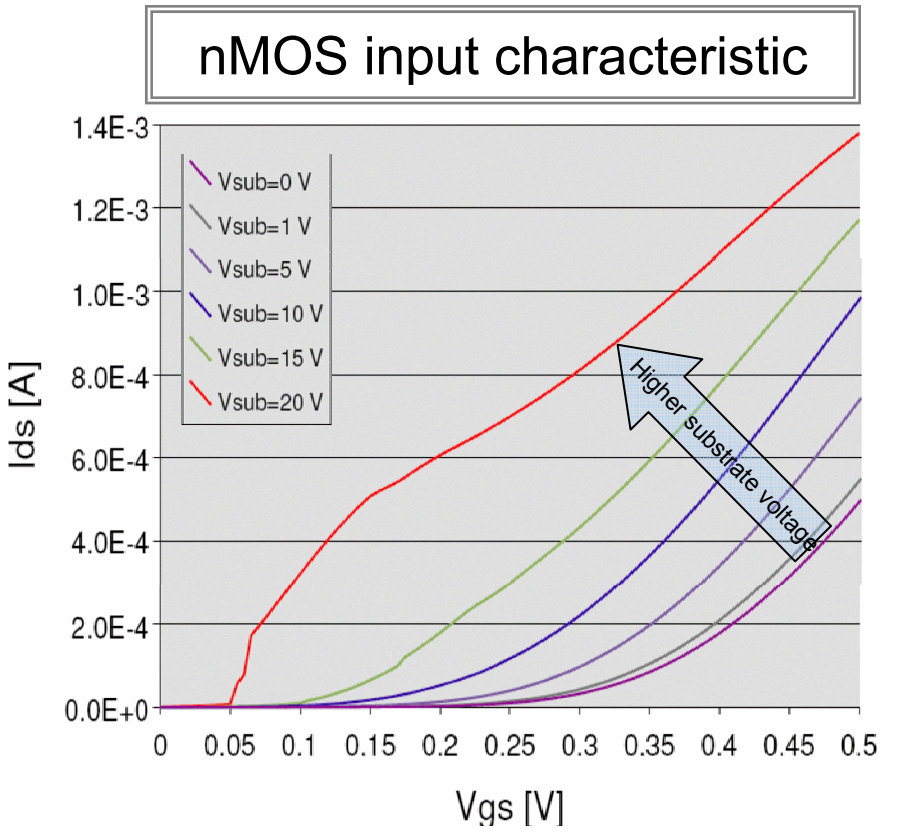
P. Denes, 27 November 2006

- 2 sections with **analog pixels**
  - Simple 3T structure
  - Biased at 1.0V (LV) and 1.8V (HV)
- 1 section with **digital pixels**
  - simple comparator and latch architecture
  - 15 transistors per pixel





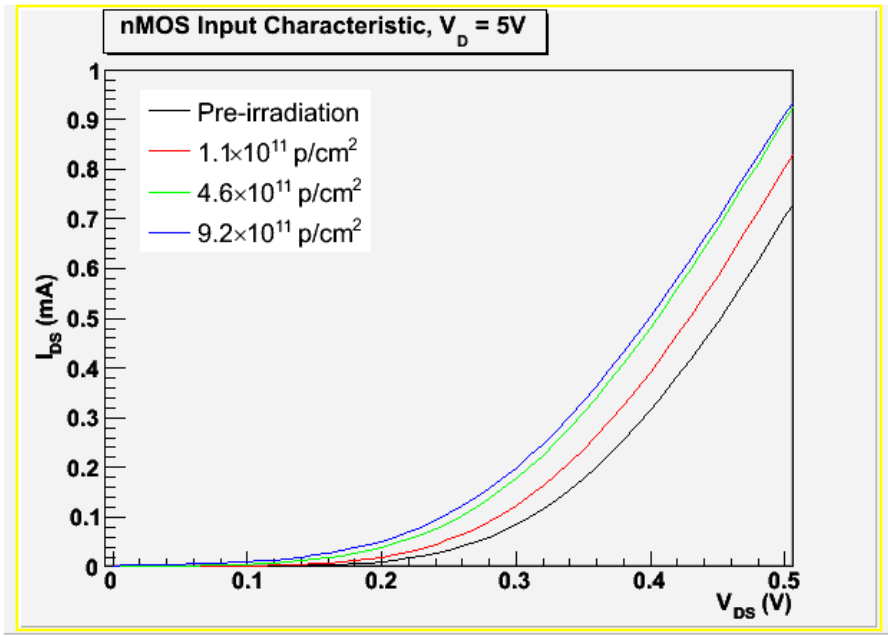
Single transistor tests

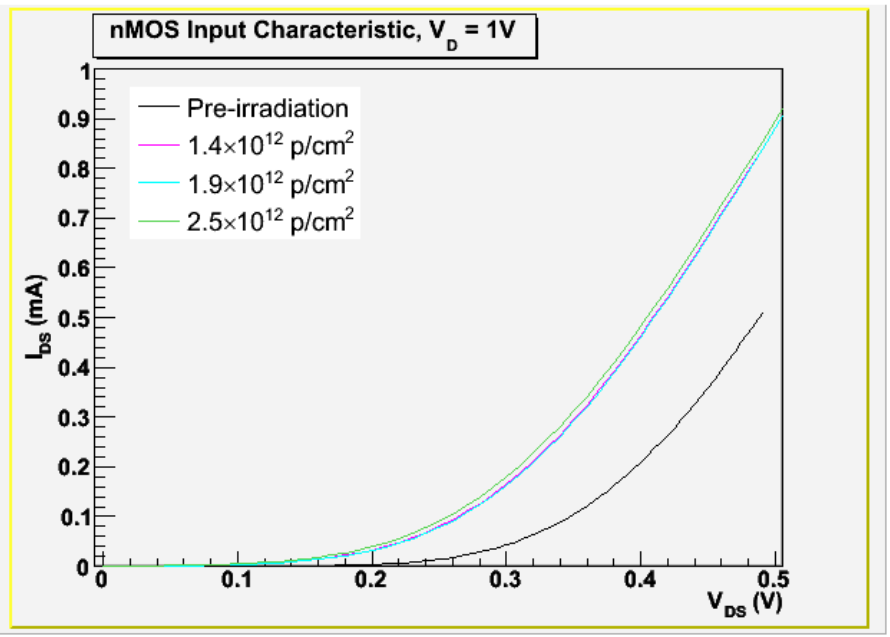


- 18 test transistors
  - p-type and n-type
  - 1.0V and 1.8V bias
  - Various body contacts: floating, source, gate
  - W = 50μm, L = 0.3μm
- Input and output characteristics measured for different depletion voltages
- Backgating causes a shift in threshold voltage as the substrate voltage increases.

Irradiation effects

- Irradiations performed at LBNL 88” Cyclotron
- **30 MeV protons**: fluence up to 2.5 x 10^{12} p/cm^2
  - Transistor measurements show a shift in threshold voltage throughout irradiation.
  - Charge trapping in BOX ⇨ increased backgating
- **1-20 MeV neutrons**: fluence up to 10^{11} n/cm^2
  - No change in transistor characteristics

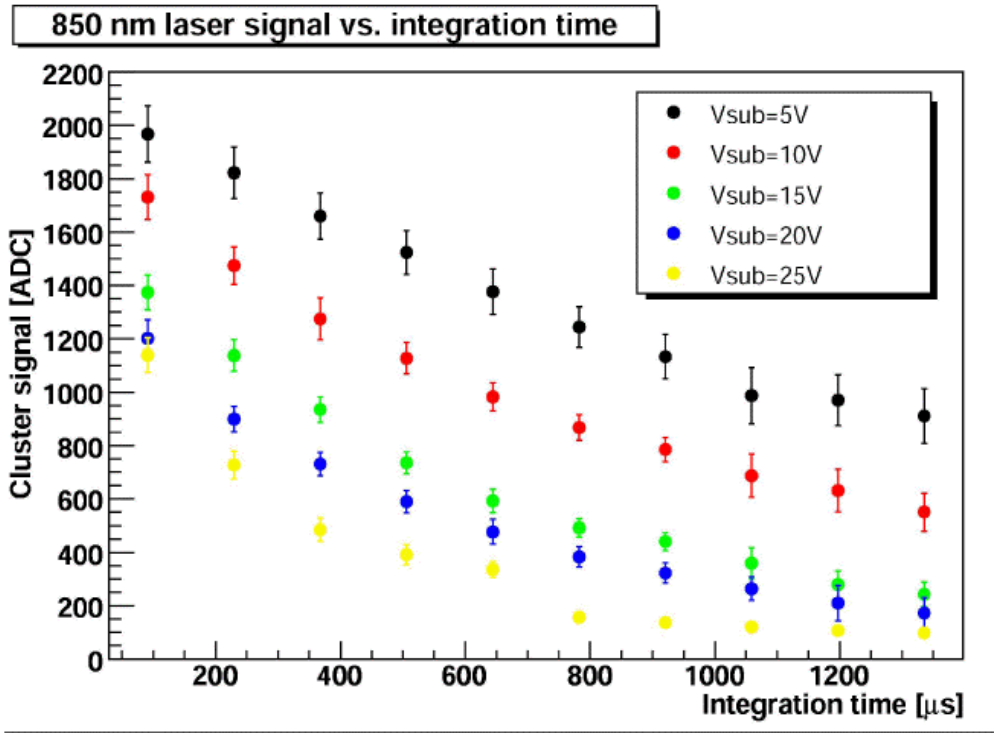




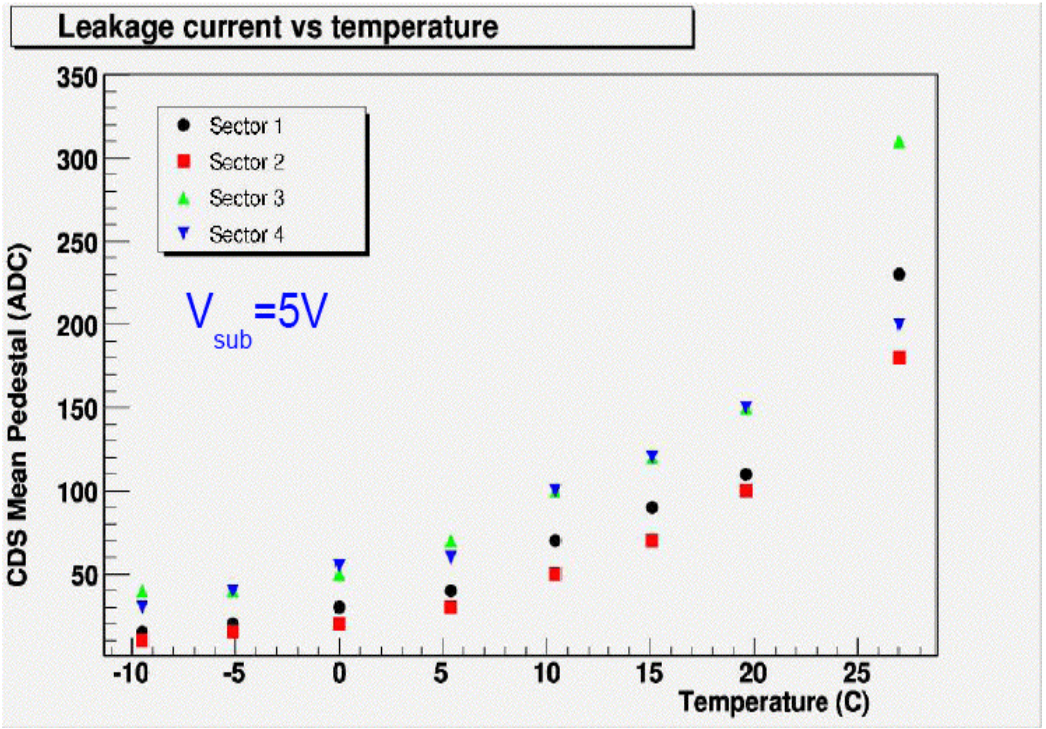
Laser studies

Charge collection properties of the SOI were tested with 850nm and 1060nm lasers focused to a ~20um spot.

- Signal loss was noted at long integration times.
  - More loss at large substrate voltages
  - Combined effect of leakage current and backgating
- To retain the entire signal, pixels must be read out immediately following charge collection.



Leakage current: Effects of cooling



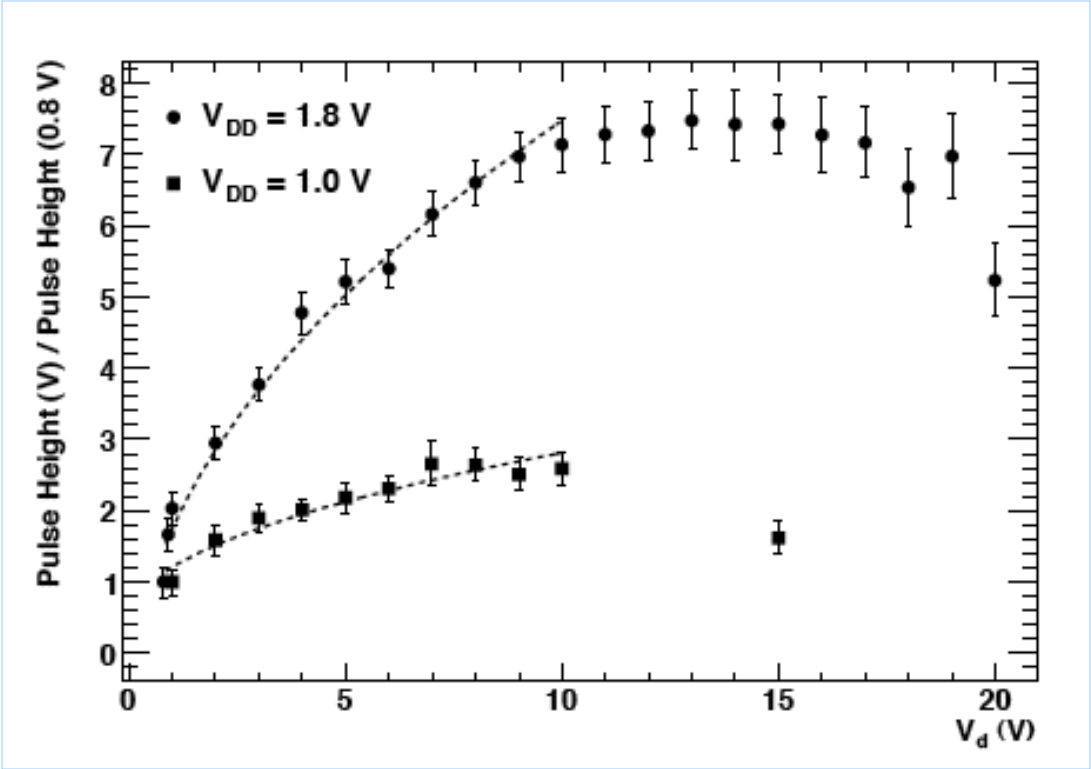
- Noise and leakage current were studied at temperatures down to -10°C
- Each pixel is read twice and the difference in ADC counts is computed --> correlated double sampling
- Fixed integration time between readings: 1.384 ms
- Decrease in leakage current at lower temperatures

Depletion region vs substrate voltage

- Depletion region thickness

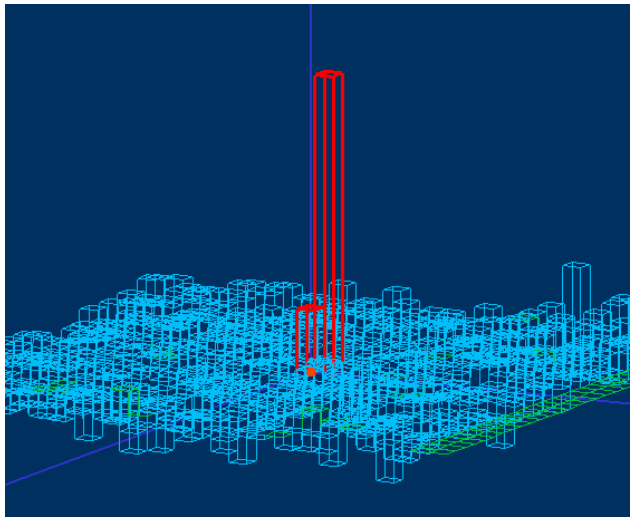
$$D \propto \sqrt{V_d}$$

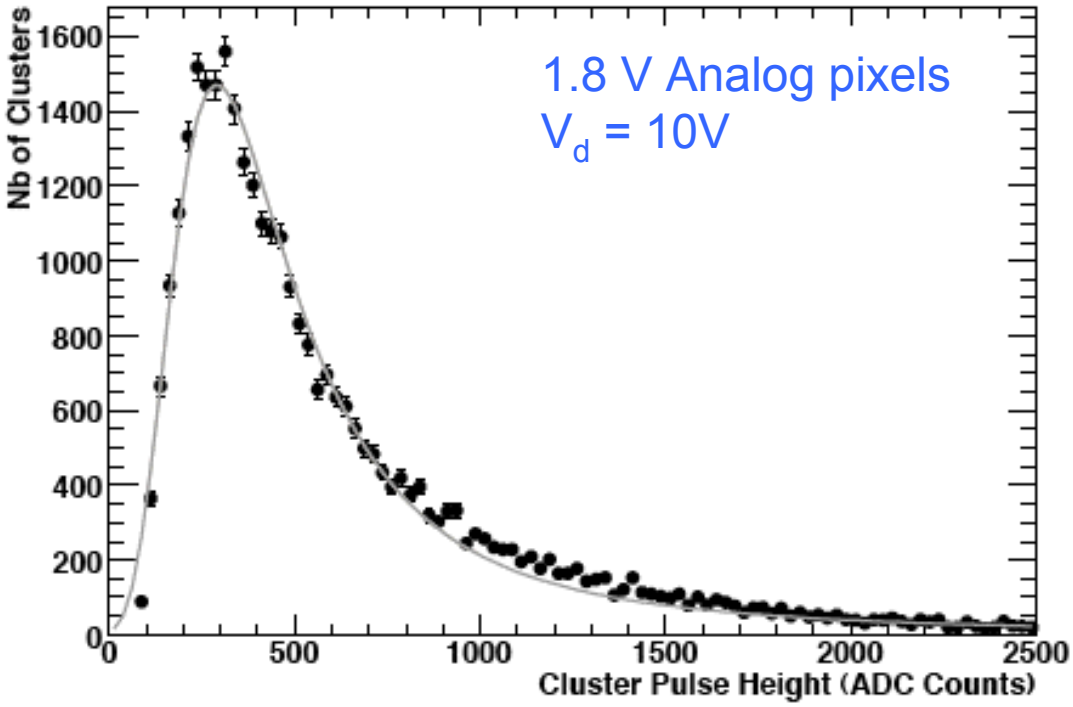
- 1060 nm laser signal for different substrate voltages
- Good agreement with expected depletion region up to V_d ~ 10V



Electron beam tests: Analog sectors

1.35 GeV electrons extracted from the booster ring of the Advanced Light Source (ALS) at LBNL.





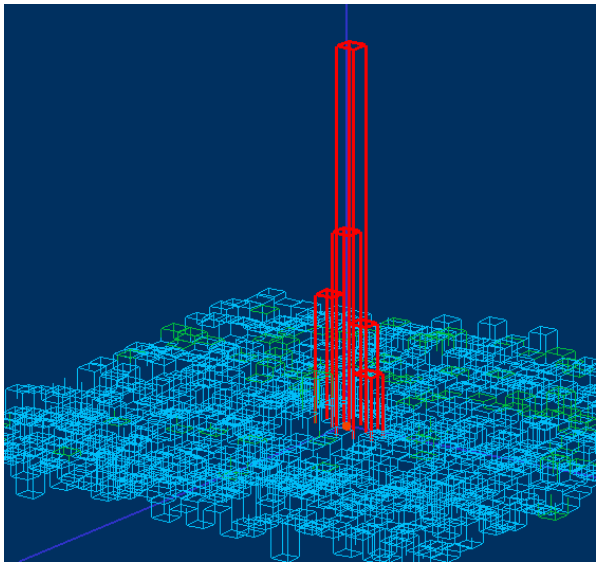
For comparison purposes, data were taken both with the beam on and off.

to appear in NIM A (2007)

Electron beam tests: Analog sectors

1.0 V Analog Pixels				
V_d (V)	Clusters / Spill (Beam on)	Clusters / Spill (Beam off)	Signal MPV (ADC Counts)	Average Signal/Noise
1	3.9	0.02	105	7.4
5	6.7	0.03	140	8.8
10	4.4	0.03	164	8.1
15	1.4	0.02	123	6.5

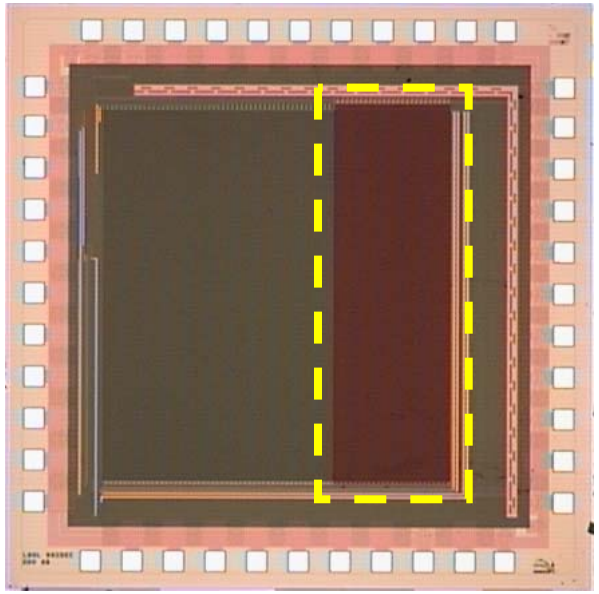
1.8 V Analog Pixels				
V_d (V)	Clusters / Spill (Beam on)	Clusters / Spill (Beam off)	Signal MPV (ADC Counts)	Average Signal/Noise
1	9.7	0.05	132	8.9
5	14.0	0.12	242	14.9
10	7.8	0.20	316	15.0
15	3.9	0.01	301	13.6



to appear in NIM A (2007)

Digital pixels

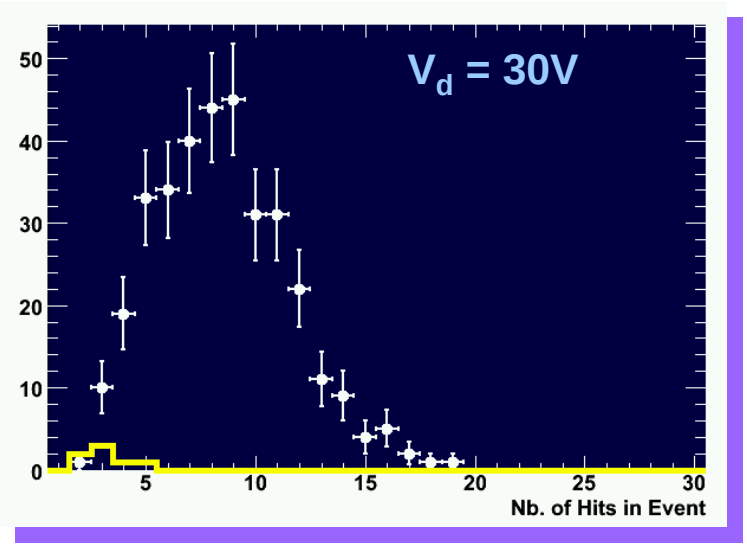
- Structure
  - In-pixel comparator plus latch
  - Adjustable threshold
  - No internal amplification
    - No static power dissipation
  - Digital circuitry active only during sampling



- Readout
  - No CDS or pedestal needed
  - Adjustable integration time
    - Reduced problem of charge loss due to leakage current

Digital pixels: ALS results

- Noticeable charge collected **only** at high substrate voltages (but not too high!)
  - Analog threshold is affected by back-gating
  - Large depletion: increased charge signal
  - At 25-30V, these effects seem to combine for best detection capabilities.



- Cluster multiplicity decreases with increasing substrate voltage

- Single transistor test data collection in progress
  - Model back-gating effect
  - Understand effect on pixel threshold

V_d (V)	Clusters/Evt w/ beam	Clusters/Evt w/o beam	<Nb Pixels>
20	3.62	0.04	1.78
25	5.81	0.04	1.32
30	8.31	0.04	1.26
35	1.60	0.01	1.14

Conclusions and Plans

- First OKI 0.15μm FD-SOI pixel prototype designed and successfully tested at LBNL
  - Analog and digital pixel detection capabilities have been demonstrated with infrared lasers and 1.35 GeV electrons
    - Up to 10-15V for analog pixels
    - 20-30V for digital pixels
  - Backgating effects become significant at high substrate voltages and after irradiation with protons

- Further electron beam tests at the ALS under way
  - Pairing with a 50 μm thin MIMOSA-5 sensor to normalize flux and correlate hits

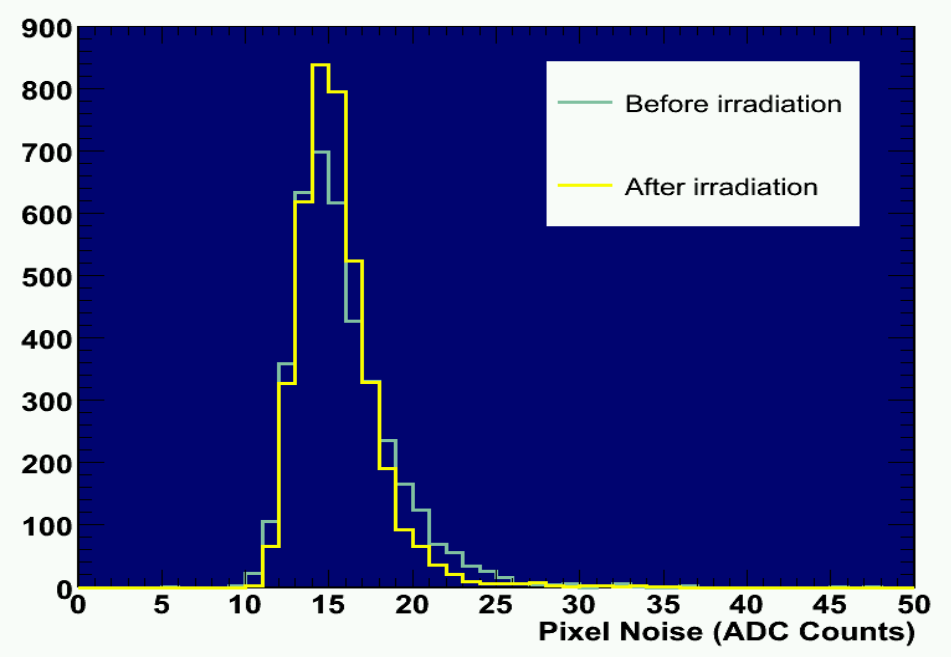
- Detailed laser studies
  - Consistency of threshold across digital pixels
  - Uniformity scan of analog pixels

- New prototype submission in December/January in optimized 0.20μm process
  - Repeat simple architecture + added functionalities

Backup Slides

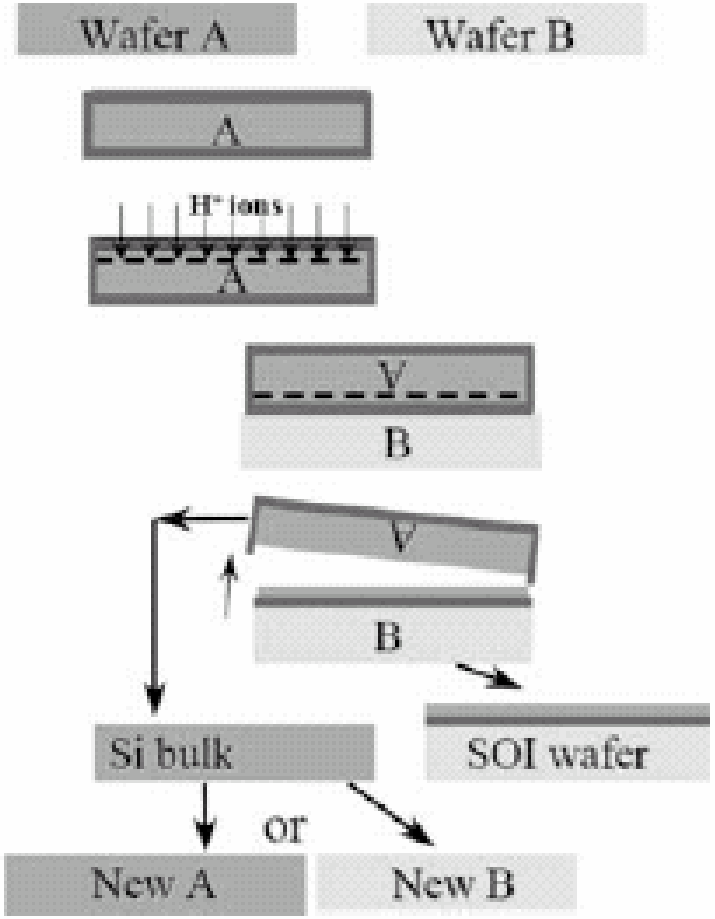
Neutron irradiation

- Neutron irradiation:
  - Fluence up to 10^{11} n/cm^2
  - 1-20 MeV neutrons
- Readout at 6.25 MHz pixel clock



UNIBOND Process

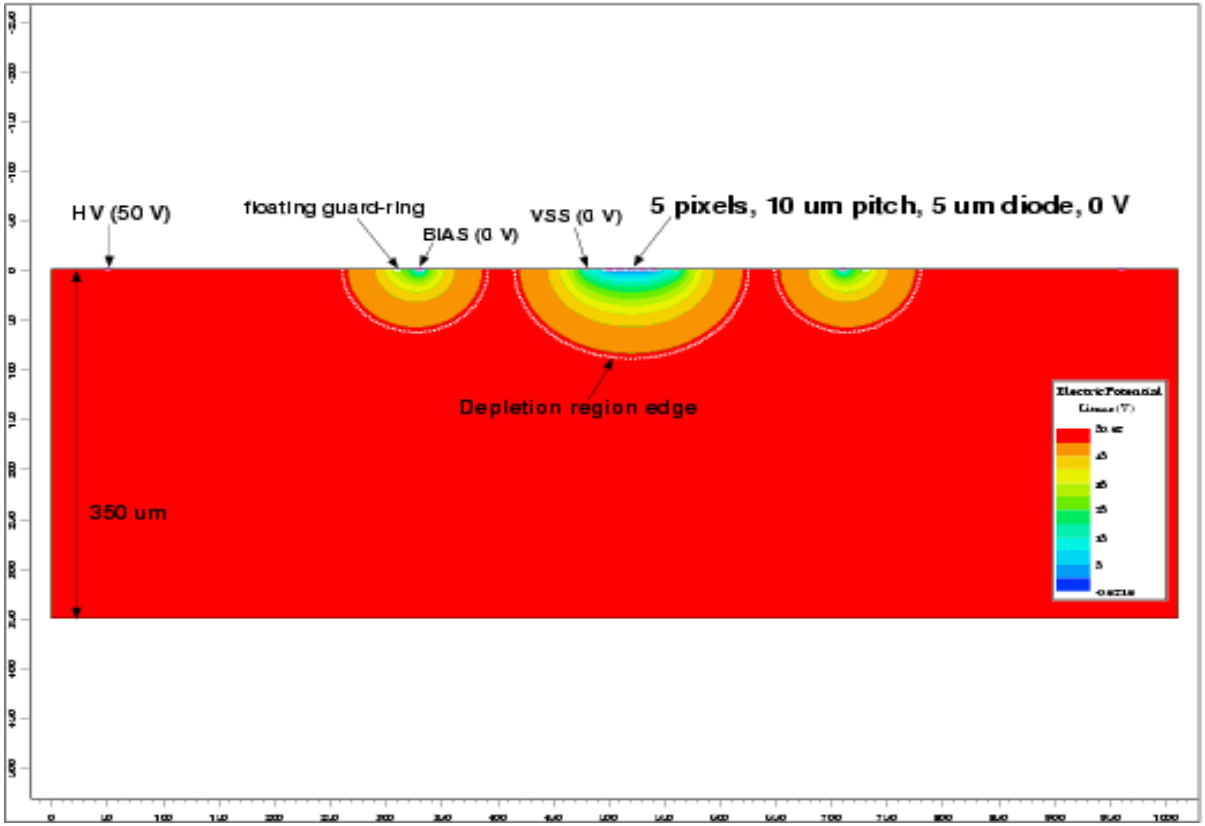
- Initial silicon wafers A & B
- Oxidation of wafer A to create insulating layer
- Smart Cut ion implantation induces formation of an in-depth weakened layer
- Cleaning & bonding wafer A to the handle substrate, wafer B
- Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
- Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
- Split-off wafer A is recycled, becoming the new wafer A or B



Y. Arai, "Electronics and Sensor Study with the OKI SOI process", TWEPP-07

TCAD Simulations

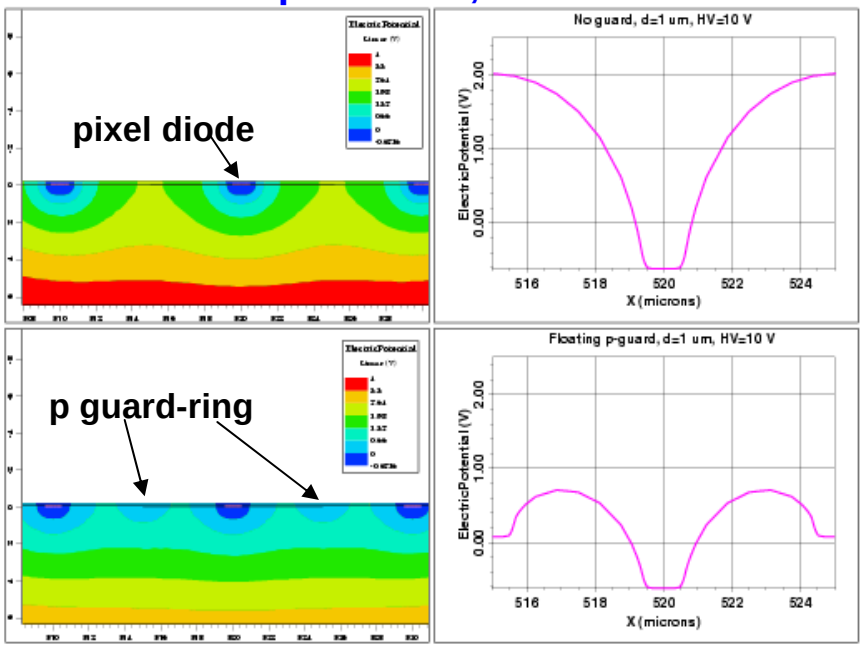
See D. Contarato's talk at LCWS 2007



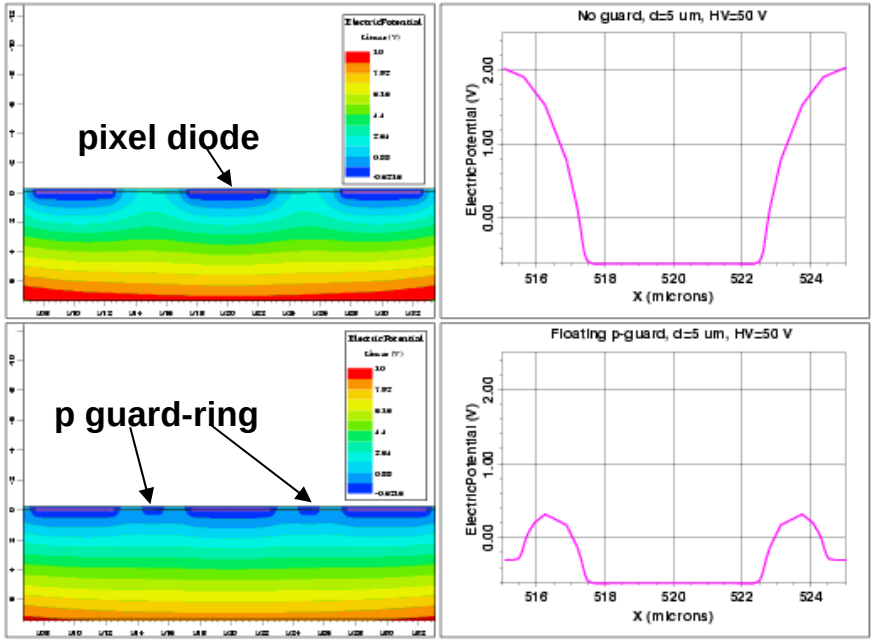
- Simulation performed with Synopsys TCAD (Taurus Device)
- 2D model of 5 pixel cluster (10 μm pixel pitch) and substrate contact regions
- 350 μm thick substrate, n-type silicon (6×10^{12} cm^{-3}); 200 nm buried oxide
- Different diode sizes (1×1 μm^2 and 5×5 μm^2)

Surface potential, choice of pixel guard-ring

1×1 μm² diode, HV=10 V

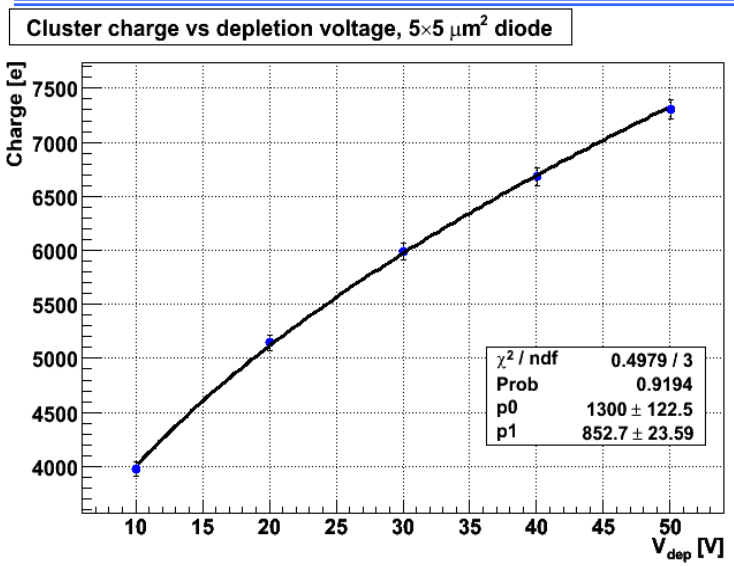


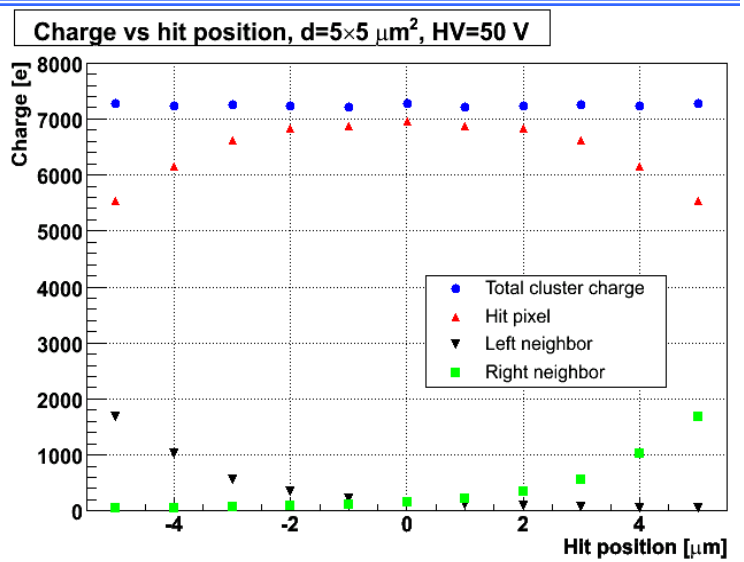
5×5 μm² diode, HV=50 V

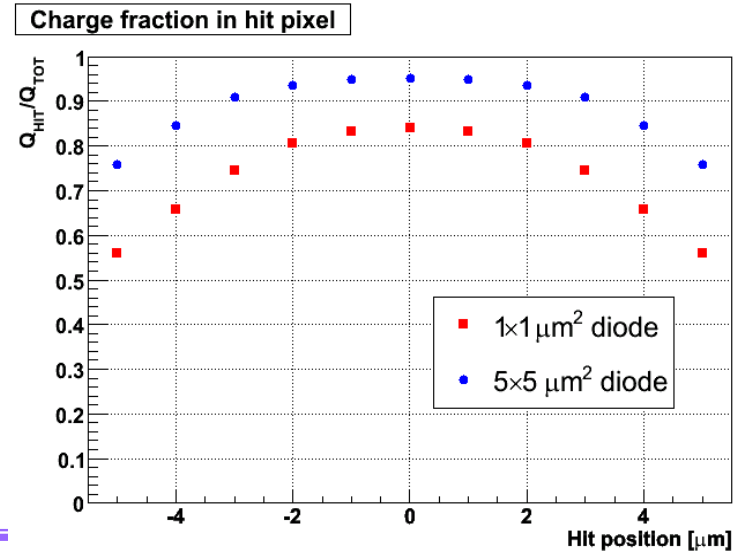


- Pixel surface potential for different diode sizes and depletion voltages
- Potential in-between pixels too high, especially for smaller diode size
- Add floating p-guard structure (1 μm wide) to keep potential low and limit back-gate effects on MOS transistors on top of buried oxide

Charge collection simulation







- Simulate passage of m.i.p. (80 e-h/μm) and charge collection in 5 pixel cluster
- Study collected signal as a function of depletion voltage and of track position within hit pixel
- Total cluster signal ~constant as a function of position within hit pixel
- Most of the charge is collected in hit pixel, expect larger cluster size for smaller diode pitch

N and P substrate connections