Development of FPCCD Readout ASIC

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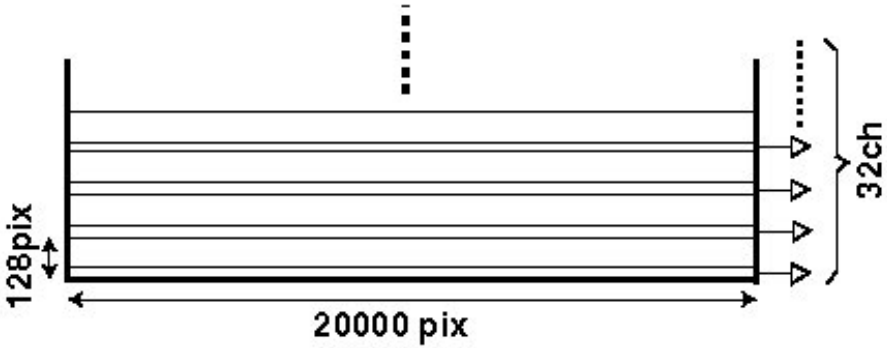
Introduction

FPCCD vertex detector

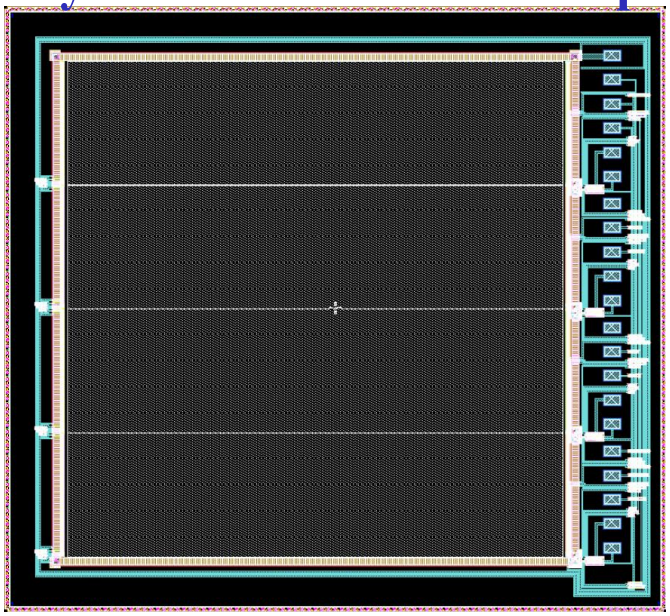
- Pixel size : 5μm
- Thickness : 15μm
- Signal level : ~500e for large angle
- Readout channel : 16 or 32 ch
  - ~20,000 x 128 pix/ch



Test-sample will be delivered in the end of 2007.

- Pixel size : 12μm
- Readout channel : 4ch
  - 512 x 128 pix/ch

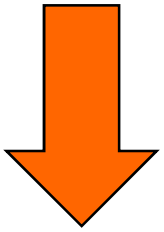
Layout of FPCCD test-sample



Motivation to develop readout AISC

Motivation to develop readout ASIC

- The FPCCD test-sample will be delivered in the end of this year.
- The FPCCD has a large number of readout pixels.
  - Test sample : 512 x 128 pix/ch
- There is no readout ASIC suitable for the FPCCD.



Readout ASIC for the FPCCD is necessary.

- For FPCCD test-sample
- To establish readout technique

Requirement to the readout ASIC

Requirement to the readout ASIC

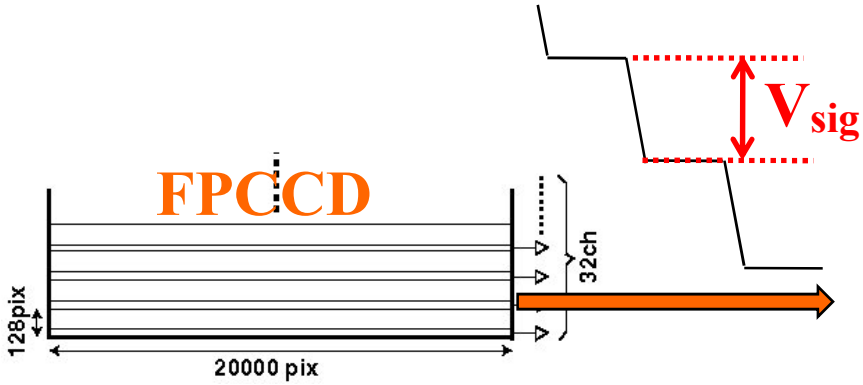
- All elements to operate and read FPCCD are contained in one chip.
- Readout rate : >10 Mpix/sec
  - [20000 x 128 pix]/[0.2 s]
- Noise level of the ASIC : < 30 electrons
  - Required total noise level including the CCD : <50 electrons
  - Noise level of FPCCD : ~30 electrons
- Power consumption : < 6 mW/ch
  - The power consumption in a cryostat should be <100 W.
  - Required total power consumption : <16 mW/ch (~100W/6000ch)
  - CCD : ~10mW/ch

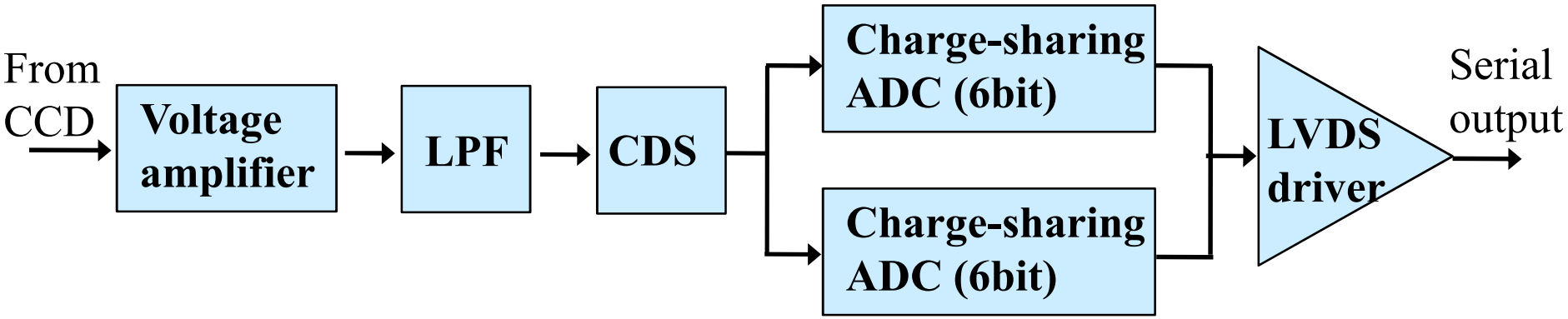
To achieve these requirement, readout ASIC is designed.

Design concept of readout ASIC

ASIC elements

- Voltage amplifier
- LPF (Low-pass filter)
- CDS (Correlated double sampling)
- ADC
  - 2 charge sharing ADC are used alternatively to achieve 10Mpix/sec.
- LVDS driver



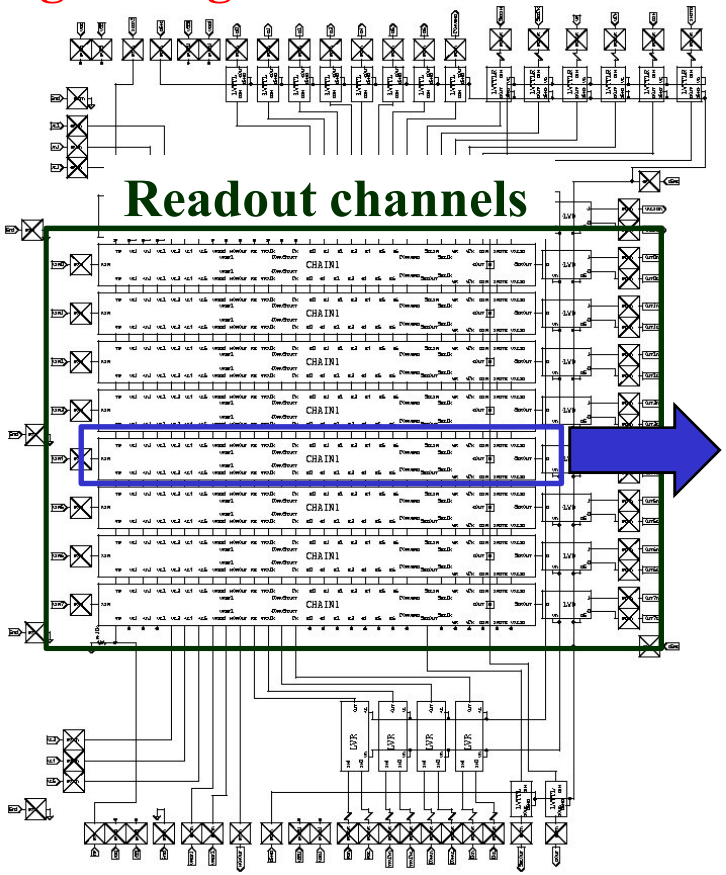


The design was optimized with SPICE simulation.

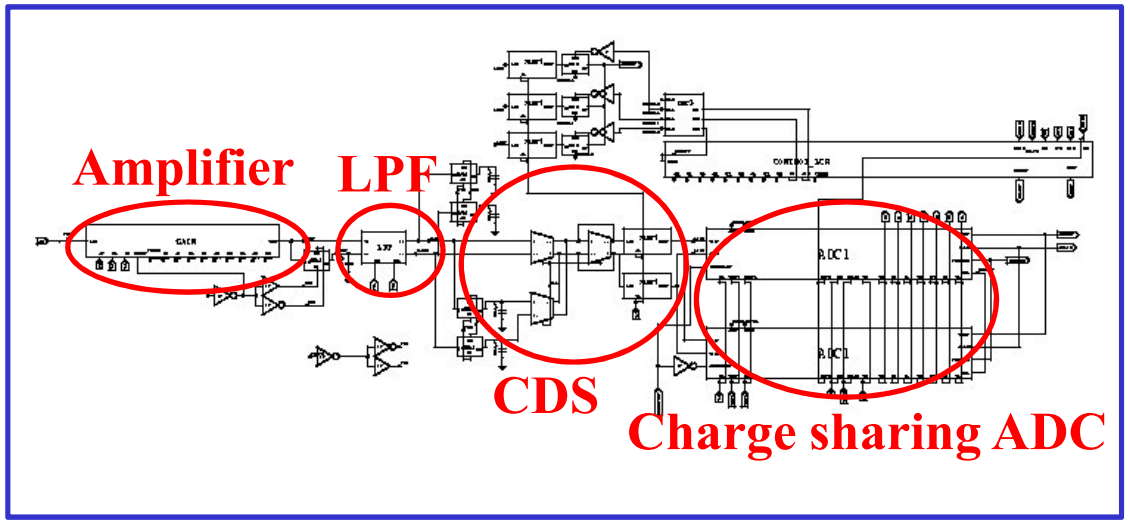
Design optimization with SPICE

- The SPICE simulation was applied to design the readout ASIC.
- The design was optimized for 0.35 μm process by TSMC.

Logic design of the readout ASIC



Logic design of the readout channels

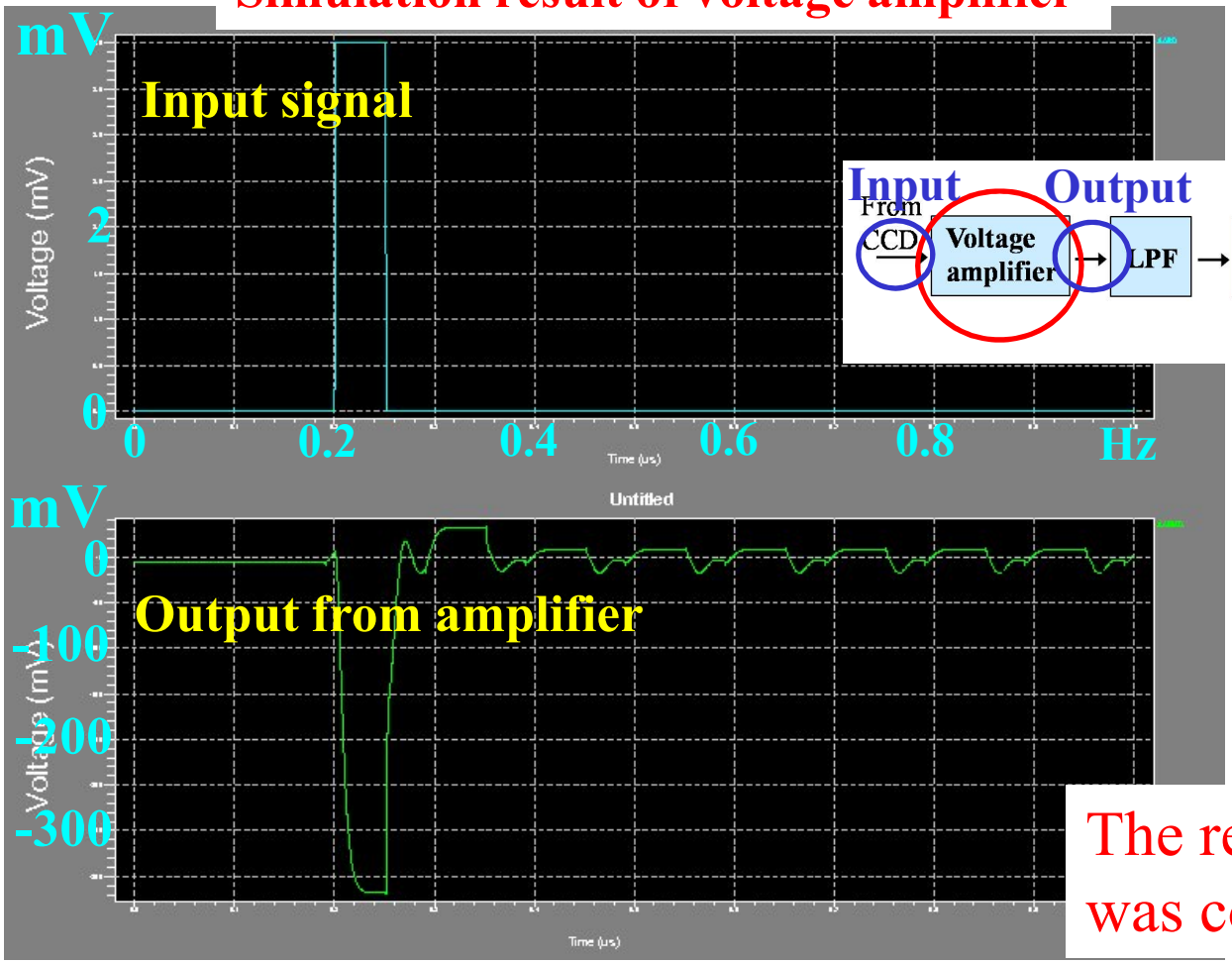


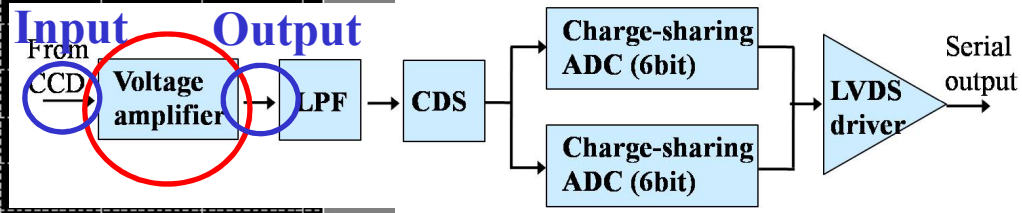
Each elements were check with simulation.

Voltage amplifier

- The amplifier was designed to have the gain of 10~100.
- The gain can be adjustable by changing bias current.

Simulation result of voltage amplifier

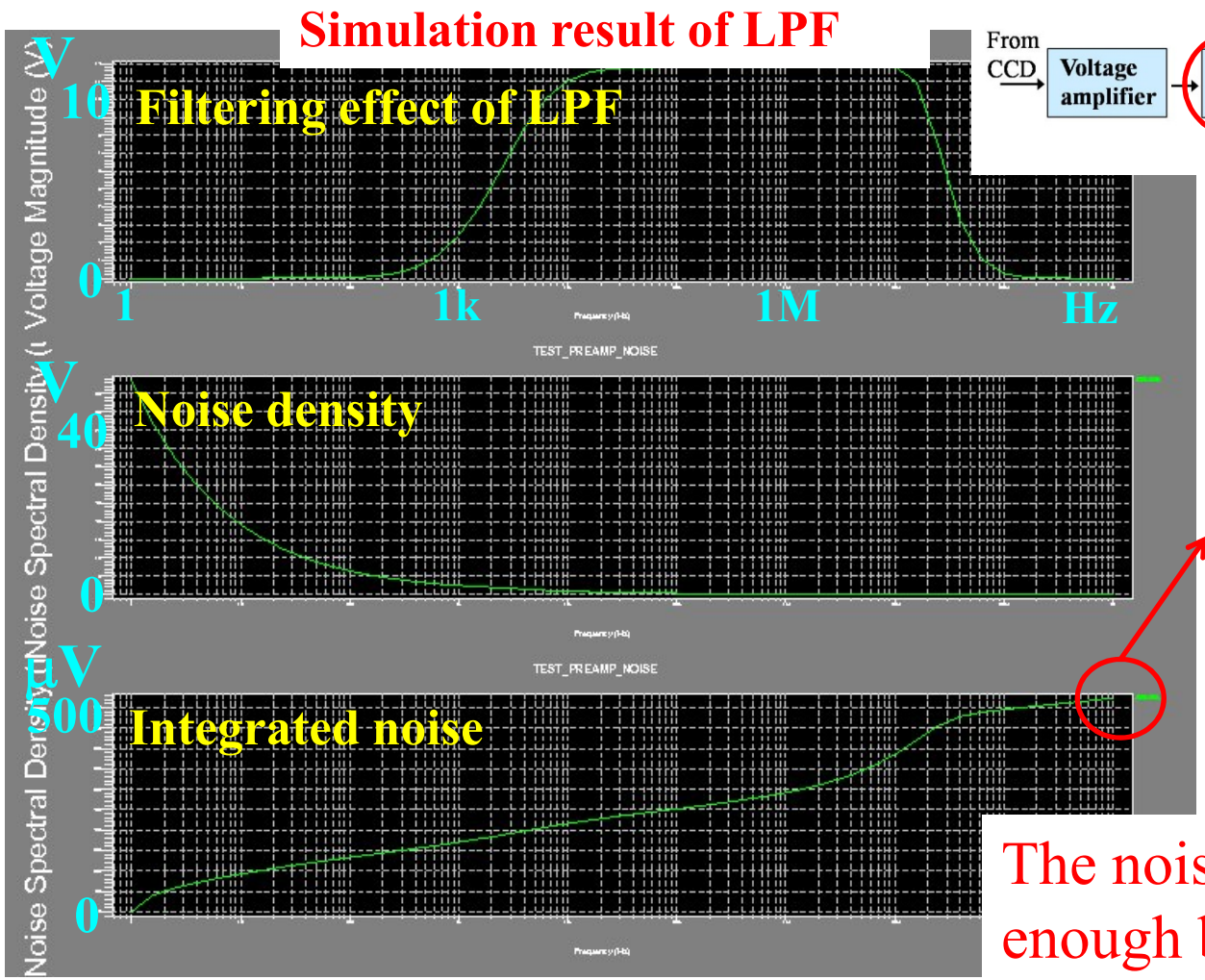


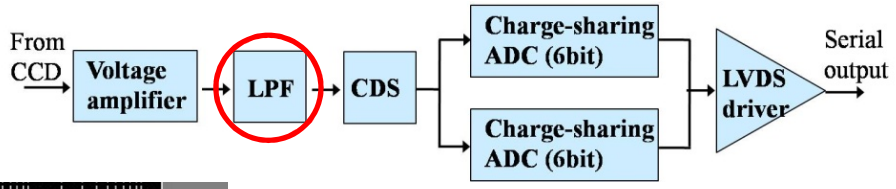


The response of the amplifier was confirmed.

Low Pass Filter

- Response of the LPF was investigated by noise analysis of SPICE.
- Adjustability of band-width was checked.





Initial noise level

~ [500μV]/[50V/e]

~ 10 e

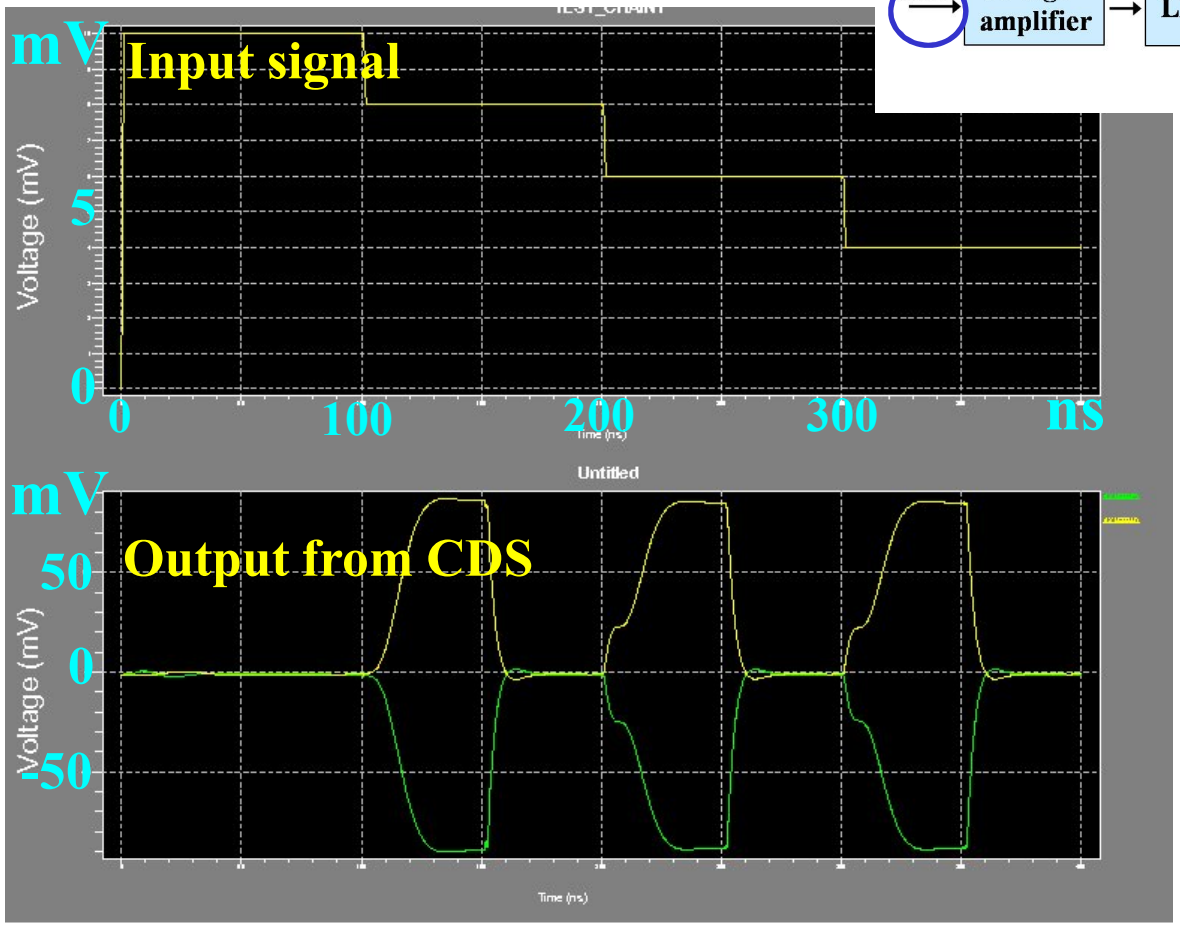
- Voltage gain : 50μV/e

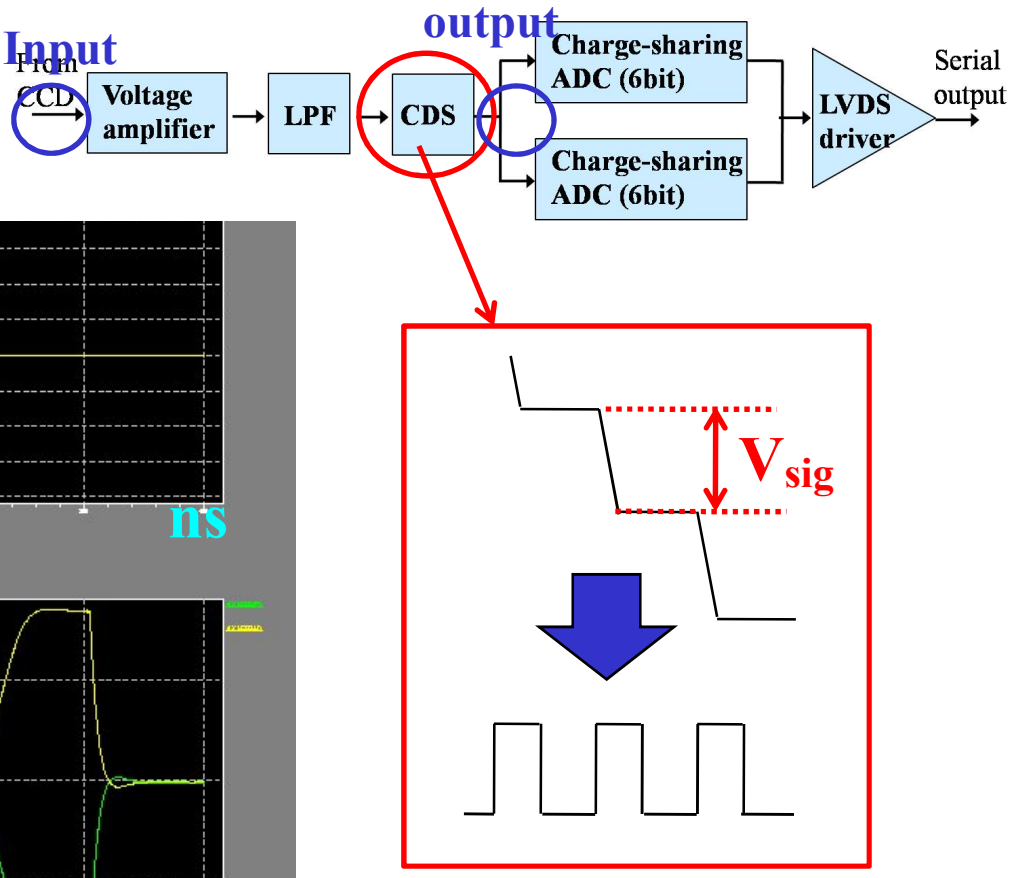
The noise level is expected to be enough below our requirement.

Correlated double sampling circuit

CDS obtains the voltage difference corresponding to charges contained in one pixel.

Simulation result of CDS



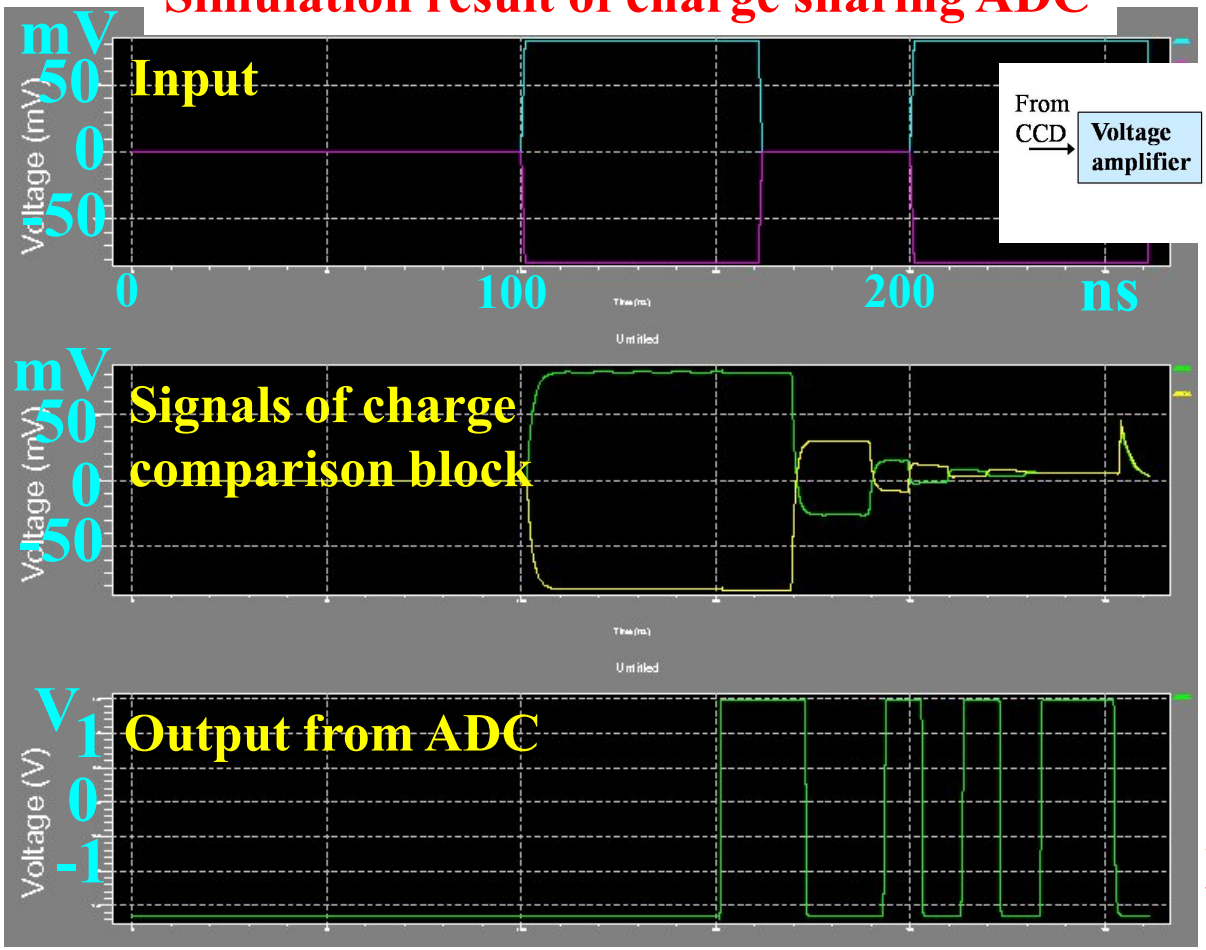


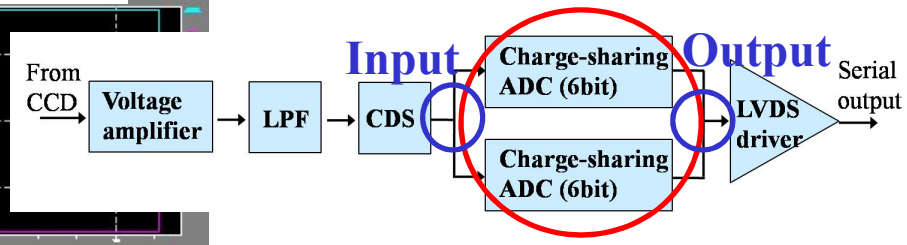
CDS circuit work correctly.

Charge sharing ADC

Charge sharing ADC performs A/D conversion, comparing stored charges in capacitors.

Simulation result of charge sharing ADC





A/D conversion can be performed with 10MHz.

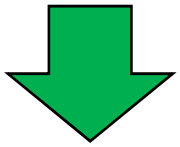
Response of all ASIC elements was confirmed.

Expected performance

Expected performance

- Readout rate : 10 Mpix/sec ⟶ **OK!**
  - Data conversion rate : 10MHz (= 5x2 MHz)
  - 260 ms/ch : [20000 x 128 pix/ch] x [10^{-7} s/pix]
- Power consumption < 5 mW/ch ⟶ **OK!**
  - Charge-sharing ADC realizes low power. (~10 μW)
- Noise level : ~10e ⟶ **OK!**
  - Estimation with SPICE simulation.

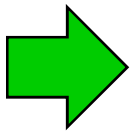
The performance will satisfy our requirement.



ASIC layout was ordered to a company (Digian technology).

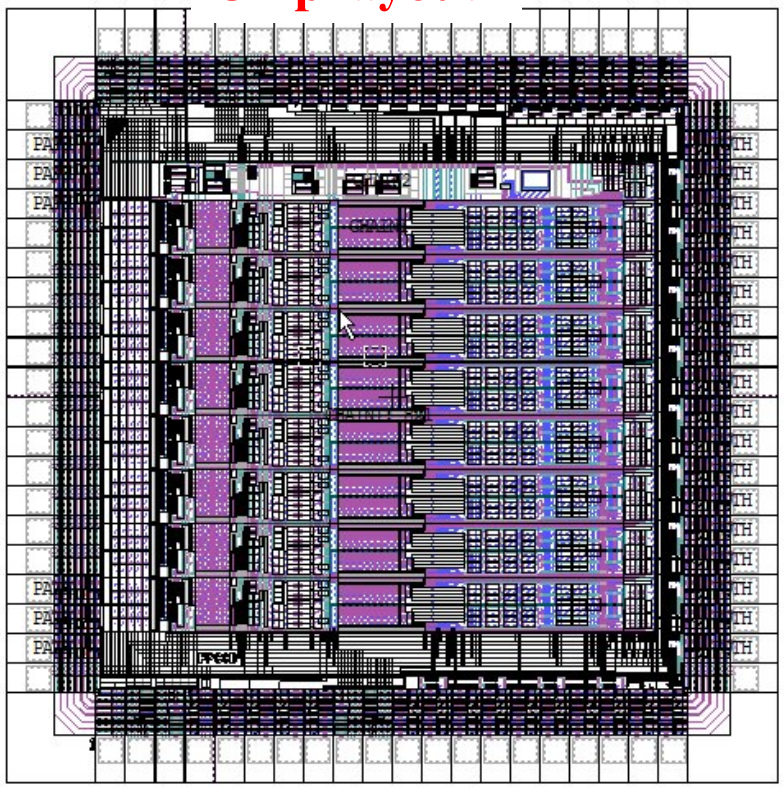
Layout check

- ASIC layout made by a company was checked.
- SPICE simulation was performed with layout data.

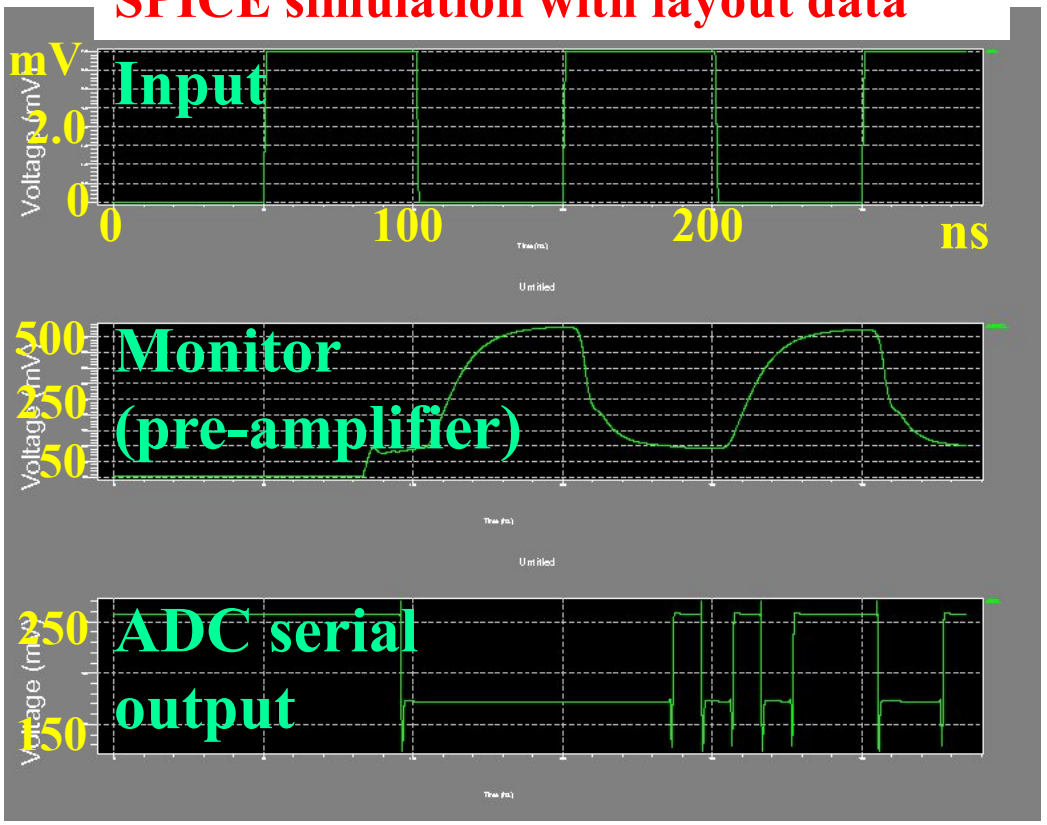


- The production was ordered to MOSIS.
- The ASIC will be delivered on Dec.

Chip layout



SPICE simulation with layout data



Specification of readout ASIC

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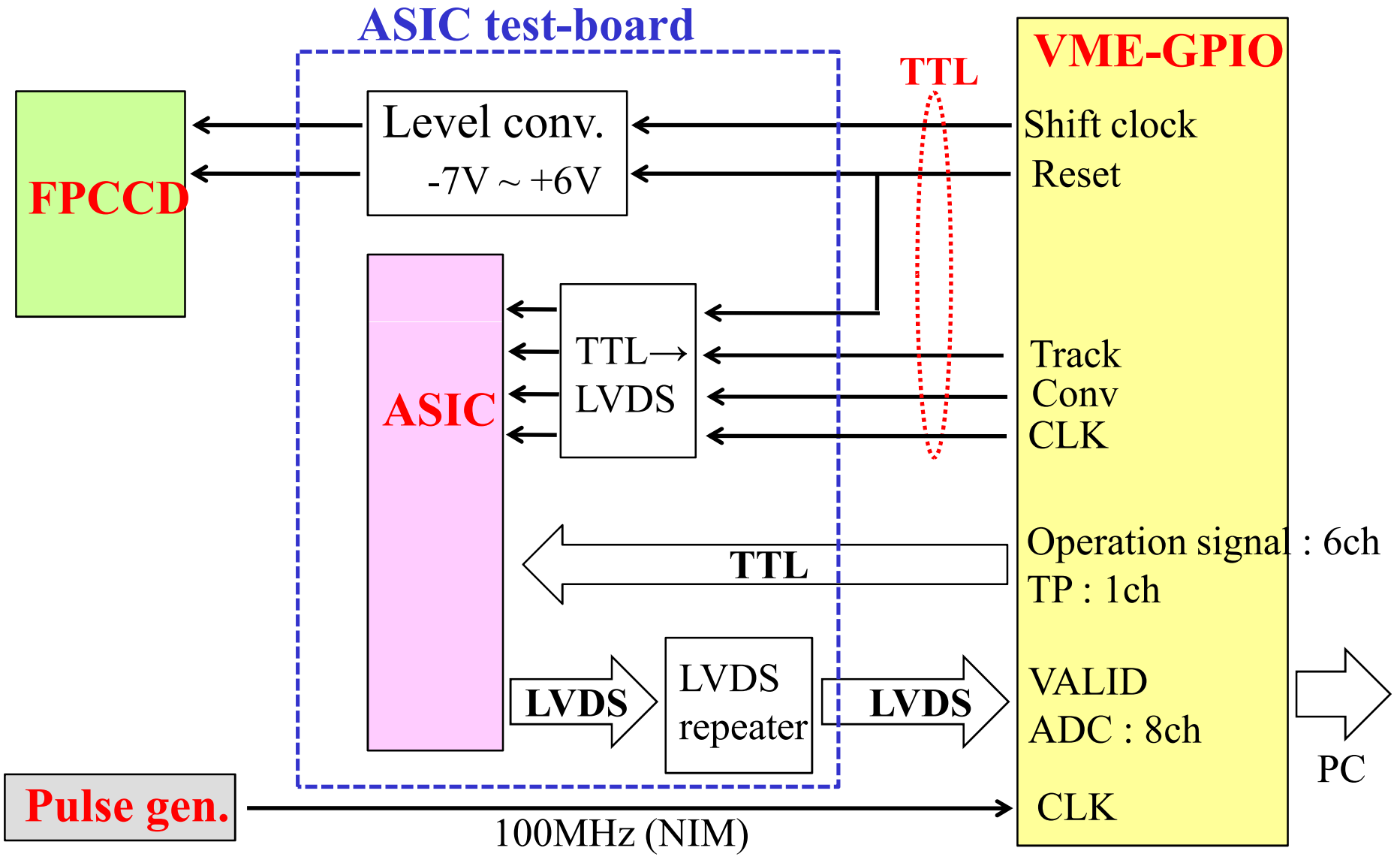
- 0.35 μm process by TSMC
- Size : 2.85 x 2.85 mm^2
- # of pad : 80
- # of signal channels : 8
- AD conversion rate : 10 MHz (=5MHz x 2)
- Clock frequency : 100 MHz
- Data width : 6bit + sign bit
- Power rail : ±1.65 V
- Analog gain : adjustable
- Frequency bandwidth : adjustable
- Interface : LVDS/LVTTL

Summary

- Development of readout ASIC for FPCCD was started.
- The ASIC design was optimized with SPICE simulation.
  - The performance will satisfy our requirements.
- The layout was made by a company (Digian technology).
  - The response was checked by SPICE simulation with layout data.
- The readout ASIC will be delivered on December.

Block diagram of Test-bench



ILC-FPCCD

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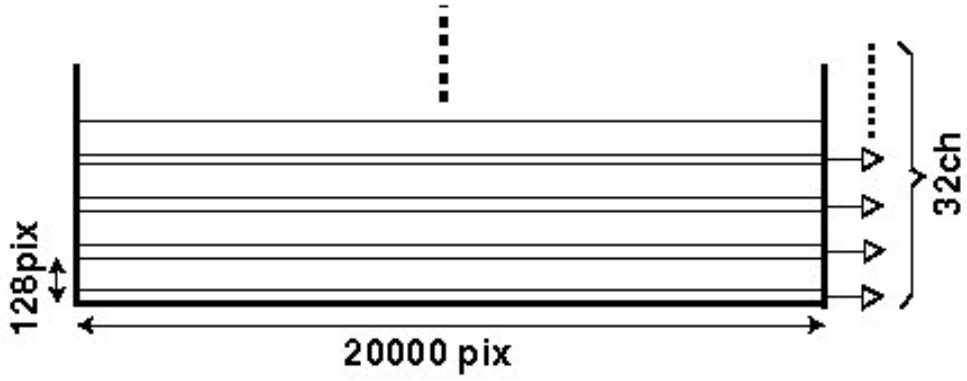
- Pixel size : 5μm
- Thickness : 15μm
- Signal level : ~500e for penetration with large angle
  → Readout ASIC must be low noise.
- Wafer size
  - L1, L2 : 10 x 65 mm^2
  - L3-L6 : 20 x 100 mm^2
- Readout channel : 16 or 32 ch
  - L1, L2 : 13,000 x 128 pix/ch
  - L3-L6 : 20,000 x 128 pix/ch

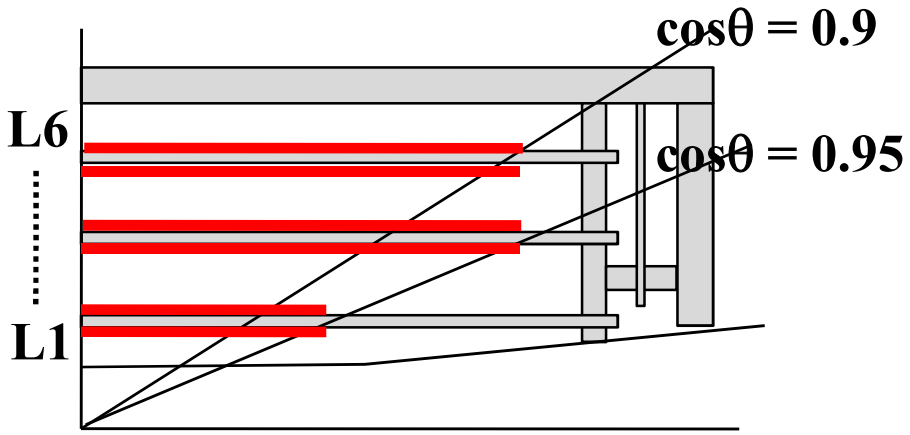


ILC vertex detector is constructed with FPCCD wafers.

FPCCD vertex detector

FPCCD vertex detector

- # of wafers : 220
- Readout channel : ~6000ch
- All pixels in one channel is read within 200ms
- Required power consumption : < 100W.
  - to be investigated



	Size (mm^2)	ch/wafer	# of wafers	# of ch
L1, L2	10 x 65	16	15(ϕ) x 2(z)	480
L3, L4	20 x100	32	16(ϕ) x 2(z)	1024
L5, L6	20 x 100	32	24(ϕ) x 2(z)	1536
Total			220	6080

Structure and performance of FPCCD determines requirement to the readout ASIC.