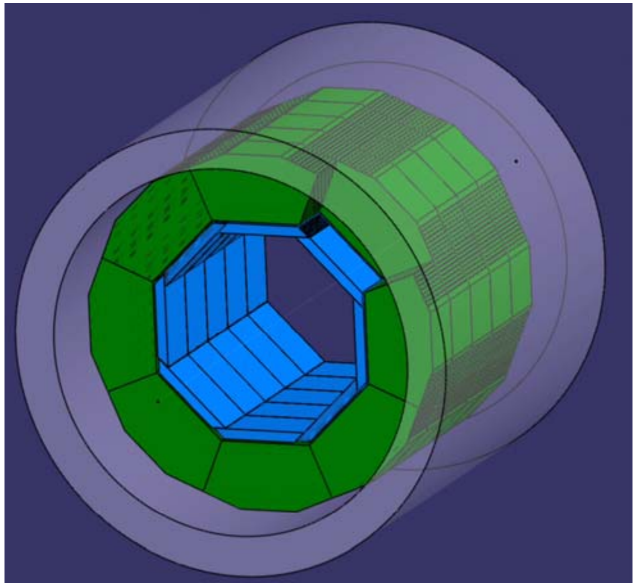
Scintillator HCAL directions



Felix Sefkow

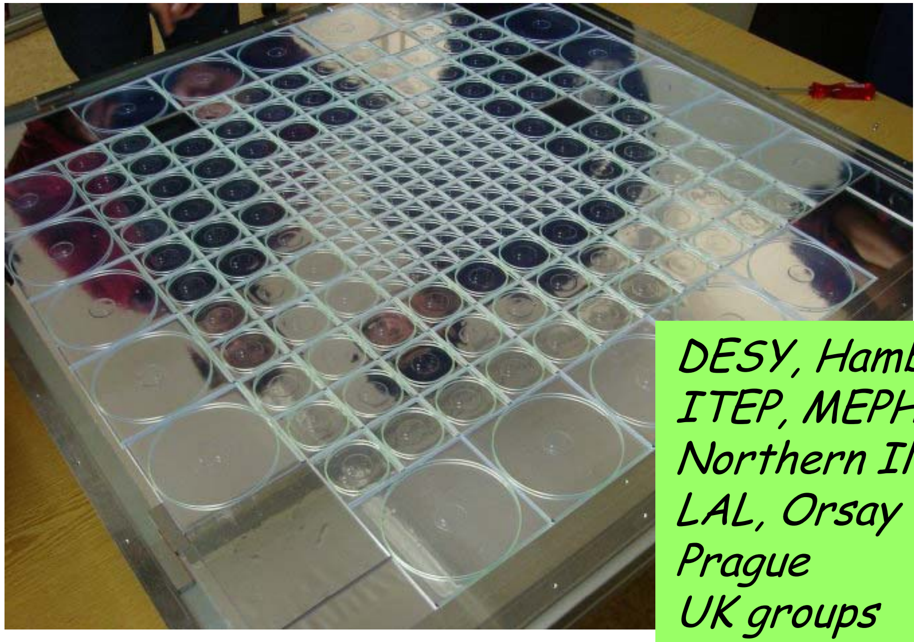
ALCPG07 Meeting at Fermilab
Oct 22-26, 2007

Topics

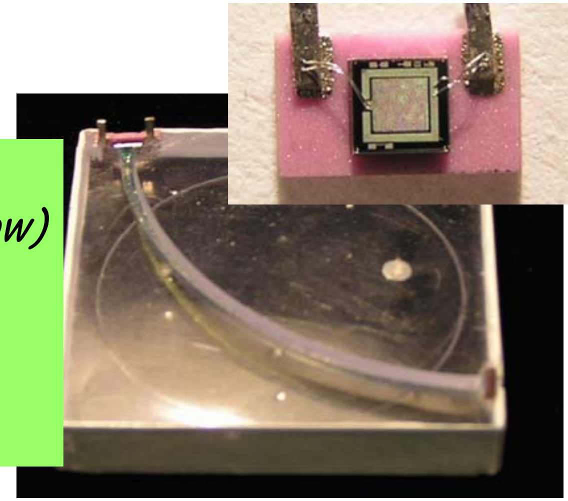
- Scintillator HCAL test beam prototype and analysis directions
- Towards a realistic technical prototype: electronics integration concepts

Tile HCAL testbeam prototype

- 1 cubic metre
- 38 layers, 2cm steel plates
- 7608 tiles with SiPMs
- CALICE electronics and DAQ
- Versatile LED calibration system



- SiPM (MPEPHI/PUSAR)
  - Gain ~10^6, Eff (green) ~ 15%, quenching R ~ 1 – 10 MΩ
- SiPM tile fibre system (ITEP)
  - 3x3x0.5 cm^3 tiles from UNIPLAST, Russia
  - WLS fibre Kuraray Y11(300) 1mm
  - 2% light xtalk per edge
  - Faces covered with 3M mirror foil

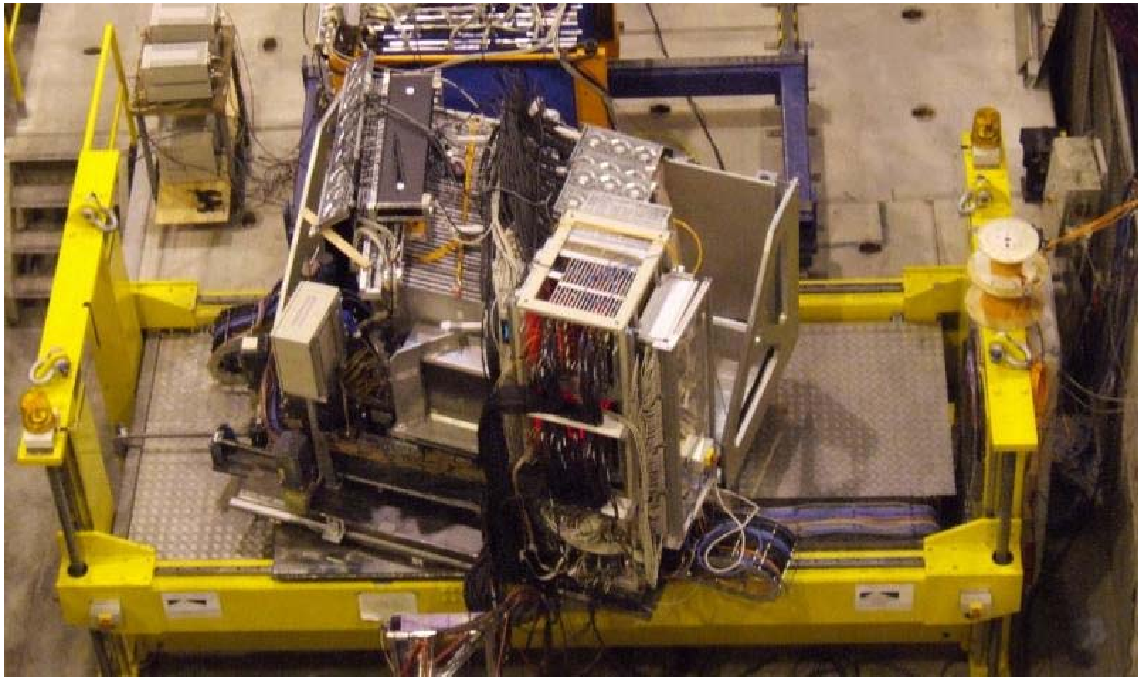


DESY, Hamburg U,
ITEP, MEPHI, LPI (Moscow)
Northern Illinois
LAL, Orsay
Prague
UK groups

Test beam installation

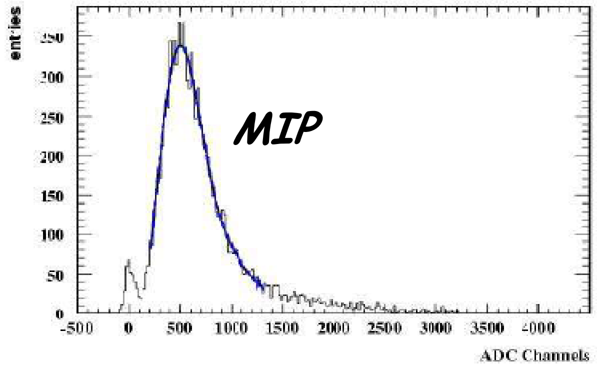
- 2006: first 23 layers in the CERN beam line
- June 2007: all HCAL active layers completed (8000 SiPMs)
- Movable stage completed, fully functional
  - Transverse and rotational scans

See F.Salvatore's talk in the test beam session

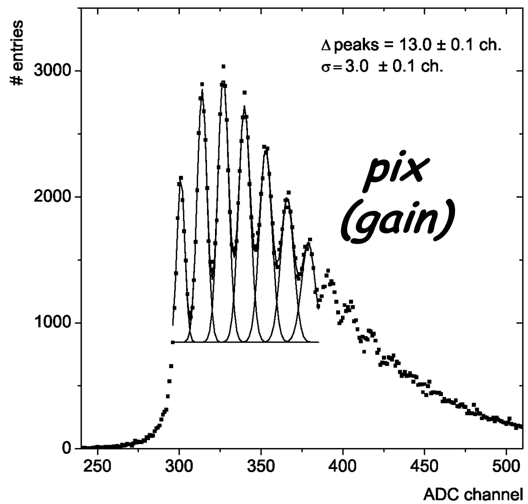


Operational experience, noise

- Robust and stable: ~ 95% up-time
- Only 1.6% dead channels
  - Mostly bad soldering contacts



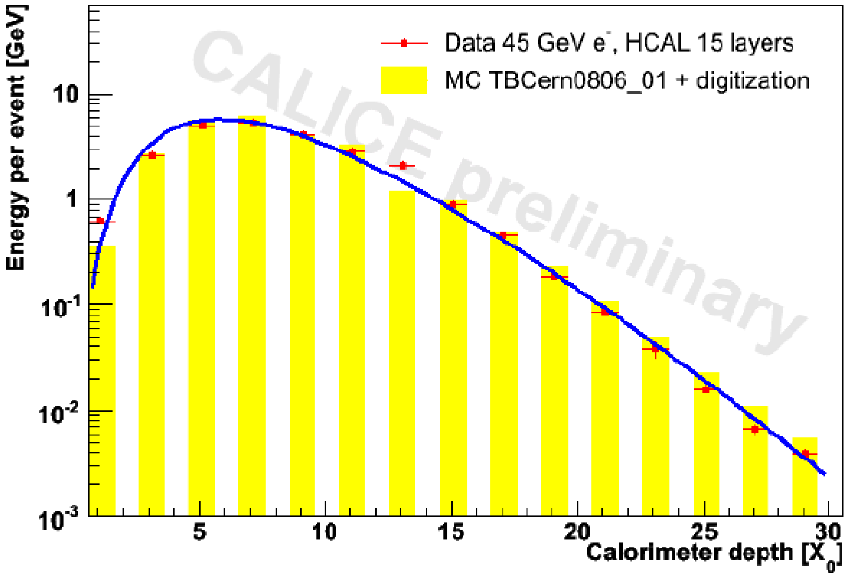
- Calibration needs 2 scales: MIP and SiPN pix
  - E[MIP] = A/A_{MIP} * F (N_{pix}) ; $N_{pix}=A/A_{pix}$
  - F is non-linearity correction (test bench)
- Operation:
  - MIP to set noise threshold (1/2 MIP, offline)
  - Pixel to verify working point (15 pix/MIP)

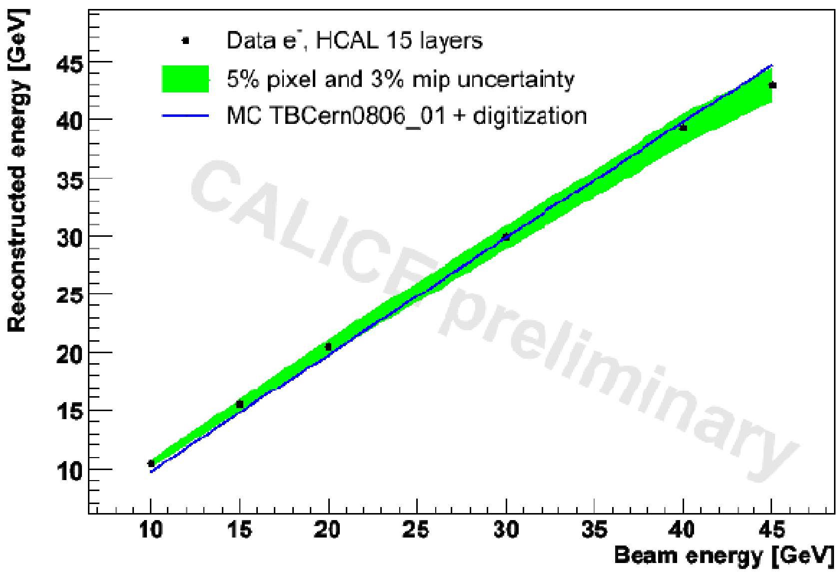


- Noise hit occupancy
  - 10^{-3} in 2006, E / hit ~ 0.8 MIP ~ 0.025 GeV
  - $2*10^{-3}$ in 2007 (non-optimal working point)

Electron data

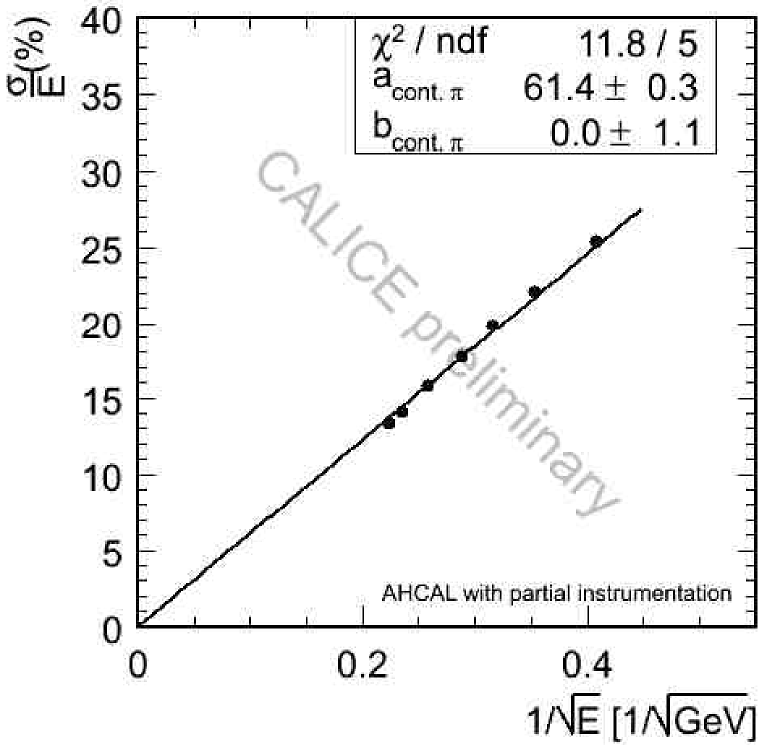
- Check detector understanding (MC) and calibration
- Profile: data shower earlier, as already seen in ECAL
- Linearity: not perfect yet, but sufficient for hadron analysis
- 2007 analysis in progress, sanity checks OK
  - Probe different detector regions and angles

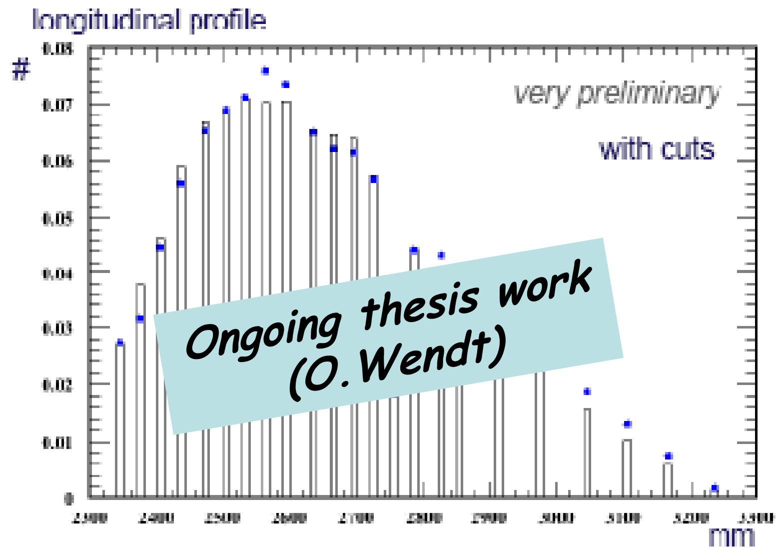




Hadron data

- Hadron data: linearity and resolution “within expectations”
  - Whatever this means: HCAL not complete yet, MC not digitized yet
  - Small constant term for contained showers ☺

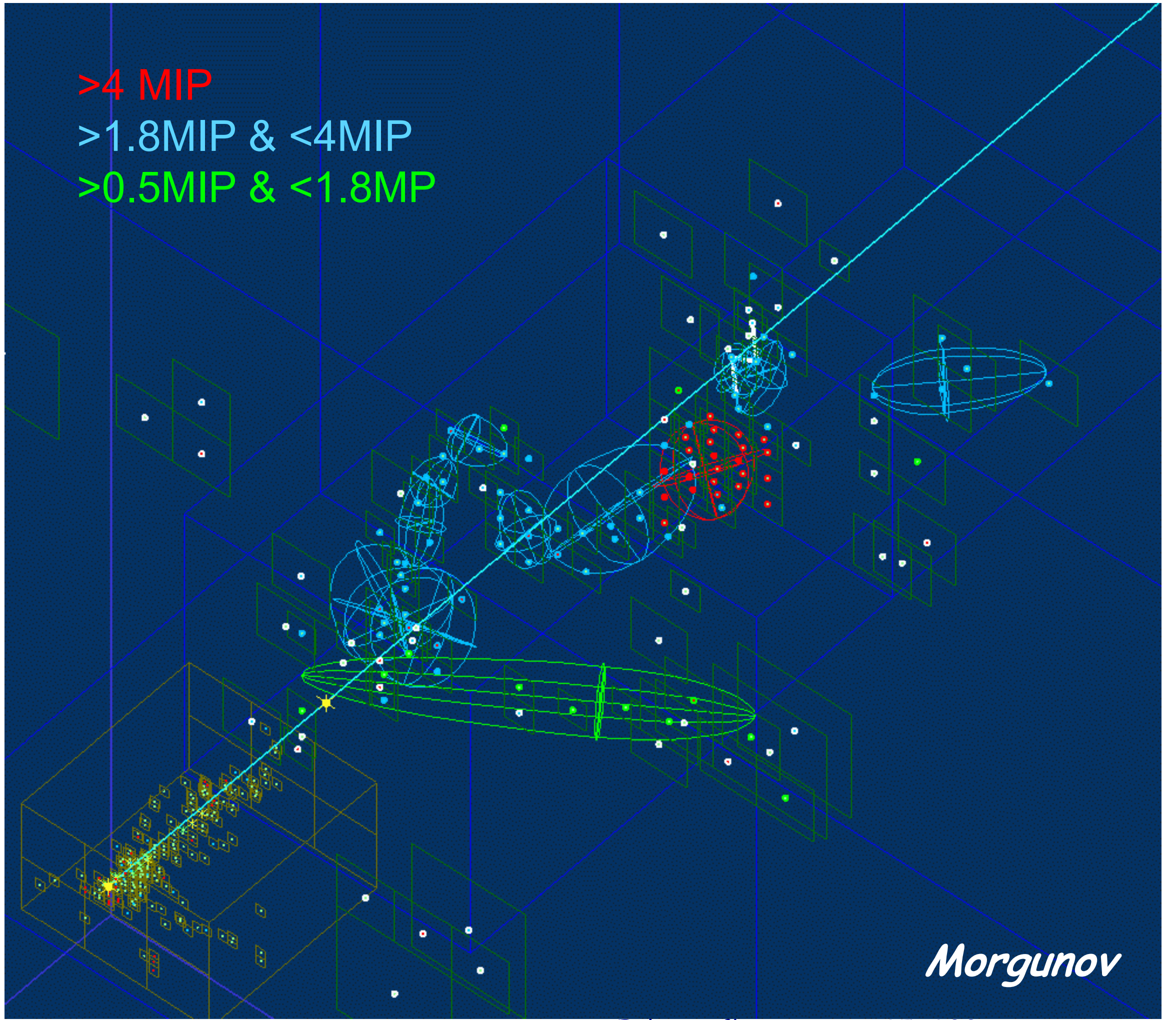




Comparisons with digitized MC (Geant 4) underway

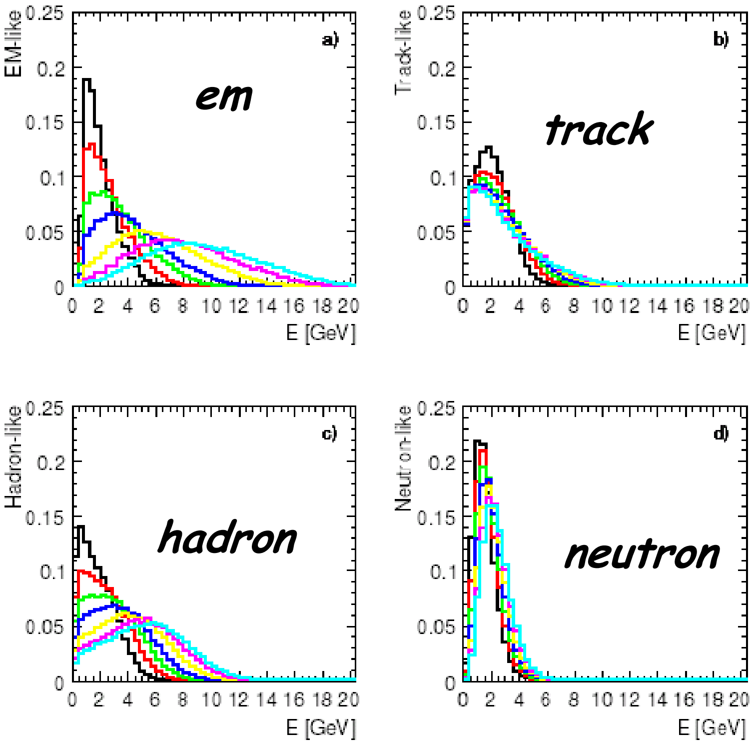
Imaging HCAL

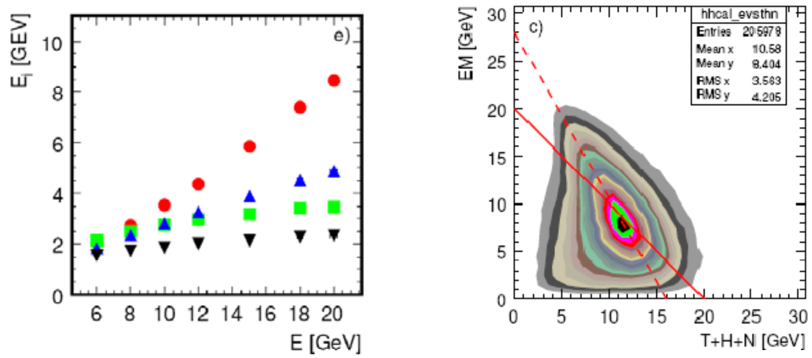
- Substructure visible
- Classification according to amplitude and topology
  - MIP like
  - Hadron like
  - EM like
- Starting point for weighting procedures



"Deep analysis"

- Ideas V.Morgunov, first steps M. Groll (PhD thesis)
- Shower decomposition, using energy and topology



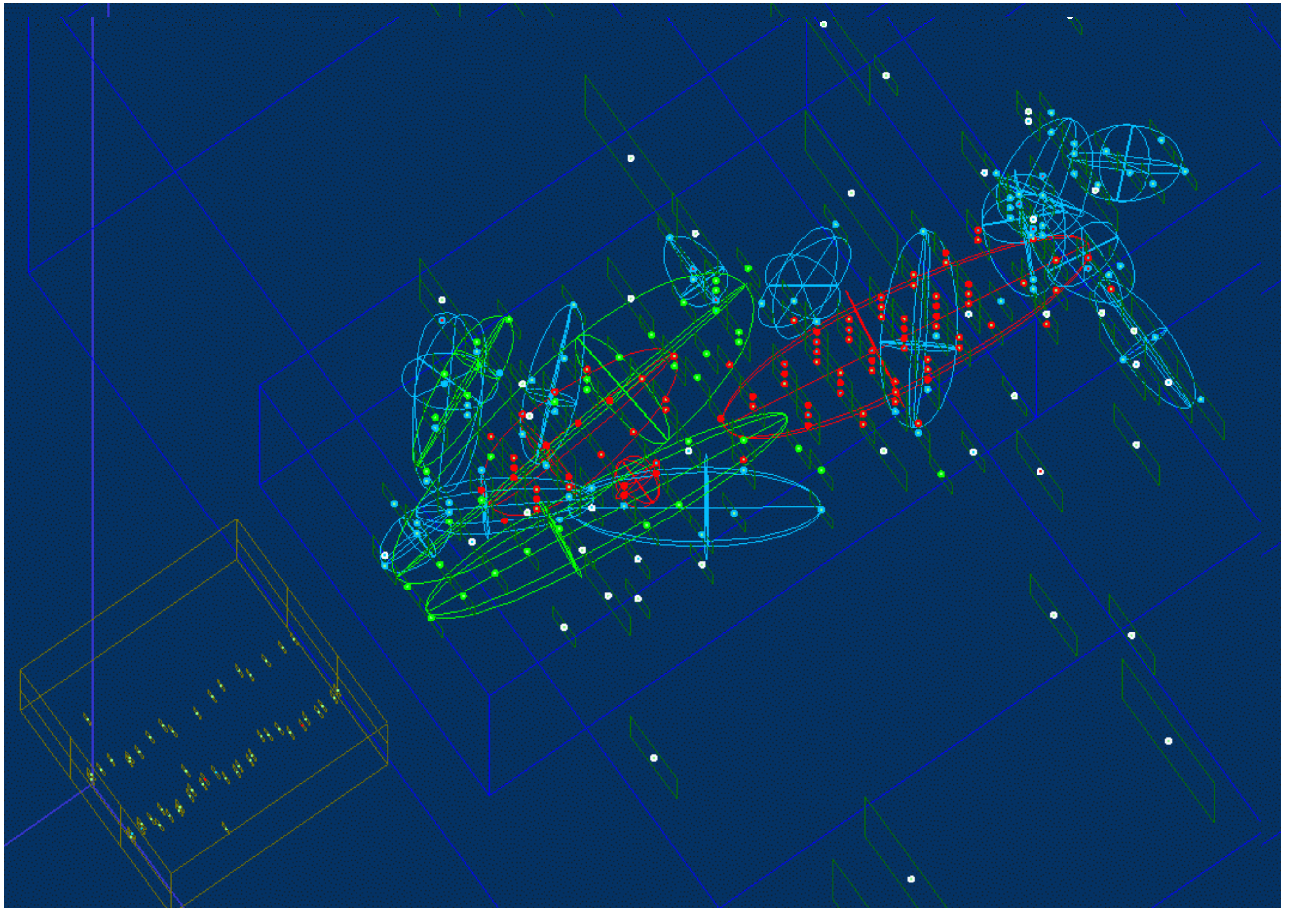


Energy dependence, correlation

Novel quality of input to shower model development

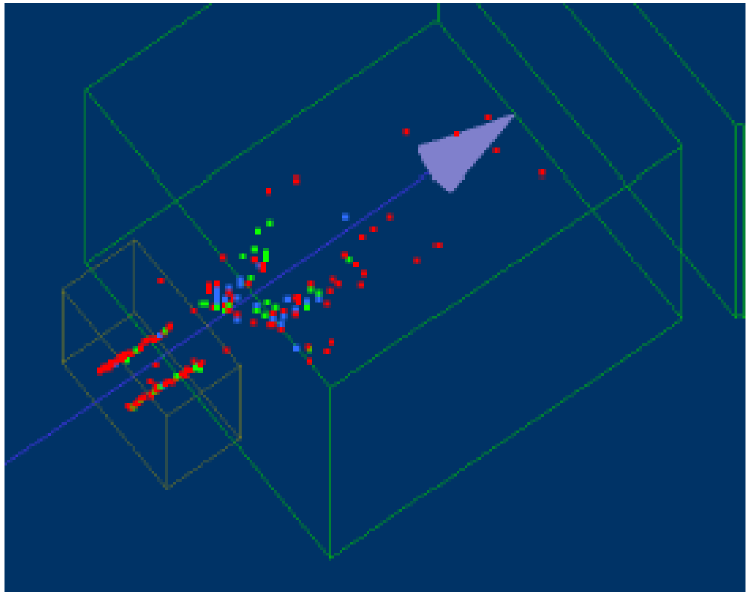
Two hadrons

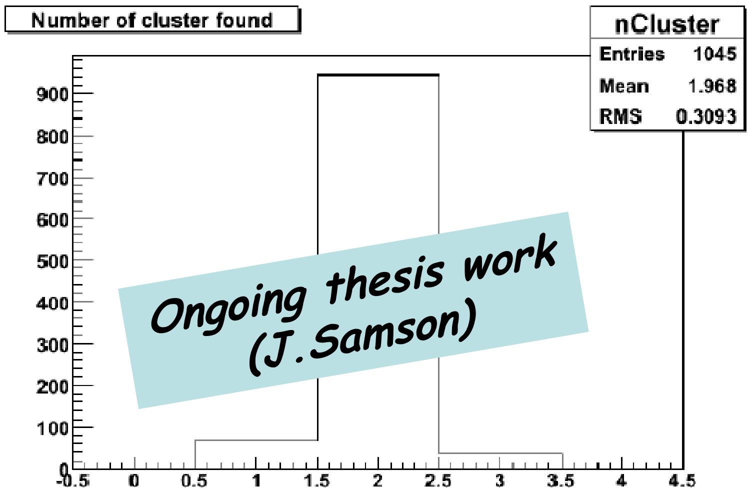
- Starting point for particle flow studies
  - Event overlays
  - Frag-ments
  - …



Event overlays

- Thanks to low occupancy, can use “event mixing” techniques
- Measure the confusion term - in data and MC





Towards benchmarking the PFLOW performance

Physics prototype:

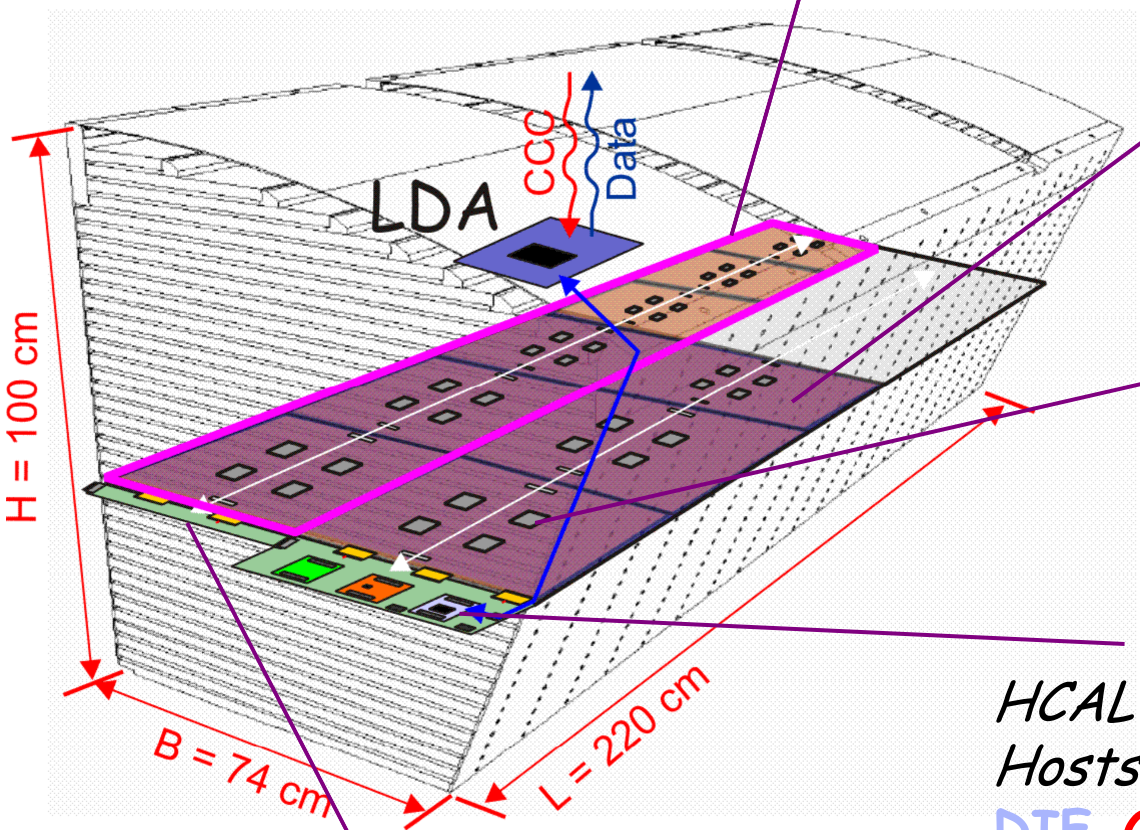
- So far – so good!
- Detector construction, commissioning and operation a truly enjoyable success
- A rich potential for data analysis
  - Needs time and a well organized software framework
- Looking forward to FNAL test beam 2008-09
  - Low energy 1-10 GeV
  - Combined analysis with different ECALs
  - Comparison with gaseous HCAL

Technical prototype

- Goal: A compact and realistic (i.e. scaleable) scintillator HCAL structure with embedded electronics
- Integration issues
  - Readout architecture
  - Ultra-low power ASICs
  - Calibration system
  - Tile and SiPM integration
  - Absorber mechanical structure
- Feed-back from test beam essential
  - Calibration concept
  - Overall detector optimization

AHCAL Half Sector - Integration

FEB



AHCAL Slab

6 HBUs in a row

HBU

HCAL Base Unit

typ. 12 x 12 tiles

SPIROC

typ. 4 on a HBU

HEB

HCAL Endcap Board

Hosts mezzanine modules:

DIF, **CALIB** and **POWER**

HLD

HCAL Layer Distributor

Slabs of an AHCAL layer

FEB

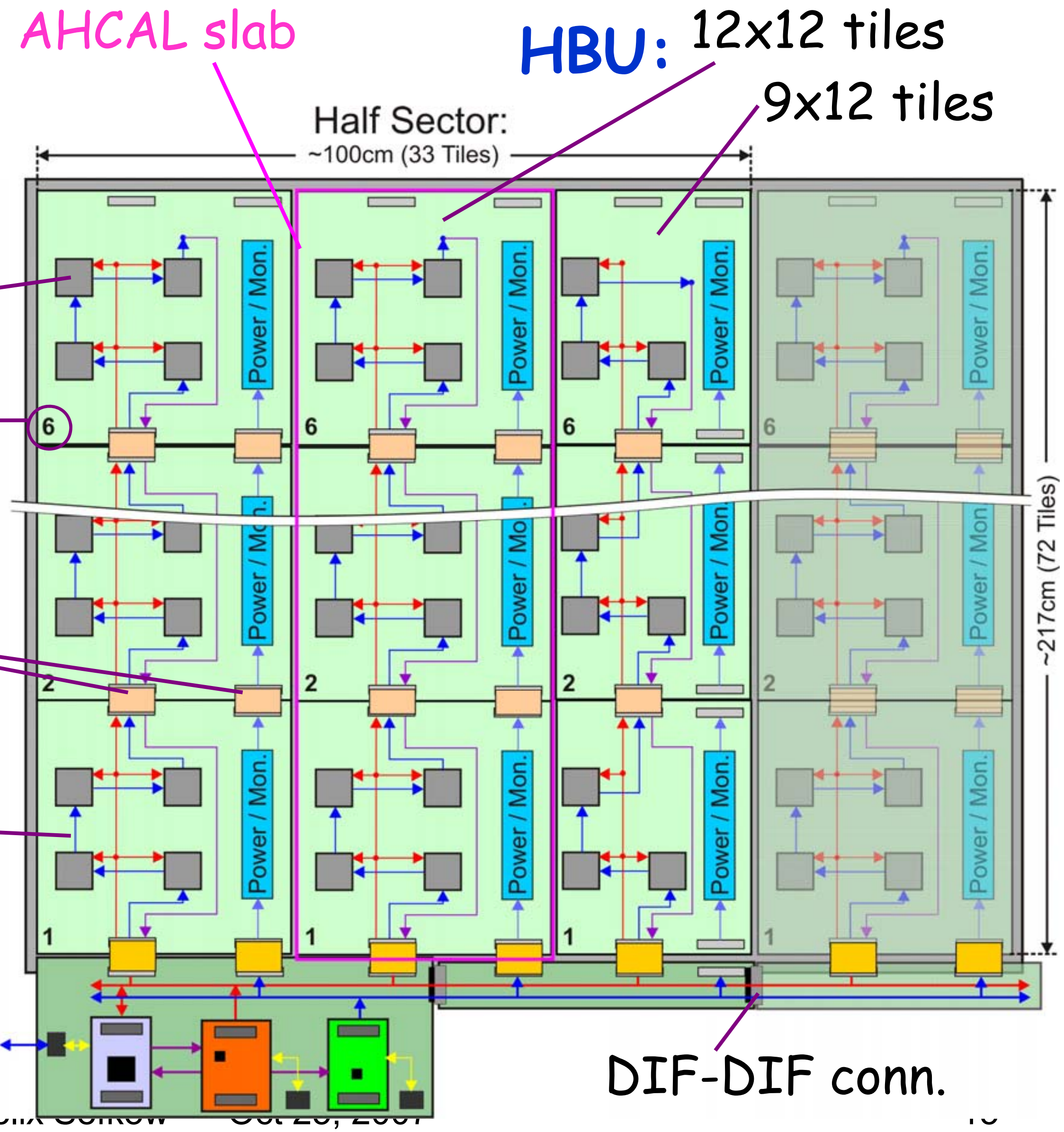
Number of channels
per layer not constant!

24 SPIROCs in chain

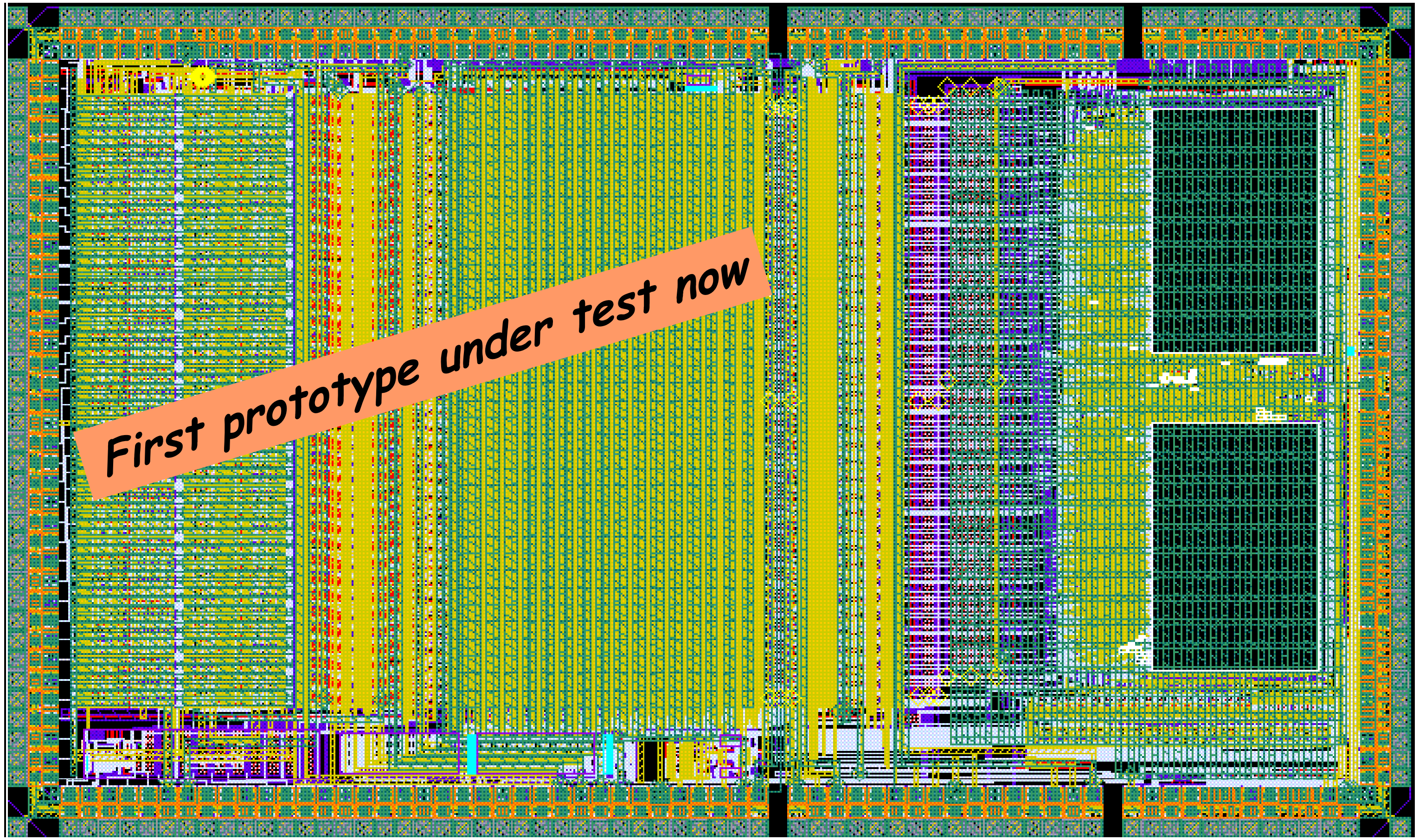
6 HBUs in a row

Two flexleads for
interconnection

Slow-Control and
Readout token

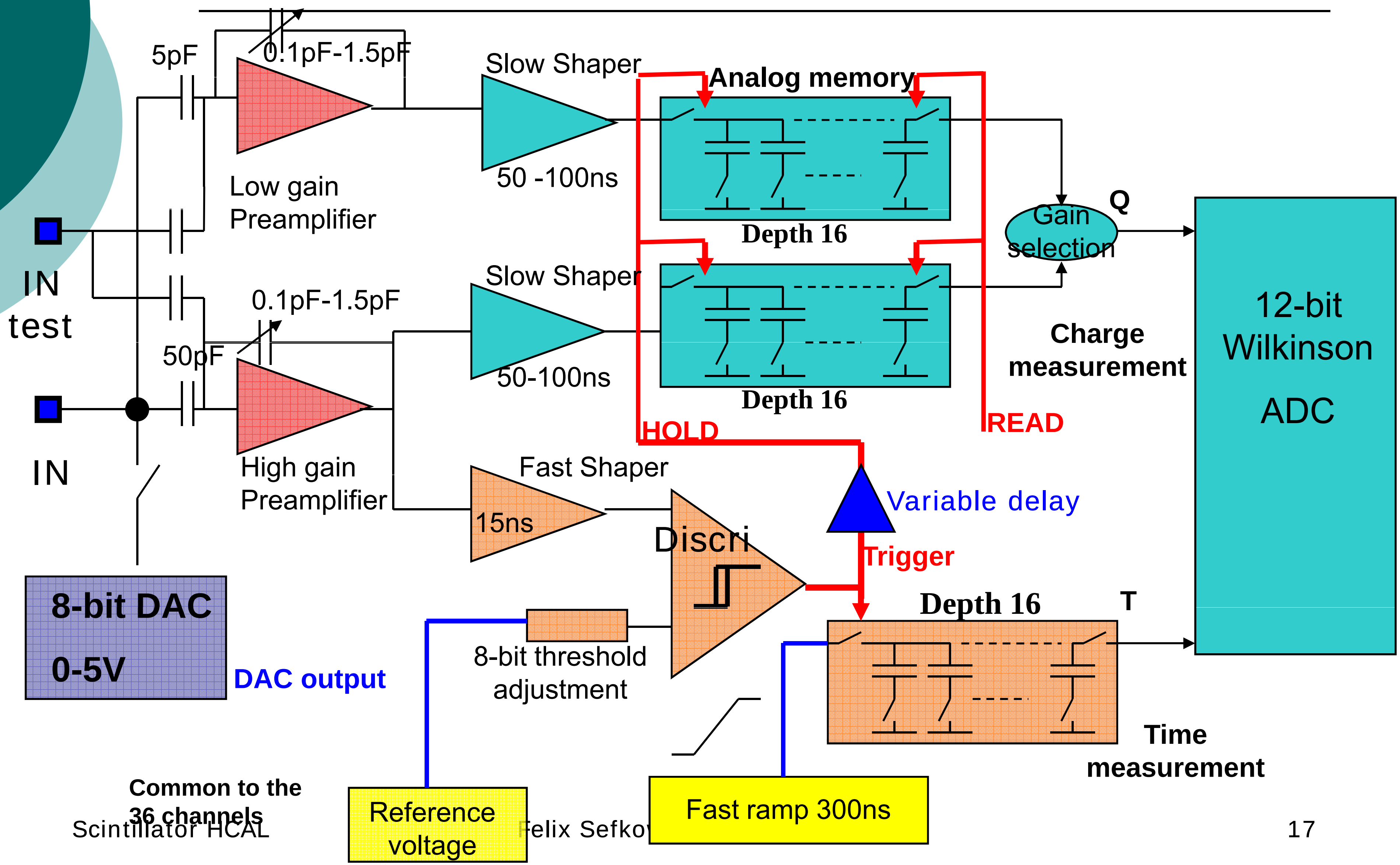


Second generation chip for SiPM : SPIROC



SPIROC has been designed to read out the CALICE AHCAL technical prototype

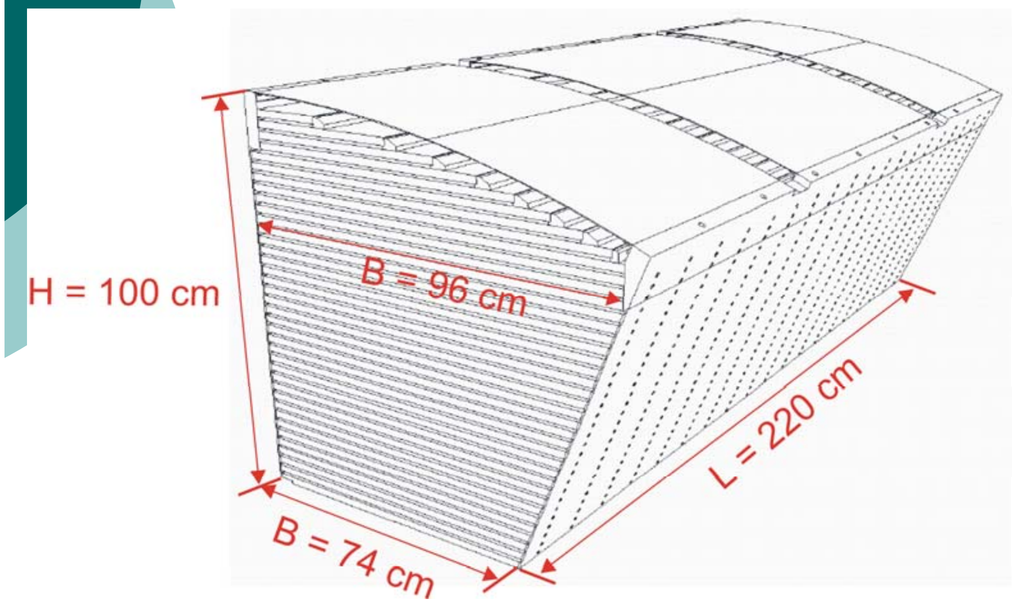
SPIROC: One channel schematic



Temperature / Power Dissipation

FEB

From P. Göttlicher (DESY)



No. channels: 1100 / m^2

Pow. Diss.: 40μW / channel
(25μW ASIC, 15μW HV,
3A / layer during bunch train)

Time constant of heat effects:
α = **6 days**

Temperature at far end (ΔT):
$\Delta T \approx 0.3$ °C

Power pulsing and a good thermal connection (cooling) enables a stable operation!

Calibration system approaches

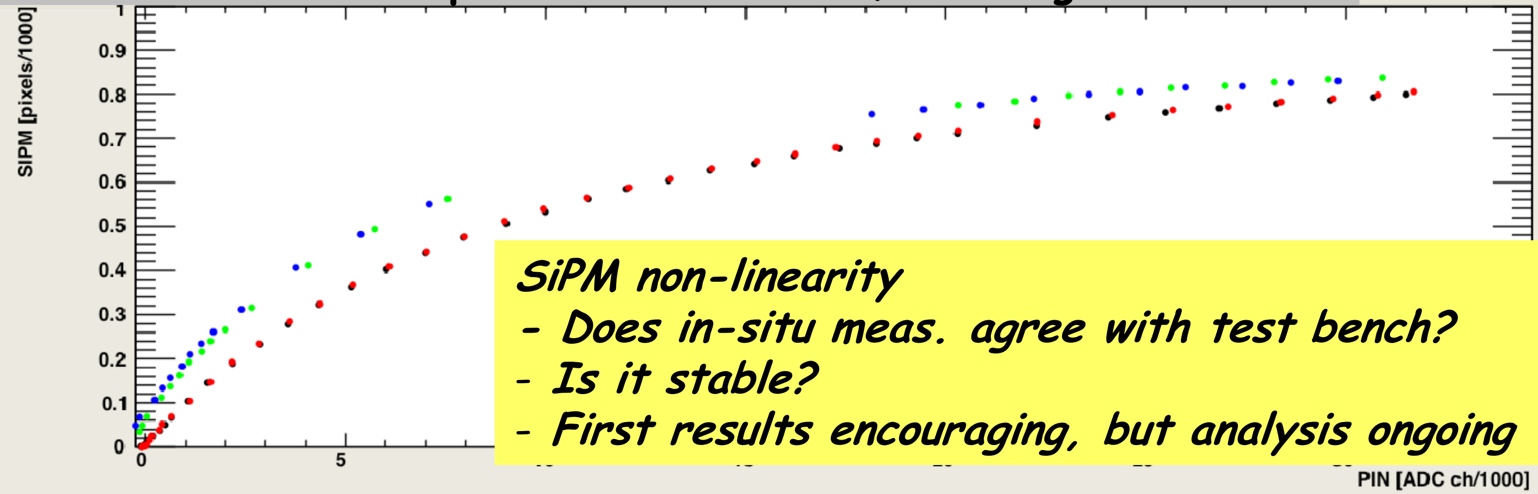
- Optical signal distribution
  - central pulse driver (one or few per layer)
  - Minimized cross-talk to readout (photo-sensors and FEE)
  - Monitoring of light source stability for reference possible
  - Most frequently made choice, experience

- Electrical signal distribution
  - Many pulse drivrs, one per single or few channels
  - Avoids optical coupling problems (stability, uniformity)
  - Can work with very small electrical and optical pulses
  - Not yet tried until now

Saturation Curves for Module 13, 5-6

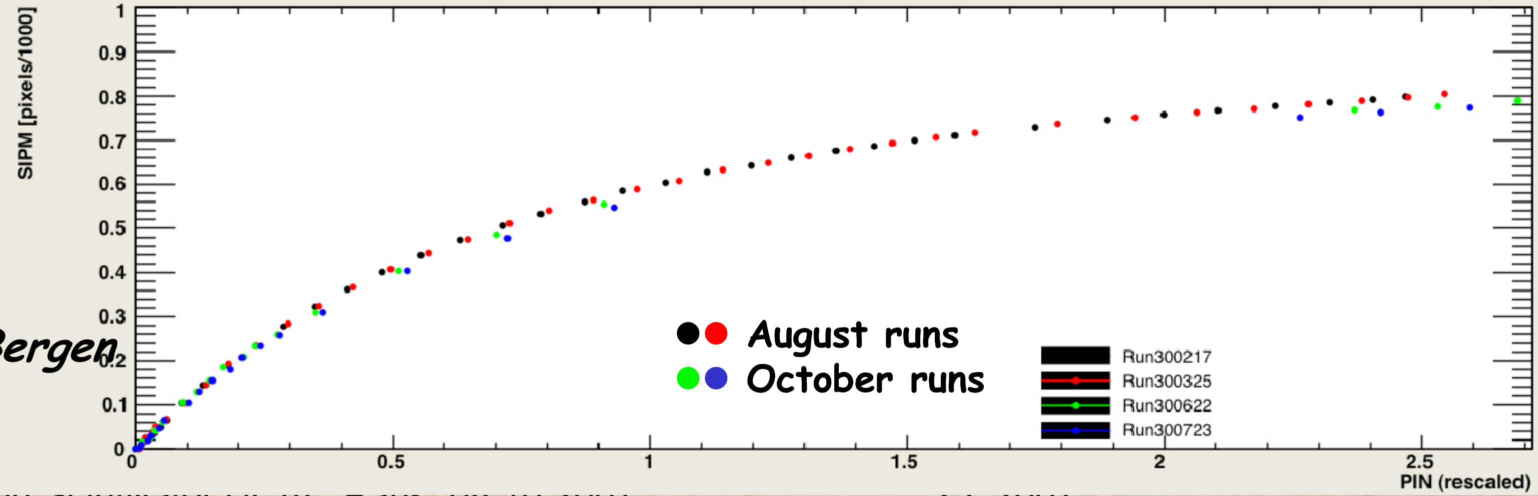
- Compare 4 runs from August & October

Saturation curve after pedestal subtraction, PIN & gain correction



SiPM non-linearity
- Does in-situ meas. agree with test bench?
- Is it stable?
- First results encouraging, but analysis ongoing

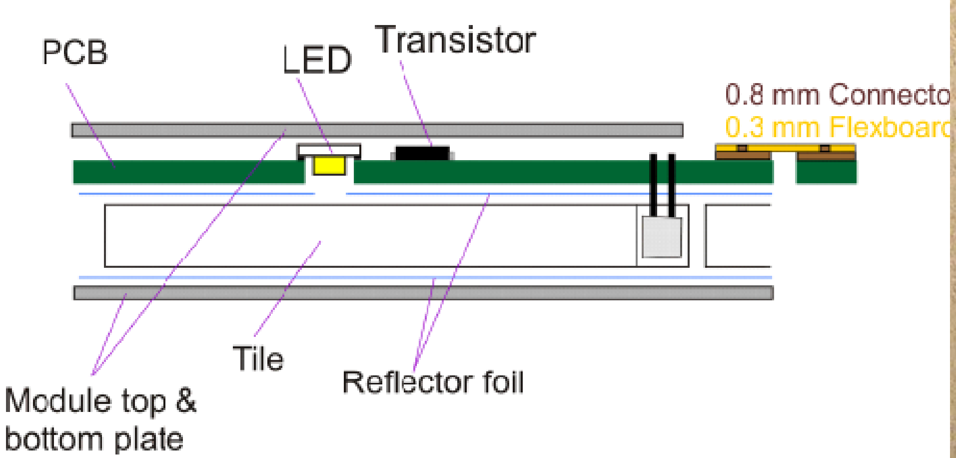
Saturation curve after adjustment to common origin with slope one

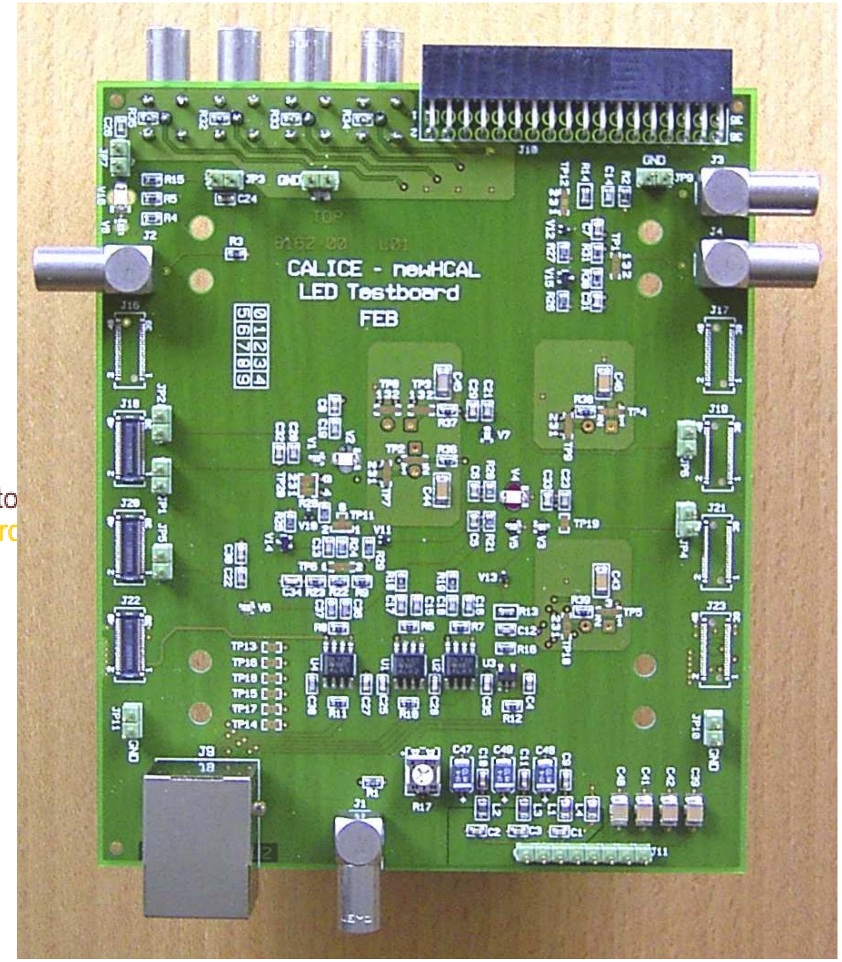


G.Eigen, Bergen

LED on board

- Proof-of-principle, check for cross-talk, uniformity
- Test also
  - Different driver schematics
  - Small connector
  - SiPM coupling

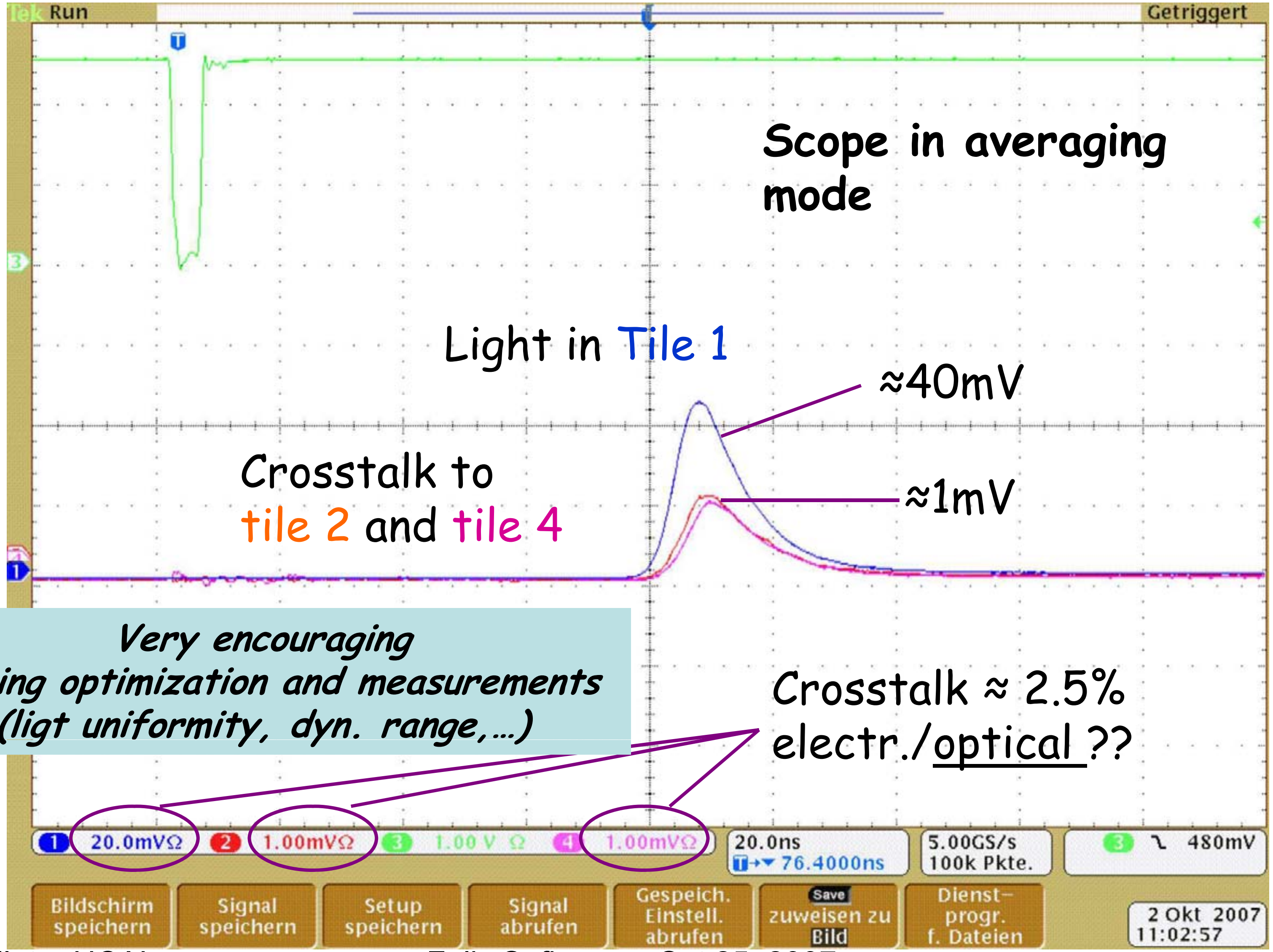




M.Reinecke, DESY

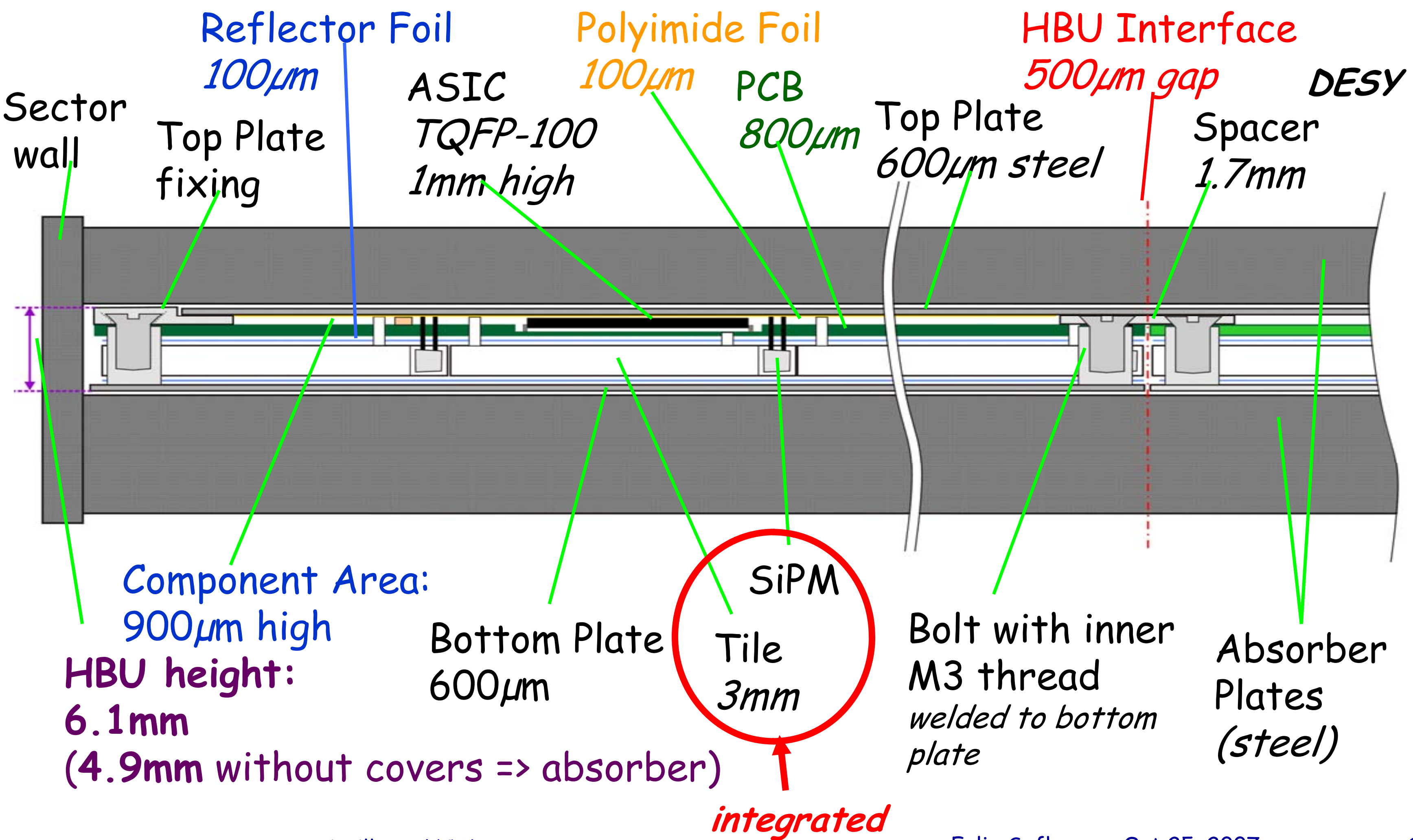
Estimate Crosstalk

FEB



Very encouraging
Ongoing optimization and measurements
(ligt uniformity, dyn. range,…)

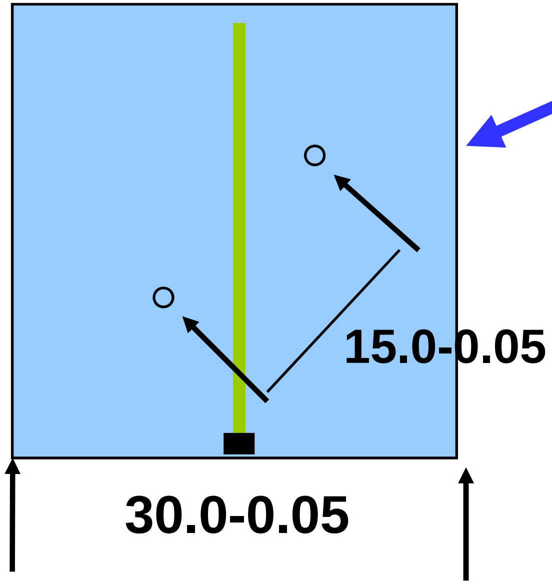
Integrated layer design

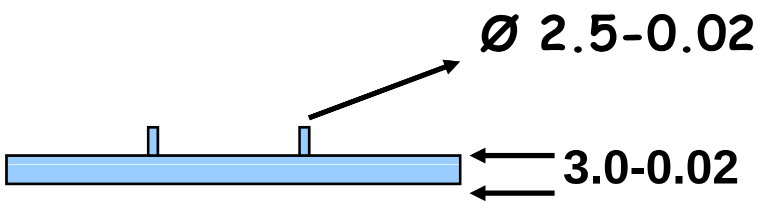


TILE

All dimensions are preliminary

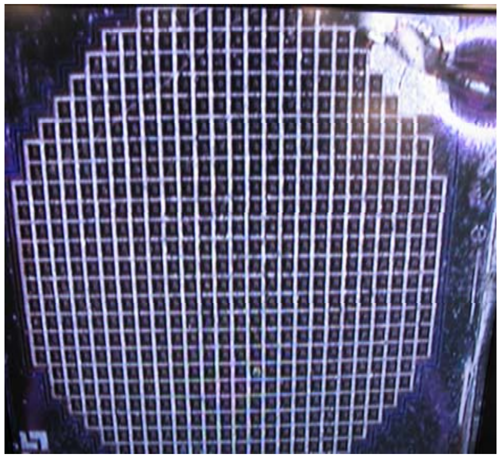
Chemically treated edges for light reflection

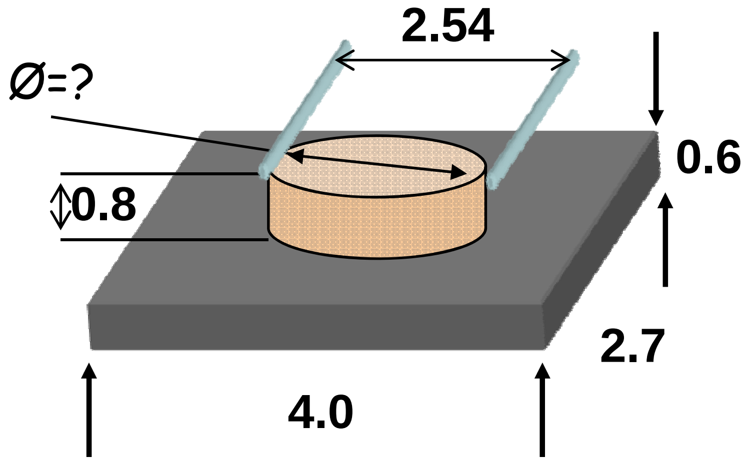




Schedule OK:
Tiles for electronics unit in 2008
For complete layer / small test stack in 2009

MGPD

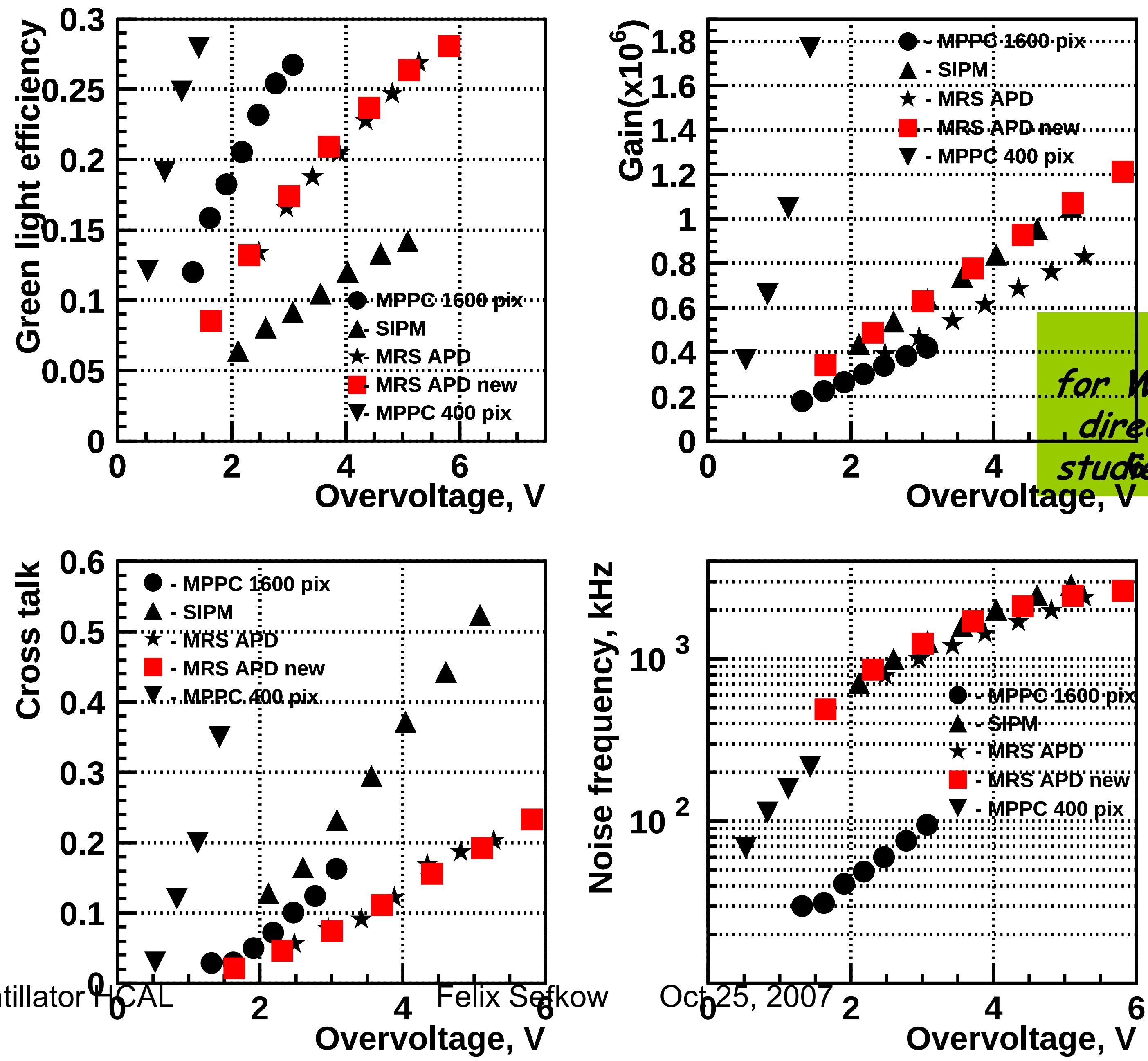




556 cells, Ø1mm
CPTA, Moscow

M.Danilov, ITEP

MGPD PROPERTIES



OK
for WLS readout;
direct coupling
studied in parallel

M. Danilov

Scint – MGPD – PCB integration

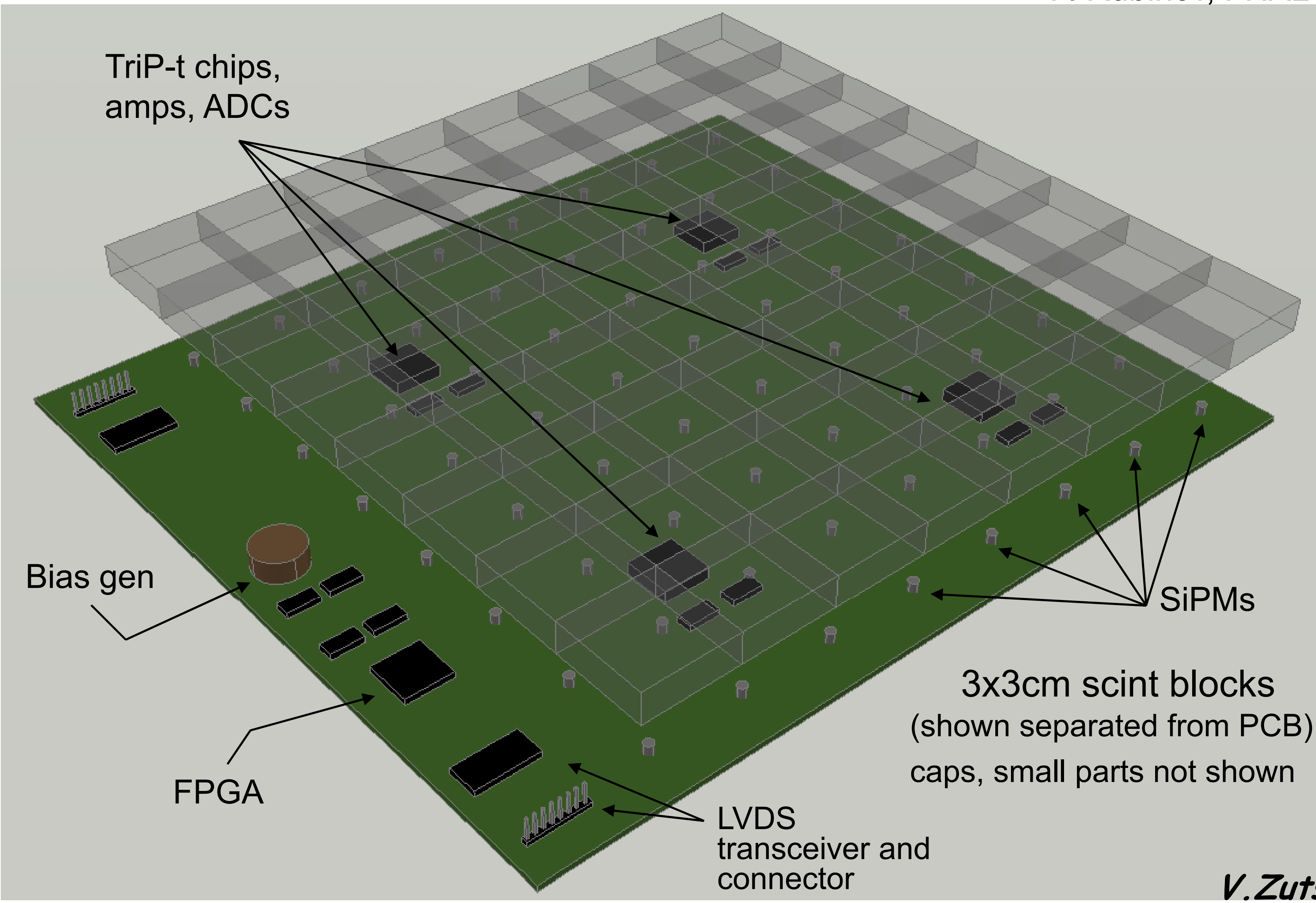
- Two possibilities:
  1. Photo-sensor scintillator unit ⇔ PCB with VFE
  2. Scintillator ⇔ PCB with photo-sensor and VFE

- Option 1, based on the good experience with TB prototype
  - Stable optical connection
  - Early and easy single channel quality control
  - independent of final electronics (schedule)
- Option 2 is followed by NIU and FNAL
  - Advantage: automated SMD technology for photo-sensor mounting

- First prototype IRL:
  - Staged approach utilizing components as they become available
  - For now use 4 Trip-t chips (with external ADC): 16 ch each
  - Place bias generation and control, LVDS communications links along the edge of the IRL (requires ~2.5cm to 3cm strip)
  - One FPGA per board, 64ch per board
- Advantages of this approach:
  - Allows the study and optimization of electro-mechanical integration required in a realistic setting
  - A truly integrated board- low voltage power and LVDS data link in, LVDS data link out, everything else done on the board
  - Reuse existing Minerva technology (bias generator, FPGA, ADCs, TDCs, LVDS protocol, etc)
  - TriP-t chips exist (several hundred extra available)

V.Zutshi

P. Rubinov, FNAL

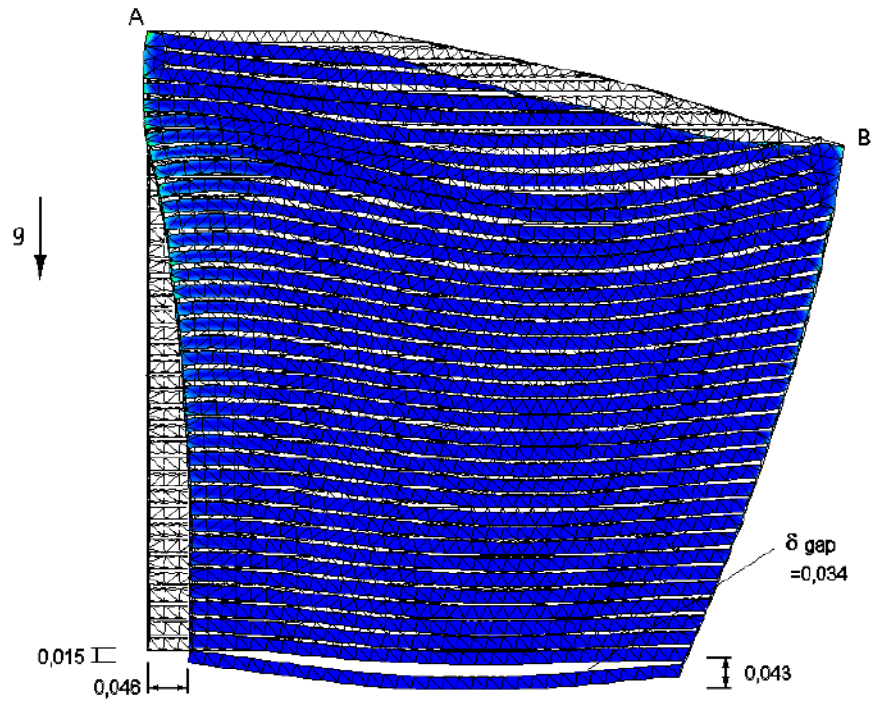


V.Zutshi

On the fabricated board the electronics will be on the underside of the board

Mechanical design

- Modular approach
- Cassette:
  - Evolve test beam prototype design
- Absorber structure:
  - Start with re-evaluation of TESLA design
  - Very ambitious concept with minimized dead material
  - Scrutinize idealizations



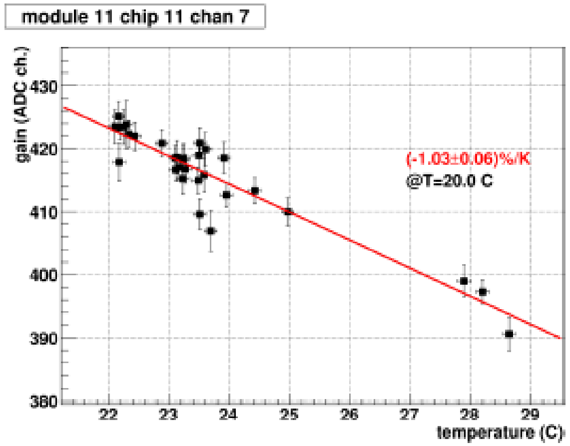
Conclusion

- Things are starting to fall into place
- A nice concept is emerging – looking forward to the design phase
- Many open issues still – modular approach leaves room for new ideas and options

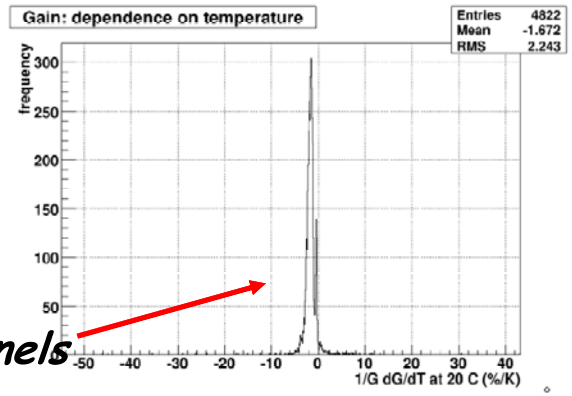
Back-up slides

Test beam calibration

- Calibration is done with MIPs (muons)
  - To be established for ILC: simulations
- Monitoring with
  - Temperature sensors
  - LED reference pulses (problematic)
  - Direct observation of SiPM gain
- Calibration electronics developed and built in Prague
  - Redundancy for cross-checks
  - Large dynamic range
- Calibration data analysis: DESY, Bergen
- Tools for multi-channel studies developed



S.Schaetzel, DESY

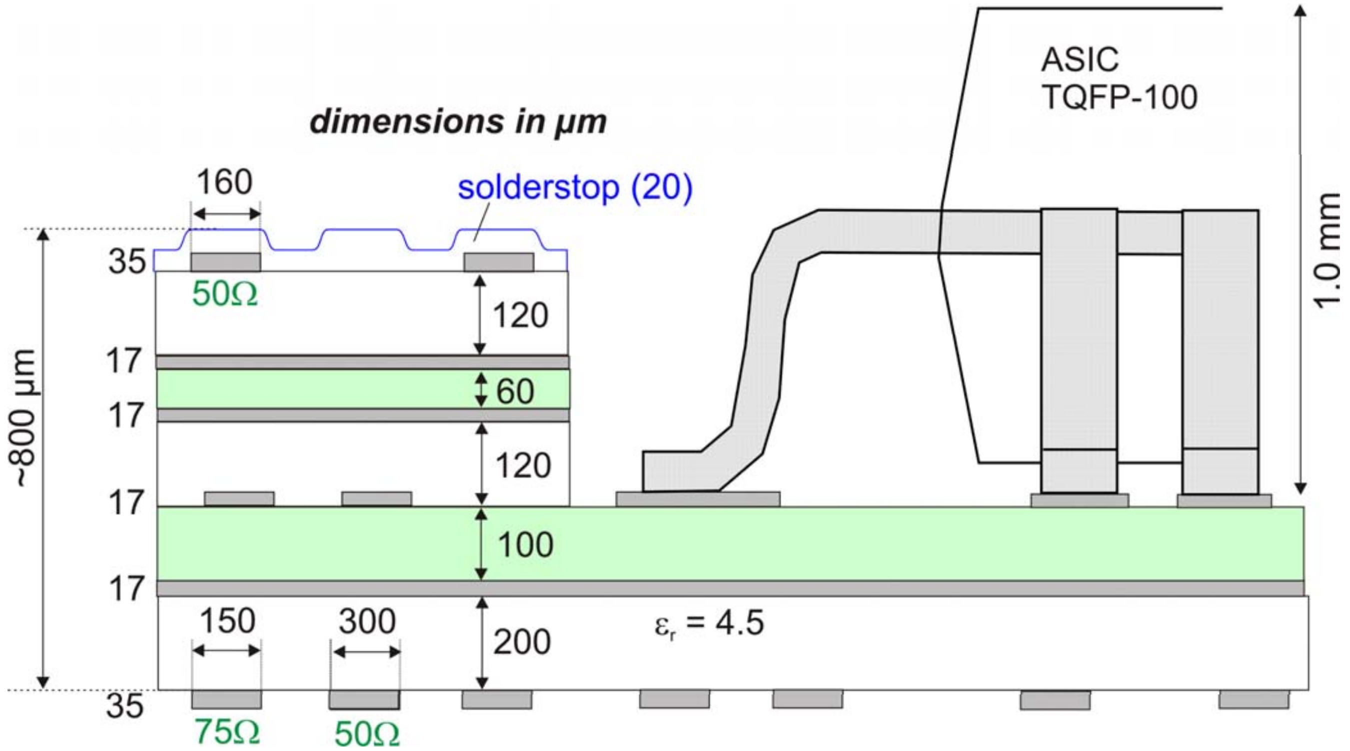


Example: temp. dependence of gain for 5000 channels

HBU – PCB Layer Structure

FEB

- -6 layer design with cut-outs for ASICS and connectors
- -75Ω Lines for high-gain SiPM setup
- -Two signal layers for impedance-controlled routing
- -**Total height (PCB + components): 1.5mm**
- -Two companies agreed on structure at reasonable costs!!

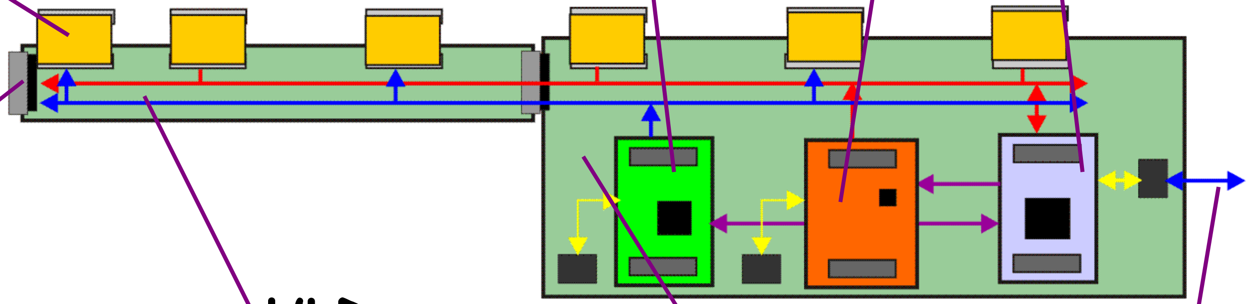


HEB Interconnection Concept

FEB

Flexlead and 80-pin connector
Interconnection to AHCAL-Layer (HBU)

POWER CALIB DIF



DIF-DIF conn.
Redundancy against failures of LDA

HLD
Changes Size from Layer to layer

HEB
Same Size for all 38 AHCAL layers

To LDA

DIF - *Detector Interface (Configuration and Operation)*
CALIB - *Light and/or Charge calibration and monitoring*
POWER - *Layer power and temperature monitors*

Mezzanine setup allows independent development of different groups.

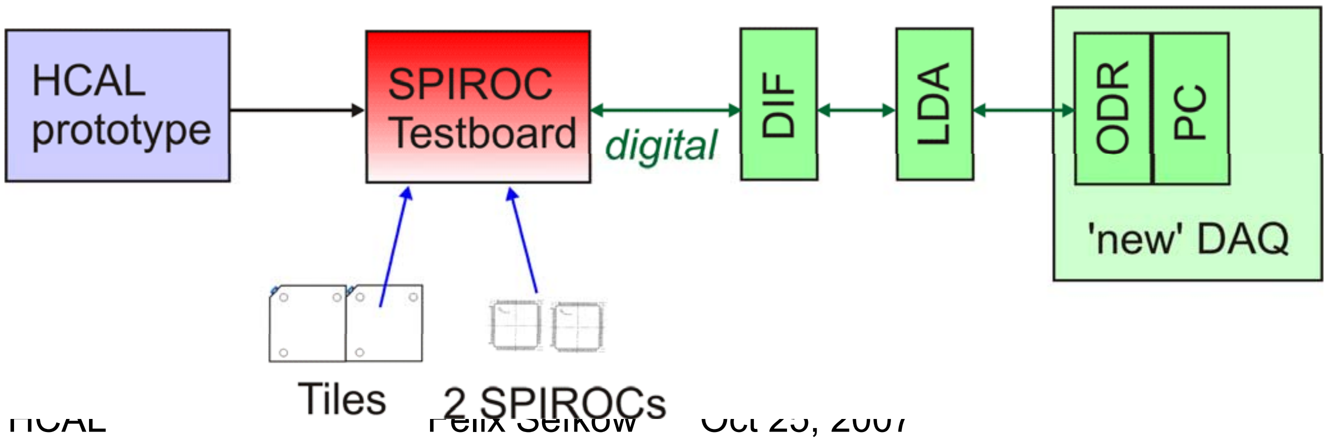
Testboard II : ASIC + Integration

FEB

SPIROC Testboard (HBU prototype):

-Assembly (Tiles, PCB, ASICs, LEDs), Cassette Construction
-Performance in the dense HBU setup:
 Noise, gain, crosstalk, power and signal integrity
-DAQ Interface
-LCS with LEDs on board.

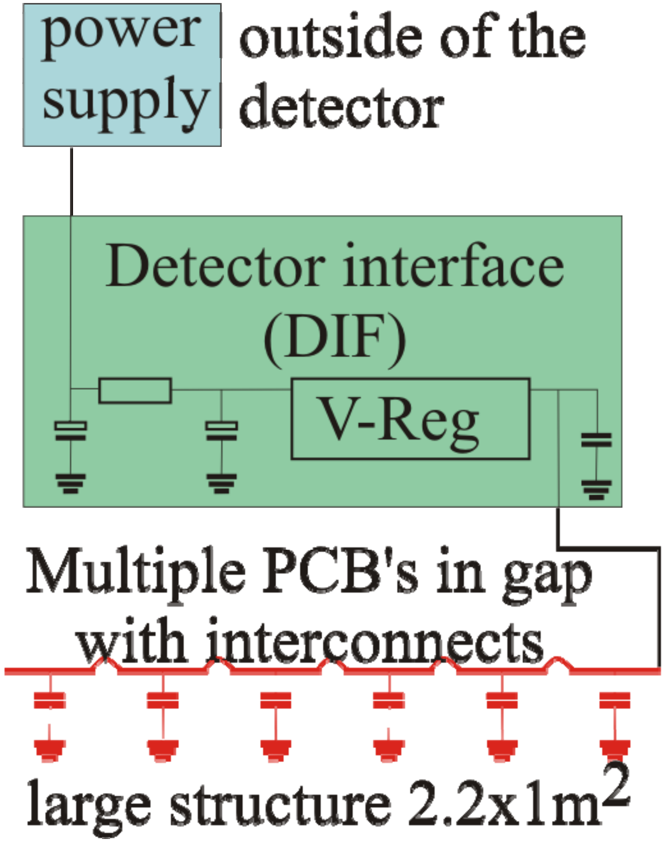
Tile integration to HBU : see M. Danilov's talk (alignment pins)



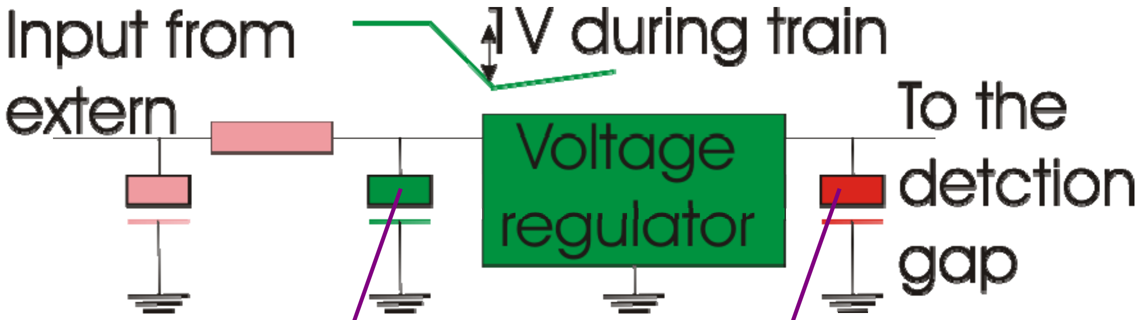
POWER to AHCAL layer

FEB

Example for
HCAL half-octant



Components on HEB, HLD



For 1V in 2ms:	For 5mV in 1µs:
3.4mF	340µF
10 SMD tantal	40 large ceramic
‚Slow'	‚Fast'

P. Göttlicher, DESY

Testboard III : Power-System

Test Power-Ground System (2.20m)

-Oscillations when switching?

-Voltage drop, signal integrity (traces, connectors)?

-SPIROC performance @ far end (blocking caps sufficient)?