The MAPS ECAL

ALCPG 07
Fermilab

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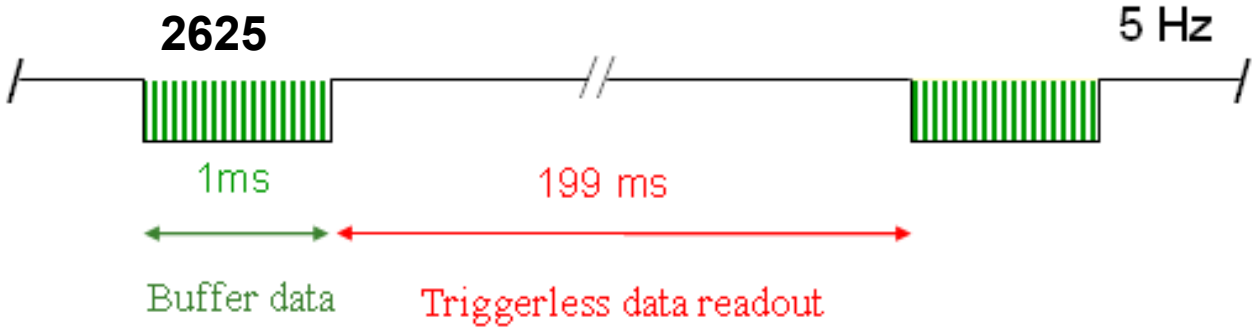
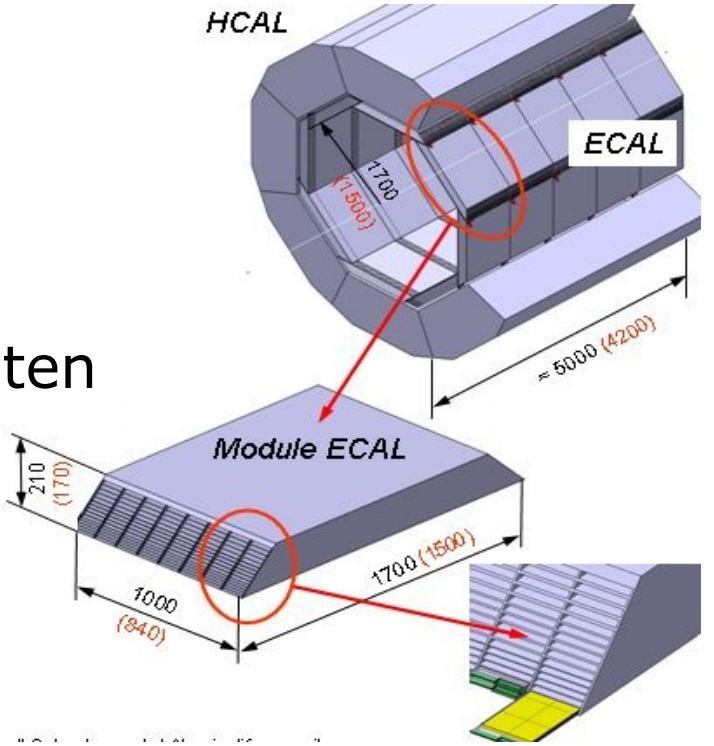
Calorimetry for the ILC

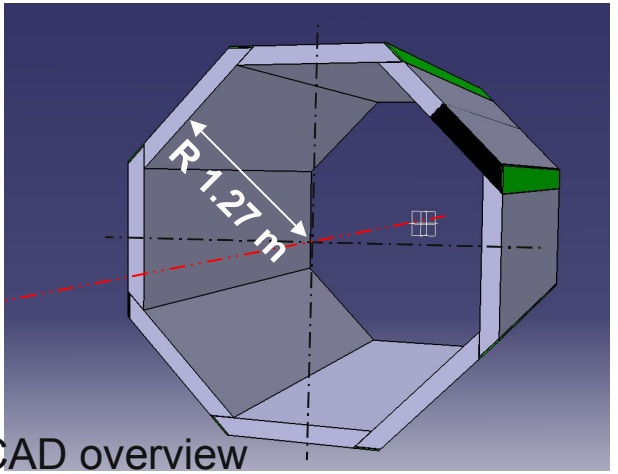


- ILC calorimetry focused on Particle Flow Approach (PFA)
  - Requirement of highly granular calorimeters
- ILC is different to LHC
  - Bunch spacing of ~ 300 ns
  - 2625 bunches in 1ms
  - 199 ms quiet time
- Occupancy dominated by beam background & noise

SiW for the ECAL

- The baseline from ILD & SiD
- Sampling Calorimeter
  - Silicon sensors embedded in tungsten sheets
- 30 layers deep
- 1.3 - 1.7 meters radius
- 1300- 2000 m^2 silicon area
- Silicon pad size 4x4-5x5 mm



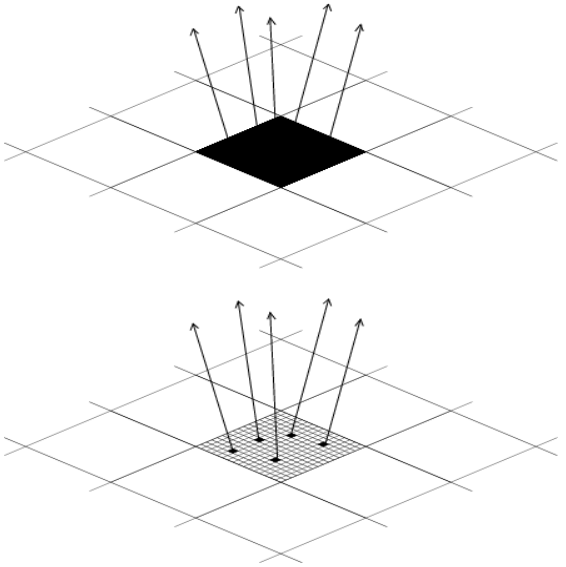


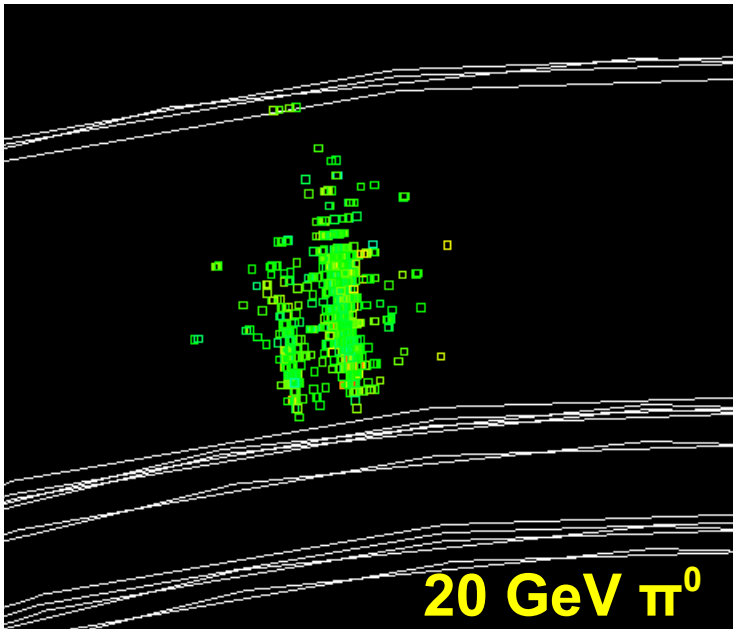
CAD overview

Is the granularity sufficient ?

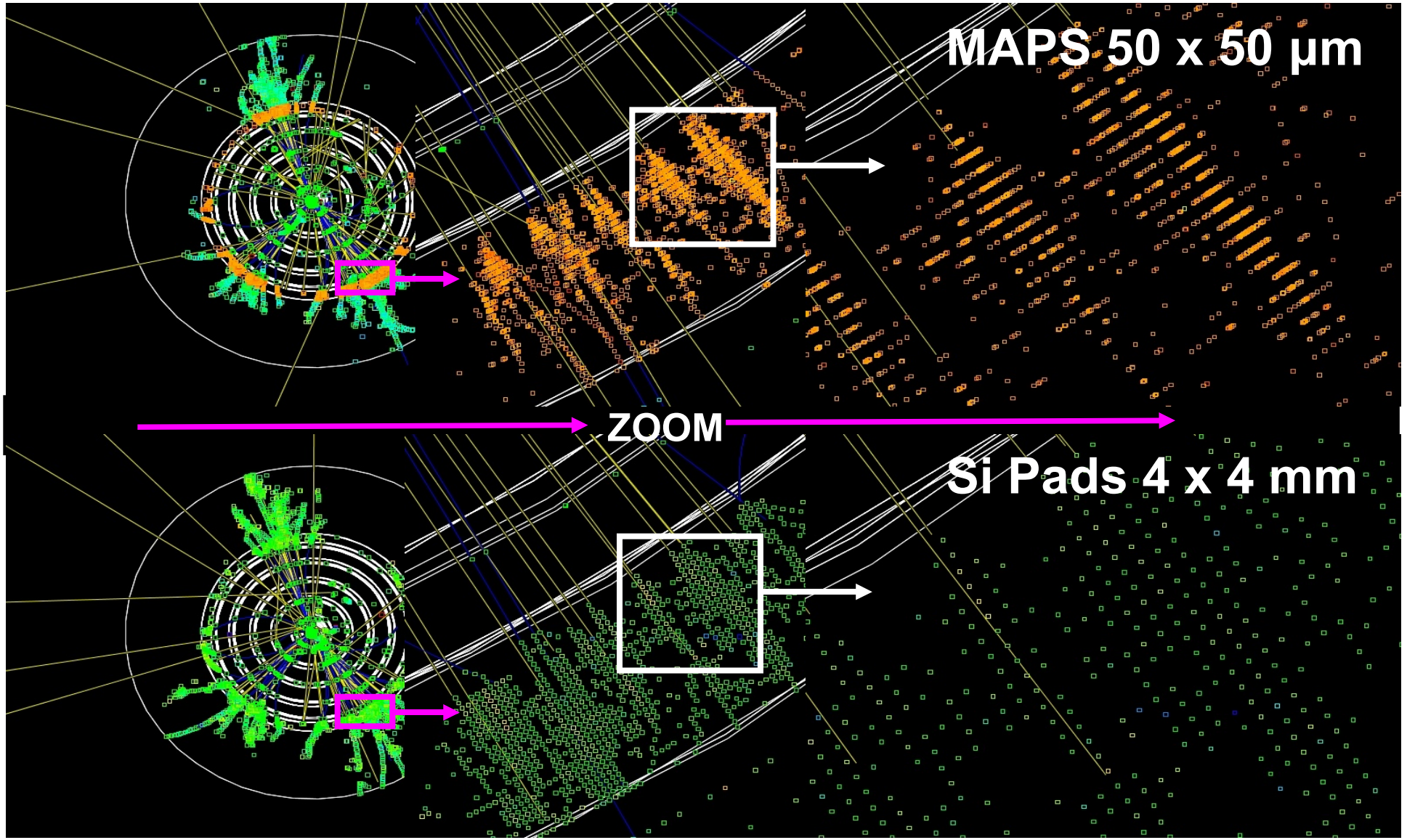
Increasing the granularity

- PFA based on
  - track-shower matching
  - clear shower separation
- Granularity of 5x5 mm may not be sufficient for
  - e.g. π^0 separation
  - clearer shower separation
- Digital Pixels with 50x50 microns
  - basically a Particle Counter
  - requires highly integrated sensor
  - ideal for MAPS



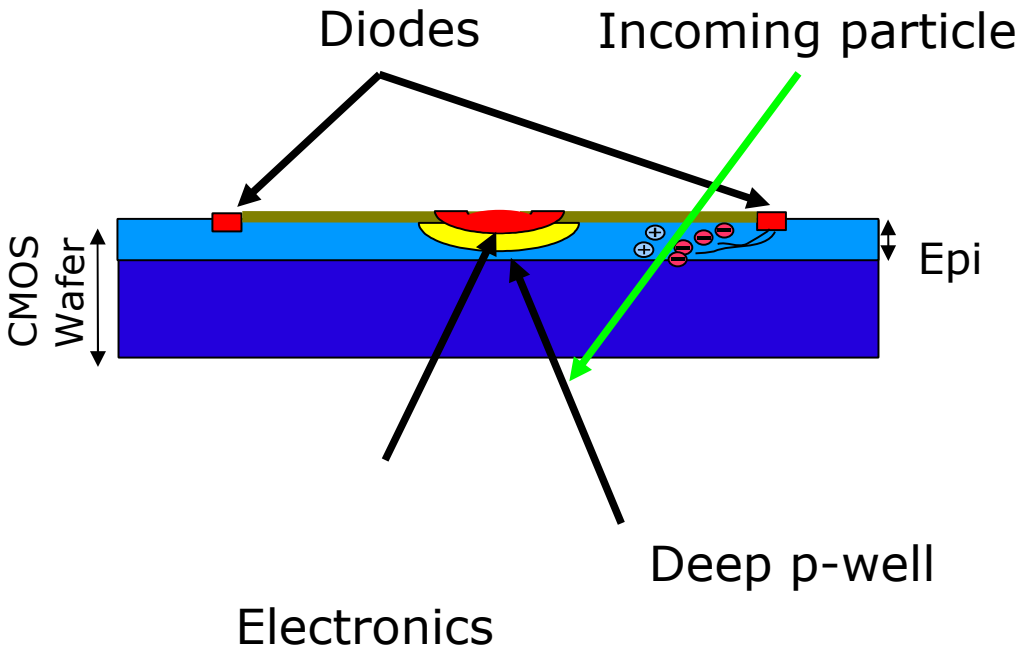


Comparison



What are MAPS ?

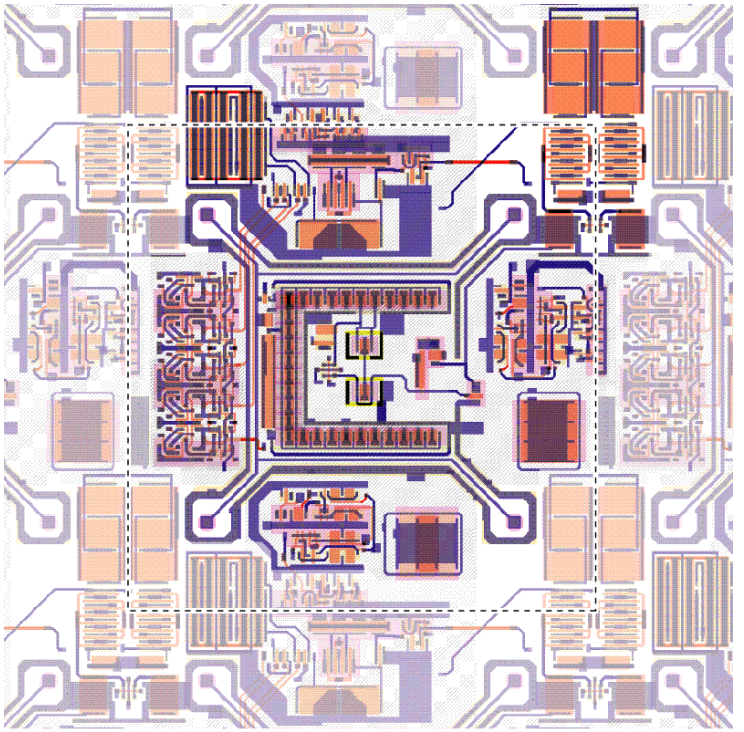
- **M**onolithic **A**ctive **P**ixel **S**ensor
- Integration of Sensor and Readout Electronics
- Manufactured in Standard CMOS process
- Collects charge mainly by diffusion
- Development started in the mid-nineties



Sensor specifications

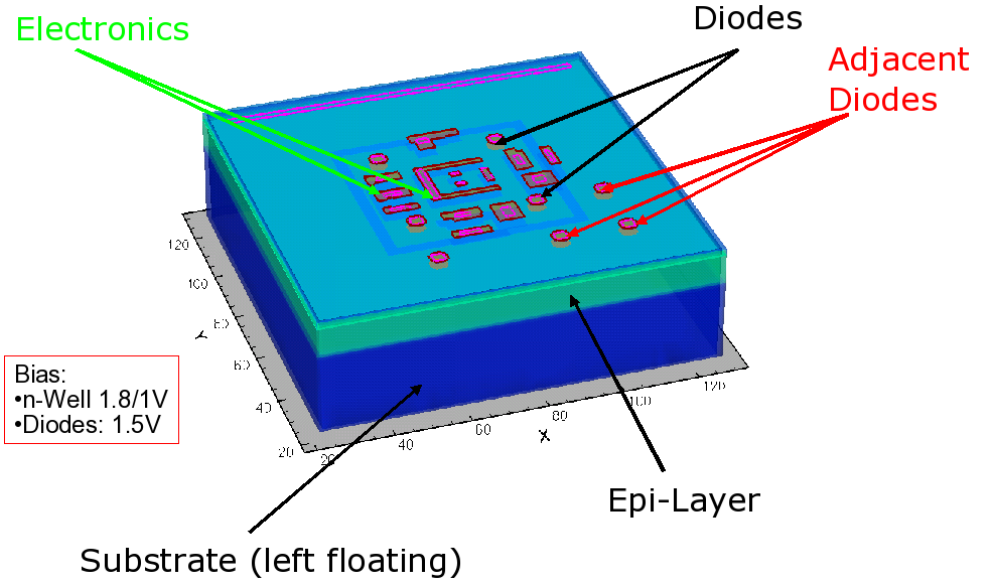
- 50x50 micron cell size
- Binary Readout (Comparator)
- 4 Diodes for Charge Collection
- Time Stamping with 13 bits (8192 bunches)
- Hit buffering for entire bunch train
- Capability to mask individual pixels
- Threshold adjustment for each pixel

⇒Usage of INMAPS (deep-p well) process

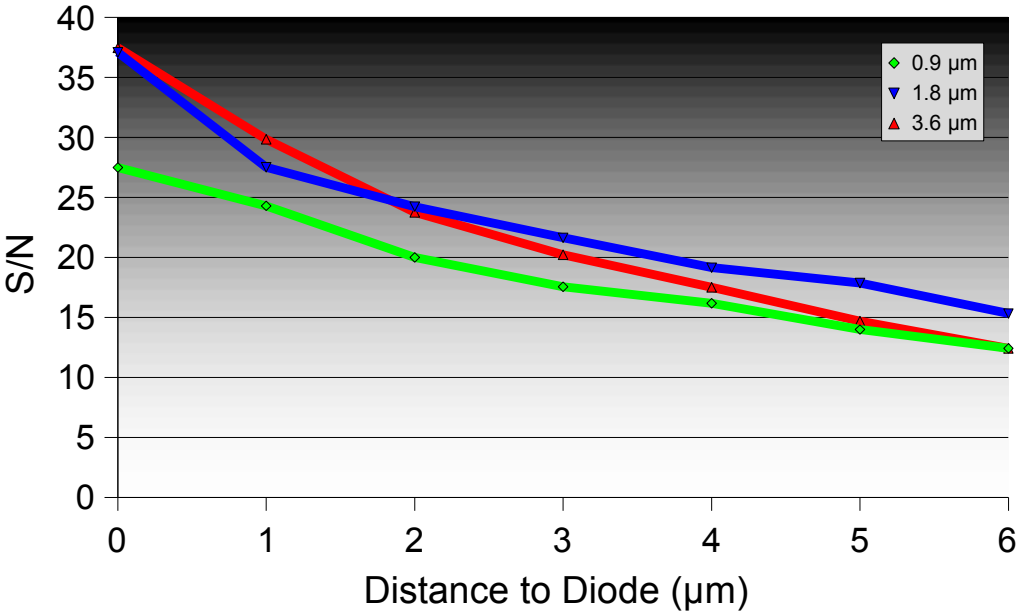


Sensor simulation

- Extensive Simulations using Sentaurus TCAD
- Allows to test many configurations
- Optimize Design parameters
  - Benefits of deep p-well
  - Number of Diodes
  - Diode Size
  - Epilayer thickness

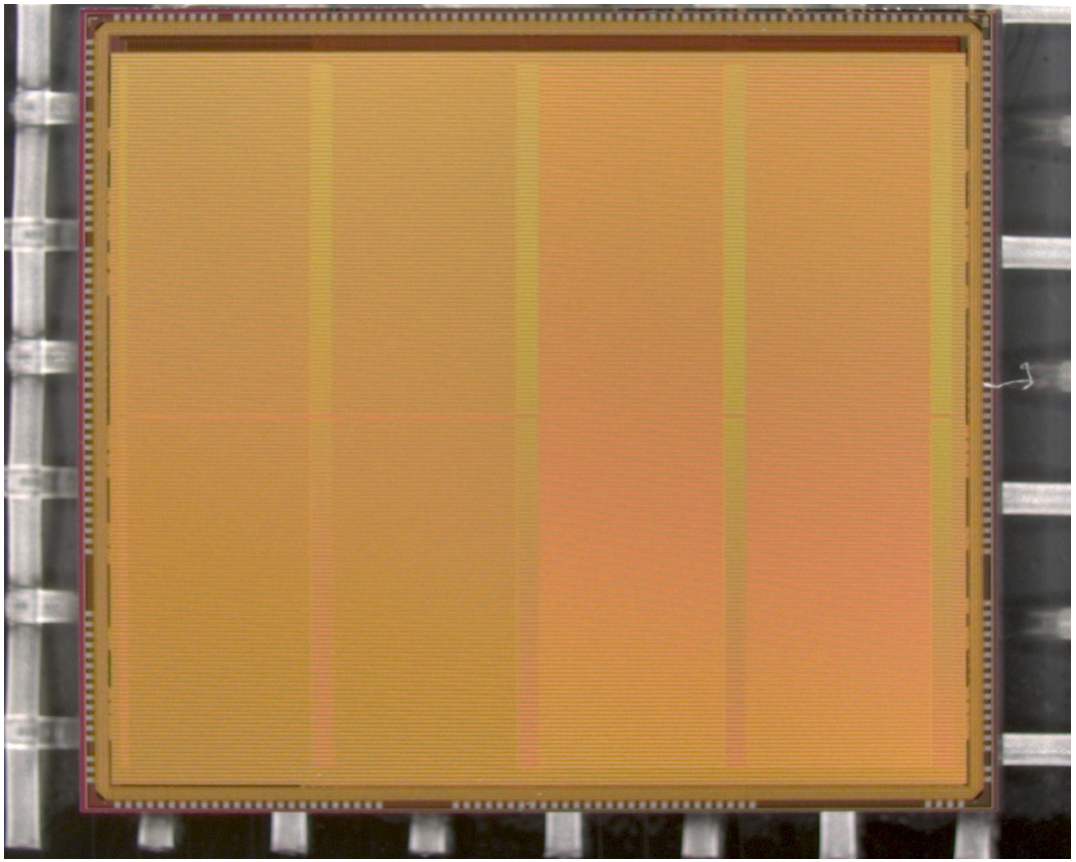


Signal/Noise in the pixel corner



The ASIC1 sensor

- Received in late July
- 0.18 microns CMOS INMAPS Process
- 168x168 Pixels
- 8.2 million transistors
- Test structures
- A lot of bond pads



ASIC1 cont'd

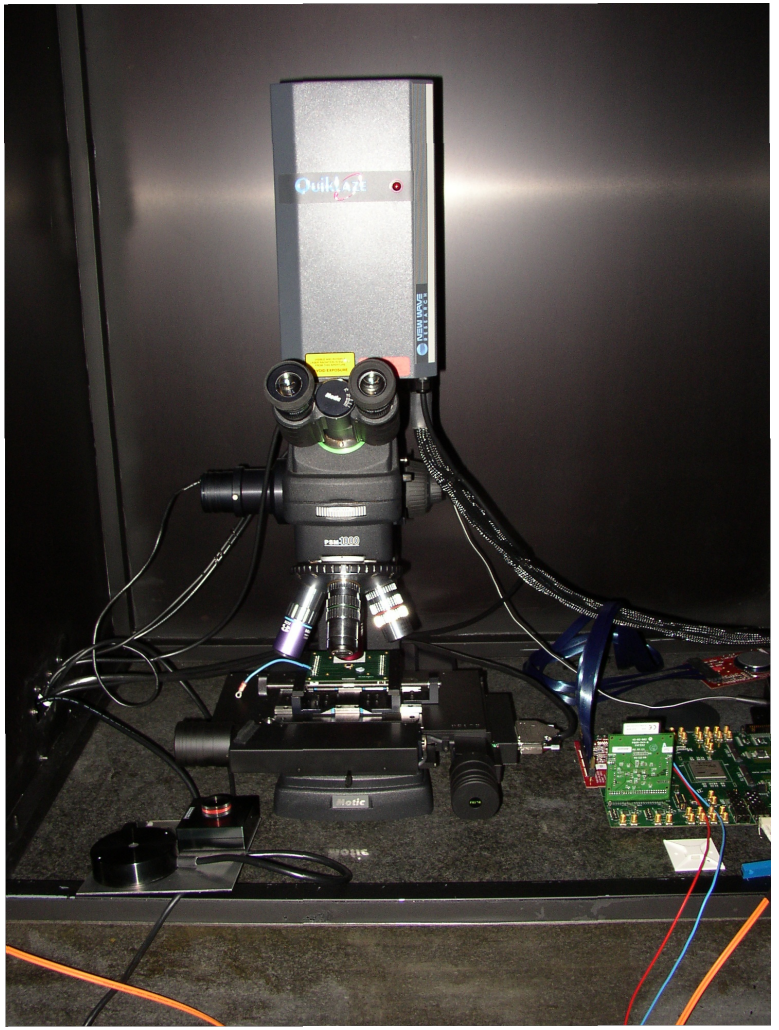
- Two pixel architectures
  - Pre-Sampler
  - Pre-Shaper
- And for two capacitor configurations
  - As there were some issues with the circuit simulation
- 4 flavors of pixels
- 4 different processes
  - INMAPS 0.18 micron with 5/12 micron Epi
  - INMAPS 0.18 micron no deep p-well with 5/12 micron Epi
- Have about 300 chips ....

Sensor testing

- Started testing program using several set-ups
  - Laser setup
    - analog characteristics
    - Pixel tests
  - Source runs with Fe^{55} and Sr^{90}
  - Cosmics
  - Test beam (December 2007)

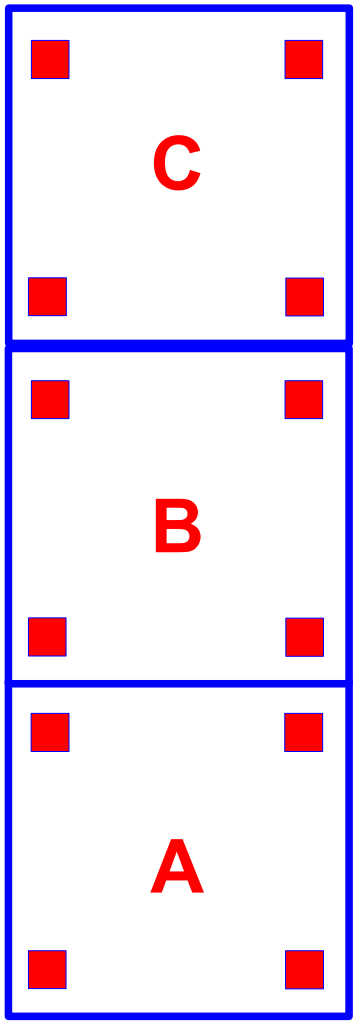
Laser setup

- Powerful Laser setup
- 1064, 532 and 355 nm Wavelength
- Accurate focusing (<2 µm at longest wavelength)
- Pulse Width 4 ns
- 50 Hz Repetition rate
- Fully automatized



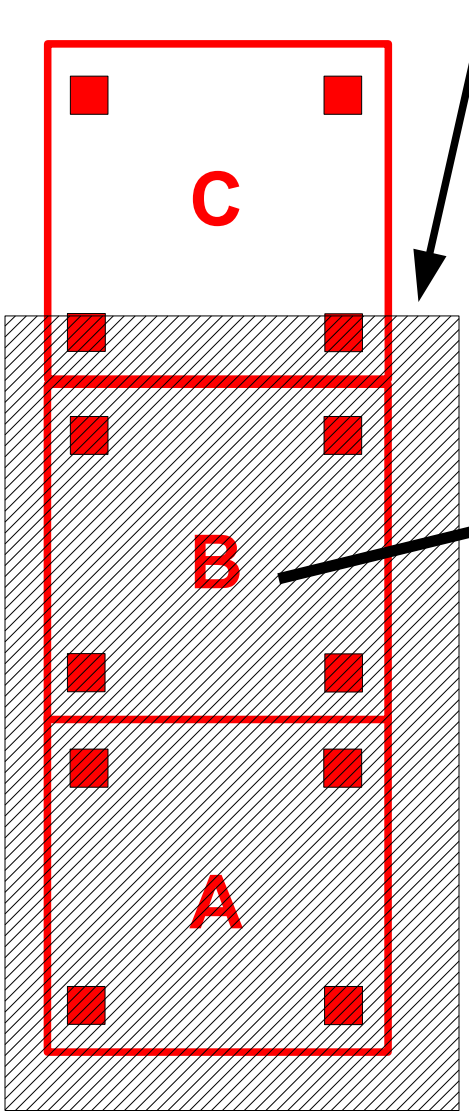
The pixel test structures

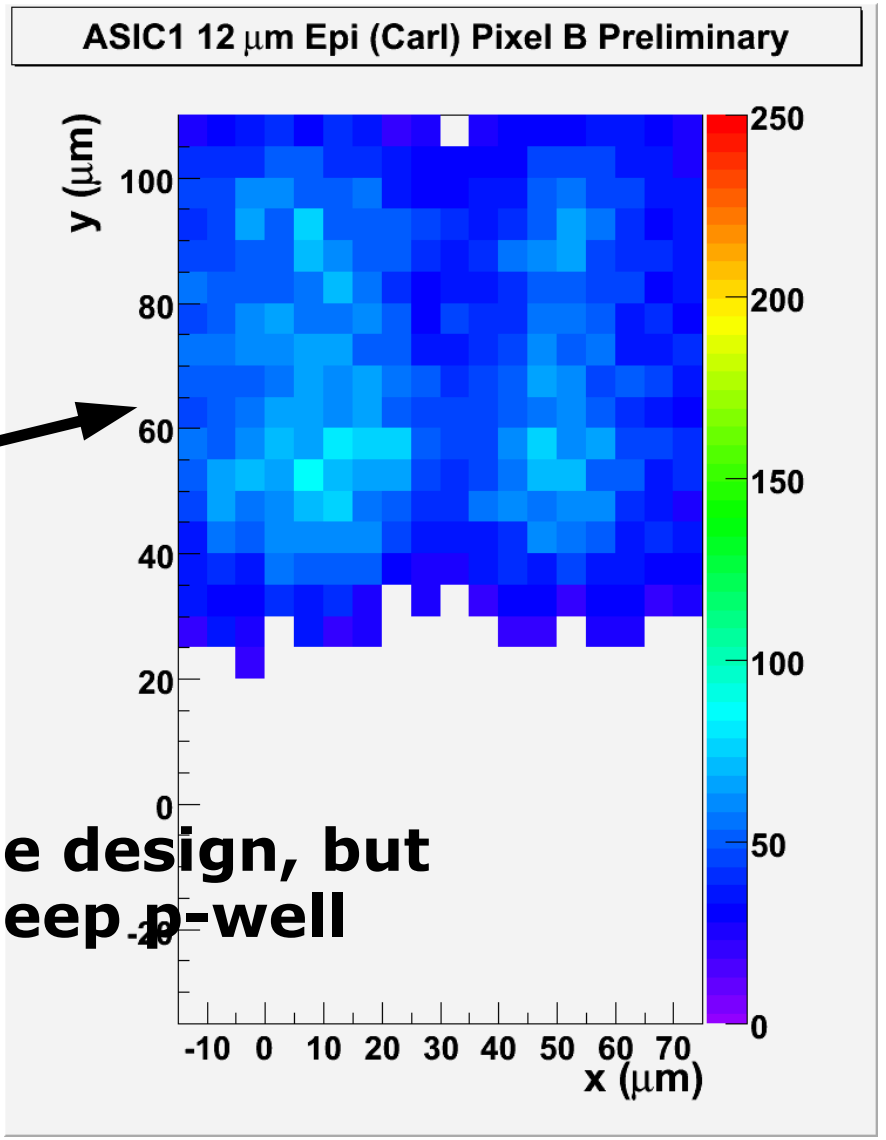
- 2 pixels with analog output (A & B)
- 1 Pixel not active & read out (C)
- Used for
  - Measurement of charge spread
  - Cross-check device simulations
  - Analog front-end testing
  - Gain calibration (to be done)
- All results are **PRELIMINARY**



No deep p-well ...

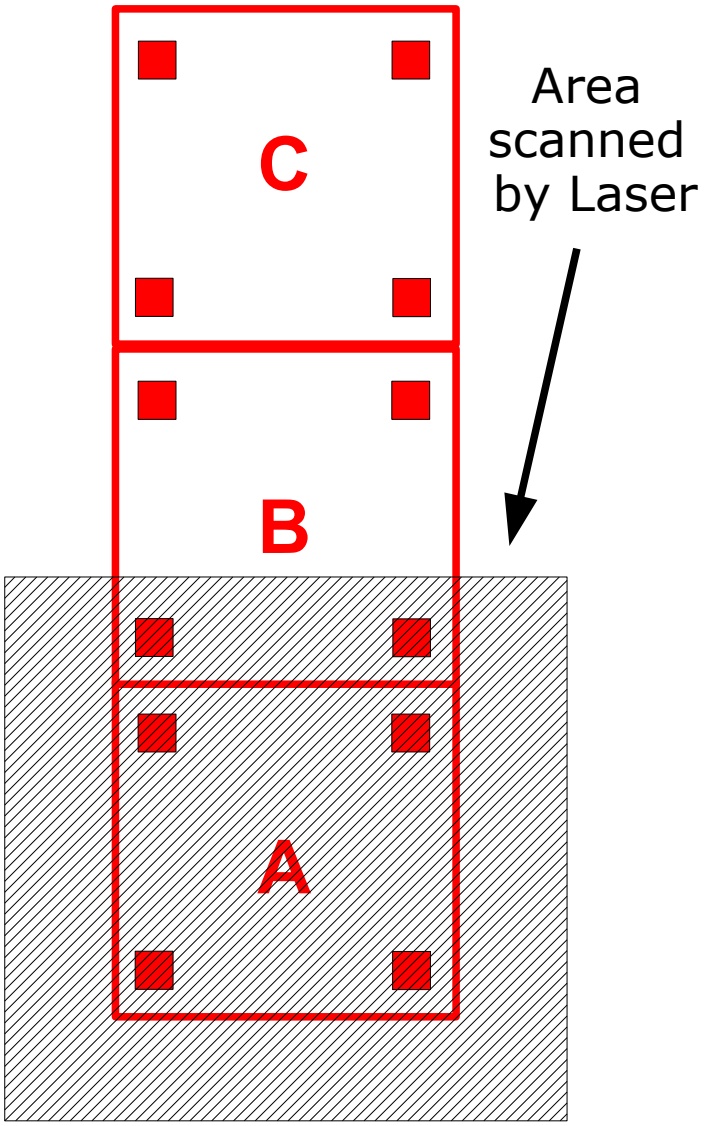
Area scanned by Laser

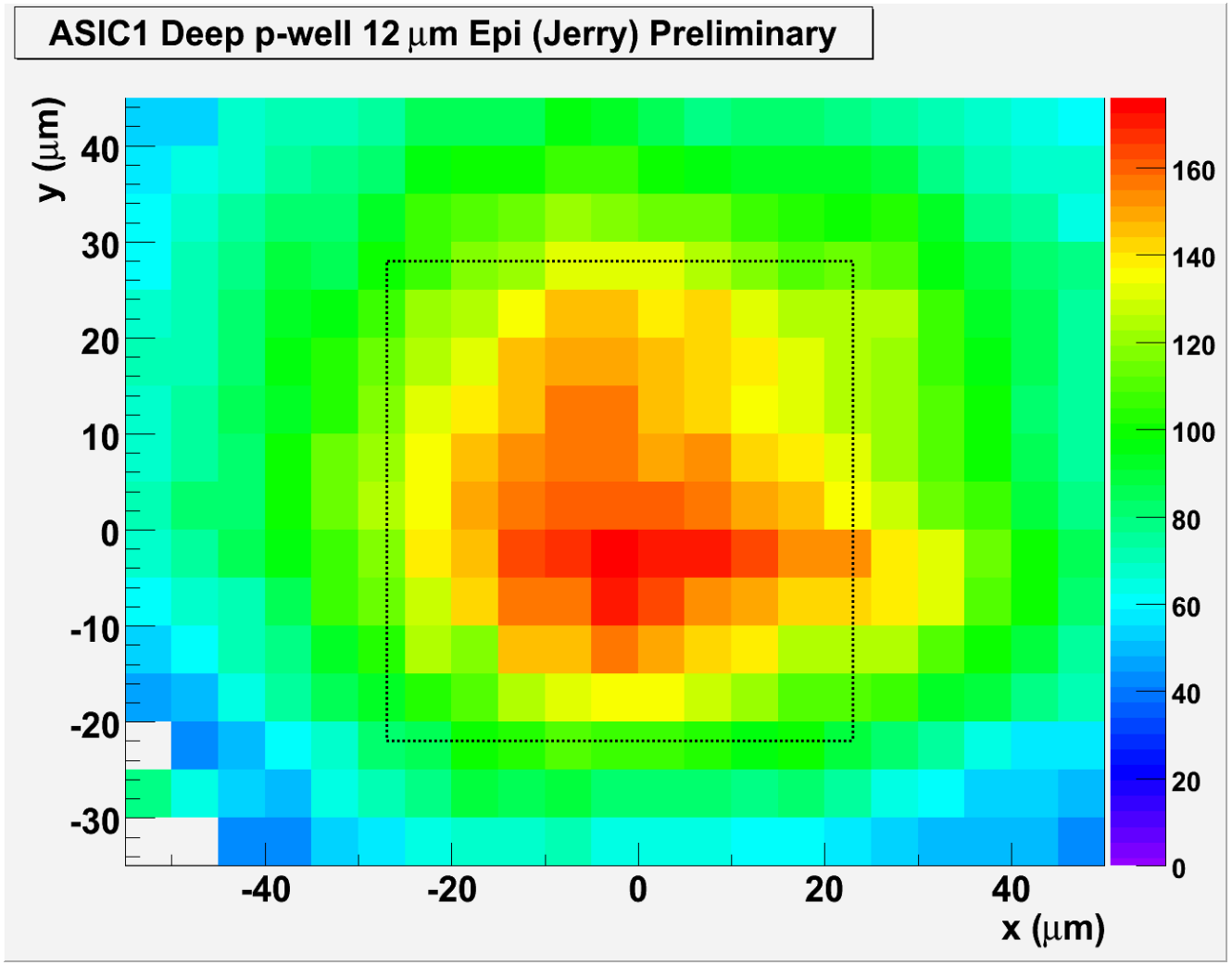




Same design, but no deep p-well

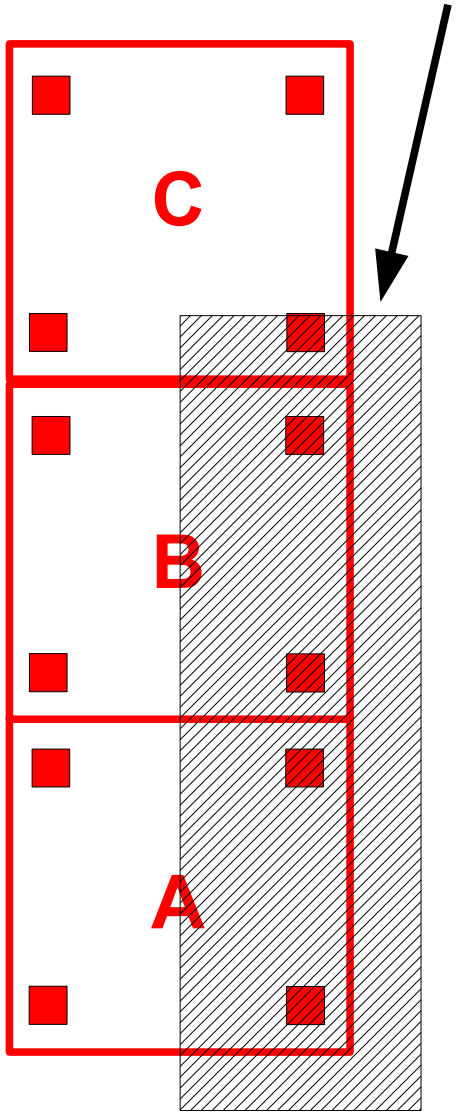
Deep p-well results (I)

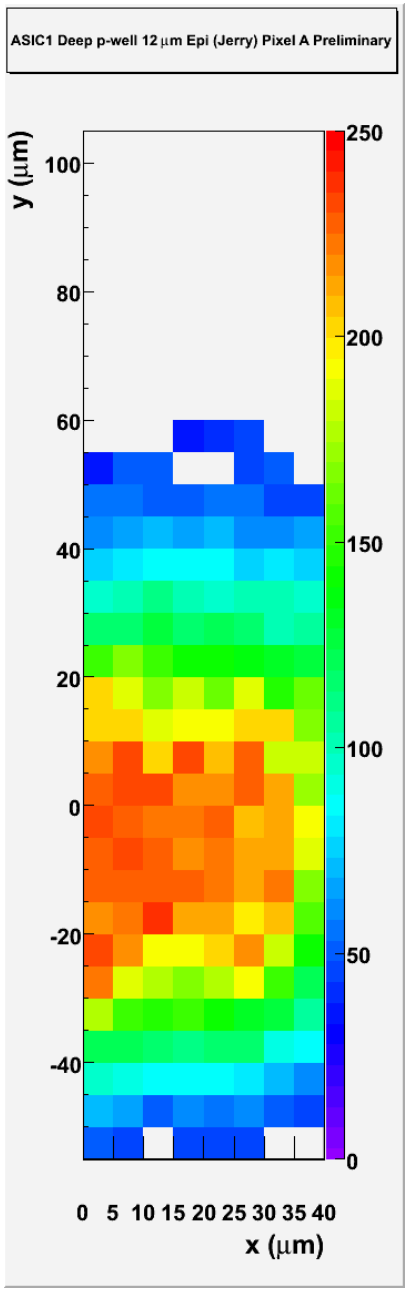


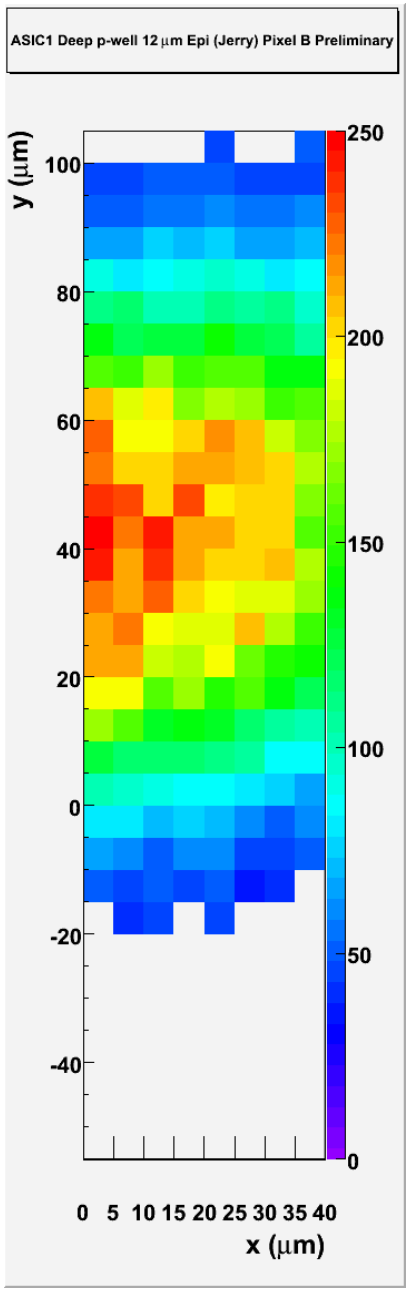


Deep p-well results (II)

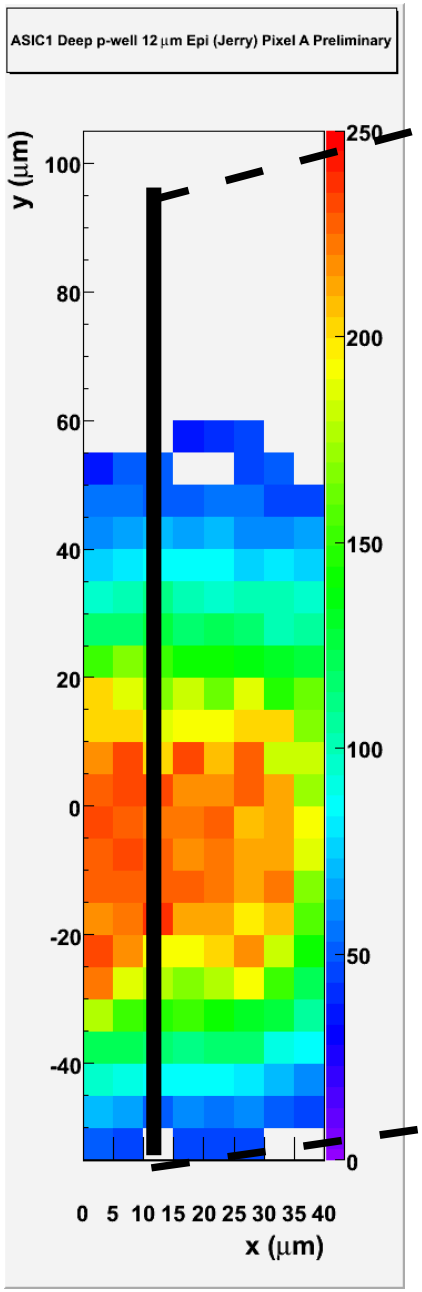
Area scanned by Laser

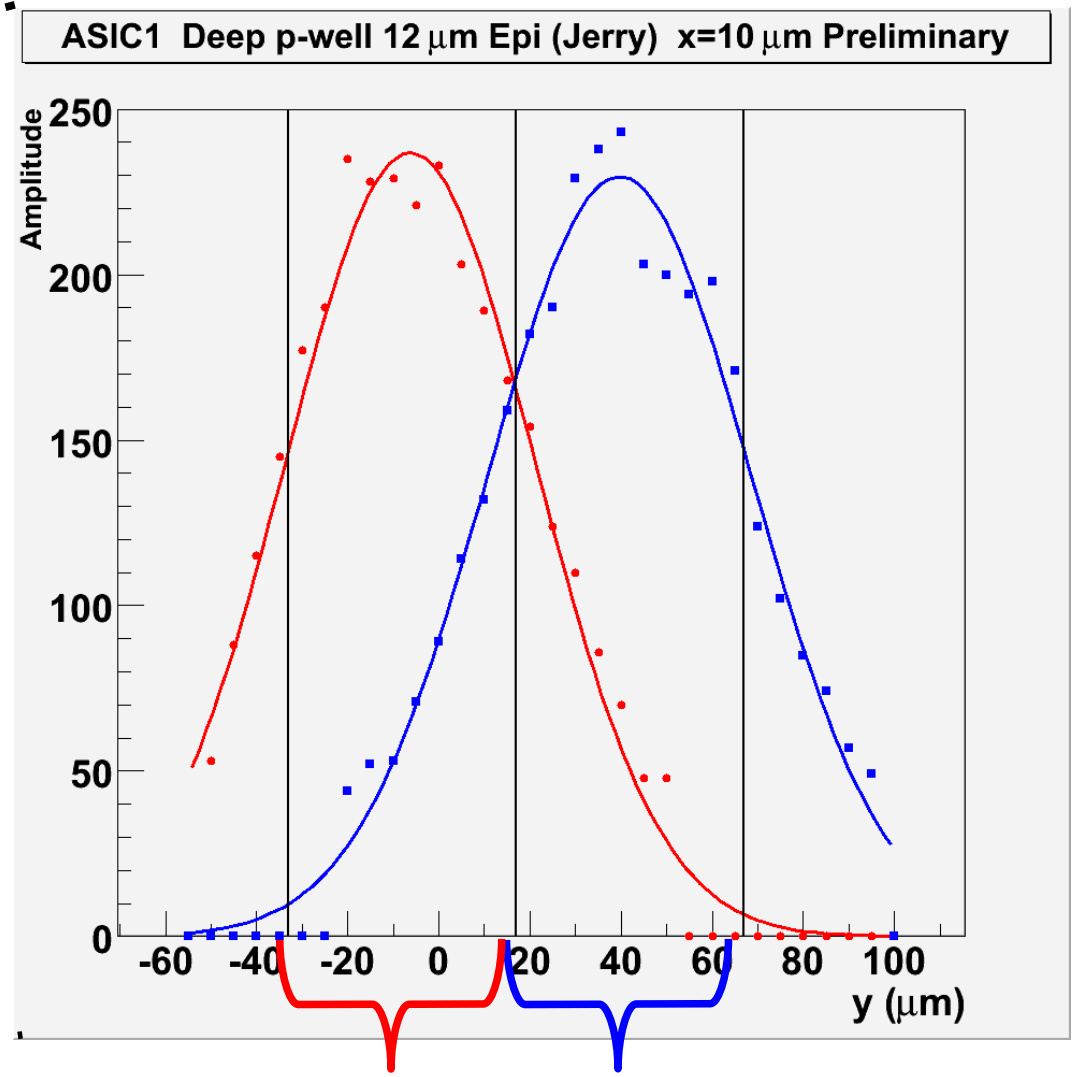






Deep p-well results (III)





Pixel A Pixel B

System issues

- A Tera-Pixel ECAL is challenging
- Benefits
  - No readout chips
  - CMOS is well-know and readily available
  - Ability to make thin layers
- Current sources of concern
  - Power consumption/Cooling
  - DAQ needs

Power

- Cooling for the ECAL is a general issue
- Power Savings due to Duty Cycle (1%)
- Target Value for existing ECAL ASICS
  - 4 $\mu W/mm^2$
- Current Consumption of MAPS ECAL:
  - 40 $\mu W/mm^2$ (From Circuit Simulation)
  - We will measure this.
- Compared to analog pad ECAL
  - Factor 1000 more Channels
  - Factor 10 more power
- Advantage: Heat load is spread evenly

Power prospects

- **ASIC1 has not been optimized for power consumption**
- Proof of Concept: Advanced Design and Technology
- Not the final product
- Options to be explored
  - Longer integrations times if pile-up acceptable, possible factor of 2
  - Lowering Operating Voltages (~10%)
  - Power pulsing
  - *Smaller feature size (~30-50 %)*
  - *Larger pixel (50 µm->100 µm) Factor 4 less*
- ASIC1 will allow us to explore some of these

DAQ needs

- O(10^{12}) channels are a lot ...
- Physics rate is not the limiting factor
- Beam background and Noise will dominate
- Assuming 2625 bunches and 32 bits per Hit
  - 10^6 Noise hits per bunch
  - ~O(1000) Hits from Beam background per bunch (estimated from GuineaPIG)
- Per bunch train
  - ~80 Gigabit / 10 Gigabyte
  - Readout speed required 400 Gigabit/s
  - CDF SVX-II can do 144 Gigabit/s already

Summary & Outlook

- A Tera-Pixel ECAL is an interesting option for the ILD & SiD:
  - Granularity & Physics possibilities
  - Construction & Cost
- ASIC1 has been manufactured and already gives a proof of principle
  - Test beam data in December 2007
- Larger ASIC2 to be designed and submitted in Mid 2008