Silicon-Tungsten EM Calorimeter R&D

Mani Tripathi
University of California, Davis

ALCPG07
Fermilab
Oct 22-27, 2007

Si/W ECal R&D Collaboration

SLAC: M. Breidenbach, D. Freytag, N. Graf, R. Herbst, G. Haller, J. Jaros

KPiX readout chip, downstream readout, simulations, mechanical design and integration

U. Oregon: J. Brau, R. Frey, D. Strom, undergraduates.

Detector development, readout electronics

UC, Davis: B. Holbrook, R. Lander, M. Tripathi, undergraduates.

Flex cable development, bump bonding

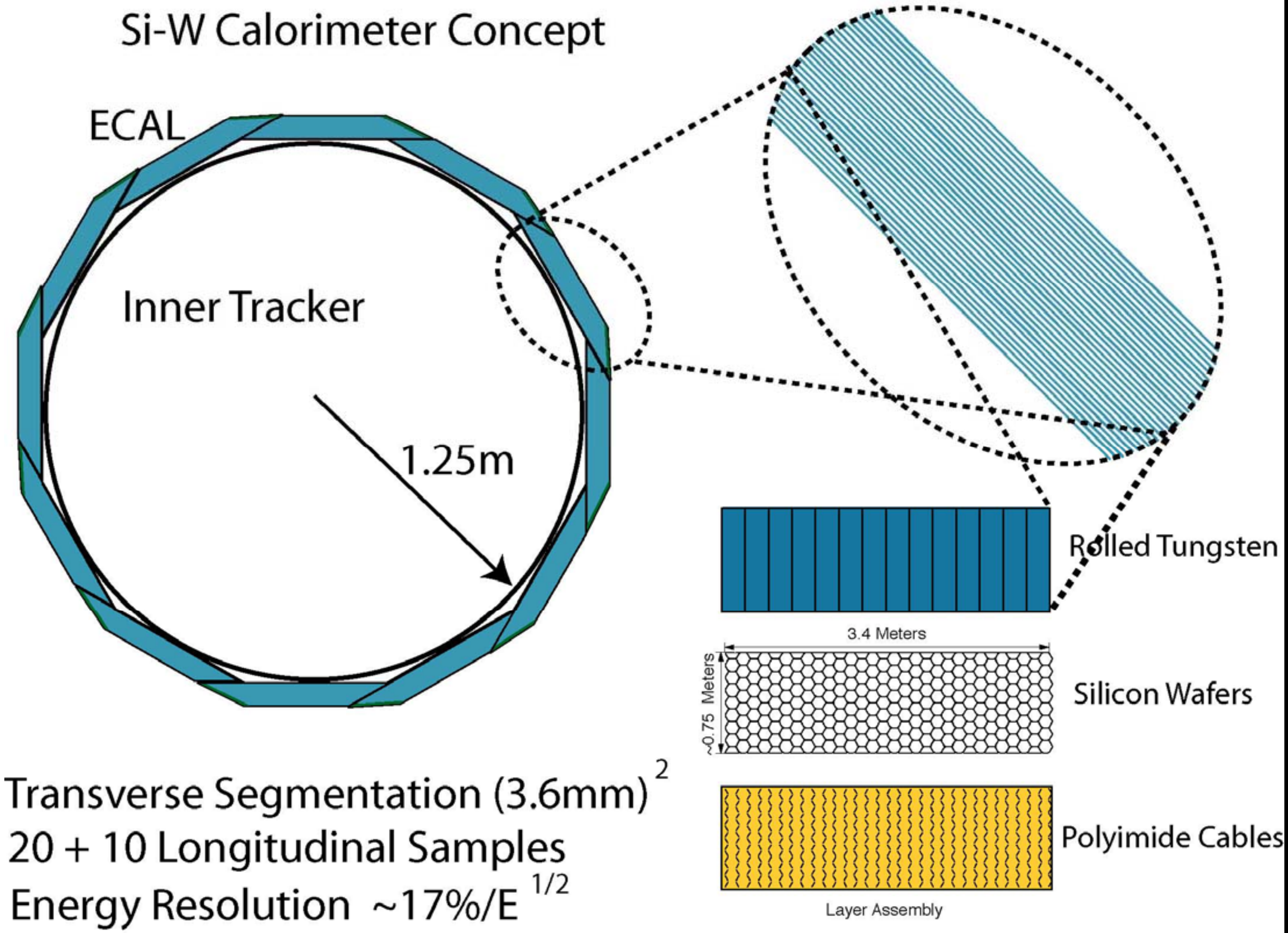
BNL: V. Radeka

Readout electronics

LAPP Annecy: S. Adloff, F. Cadoux, J. Jacquemier, Y. Karyotakis

Mechanical design and integration

Si-W Calorimeter Concept



Baseline configuration:

- transverse seg.: 13 mm^2 pixels
- longitudinal seg:

(20 x 5/7 X_0)
+ (10 x 10/7 X_0)

⇒ **17%/sqrt(E)**

- 1 mm readout gaps

⇒ **13 mm effective Moliere radius**

Currently optimized for the SiD concept

Goals of the R&D

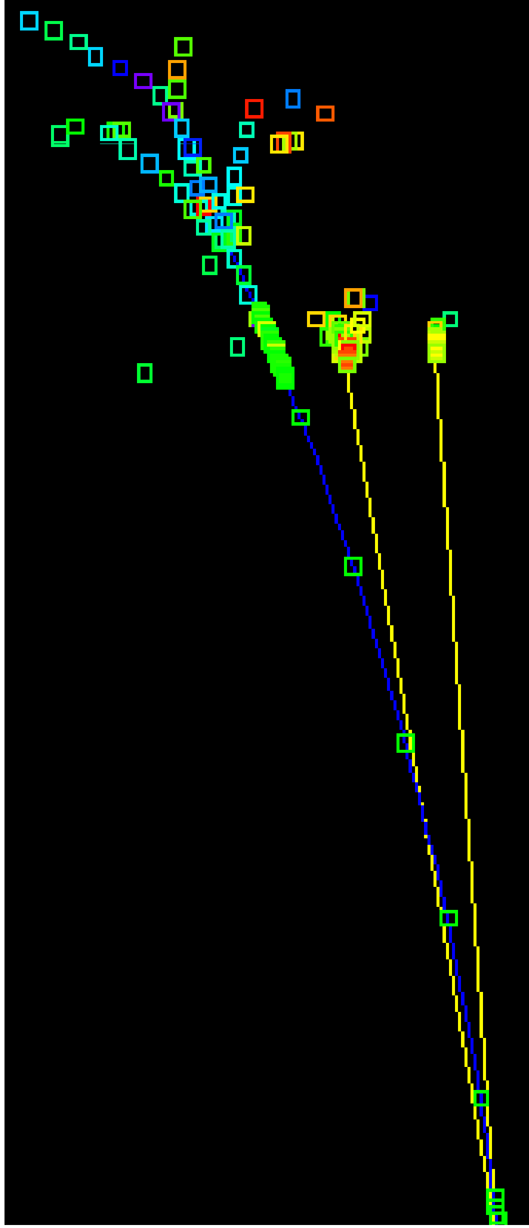
<u>The ILC needs a practical ECal which meets (or exceeds) the stringent physics requirements using a proven technology.</u>

- The physics case calls for a dense (small R_m), highly segmented "imaging calorimeter" with modest EM energy resolution

  $\Rightarrow$ W-Si pixel sampling calorimeter

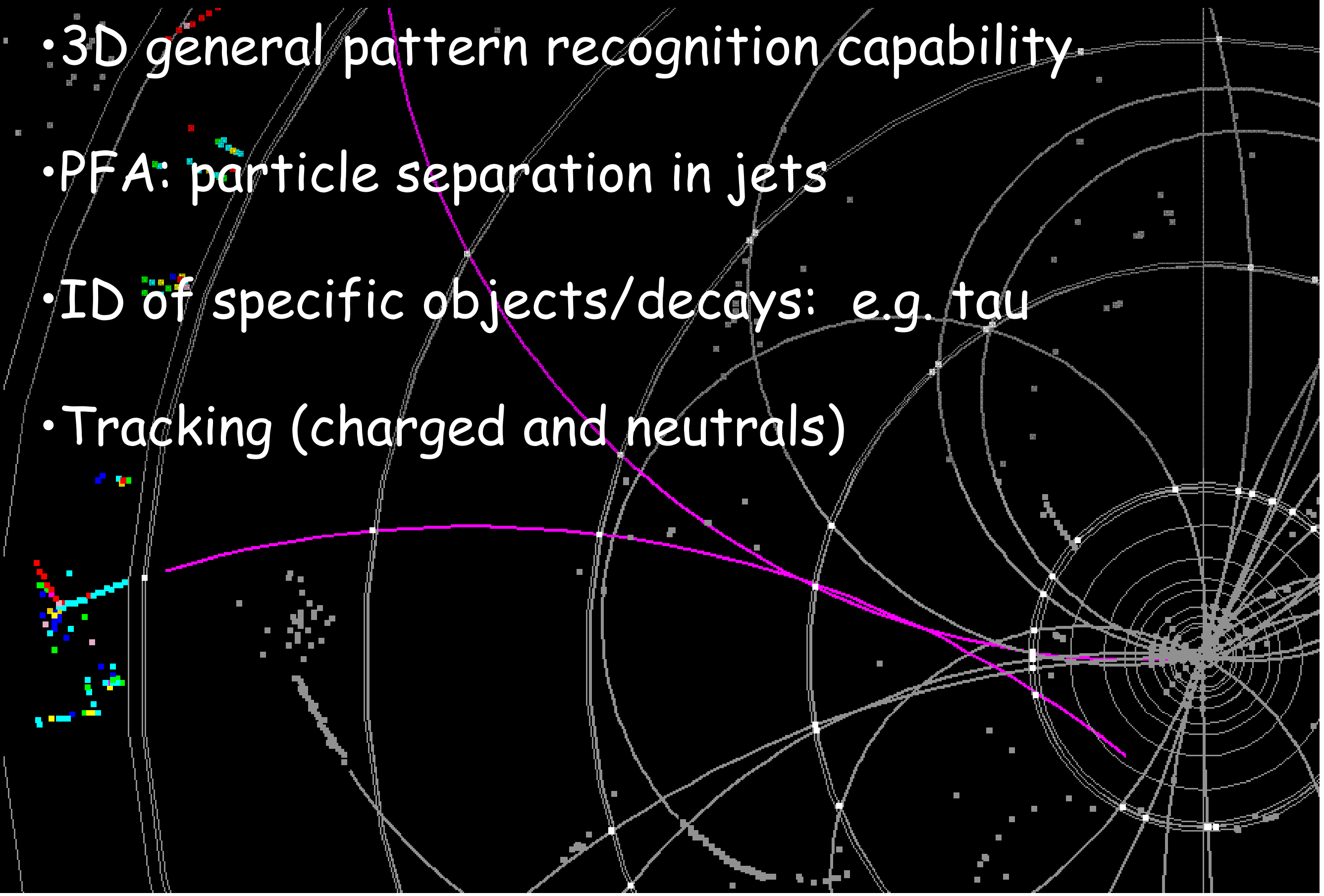
- The key to making this practical is a <u>highly integrated electronic readout:</u>
  - readout channel count = pixel count /~1000
  - cost ≈ independent of cost for segmentation > 2-3 mm
    - 3.6 mm is current default
  - allows for a small readout gap (1 mm) $\Rightarrow$ small effective R_M (13 mm)
  - Low power budget (passive cooling)
  - Large dynamic range of energy depositions (few thousand)

An “Imaging Calorimeter”



High Degree of Segmentation ⇒

- 3D general pattern recognition capability
- PFA: particle separation in jets
- ID of specific objects/decays: e.g. tau
- Tracking (charged and neutrals)



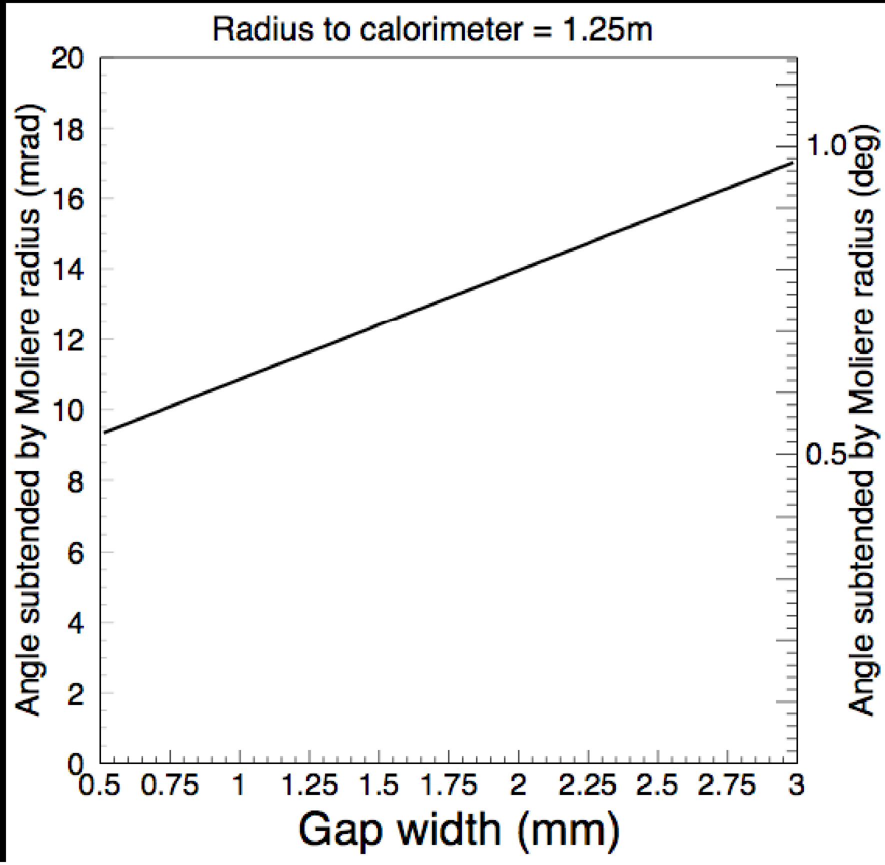
Segmentation requirement

- In general, we wish to resolve individual photons from jets, tau decays, π^0 decays etc.
- The resolving power depends on Moliere radius and segmentation.
- We want segmentation significantly smaller than R_M

Config.	Radiation length	Molière Radius
100% W	3.5mm	9mm
92.5% W	3.9mm	10mm
+1mm gap	5.5mm	14mm
+1mmCu	6.4mm	17mm

Assumes 2.5mm thick tungsten absorber plates

Critical parameter for R_M is the gap between layers.

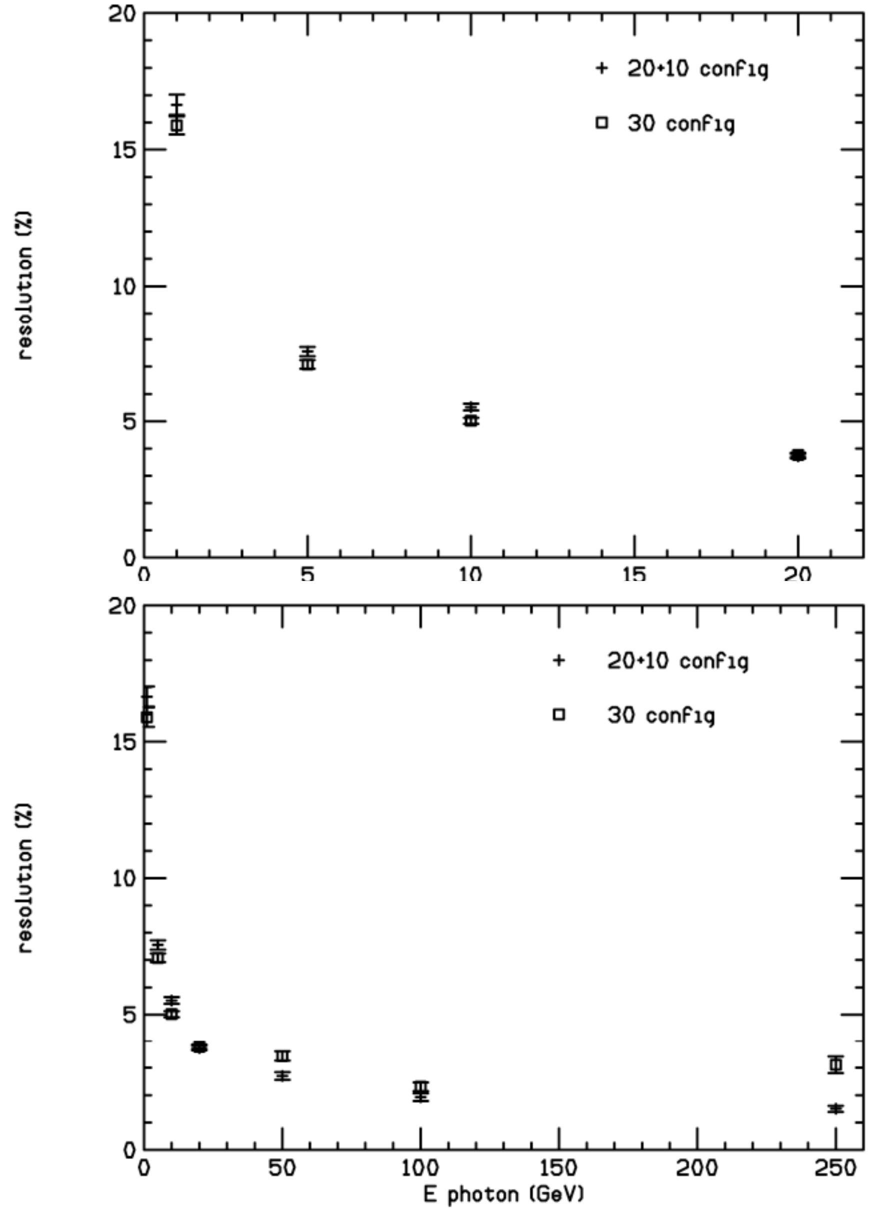


Longitudinal Sampling

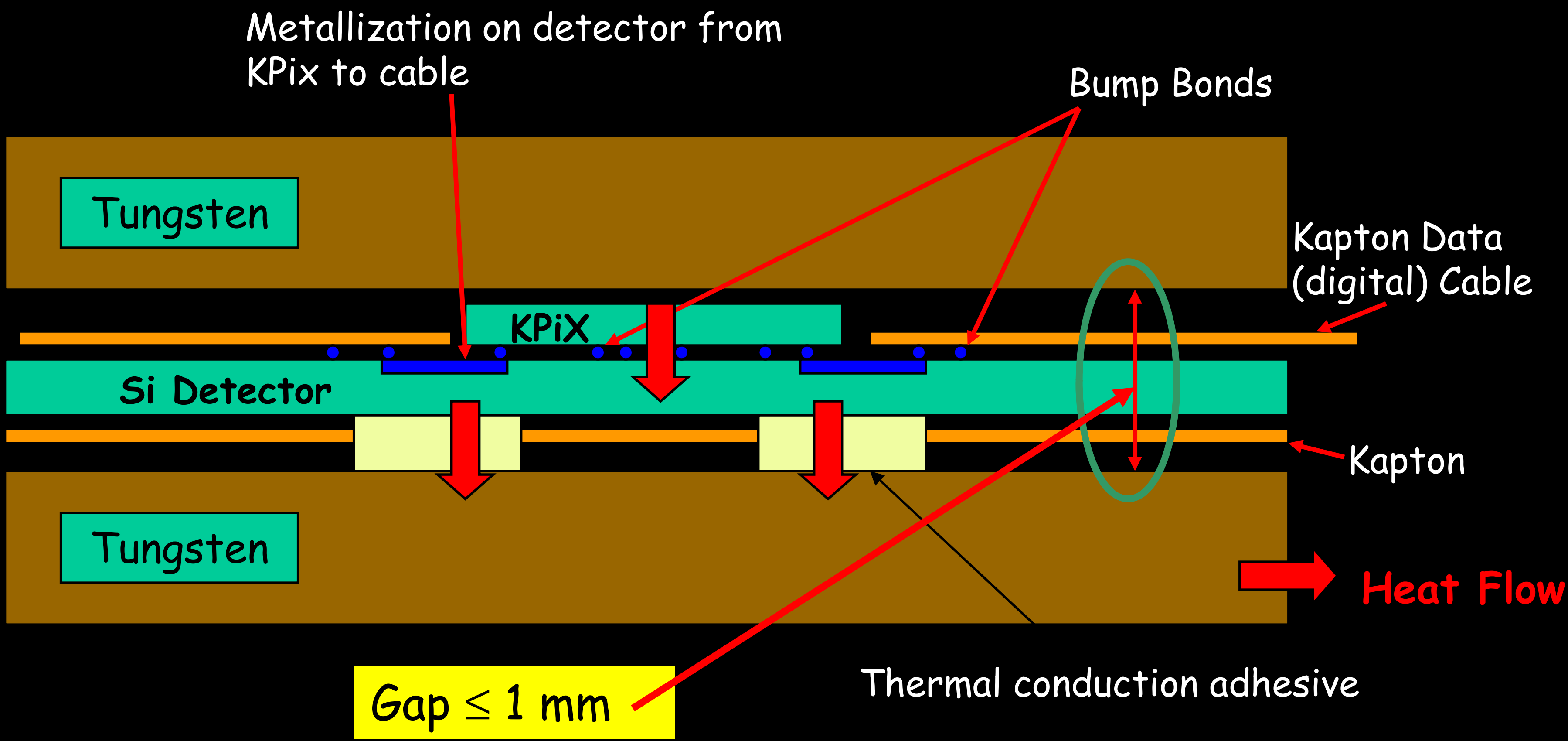
Compare two tungsten configurations:

- 30 layers x 5/7 X_0
- (20 x 5/7 X_0) + (10 x 10/7 X_0)

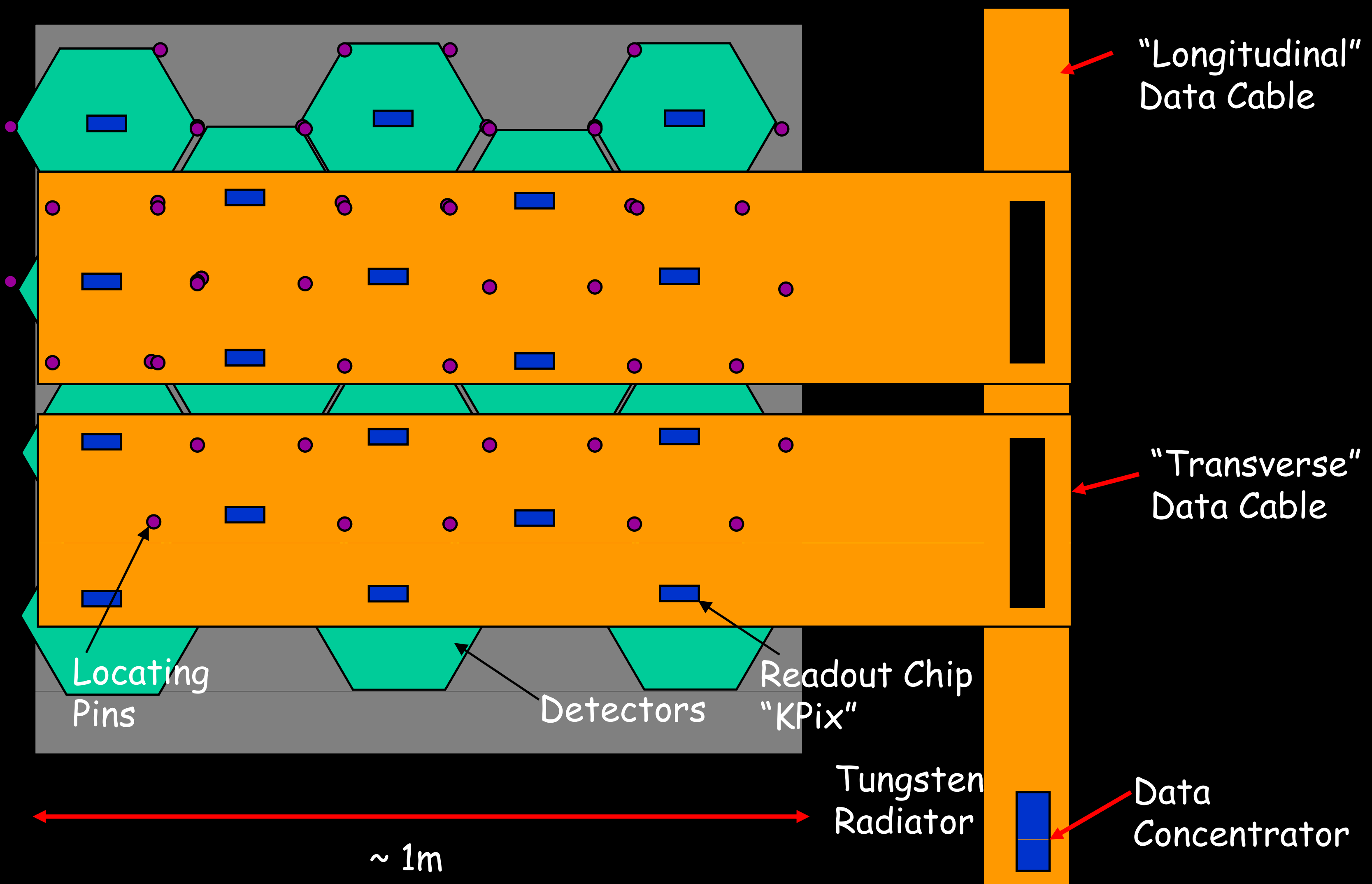
- Resolution is 17% / √E , nearly the same for low energy (photons in jets)
- Better for the 20+10 configuration at the highest energies (leakage) ⇒ adopt as baseline



Readout gap cross section (schematic)

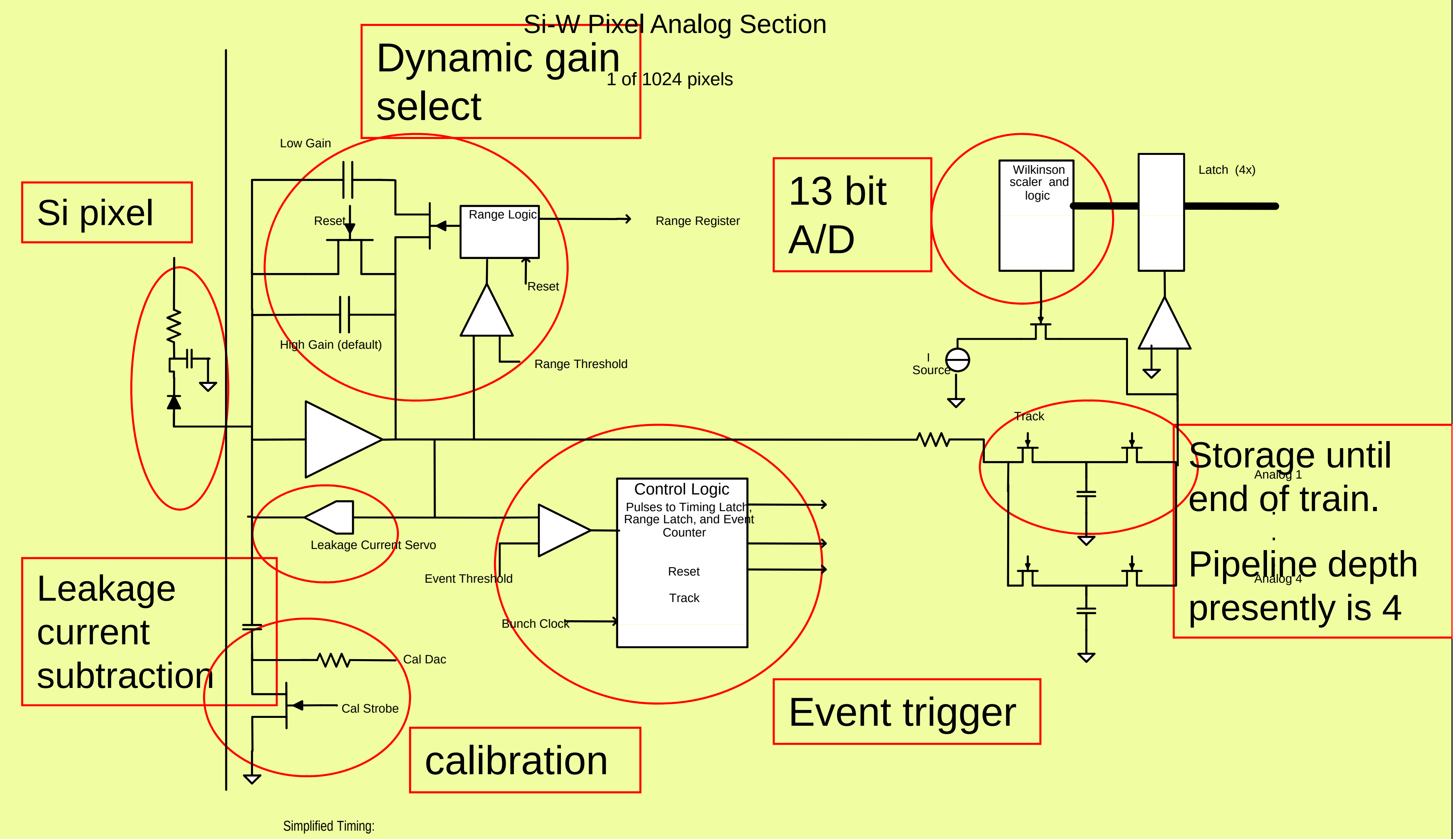


Conceptual Schematic



(Not to scale)

KPiX Unit Cell: Analog Section



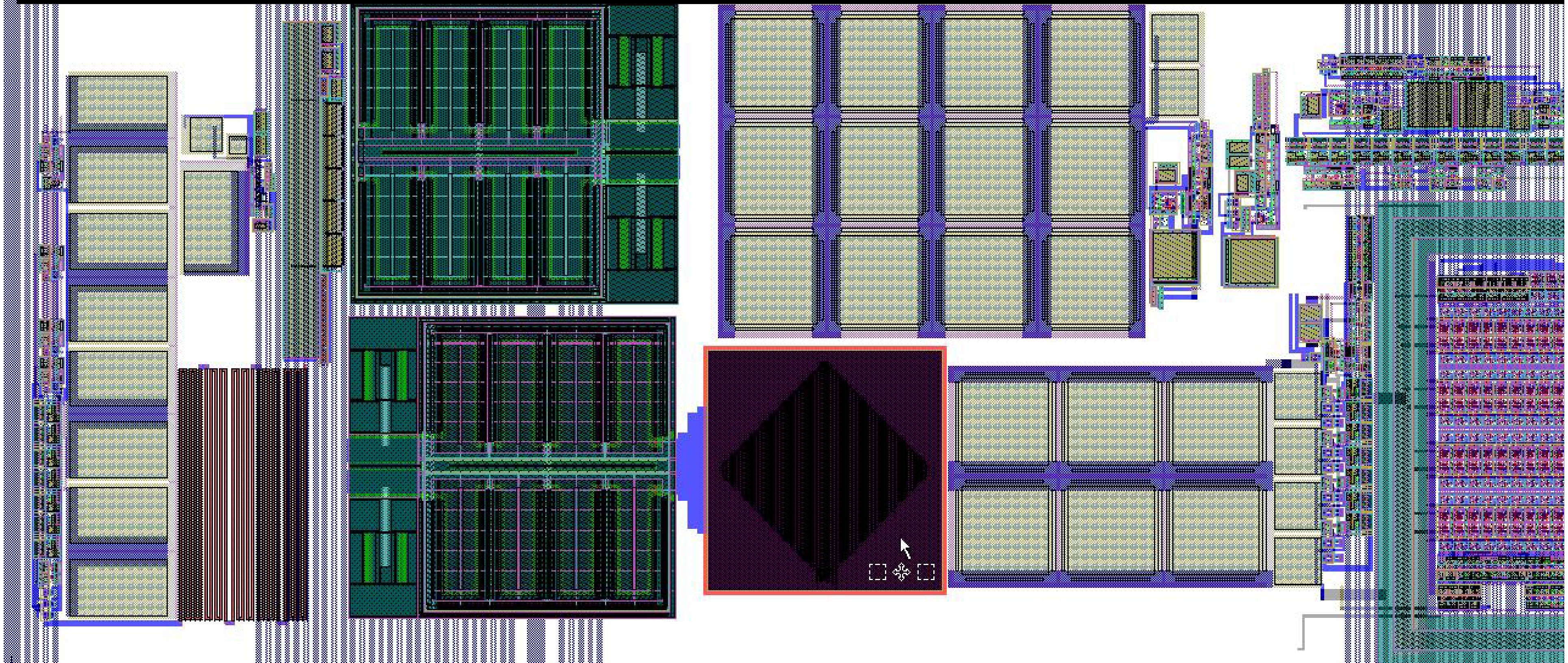
- KPiX also being considered for Si tracker and DHCal with GEMs

Electronics requirements

- Signals
  - <2000 e noise
  - Require MIPs with S/N > 8
  - Large dynamic range: Max. signal is ≈2500 MIPs (for 5mm pixels)
- Capacitance
  - Pixels: 5.7 pF
  - Traces: ~0.8 pF per pixel crossing
  - Crosstalk: 0.8 pF/Gain x Cin < 1%
- Resistance (traces)
  - 300 ohm max
- Power
  - If < 40 mW/wafer ⇒ allows passive cooling (as long as power is cycled off between bunch trains)
- Provide fully digitized, zero suppressed outputs of charge and bx time on one ASIC for every wafer.

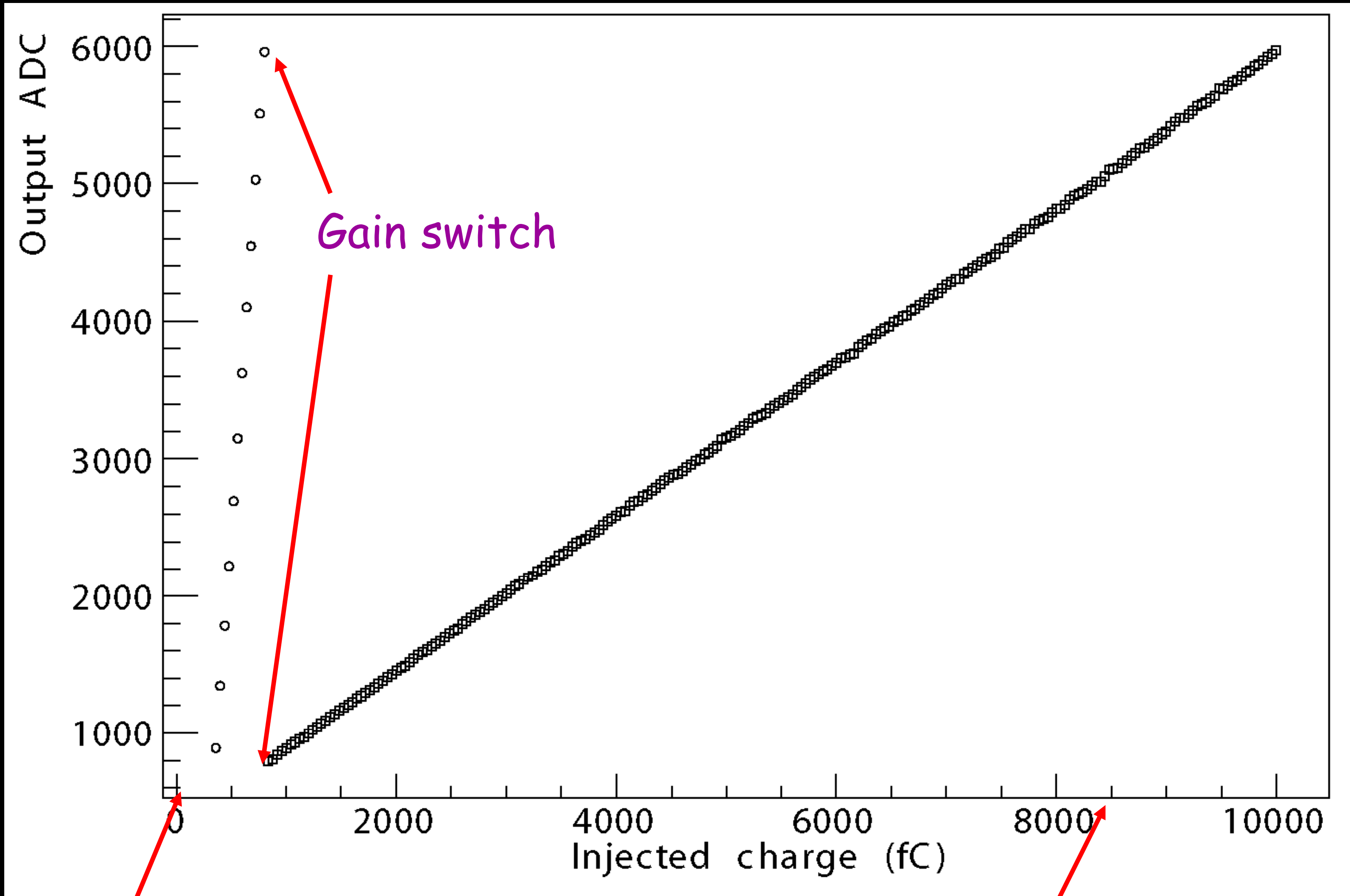
Unit Cell of KPiX

Complexity and A large number of functions => several rounds of prototyping.



A 64-channel prototype (version 5) is currently under test

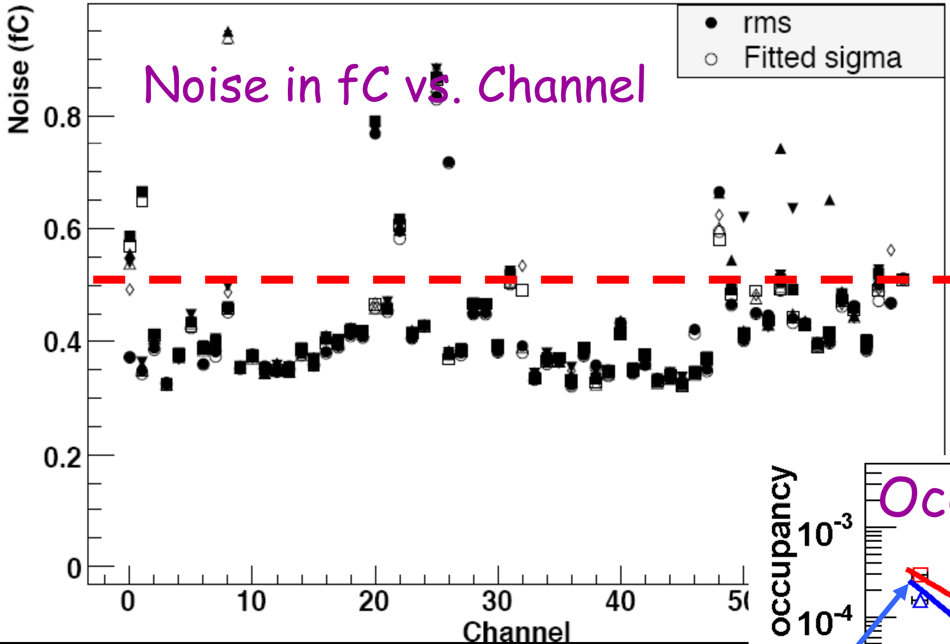
Dynamic Range



1 MIP (3.9 fC)

Max signal: 500 GeV electron

Noise in KPiX-4

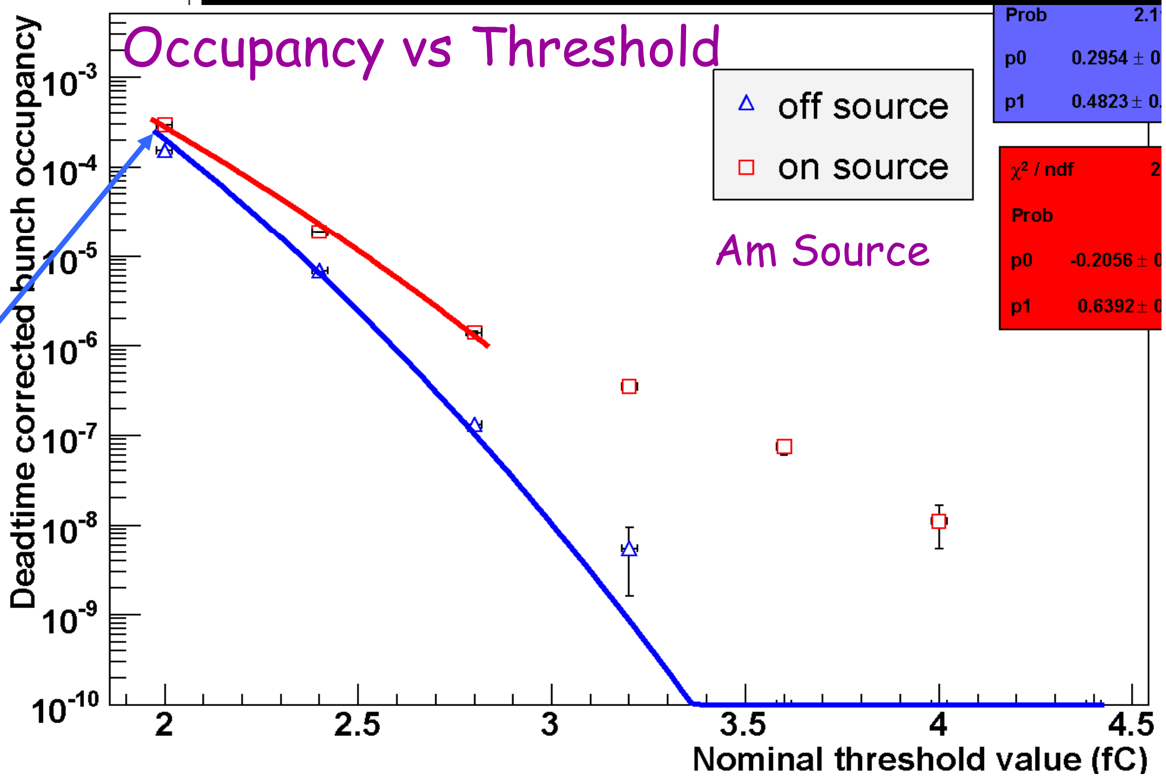


1 MIP = 3.9 fC
ECal S/N Spec is 8/1

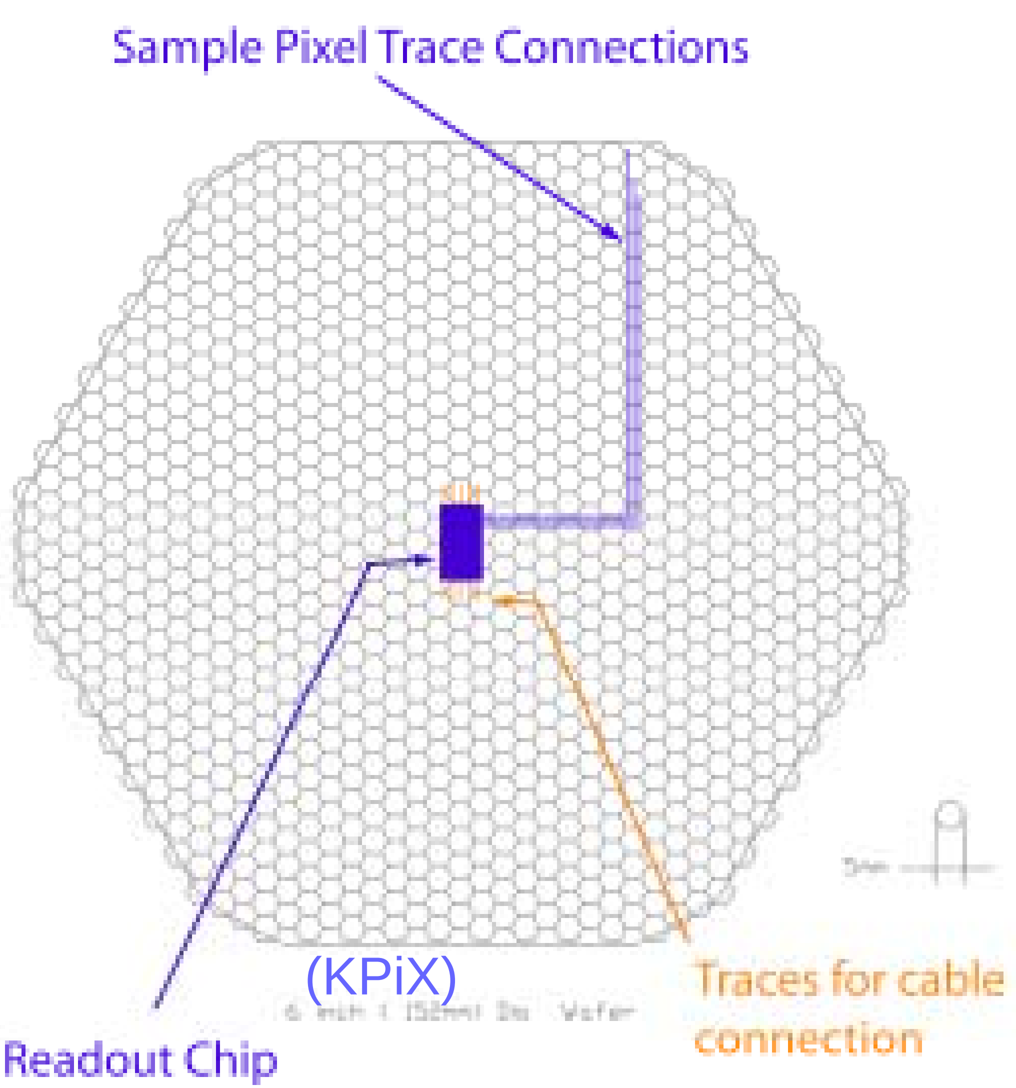
⇒ Noise should be below (~0.5 fC)
(Need to understand outliers)

- Power ~ 20 mW!
- (ECal spec is < 40 mW)
- Noise is Gaussian (~2x10^{-4} @ 2 fC)

Can set threshold @ ~0.5 fC



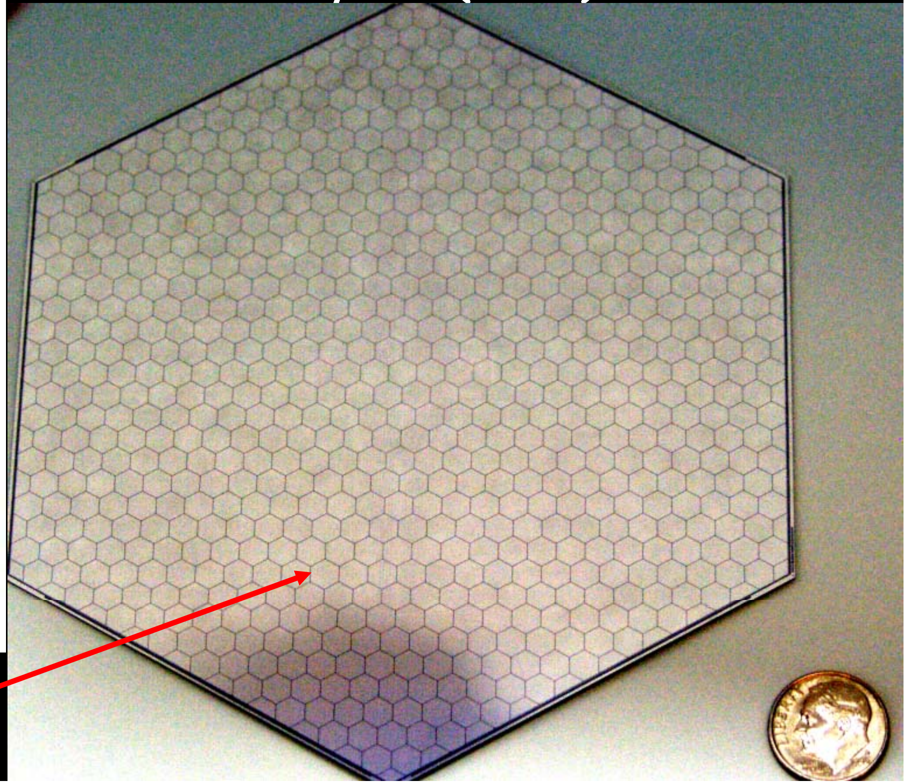
Si detector: layout & segmentation



One KPiX readout chip for the sensor (1024 pixels, 6 inch wafer)

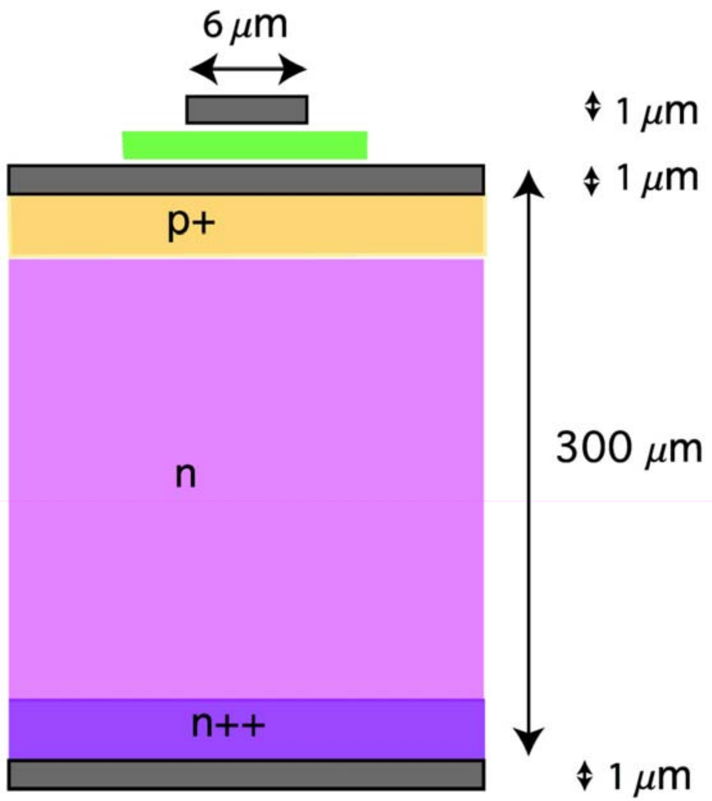
Limit on segmentation from chip power (~20 mW per chip).

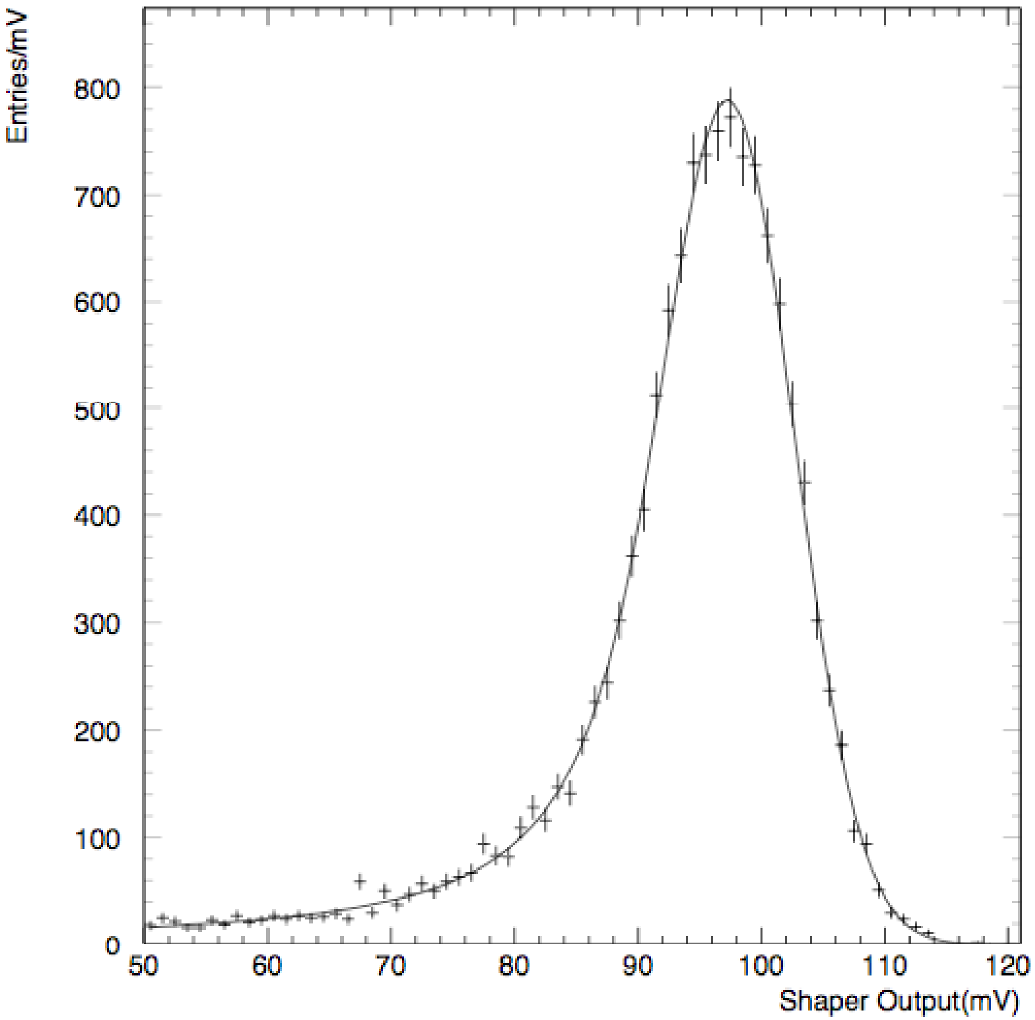
Use DC-coupled detectors: only two metal layers (cost)



Fully functional v1 prototype (Hamamatsu)

Response of Detectors to 60KeV Gamma's from Am241

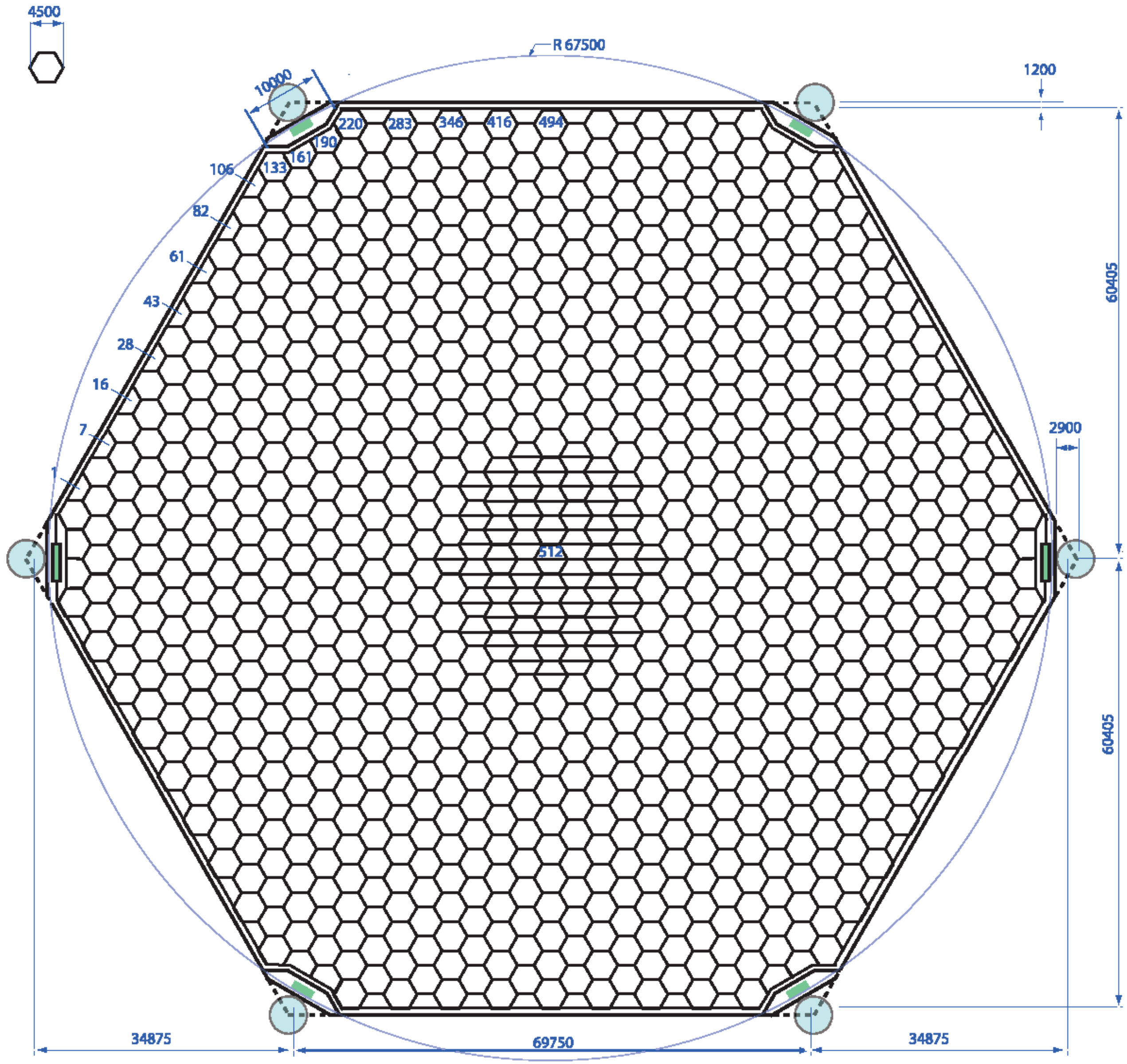




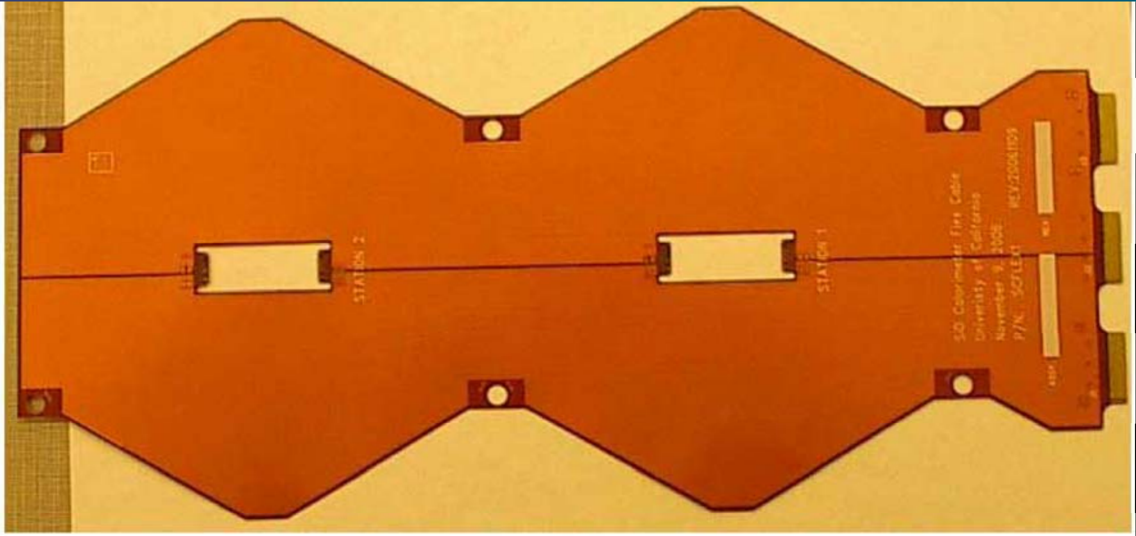
Possible ~1% wafer-wafer calibration?

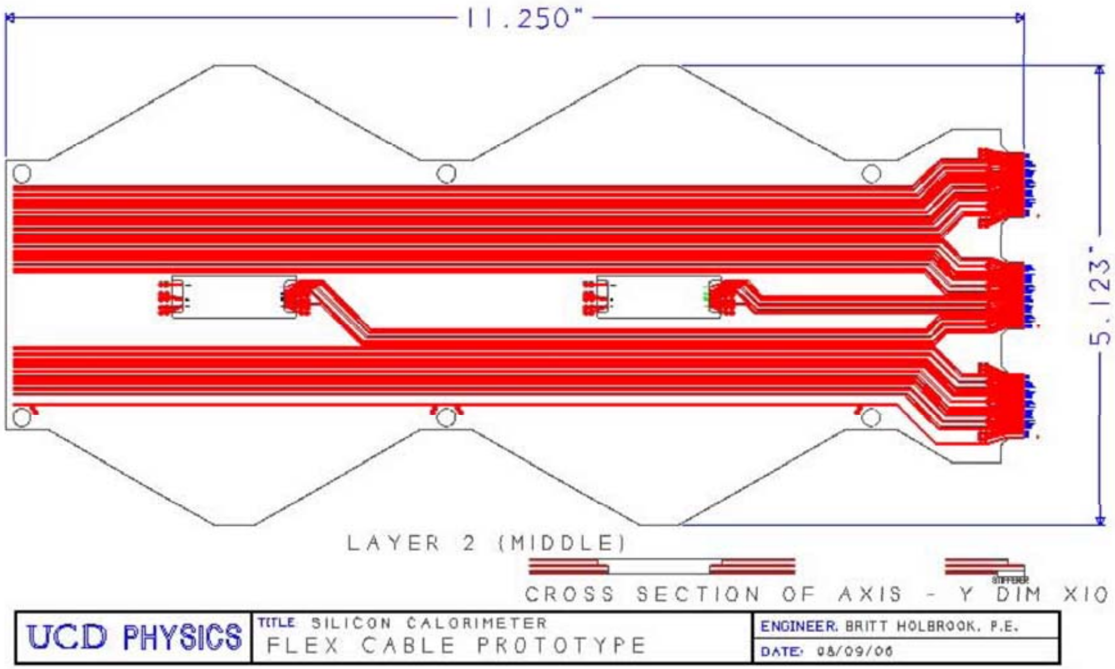
Si detector –Version 2

- Intended for full-depth test module
- 6 inch wafer
- 1024 13 mm² pixels
- Improved trace layout near KPiX to reduce capacitance
- Procurement in progress (it will take 6-12 months to complete the 40-wafer purchase – funding limited)



Readout flex cable





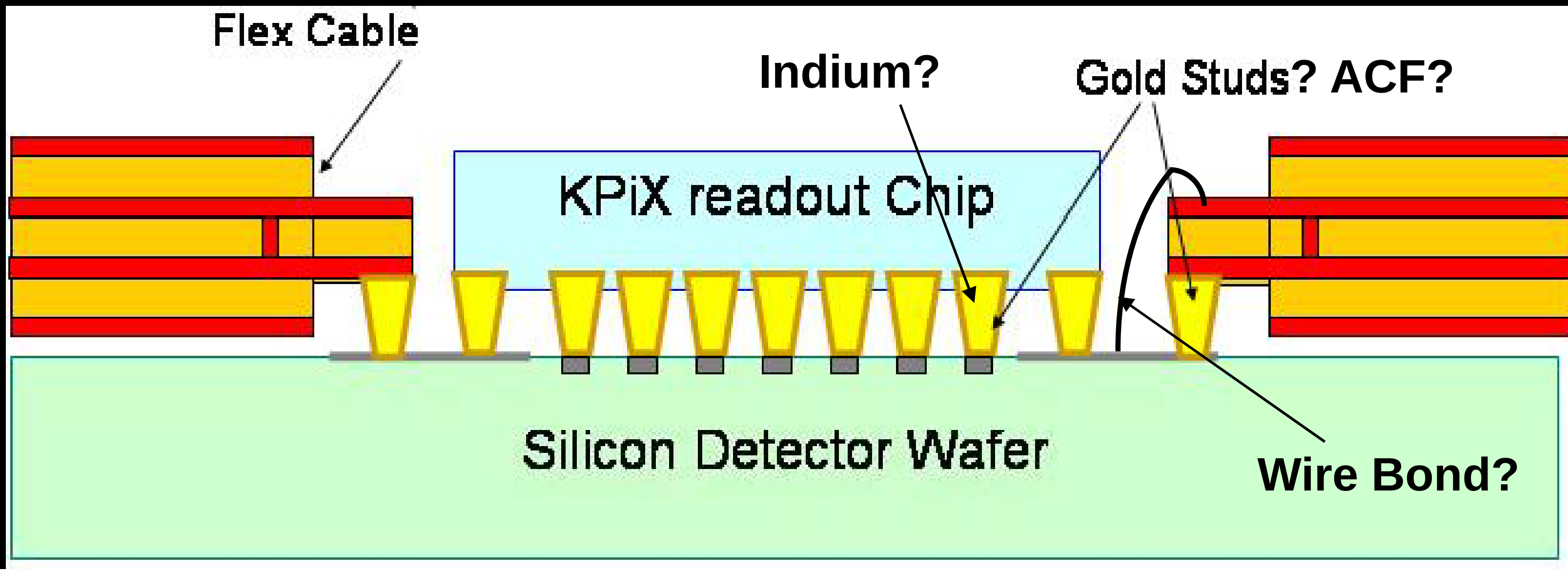
- First prototype:
  - 2 chip stations
  - Buried digital signal layer between power and ground planes
  - Wire bond connections
- For ECal:
  - ~6 stations: should be OK
  - Would like to determine length limit for next round (vias and multi-layers difficult for ~1m)

Interconnect issues

Technologies being considered:

KPiX to Sensor: Indium Bump Bonding
Gold Stud Bonding
Anisotropic Conducting Film

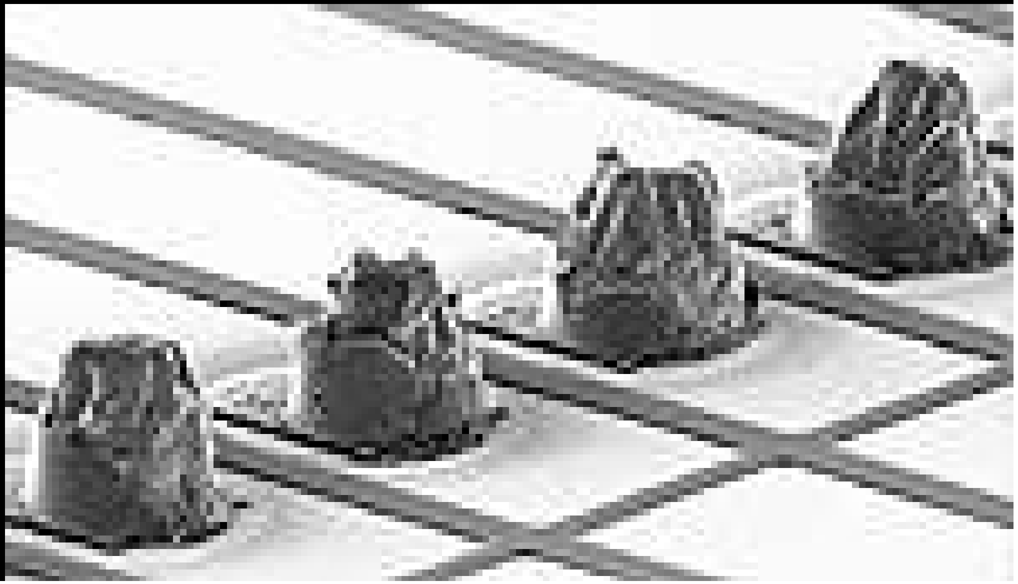
Flex Cable to Sensor: Wire Bonding
Z-axis Conducting Film
Gold Studs



Indium Bump Bonding

Indium Bump Bonding is a mature/commercial technology. UC, Davis has developed the process for prototyping purposes. Our facilities include a Class 100 clean room (10,000+ sq. ft.) and several pieces of specialized equipment. All the steps are done in-house:

- Photoresist spinning
- Mask making
- Alignment, UV exposure
- Ti/W sputtering
- Indium deposition
- Flip-chip bump bonding

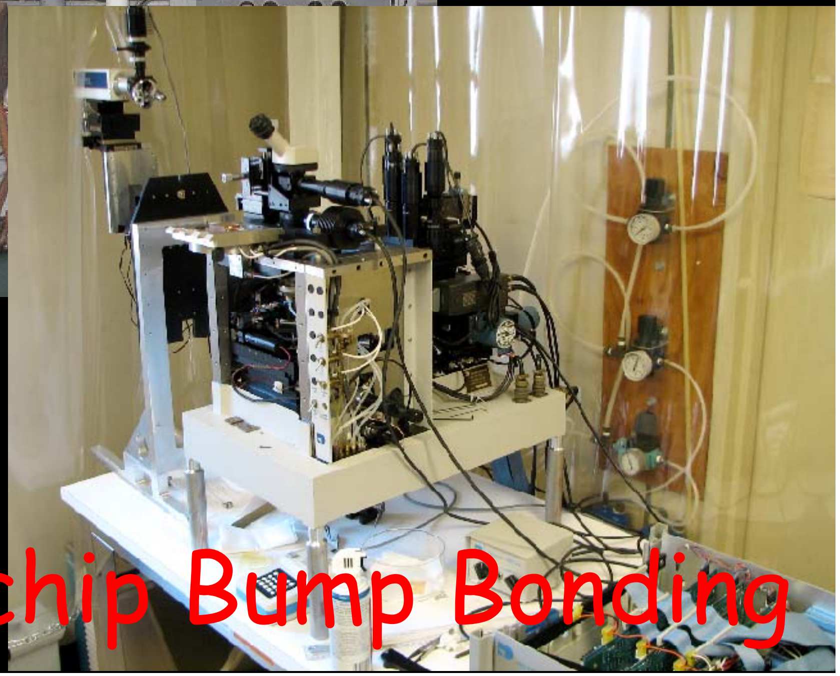


Indium Bumping Process

UV Exposure

Indium Deposition

Ti/W Sputter



Flip-chip Bump Bonding

Gold Stud Bump Bonding

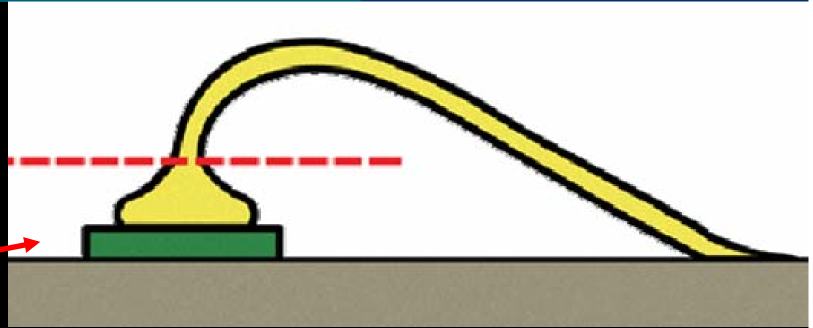
Palomar Technologies
Vista, Ca.

- Machine Development
- Process Optimization
- Prototyping

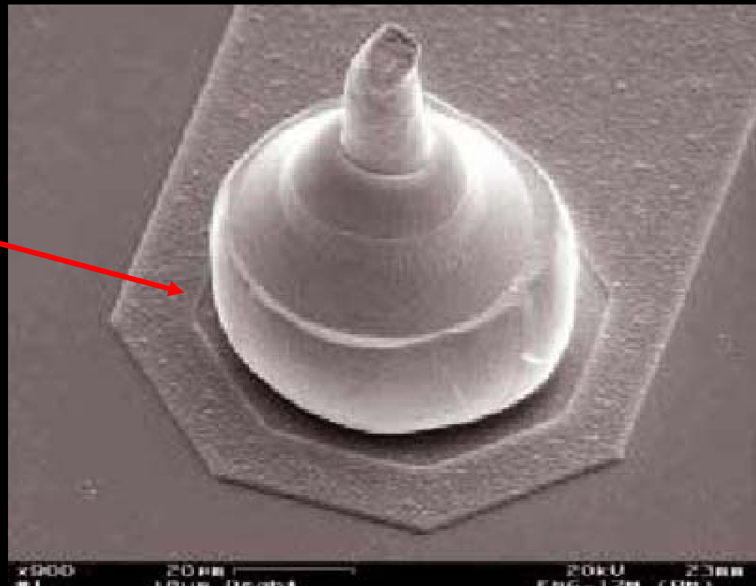
Gold Stud Growth

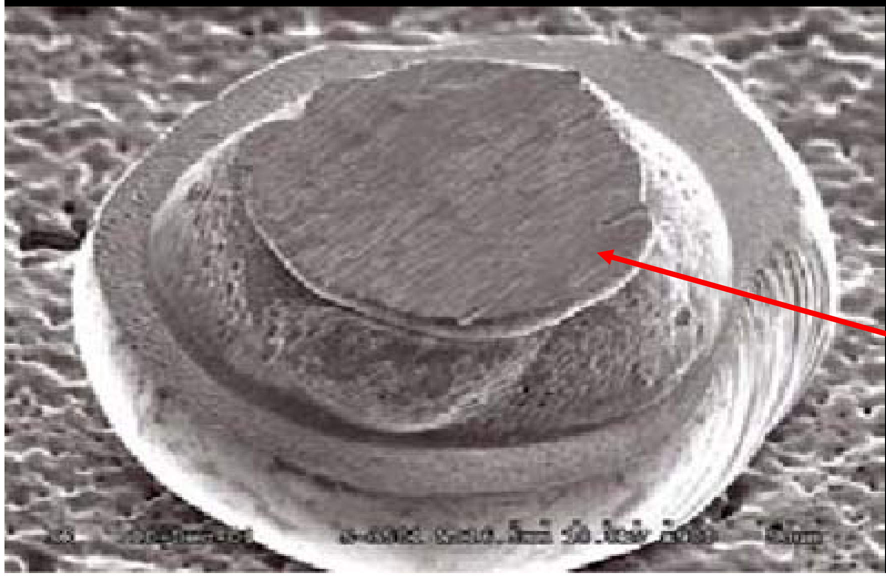
Palomar Technologies:

Step 1: A ~25 μm gold wire is bonded to the pad.



Step 2: The wire is snapped off leaving a stud behind.





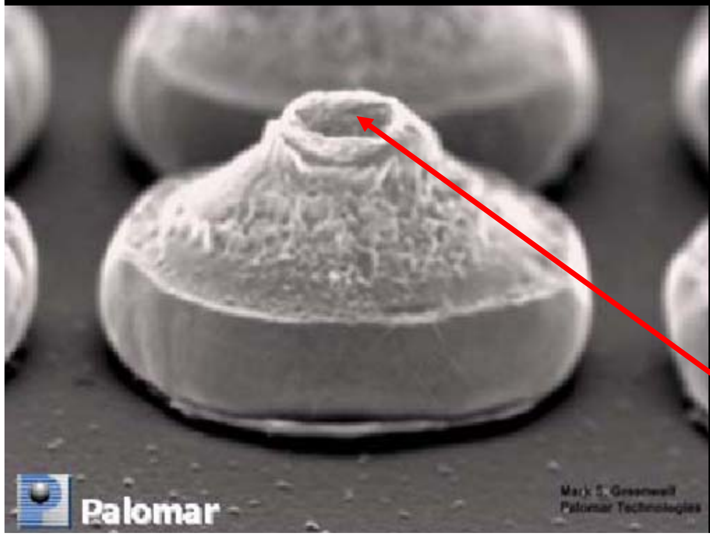
Step 3: The stud is "coined" (flattened) to provide a better shape.

Adhesive Attachment

Palomar Technologies:

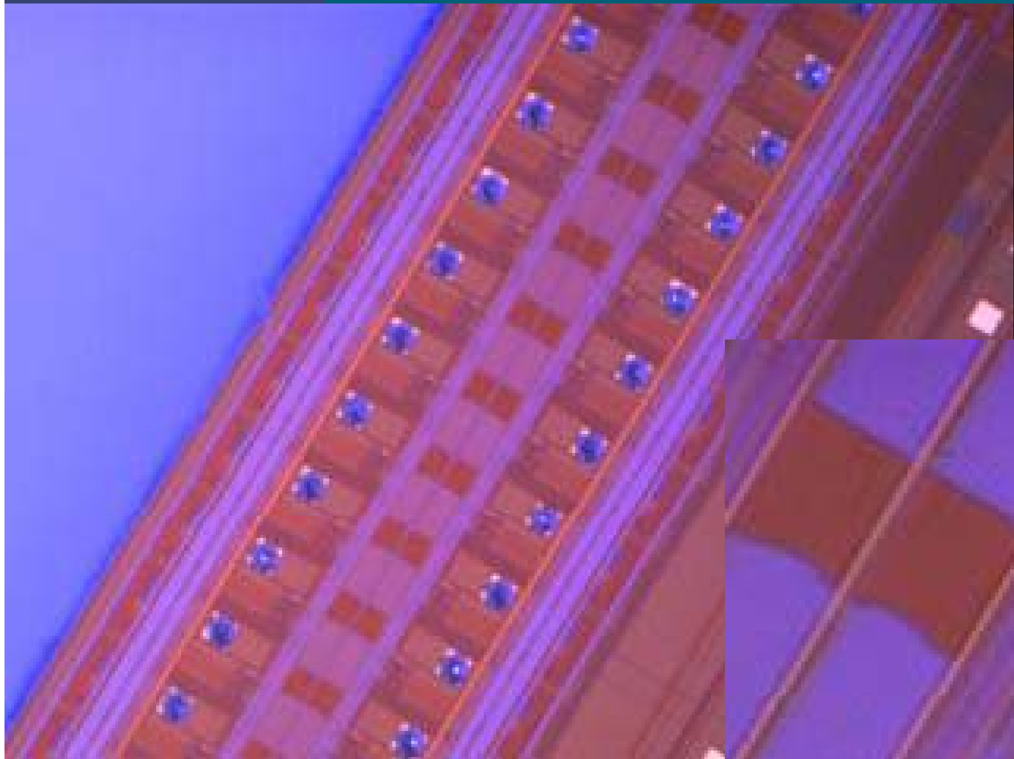
The tips of the studs are dipped into a conductive epoxy.
(Alternately, epoxy "dots" can be dispensed on the opposite wafer).

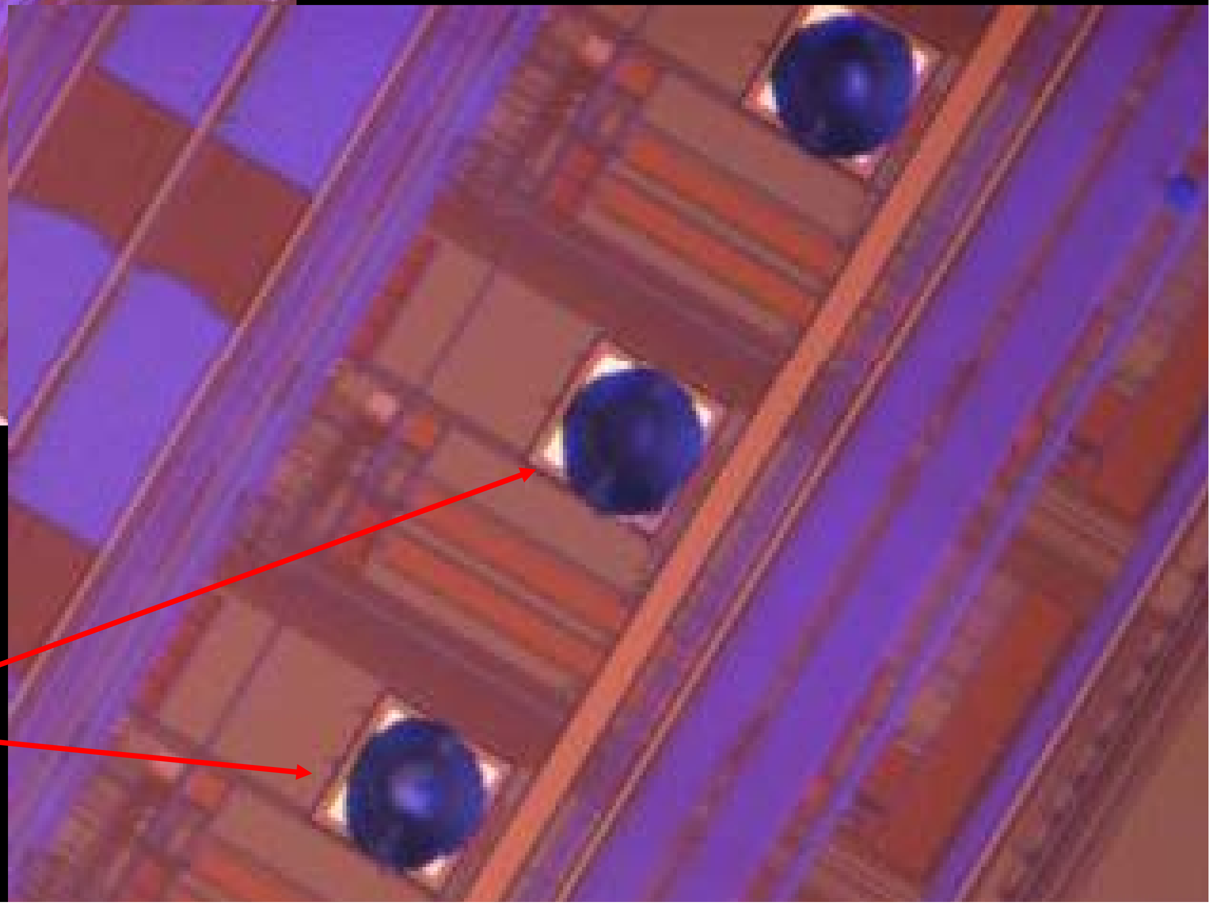
After a flip-chip alignment, the chips are compressed.



An optimum stud shape for adhesive attachment has been developed. Instead of "coining" the wire is pushed back into the ball after snapping. The result is a matted surface.

KPiX with Gold Studs

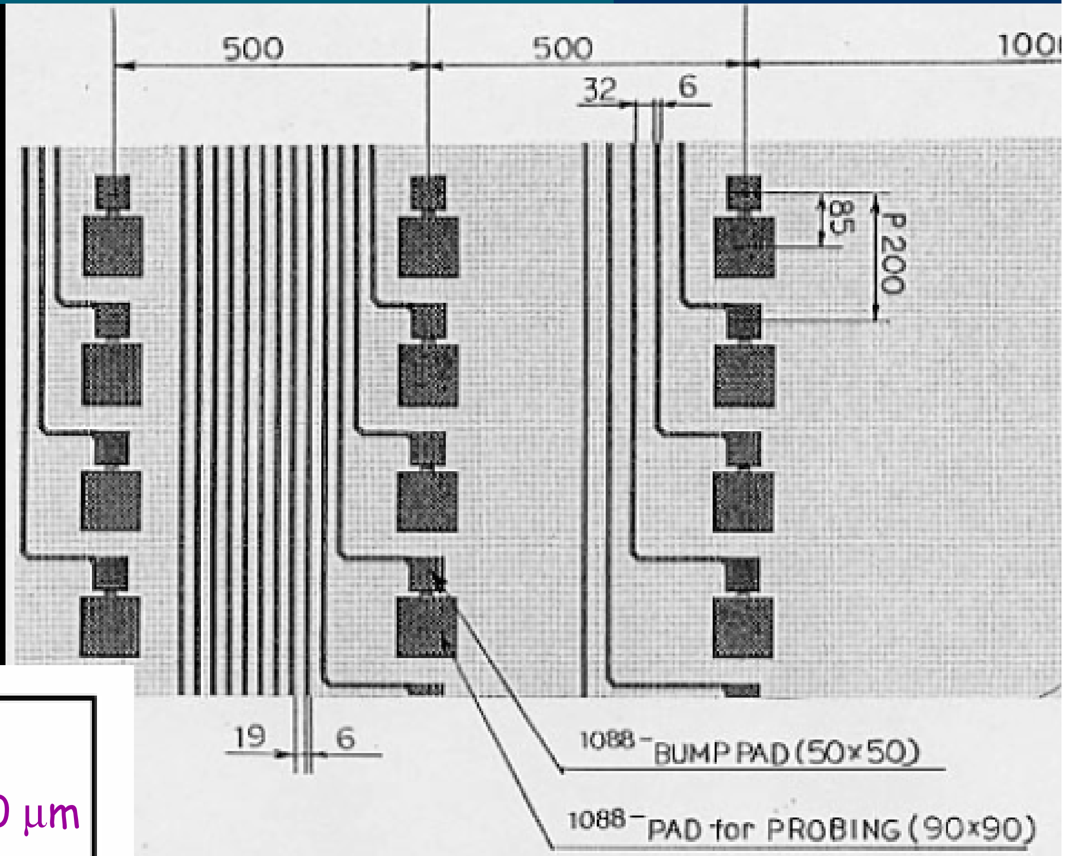


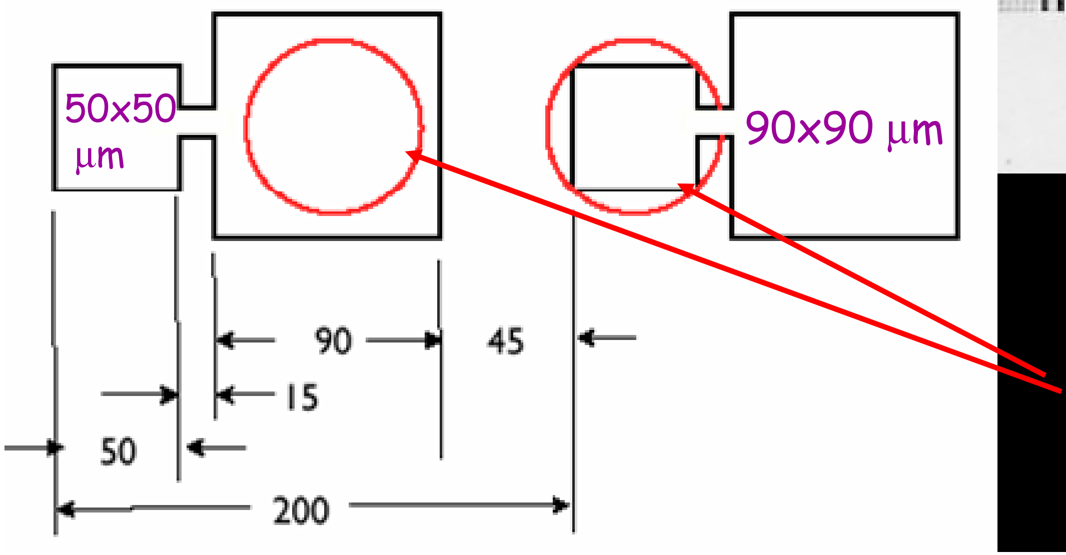


Studs are well-formed and centered on the 70x70 μm pads.

Si-W Bump Bonding

The limitation on bonding pitch comes from the spread of the epoxy (the effort is in minimizing the amount of epoxy that can be tipped/deposited).





The expected spread of 70 µm (red circles) is adequate for Si-W needs.

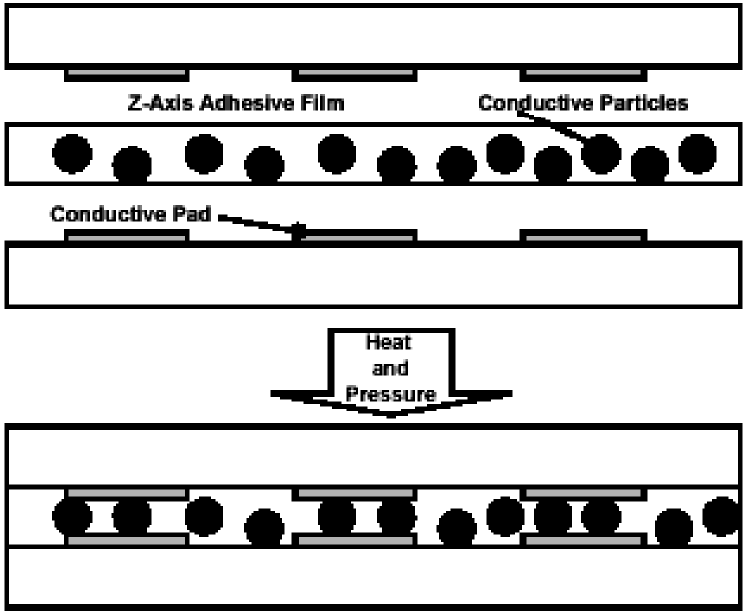
Z-Axis Conducting Adhesive

3M: 7303 ACF Adhesive

~45 μm particles
~75 μm film thickness

≥250 μm pad pitch

Bonding Conditions:
140°C @ 260 PSI for 25 secs



Cairns et al, SID Digest, 2001

Contact resistance ≤0.2 Ω (for flex-cable to PC board).
≤0.2 Ω maintained after 80°C for 1000 hours or 25°C for 4 yrs.

Flex cable to Wafer attachment is not common => R&D.

Thermoplastic Conducting Adhesive

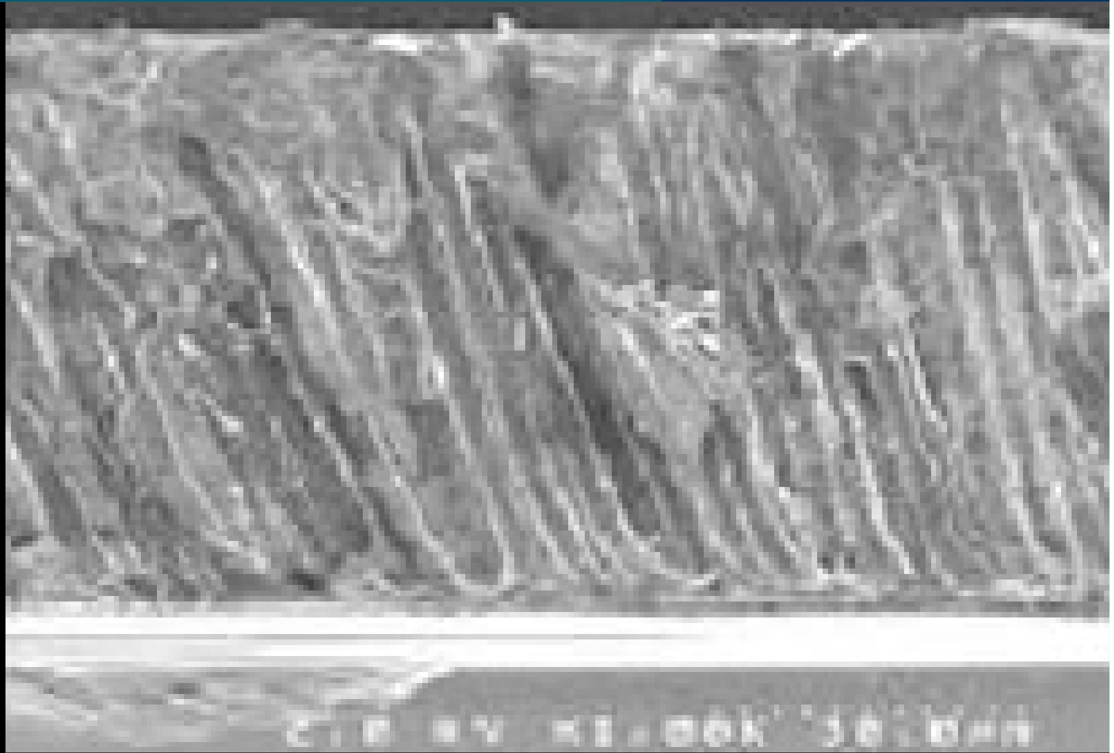
Btechcorp:

Metal fibers in a matrix
~2 x 10^7 fibers/in^2

≥11 μm pad pitch

Low Cure pressure: 50 psi

Thermal Conductivity ≥ Cu
Smaller resistance



Carbon fiber structure.

Cheaper. Candidate for both KPiX to Sensor and Flex cable to Sensor attachment => Further R&D.

Status Summary

- KPiX readout chip
  - Currently studying v5 prototype (2x32 channels)
    - Improved biasing of MOS capacitors; new poser bus for comparators
    - Optimized shaper time constants
  - Perhaps submit 1024-channel KPiX in Jan '08

- Silicon sensors
  - v2 prototype submitted to industry (40 sensors)
  - Schedule funding limited

- Interconnect issues
  - Bump bonding – Gold stud prototyping is underway
  - Flex Cable – Working with vendor to improve yield
    A 6-station cable is being designed

Plans (near term)

→ Construct a "Tower": full-depth, single-wafer wide module with 1024 channel KPiX chips bonded to sensor wafers and read out via flex cables (~30 layers).

→ Test in a beam: (1) electrons
(2) hadrons with HCal

The R&D leading to an "ILC-ready" Si-W ECal technology is progressing well