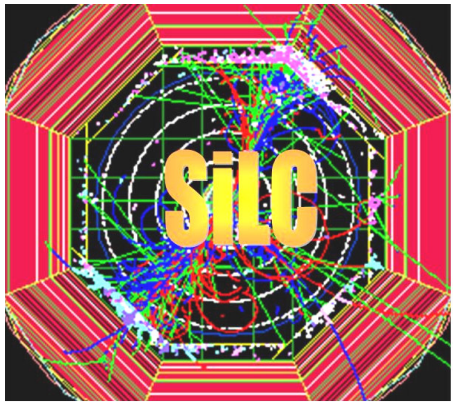


SiLC latest advances

Latest advances on:

- Large size prototypes & related issues (new sensors, construction of modules…)
- Insulating frame
- Alignment
- Front end electronics
- Test beams
- Simulations (other talk at this workshop)

On behalf of the SiLC* collaboration:

LAPP Annecy, U. of Michigan Ann Arbor, U. of Barcelona, IMB-CNM/CSIC Barcelona, HIP Helsinki, VTT Helsinki, IEKP Karlsruhe U., U. of Liverpool, Moscow State U. Obninsk State U., LPNHE/IN2P3-UPMC Paris, Charles U. Prague, SCIPP and UCSC in Santa Cruz, Yonsei U, Korea U, Seoul National U, SungKyunKwan U., Kyungpook U, Daegu and Seoul, IFCA/CSIC-U. of Cantabria Santander, INFN-Torino and Torino U. IFIC/CSIC –Valencia U, HEPHY Vienna, HPK Hamamatsu City. Collaboration with DESY (beam test & telescope) and CERN (beam test & bonding Lab)

•SiLC= Silicon tracking for the Linear Collider, Generic R&D collaboration

A. Ruiz Jimeno (IFCA), ALCPG07, Fermilab, 10/23/2007

What's new since Beijing review ?

SiLC proposal to the ILC R&D Review Panel

Proposal to the ILCSC R&D Panel on Tracking for the ILC
Submitted on January 29, 2007, by

The SiLC Collaboration

(Silicon Tracking for the Linear Collider)

Dept. of Physics, University of Michigan in Ann Arbour, USA
LAPP, IN2P3/CNRS in Annecy, France
University of Barcelona and University Ramon Lluli in Barcelona, Spain
Centro Nacional de Microelectronica (IMB-CNM) and CSIC in Bellaterra, Spain
Dept. of Physical Sciences and Helsinki Institute of Physics (HIP), University of Helsinki, and VTT Technical Research Center of Finland, in Helsinki, Finland
Inst. für Experimentelle Kernphysik (IEKP), Karlsruhe University in Karlsruhe, Germany
Liverpool University in Liverpool, UK
Moscow State University and SiLab in Moscow, Russia
Dept. of Applied Physics, Obninsk State University of Atomic Energy in Obninsk, Russia
LPNHE, University Pierre and Marie Curie, IN2P3/CNRS in Paris, France
Charles University in Prague, Czech Republic
Santa Cruz Inst. of Particle Physics (SCIPP), University of California in Santa Cruz, USA
Inst. de Fisica de Cantabria (IFCA), University of Cantabria and CSIC in Santander, Spain
Depts. of Physics of Yonsei University, Korea University, Seoul National University and SungKyunKwan University, all in Seoul, and Dept. of Physics of Kyungpook National University in Daegu, Korea
INFN-Torino and University of Torino in Torino, Italy
Inst. de Fisica Corpuscular (IFIC), University of Valencia and CISC in Valencia, Spain
Inst. of High Energy Physics (HEPHY), Austrian Academy of Sciences in Vienna, Austria
Hamamatsu Photonics K.K. in Hamamatsu City, Japan

Edited by *Aurore Savoy-Navarro*[*)]

[*)] Contact: aurore@lpnhe.in2p3.fr

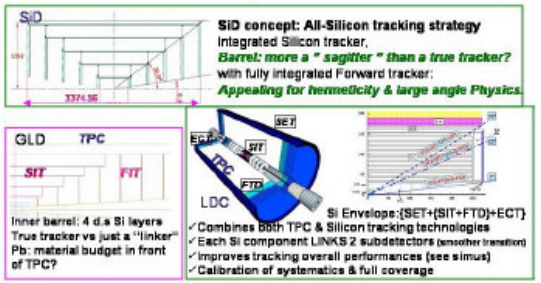
Tracking Review General Questions: Answers from the SiLC R&D Collaboration

Introductory remark:

The SiLC R&D collaboration is dedicated to the development of the new Silicon tracking systems for the ILC experiments. This R&D activity follows the tracking schemes presently defined in the various ILC detector concepts that include Silicon tracking, namely GLD, LDC and SiD where teams of SiLC are collaborating. The tracking strategy in those 3 concepts mainly differs by including a gaseous detector as central tracker (GLD and LDC), or not (SiD). In any case, 4 tracking regions can be considered:

- The outer layers both in the barrel and the End Cap regions
- The inner layers including as well the barrel and forward components near to the vertex detector.

The tracking schemes here below are therefore the starting point for the SiLC studies:



Si Envelope is like stretching a all Silicon tracking into 2 parts: inner and outer ones and install a TPC in between.
SiLC:UNIQUE place to study/compare these various crucial tracking concepts

Tracking schemas in the various ILC detector concepts with, for each case, the main issues/questions that SiLC R&D is currently addressing

SiLC, ALCPG 2007

1°) Construction of large structure Si tracking prototypes

- **New sensors**
  - ► New µstrip sensors from HPK, including test structures and special treatment for alignment.
  - ► Thinning tests by LPNHE with Edgetek
  - ► Direct wiring (inline pitch) of the FEE onto µpistes (LPNHE, HPK)
  - ► Prospects: New Firms (apart from HPK), New technology (3D)
- **Tooling for new module construction**
  - ►Based on already equipped places: IEKP, Liverpool, IFIC
  - ►Starting expertise: LPNHE (plus collaboration with CERN)
- **Design and construction of large prototypes**
  - ►Two main cases:
    - plans of Si layers for central or XUV Forward device (1st ready by end 2007)

(*will be used for combined tests with vertex detector and/or calorimeter prototypes)*

- Prototype of the Silicon envelop for LCTPC combined test (2008)

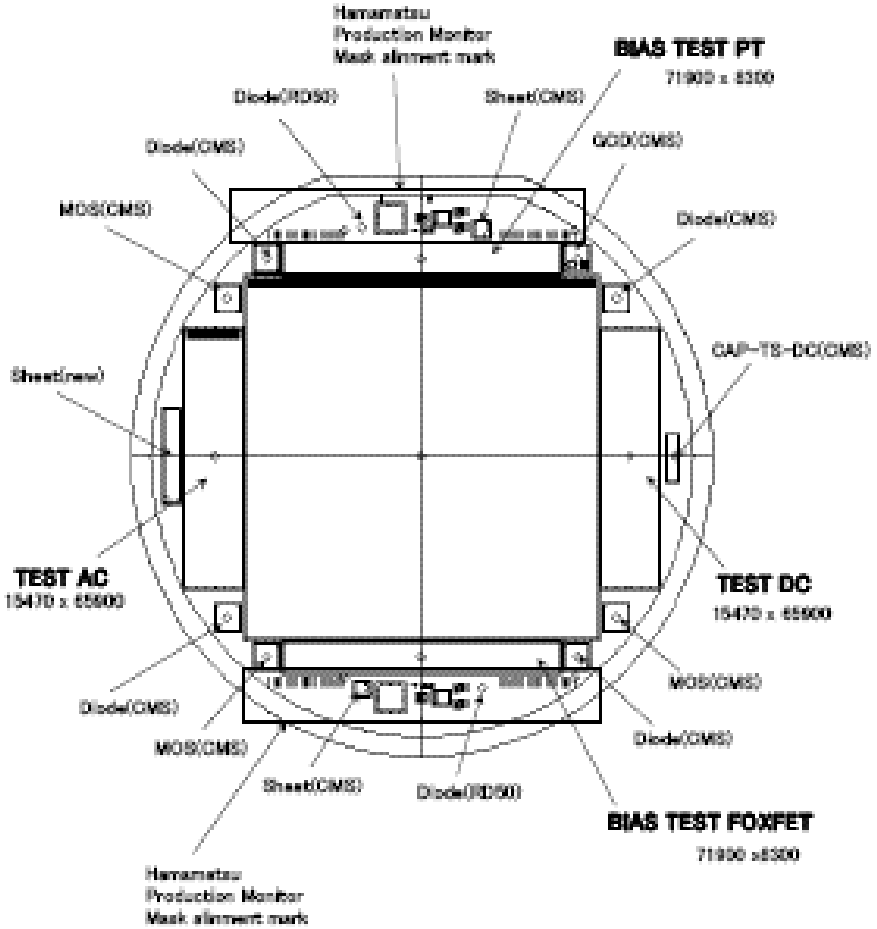
The construction of prototypes start addressing the main issues: i.e. light support structure, compact low power dissipation electronics, new sensors with smaller pitch and thinner.

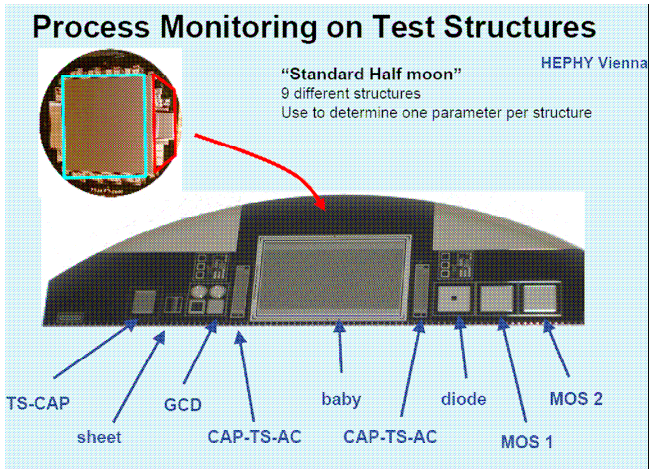
SiIC work program for sensor R&D 2007-2008

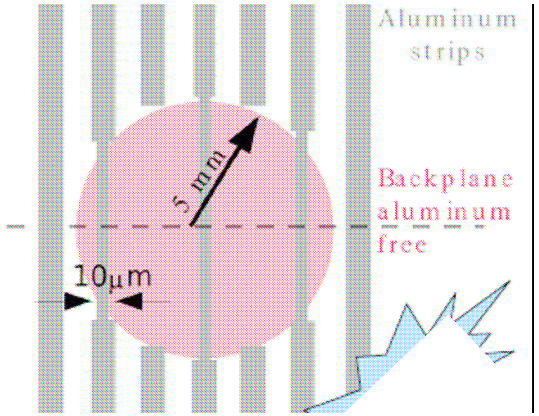
IEKP Karlsruhe, HEPHY Vienna, LPNHE, IFCA+IMB/CSIC, HPK

- Step 1 (2007)
  - ✓ Wafer thinning (100, 200, 300µm)
  - ✓ Strips larger wafer (50 µm pitch)
  - ✓ Improve standardized test structures and test setups
- Step 2a (2008-)
  - ✓ Move from pitch adapter to in-sensor-routing
  - – Test crosstalk, capacitive load of those sensors
- Step 2b (2008-)
  - ✓ Test 6” double sided sensor
- Step 2c (2008-)
  - 8” (12”) single sided wafer
- Step 3 (2007-)
  - ✓ New firms (Liverpool+Micron & E2V)
  - New technology: 3D based (IMB-CNM, HIP, VTT, HEPHY, LPNHE)

New 6” µstrip wafers with tests structure(HEPHY) ordered to HPK (April 07): sensors are 9.05x9.05cm^2, 320µm thick, 50µm pitch; 5 sensors out of 35 ordered are specially treated for alignment with laser; Delivered October 1st 2007, equipping the first module at test beam at CERN (October 2007)





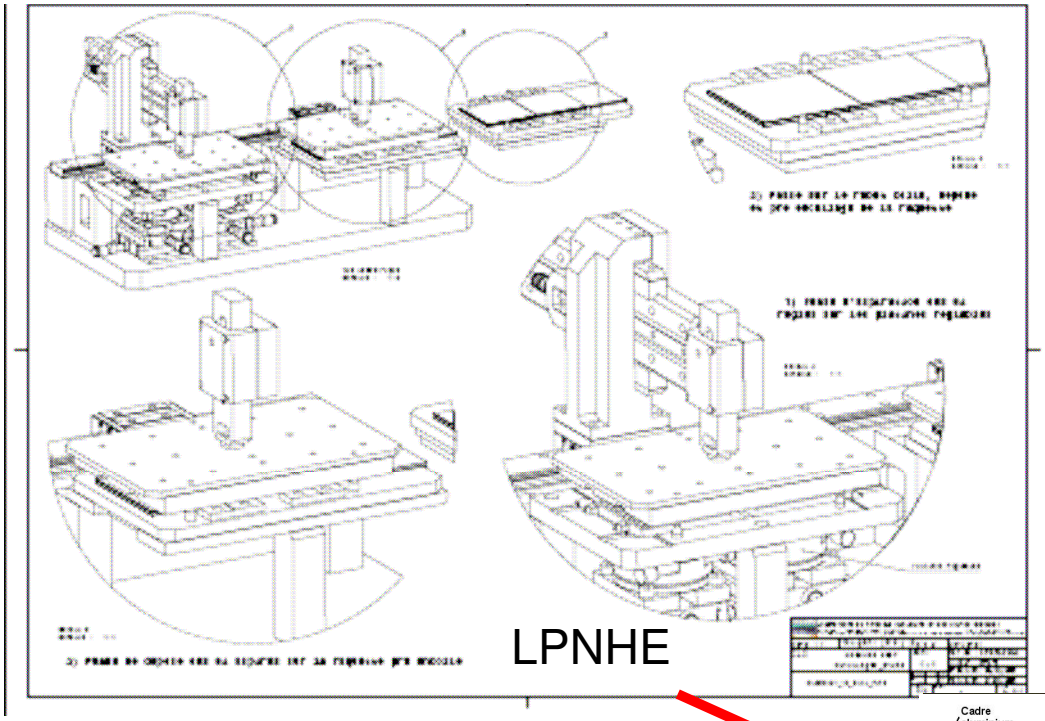


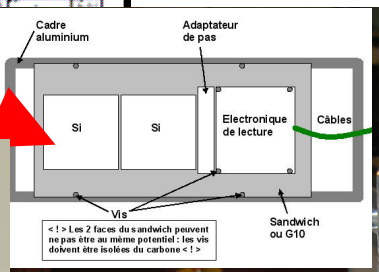
Design finalized by:21/6/07; Sensor with test structure delivered October 22, will be fully characterized by HEPHY.

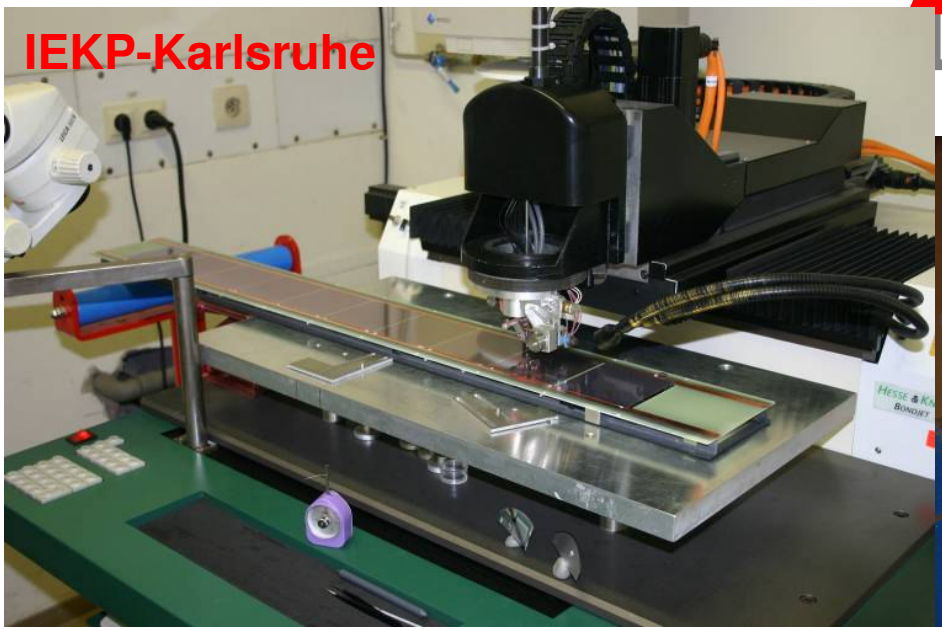
5 wafers treated for alignment

Tooling for construction of modules: tiles (i.e. One sensor module) to long ladders

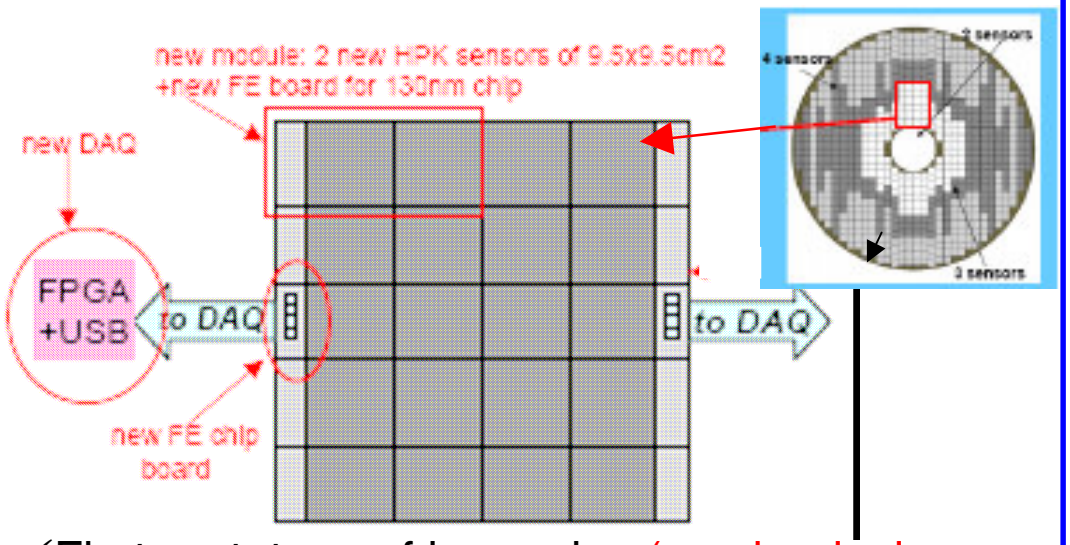
- Need to develop new expertise and tooling at LPNHE (well in progress)
- and use already existing expertise and tooling: IEKP Karlsruhe, IFIC, Liverpool, etc….
- Bonding Lab at CERN (A. Honma, I. McGill, M. Moll)





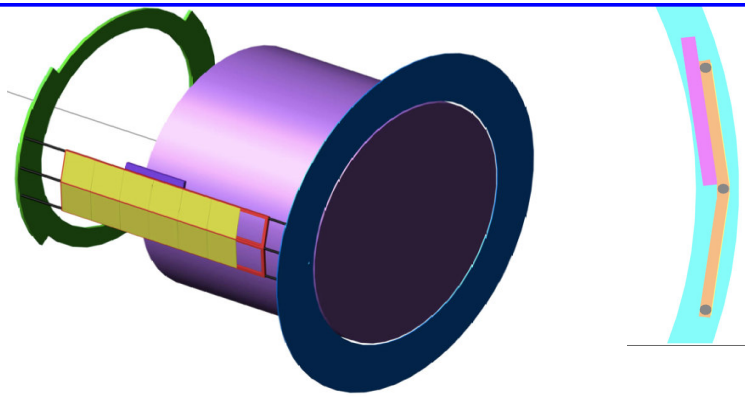


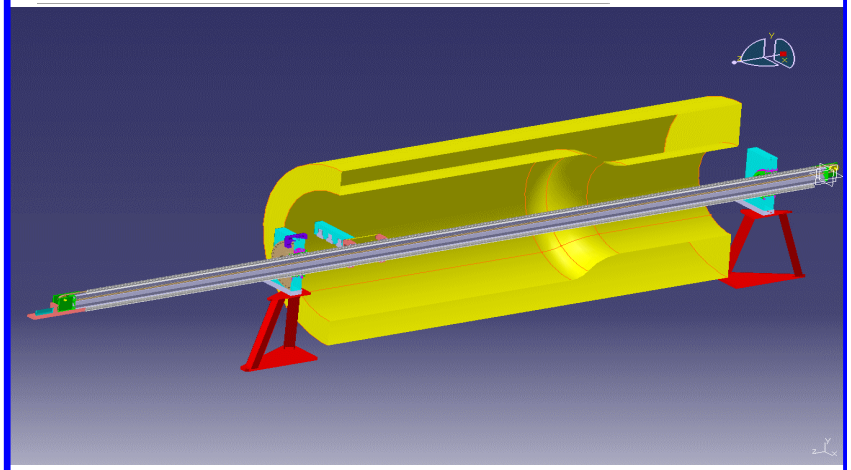
Large size Si prototypes:

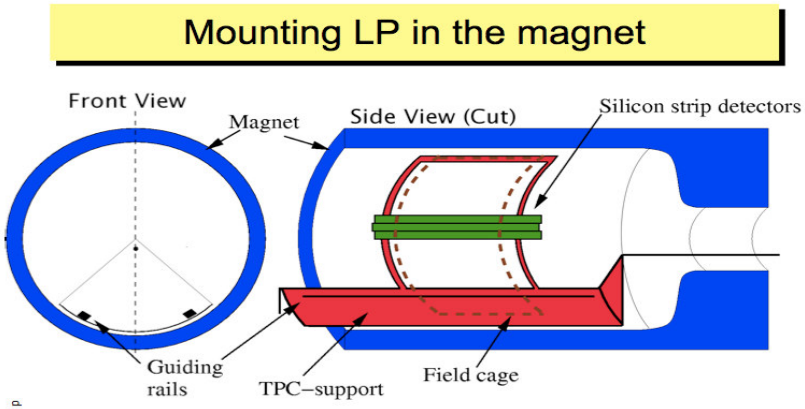


- ✓First prototype of large size (mechanical structure ready end of 2007). Evolutive system.
- ✓First module just tested @ CERN tb (**Oct 07).**
- ✓Four such plans to be built and equipped (sensors and FEE) for 2008-2009 T.B.
- ✓Will provide 2 XY/track or 1 XUV if FWD.
- ✓Cooling prototype will be adapted to it.
- ✓System available for combined test beam with µvertex prototypes and/or Calorimeter prototypes
- ✓Alignment system prototype (IFCA) will be included to it.

SiLC, ALCPG 2007







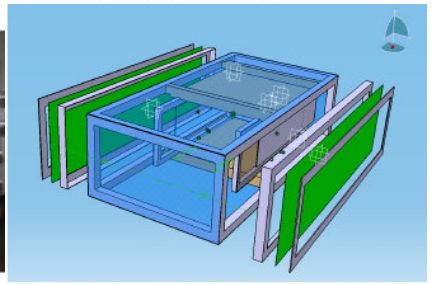
Tests with LCTPC (Fall 08)

IEKP, HEPHY, DESY, LPNHE

2°) Insulating envelop *(LPNHE +OSU+Torino U.)*

Important to have a thermal and electrical insulating frame for protecting the Si detector from environment effects (power dissipation from the neighbours, electrical compatibility etc…). Prototype in construction using LHC experience and results with FEE

Insulating cage for DESY test beam



Light prototype (0.5% X0) in composite material will be made by OSU &Torino

Actual FEE results: ~ 0.6mWatt/ch
No Power cycling included yet
→Main problem: power dissipation from neighbours

	Preamp	Shaper	Zero suppr.	Pipe-line	Total Analog	ADC	Logic	Total Digital
50mm/ch	90	180			270			
130mm/ch	148	148	198	10	575	66		
Common				100		5	96	101

3°) Alignment prototype

IMB-CNM New sensors *& LPNHE* **(FEE)**

Basic idea (developed first by AMS & CMS):

Use laser beam in the IR region ("pseudo-track" of infinite momentum) to cross several sensors consecutively. Main advantages:

- **No mechanical transfer errors between fiducial marks and the modules**
- **Minimum impact on system integration and none on DAQ**

Two-fold approach:

1) Integration with SiTra:

1.1) Mandatory change in the module:

∅~10 mm window where Al back-metalization has been removed (requires 1 new mask and sensor back processing)
(This is included in new HPK sensors)

1.2) Optional changes in alignment window

Strip width reduction
Alternate strip removal
Thickness optimisation
→ Transmittance improved

2) R&D on transparent Silicon µstrip sensors:

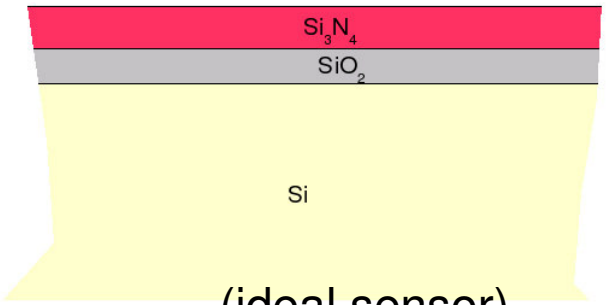
- IFCA with IMB-CNM (Barcelona) develops prototypes of new sensors that can achieve maximum transmittance in a wavelength range
- Aluminium electrodes and strip are perfect mirrors. Substitute Al electrodes by TRANSPARENT ELECTRODES (ITO, AZO....)
- Wide margin for changes and experimentation to obtain best optical and electrical sensor

Status

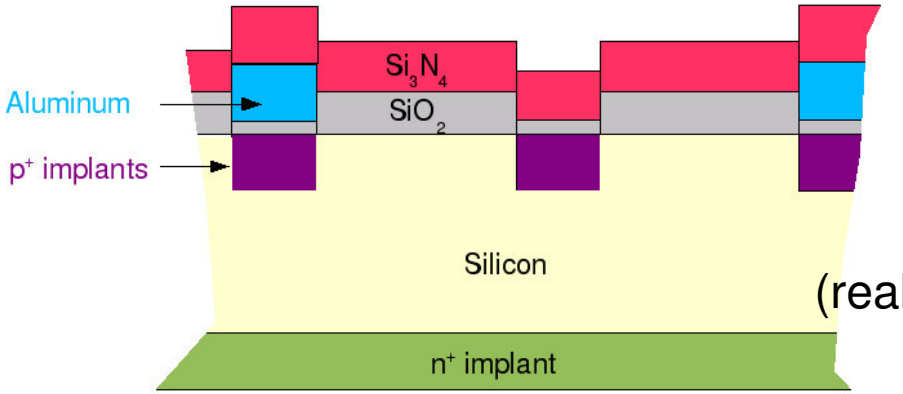
Ordered 5 sensors to HKP with alignment window (to be tested on optical test bench & test beam)

R&D IFCA-Santander&CNM-Barcelona:

- Scalar simulation of multiple reflections inside the multilayer of the sensor **... done**
- Optimization of multilayer design to achieve maximum T at λ_{IR}±5nm (laser spectral width) … **done**
- Vectorial simulation of diffraction processes due to strip segmentation ... **in progress**



(ideal sensor)



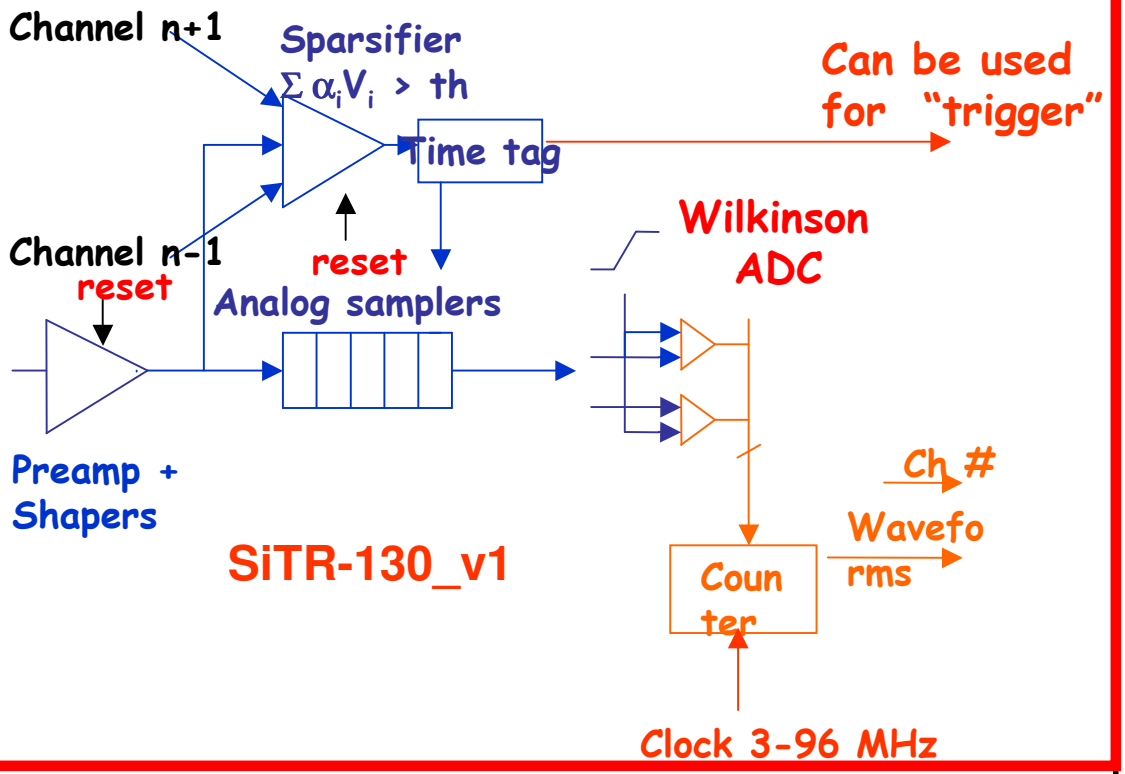
(real sensor)

Basic samples will be produced by IMB-CNM on September to:

- characterise each layer individually (refraction indexes)
- study the effect of Silicon doping on transmittance
- Validate scalar and vectorial simulation

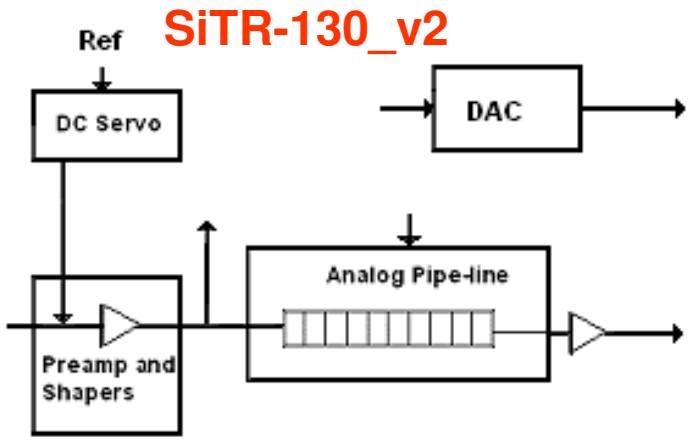
4°) FE Electronics: *(LPNHE + LAPP+B.U.)*

- **Tests of 2 versions SiTR-130_v1 & _v2 received Nov 06 & Jan 07**
- **Design of SiTR-130 for mini production (10-20 K ch) and readout of prototypes in 2008 (in progress)**



Version 1: LPNHE *Received end 2006*

Tests in fonctionality OK, tests with Si detector & detailed characterisation: well advanced (test beam)



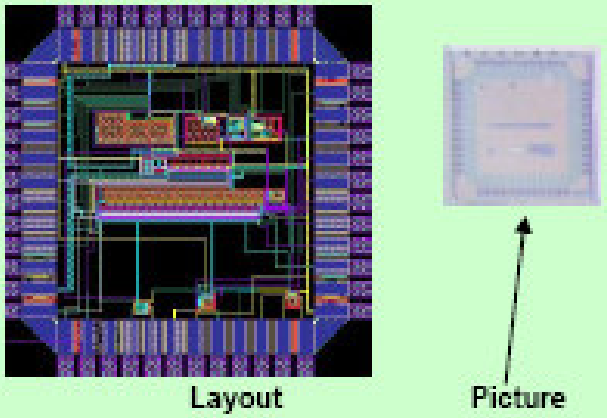
Version 2: LAPP

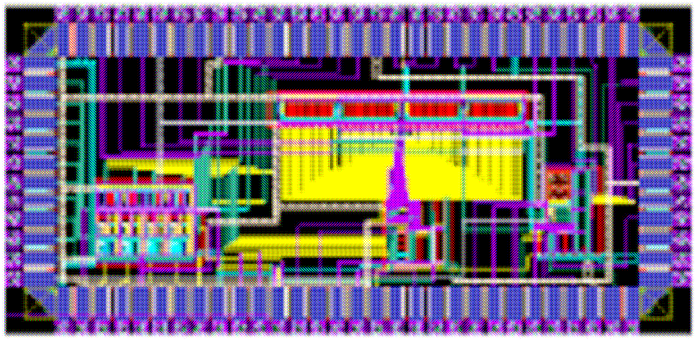
DAC: calibration

Pipeline improved wrt version v1.

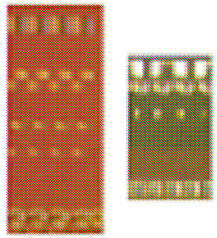
Received 5/1/07: test at LAPP

Layout & photographs of the chips SiTR-130_1 et _2

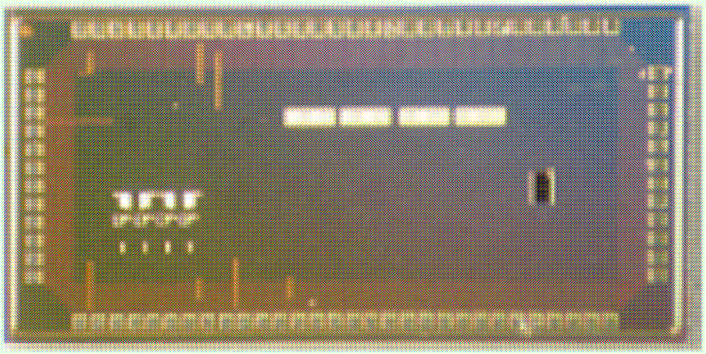




Layout of the 130nm chip including sampling and A/D conversion



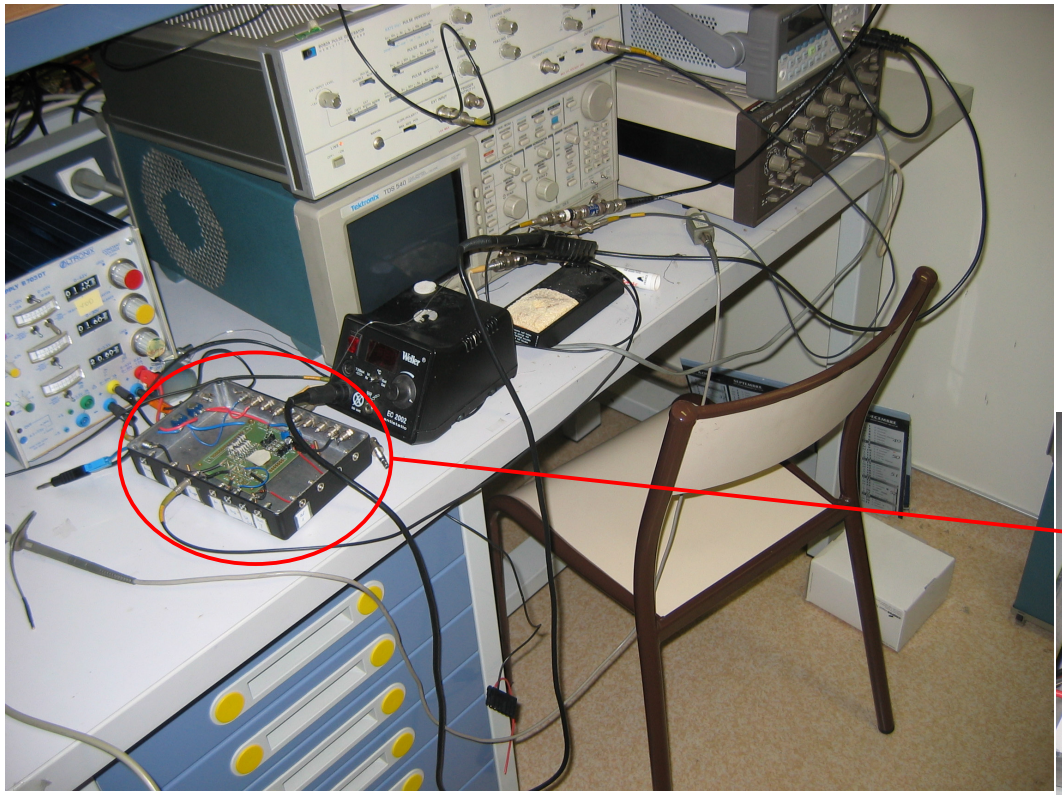
180nm 130nm



Picture

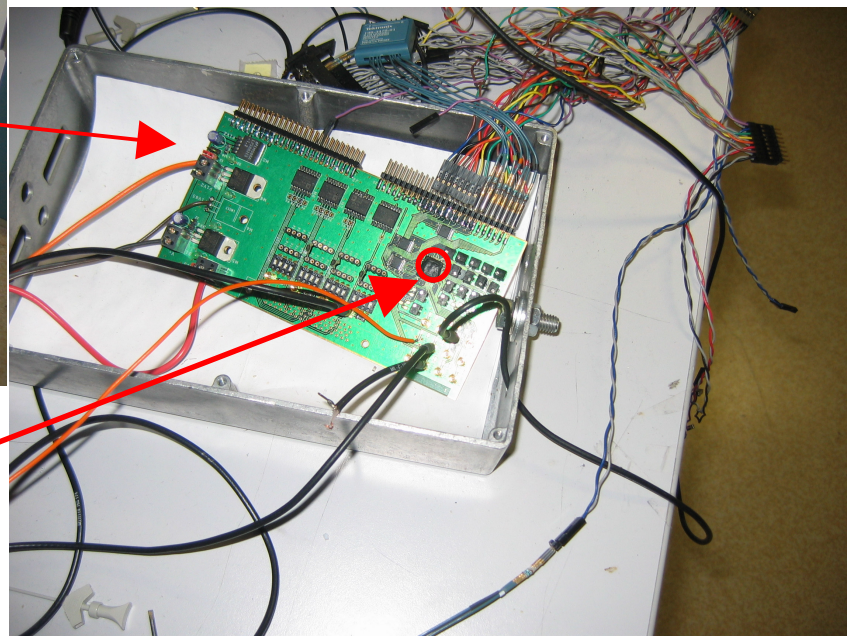
Chips received end 2006 and beginning 2007. Both tested in 2007

Fonctionality tests of SiTR-130_v1



Lab test bench of fonctionality of the chip at LPNHE

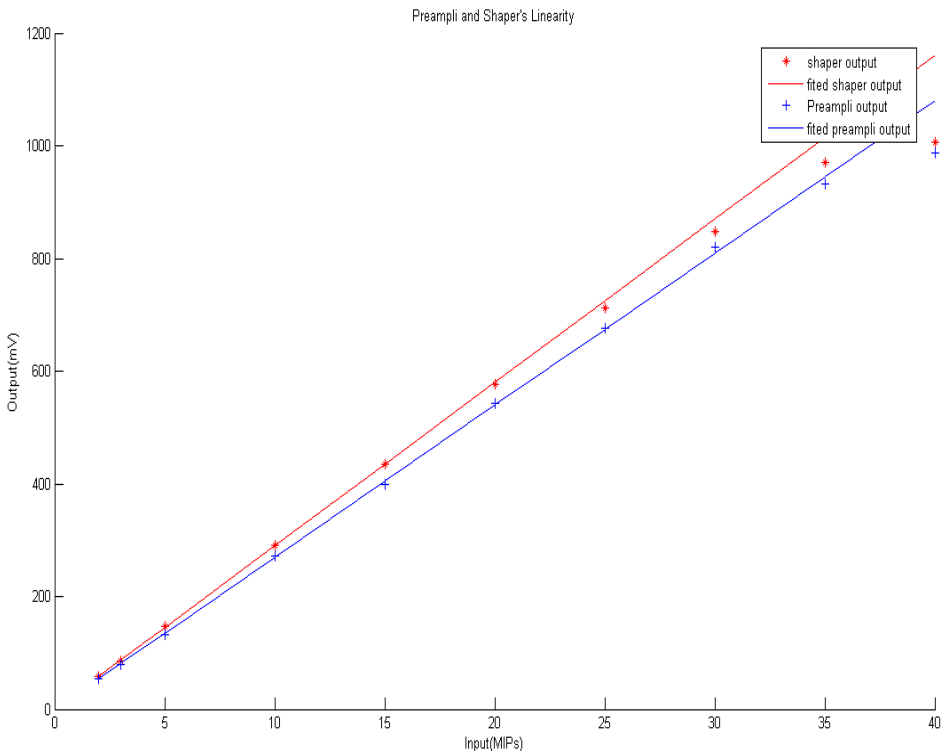
Test board for SiTR-130_v1

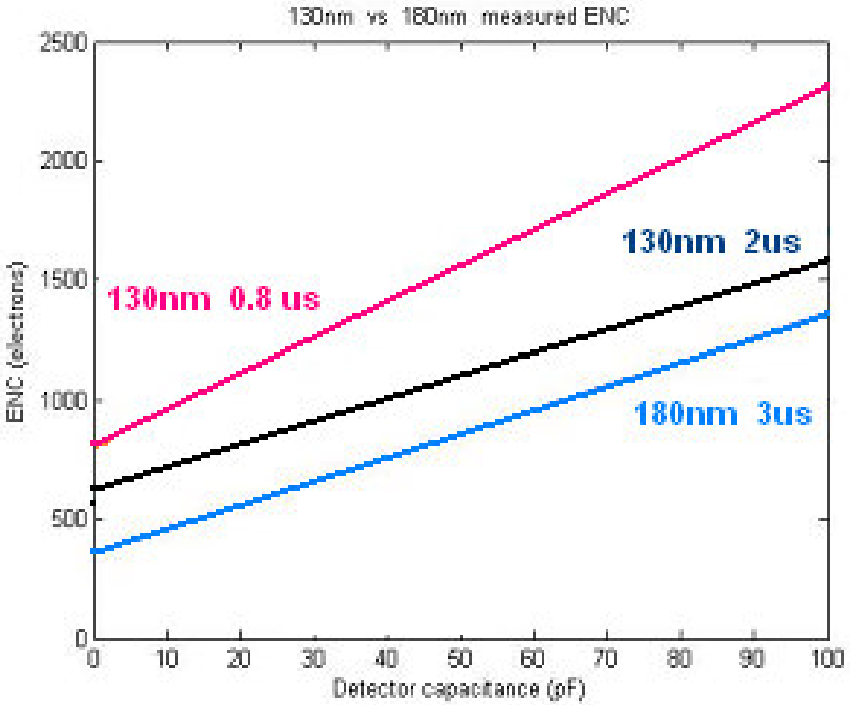


Chip SiTR-130_v1

Another test bench system is being installed at LAPP in order to fully test SiTR-130_v2 . This test bench will be fully automatized.

Results in fonctionality of SiTR-130 v1





Preamplier :
- Gain = 27mV/MIP
- Dynamique = 25MIPs (<1%)
  = 30MIPs(<5%)

Shaper :
- Gain = 29mV/MIP
- Dynamique = 20MIPs(<1%)
  = 30MIPs(<5%)

Noise performances:

130nm @ 0.8 **µs** : 850 + 14 e-/pF

130nm @ 2 **µs** : 625 + 9 e-/pF

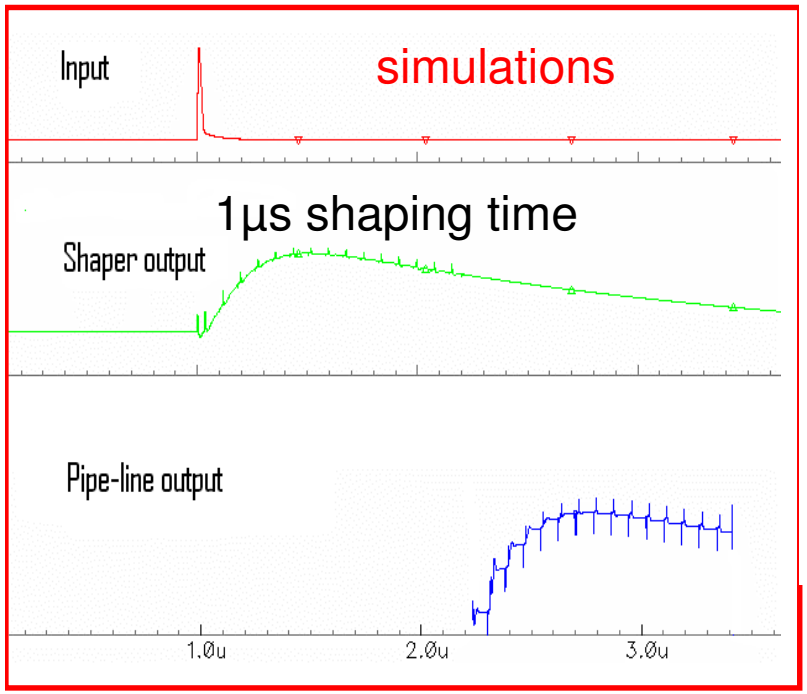
625 x sqrt(2/3)=510 **e-/pF**

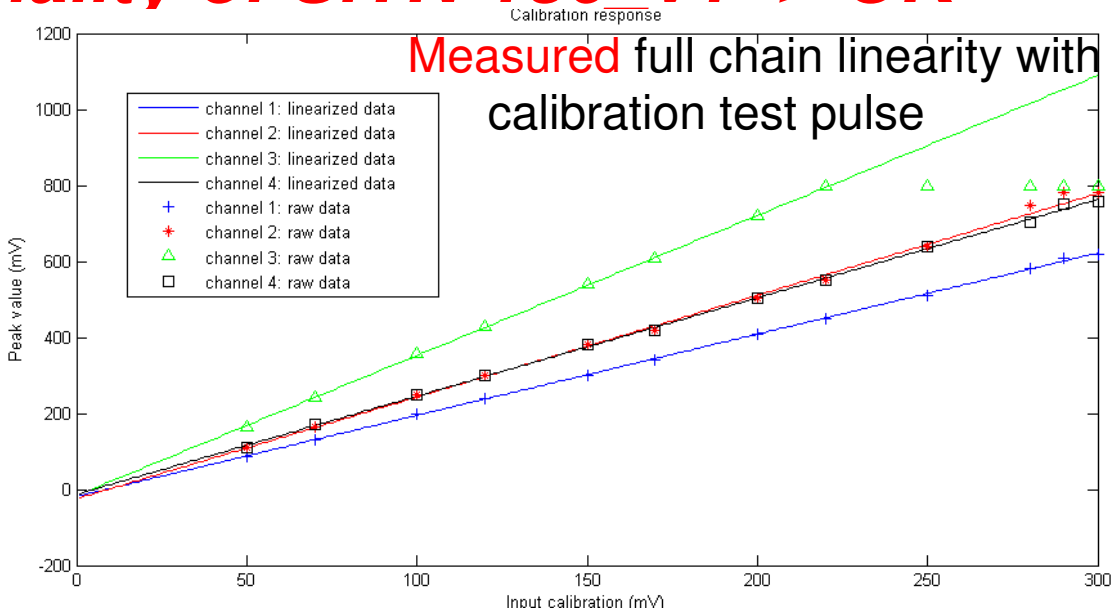
180nm @ 3 **µs** : 375 + 10.5 e-/pF

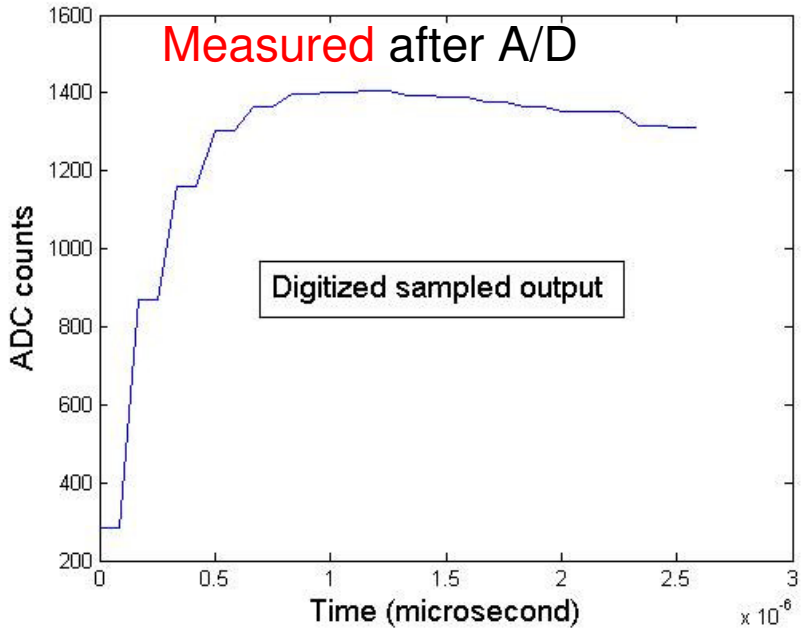
Power dissipation per channel= **600 µW**

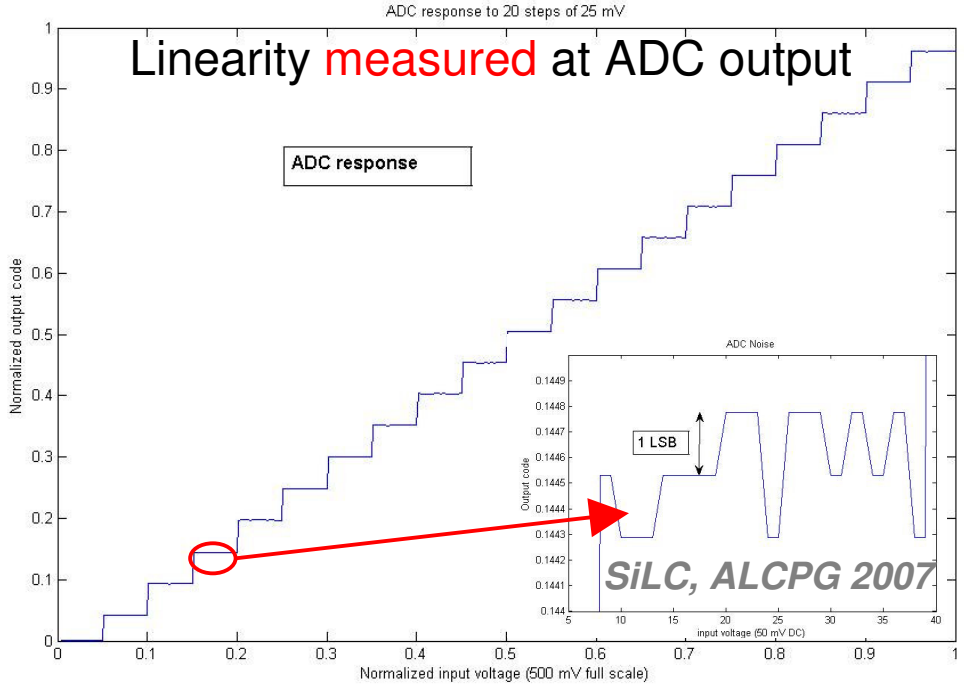
Channel size (preamp+shaper+zerosup.+sampler:
90µmx700µm in 130nm CMOS techno

Results in fonctionality of SiTR-130_v1=> OK







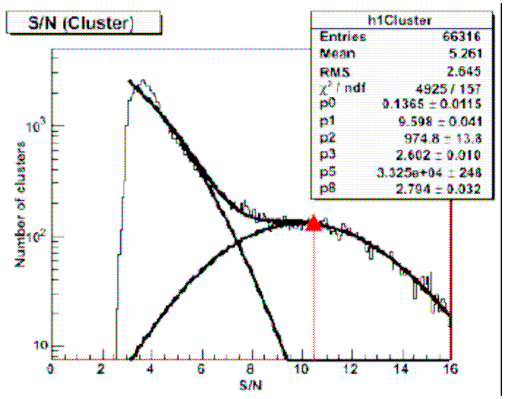


SiTR-130_v1 et v2: still to be done

Detailed characterisation of the A/D converter

- Linearities — integral, differential
- Noise — fixed pattern, random
- Speed — Maximum clock frequency

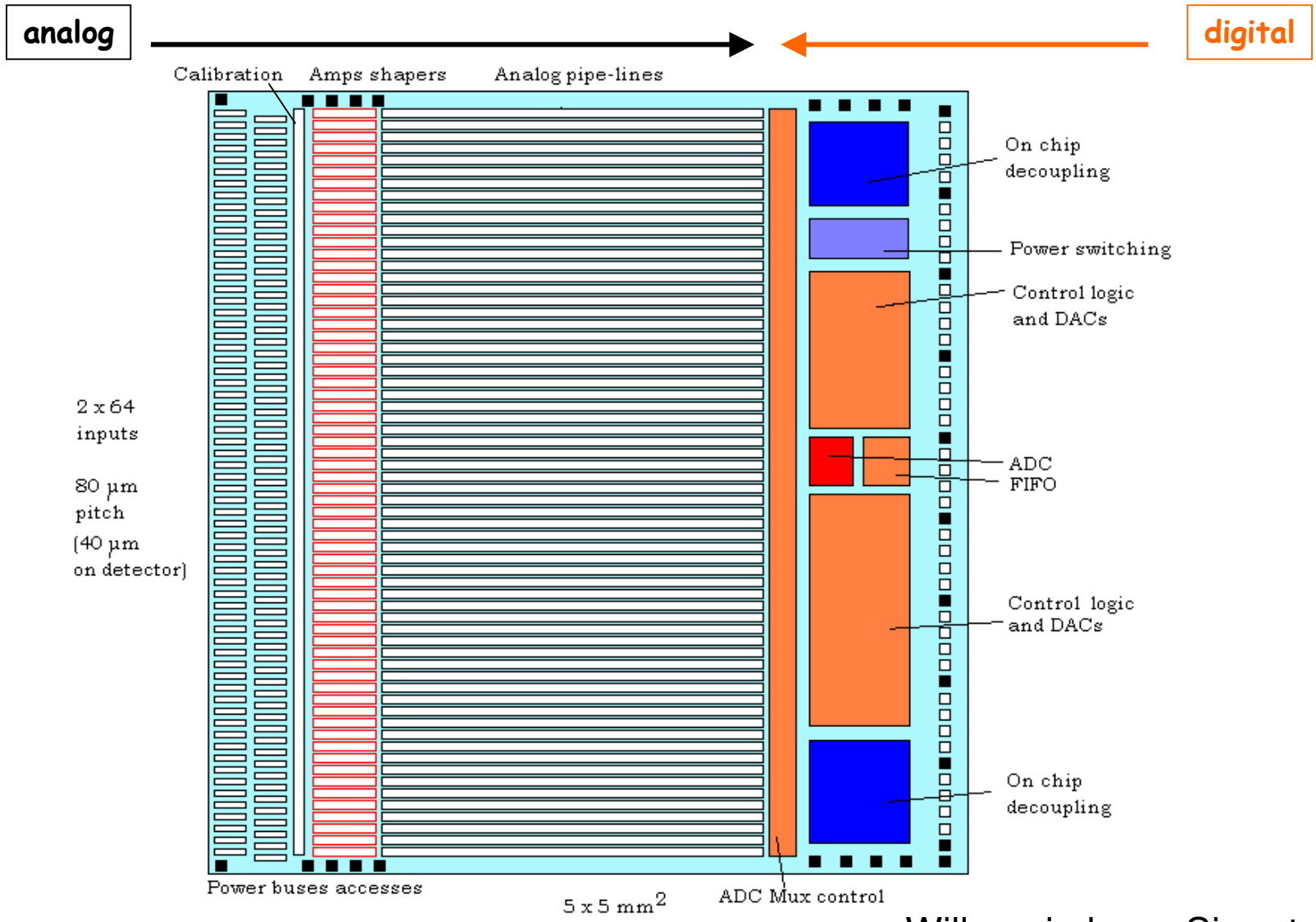
Number of effective bits (ENOB): first estimate 10 bits and full characterization of SiTR-130_v2 autLAPP



Tests of SiTR-130_v1 mounted on FE board connected to a Si module made of one CMS sensor (9,45cm strip long, 125µm pitch) made by IEKP, tested at the Paris Lab test bench in Paris before testbeam at CERN.
Tests with LD1060nm ➔ The electronic chain works fine
Tests with radioactive source OK
Tests just ongoing at CERN t.b. in October.

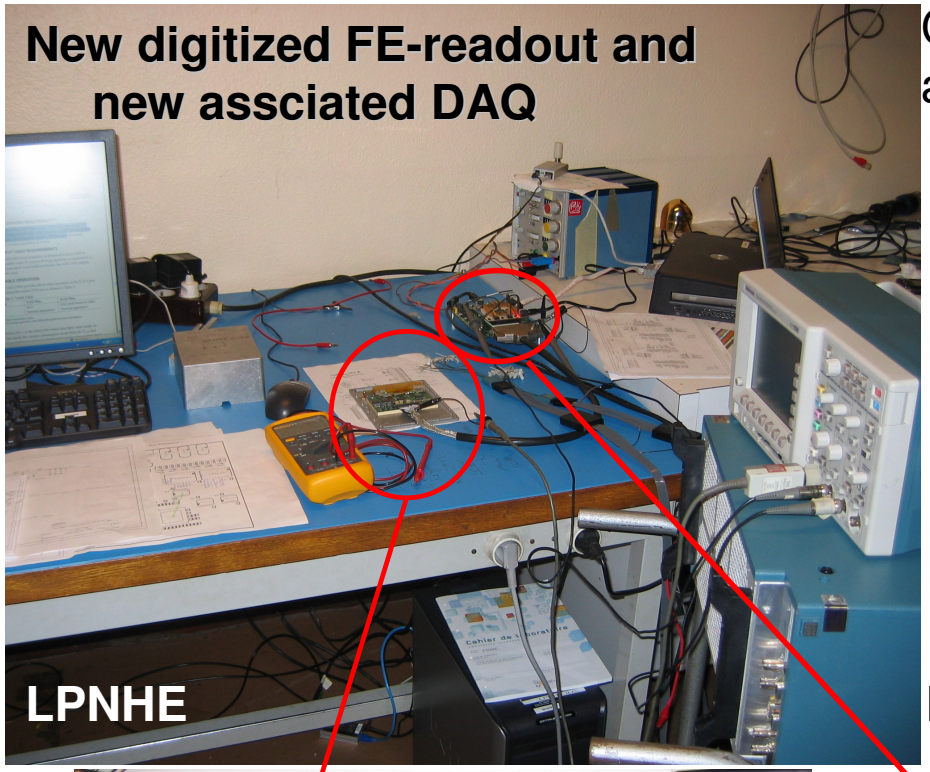
All these tests are crucial for the new SiTR-130_128ch, based on same design, but with 128 ch/chip and power cycling; New chip will be sent to foundry February 08 (EUDET).

128-channel chip = next chip production

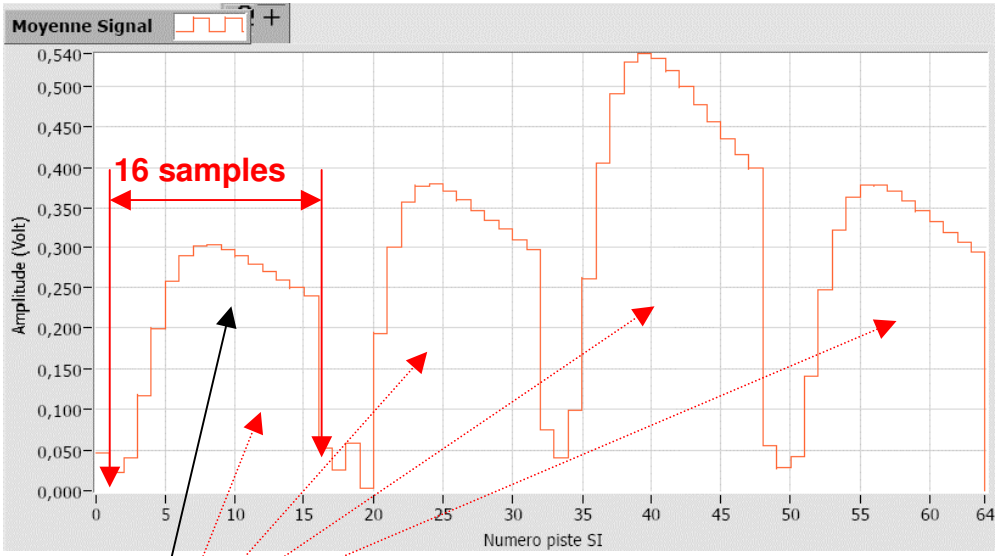


Will equip large Si prototypes for 2008 and 2009 test beams.

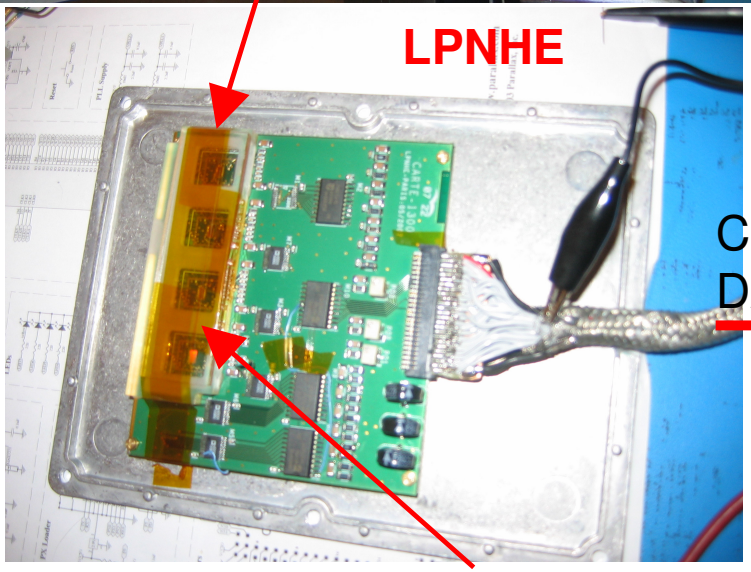
SiLC, ALCPG 2007



Calibration test pulse included in the FE board allows verifying the functioning of the FE chain

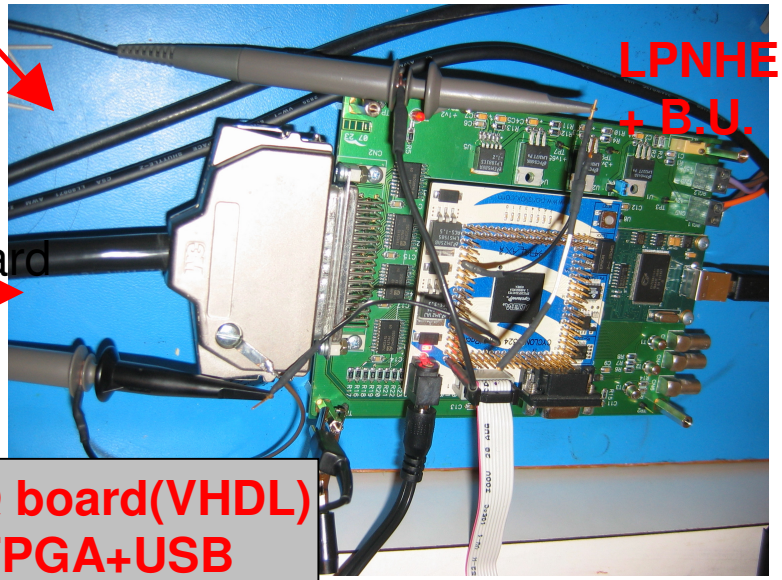


Here: 16 samples response for each of the 4 channels in the prototyped FE chip.



FE hybrid with 4 SiTR-130_v1
→ Total number of channels = 16

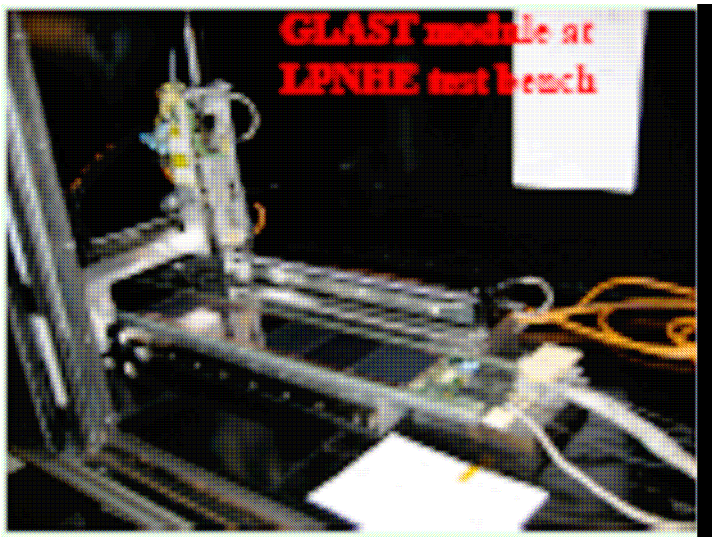
Cabe to DAQ board

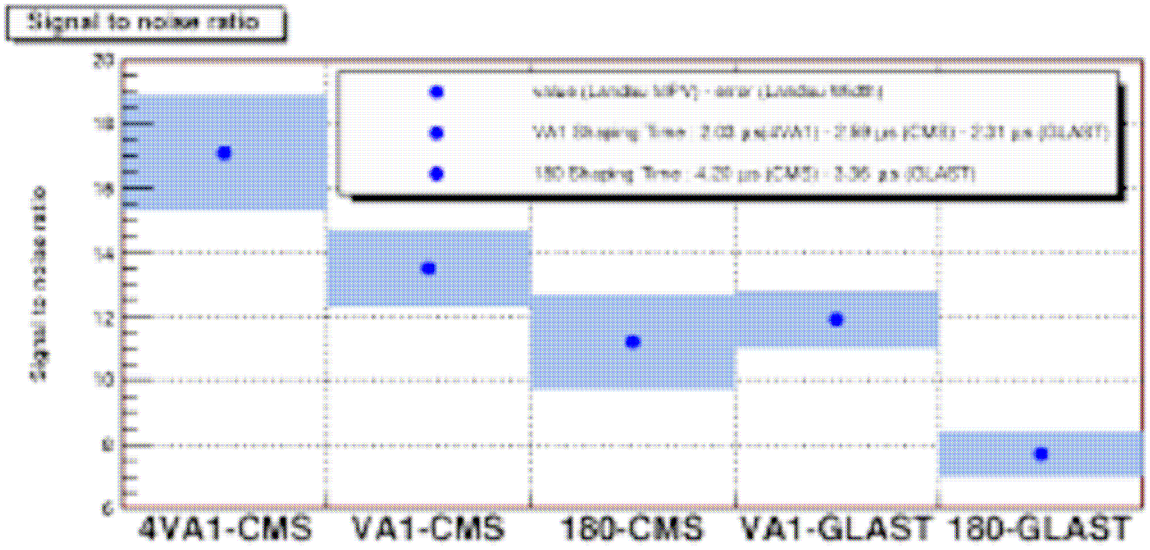


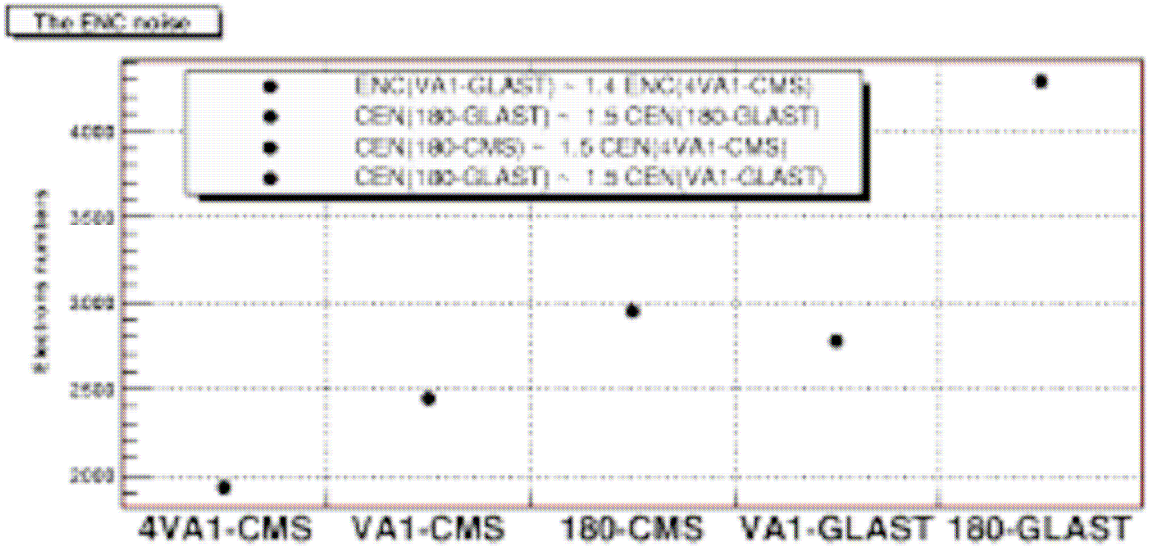
DAQ board(VHDL)
FPGA+USB
!New!

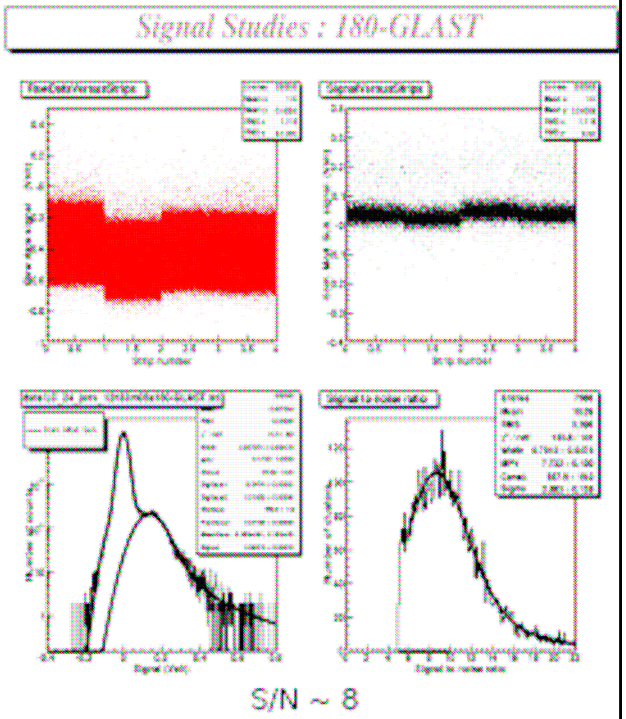
Characterization of Si detectors & FEE

Measurements S/N (MPV) and noise (ENC) at Lab test bench, on modules with 3CMS & 10 GLAST, read out by VA1 (ref) and SiTR-180 ***(first DSM FE proto)***



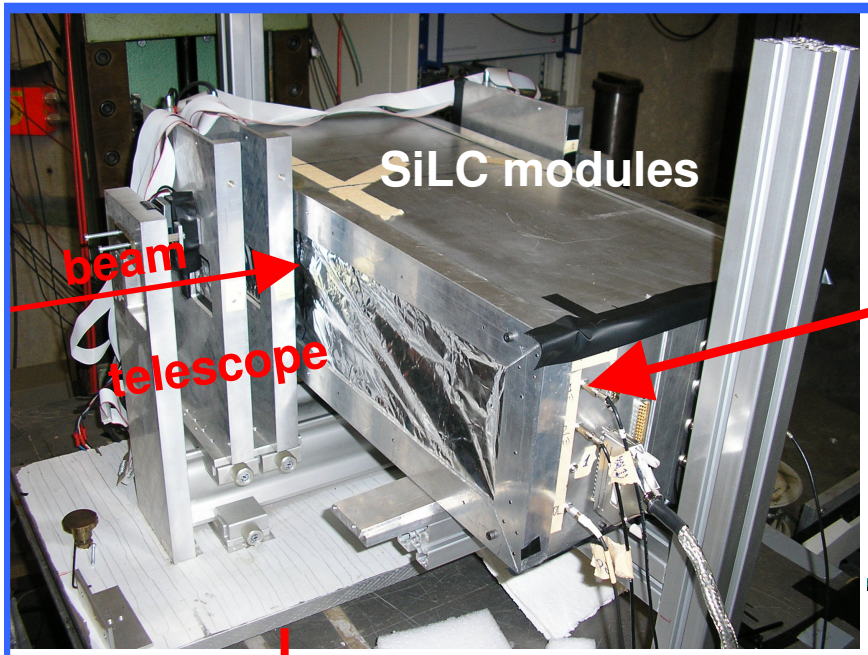


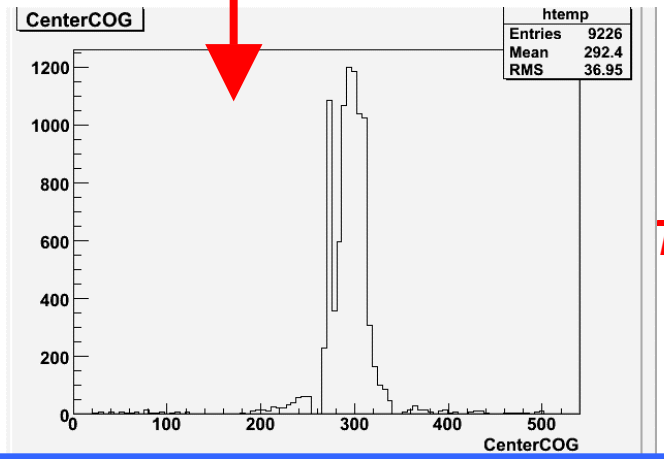




5°)Beam Tests *(CU Prague, IFCA, IEKP, LPNHE, Torino, HEPHY ….)*

- Beam test at DESY: June 4-15 2007, continuation of the beam test in Nov06, prepa:
- Beam test at CERN: October 10-22,2007, just successfully achieved
- Preparation of beam tests for next years





Beam test at DESY: 5 GeV electron beam
B.U., DESY, IEKP, LPNHE, CU Prague, IFCA

→ Continuation of tests at DESY (Nov 06) & new Lab tests at LPNHE testbench with CMS-180nm vs VA1 (i.e. reference)

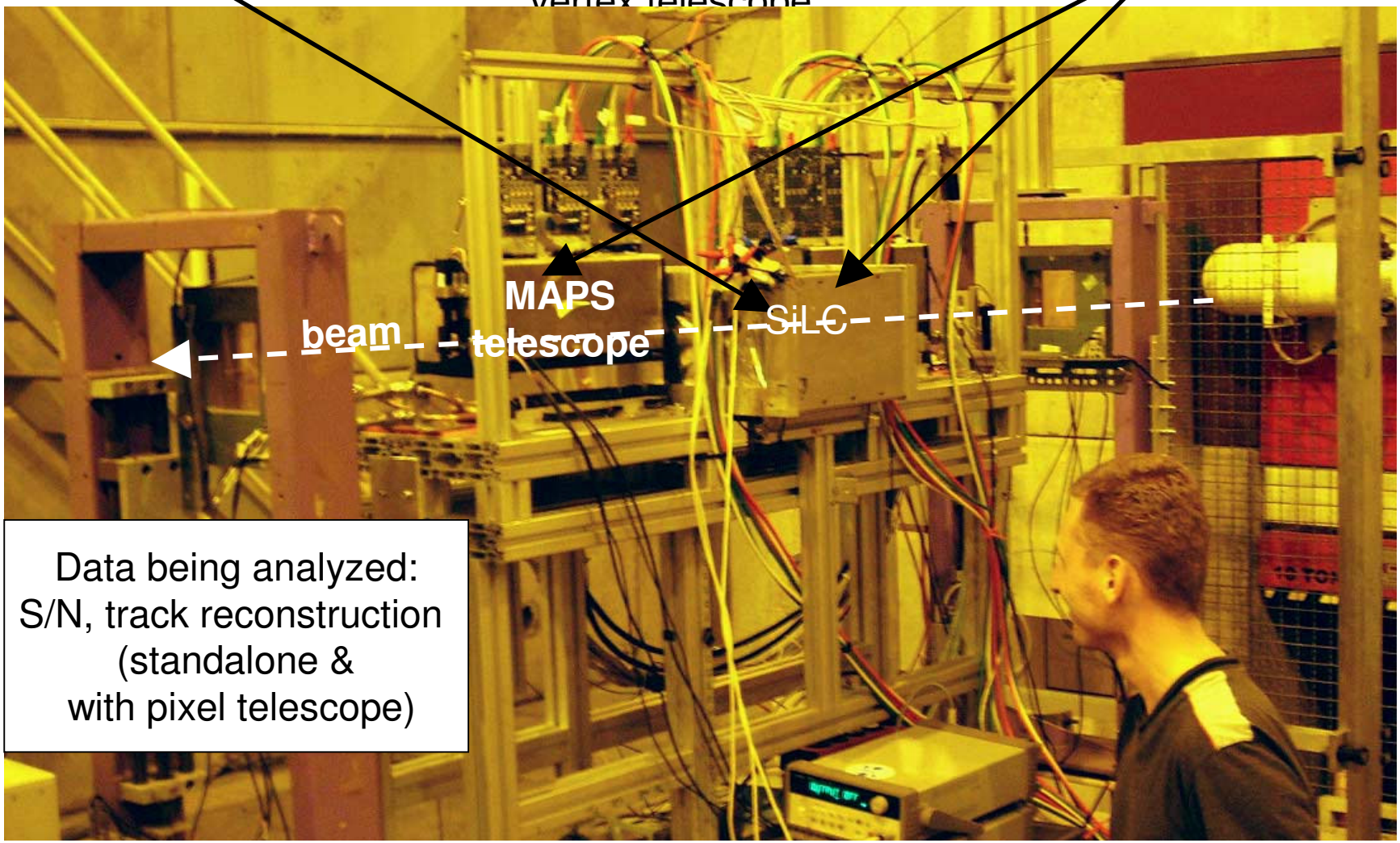
→Attempt to test S/N with Si module: 3CMS & 16ch of SiTR-130_v1prototype

- New DAQ Hardware: digitized FE+ FPGA + USB interface
- New DAQ software (VHDL + LabView)
- New FE board
- New cabling
- Preliminary tests at the Paris Lab test bench DAQ hard + soft, new chip on FE board connected to Si module

The complete new 130nm-system could not be ready for June tests thus tests were pursued at Lab, in preparation of CERN beamtest

Test Beam at CERN: October 10-22, 2007, H6 SPS beam

3 SiLC silicon modules in the Faraday cage, installed in between the 2 sets of MAPS vertex telescope



SiLC: IEKP Karlsruhe, LPNHE Paris, CU Prague, IFCA Santander, Torino INFN & Uni, and collaboration with Maps telescope: DESY & Geneva U. *SiLC, ALCPG 2007*

Main aspects of CERN T.B.

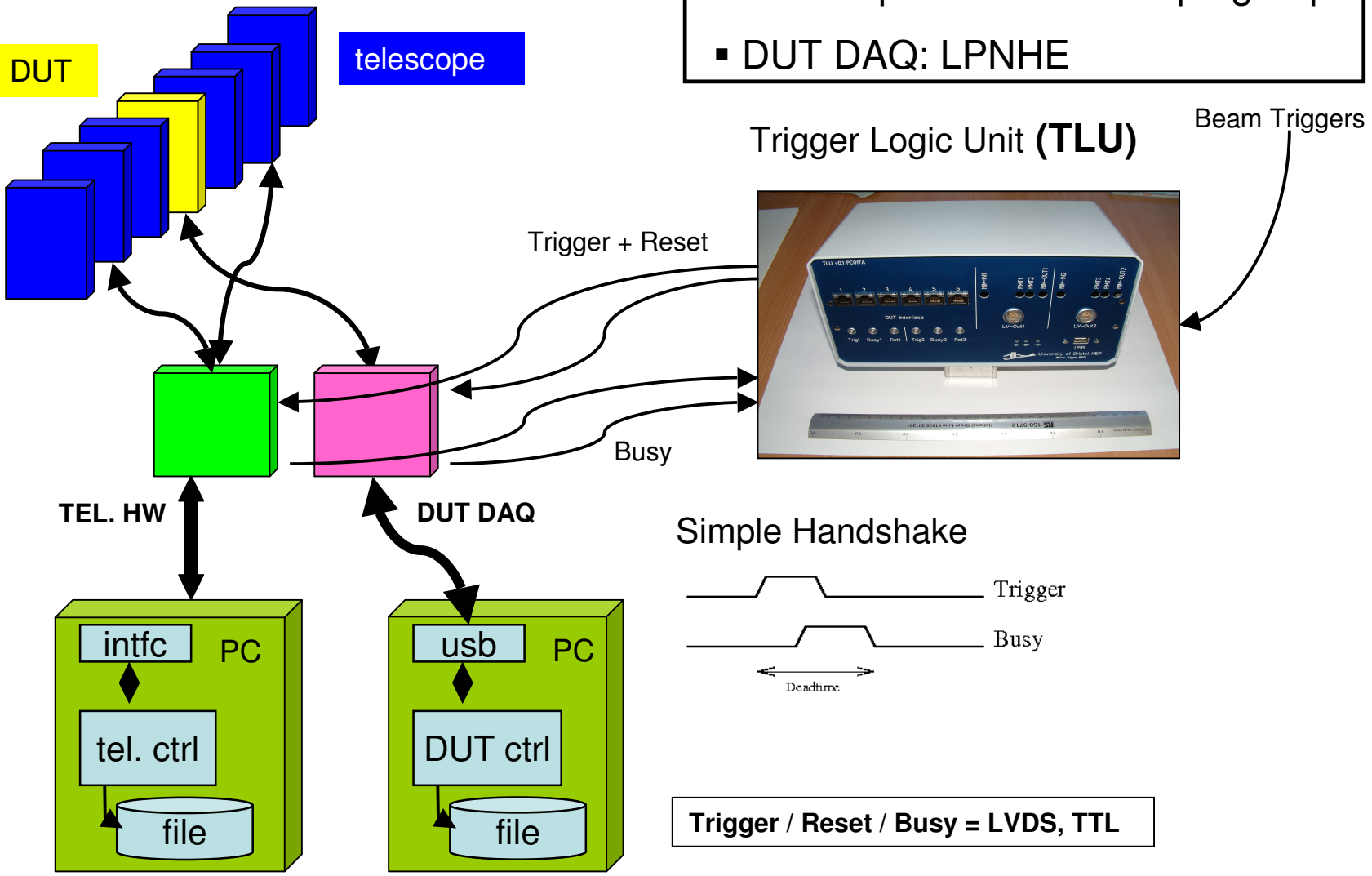
- One module made of 2 new Si HPK sensors identical to those that will be used for the large size prototypes for next year t.b., read out by SiTR_130 chip
- One module made of 3 CMS large sensors, read out with SiTR_130 chip
- One module made of 3 CMS large sensors read out with VA1chip (reference readout).
- New FE electronics prototype: full readout chain in 130nm UMC CMOS (4 channels per chip)
- New DAQ adapted to new digitized FE readout and to the common EUDET-ILC DAQ (for combined tests)
- Combined test beam with vertex EUDET telescope, i.e. 6 plans of MAPs pixels.

The SiLC collaboration has acquired expertise in running test beam especially since this last test beam at CERN. The system built with 3 modules can be used in standalone mode and will also serve as a telescope system for the forthcoming test beam with large prototypes. Plus expertise in running in combined test mode (here with vertex detector device)

TELESCOPE + DUT TESTBEAM

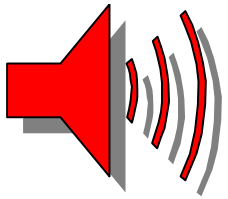
DUT= 3 Si µstrip modules (SiLC)
EUDET Telescope = 2x3 MAPS layers

- Overall DAQ + Beam & trigger:
  IFCA + CU Prague
- Telescope DAQ: Telescope group
- DUT DAQ: LPNHE

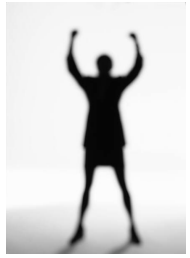


Simple Handshake

Trigger / Reset / Busy = LVDS, TTL



Advances in 2007



- Important progress in 2007 on:
- **New Si sensors** starting to be produced (several interested firms)
- **Front end chips**: full digitized FE readout chain characterized in real life test beam conditions.
- New **large area Si tracking prototypes**: IEKP, HEPHY, LPNHE and fruitful collaboration with CERN.
- Alignment prototype & insulating envelop prototype.
- **Collaboration** started with other sub **detectors:TPC & µvertex**
- **Beam tests** performed at DESY, starting at CERN , FNAL?
- More SiLC teams joining beam tests (prepa & construction)
- **Simulations studies** (use of pixels; internal and forward regions etc..)
- **Industrial firms starting active contributions** on crucial aspects: new sensors & inline pitch adapter (new Si modules).
- R&D SiLC collaboration developing well: regular meetings of the whole collaboration or on dedicated topics, and
- Fruitful **synergy with LHC**