ALCPG07
October 22-26, 2007
Fermilab, Batavia, Illinois, USA
http://ilc.fnal.gov/conf/alcpg07/
Joint meeting of the American Linear Collider Physics Group and ILC Global Design Effort
AdvancedTCA

ATCA based 16 channels 12bit 500MHz DIGITIZER

Status of Project

10/31/2007

Alexey Semenov, Manfred Wend
ATCA Digitizer

Why we are needed a new architecture and packaging standard for the ILC instrumentation?

- ✓ Recent accelerators have availability 40-70%
- ✓ The ILC will be 7-10 times the size of any comparable existing linear machine

- ➢ So, it is essential that the ILC controls, instrumentation and electronics systems be designed with *High Availability* architectures!
- ➢ And this architecture should provide *High Availability* at both *hardware and software* levels!

Why the Advanced Computing Telecommunications Architecture (ATCA) is a strong Candidate Platform for ILC Instrumentation?

- This is not just the fastest technology!

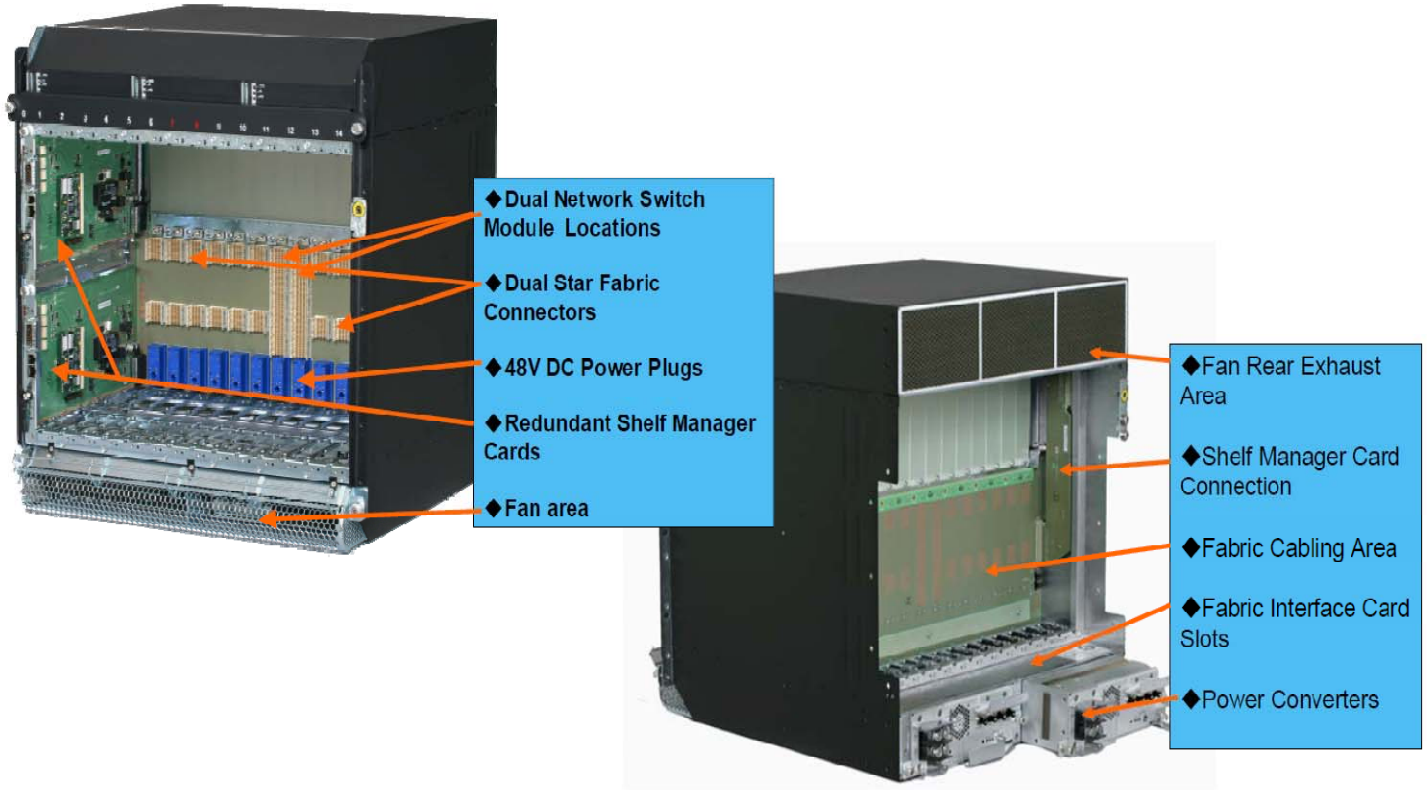
ATCA	2.5 Terabits/sec
ExpO x16	40 Gigabits/sec
VITA 41	20 Gigabits/sec
PICMG 2.16	1000Mbytes/sec
PCI 64 x 33MHZ	533Mbytes/sec
VME 320	320Mbytes/sec
VME 64x	160Mbytes/sec
PCI 64 x 33MHZ	133Mbytes/sec
VME64	80 Mbytes/sec
VME32	40Mbytes/sec
VME16	20 Mbytes/sec

- Scalable capacity up to 2.5Tbs
- Dual Star, Mesh, and Replicated Mesh topologies
- Board size: 8U (322.25mm) high and 280mm deep
- 140 sq. inch compared with 54 sq. inch for VME and cPCI
- Slot pitch is 1.2" (taller components like next generation CPU's)
- 8 high speed differential pairs per channel (4 ports per channel, 2 pairs per port), each pair capable of data transmission up to 5 Gbps

Why the Advanced Computing Telecommunications Architecture (ATCA) is a strong Candidate Platform for ILC Instrumentation?

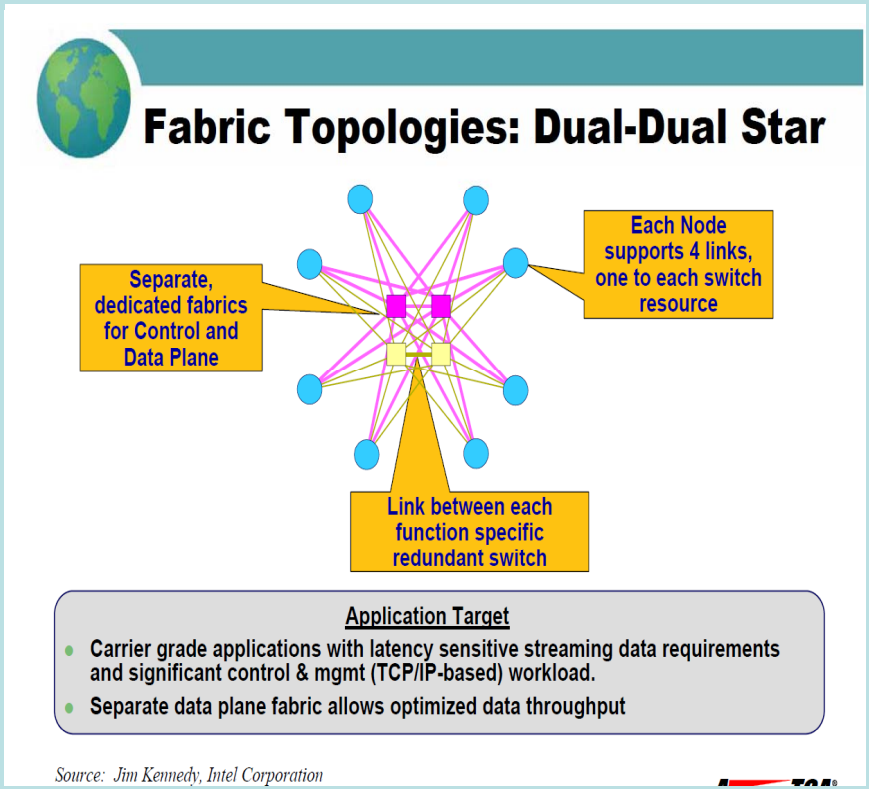
- This system contains the essential features to guarantee a *Service Availability* of a crate full of processing and instrumentation electronics of 99.999% (Five 9's) ~ *5 min downtime/year*:
  - ✓ Dual redundant communication processors and links
  - ✓ Redundant control and data planes
  - ✓ Redundant -48V power feeds
  - ✓ Single board failure domain
  - ✓ No single point of failure for any system interconnect
  - ✓ Intelligent crate (shelf) diagnostics and management
  - ✓ Hot-swap capability for all boards & active modules
- ATCA is an *open standard platform* designed by a strong industry consortium (PICMG)

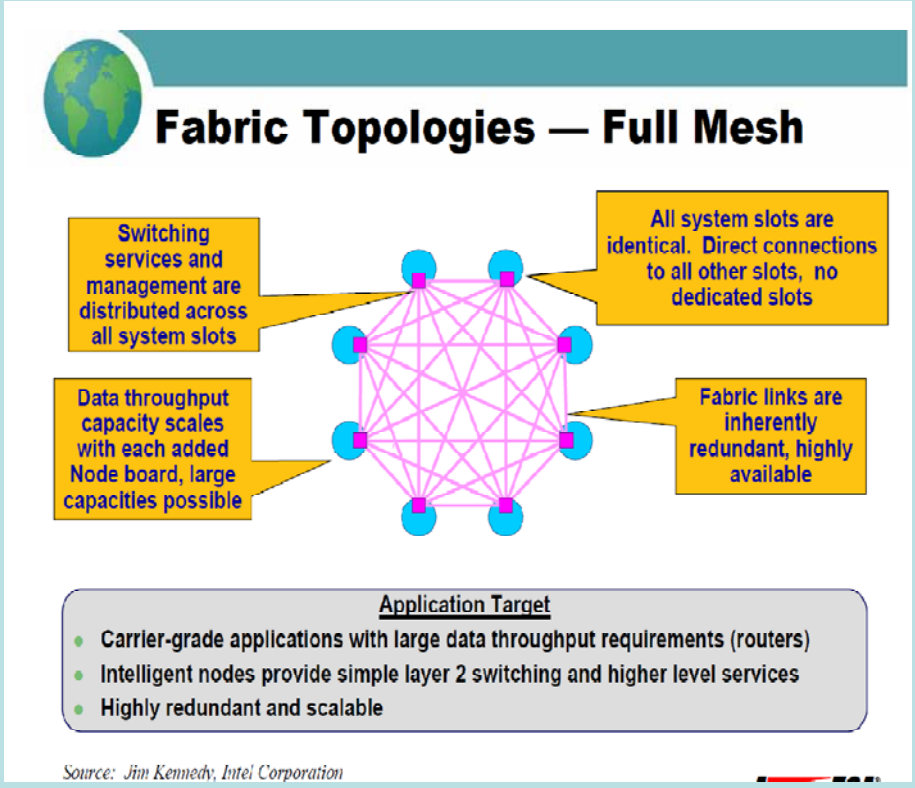
Why the Advanced Computing Telecommunications Architecture (ATCA) is a strong Candidate Platform for ILC Instrumentation?



Why the Advanced Computing Telecommunications Architecture (ATCA) is a strong Candidate Platform for ILC Instrumentation?

➢ *No single point of failure for any system interconnect!*





- ✓ **ATCA - Advanced Computing Telecommunications Architecture - is an**

standard platform originally designed for Telecommunication industry,

not for Instrumentation!

Main Question is:

- ➢ **What is the best way to check how good is this Platform for ILC Instrumentation?**

- **What is the best way to check how good is this Platform for ILC Instrumentation?**

-

The Design
***multi-channel*(16),**
***12 bit resolution*,**
***fast*(500MHz)**
ATCA *Digitizer*

Today's Standard Tools for Diagnostic and Control:

- ✓ **Digital Down Converters**
- ✓ **Digital Dumpers**

All Based on accurate and fast Digitizers !

Project Critical Point #1:

- **High Data Rate :**
  - ✓ **ADC to FPGA (500MSPS)**
  - ✓ **FPGA to DAC (max 1200MSPS)**
  - ✓ **FPGA to/from DDR2 RAM (633MSPS)**
  - ✓ **Fabric Interface (1000MBPS)**
  - ✓ **Base (Ethernet) Interface 10/100/1000MB**

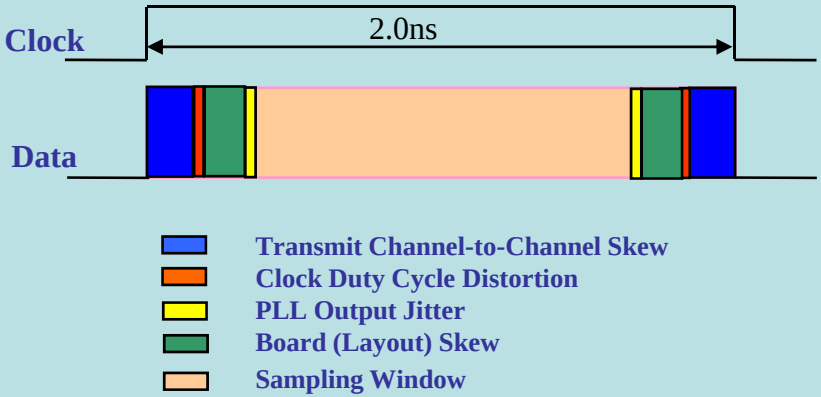
Solutions:

LVDS

Dynamic Phase Alignment (DPA)

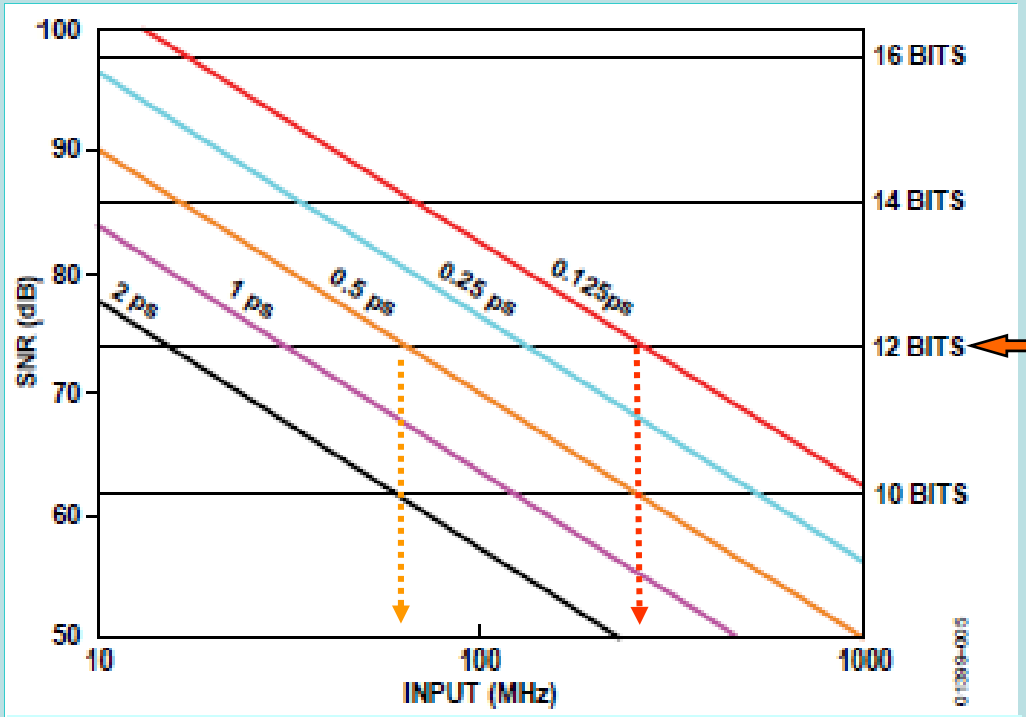
Dynamic Auto-Calibration Circuit

Timing Budget Analysis of 500MHz System



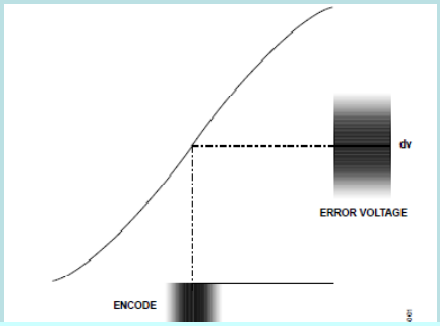
Project Critical Point #2:

- **ADC & DAC Clock Jitter: How to reach 0.1- 0.5 ps RMS ?**



Signal-to-Noise Ratio Due to Aperture Jitter

Quantization Limit

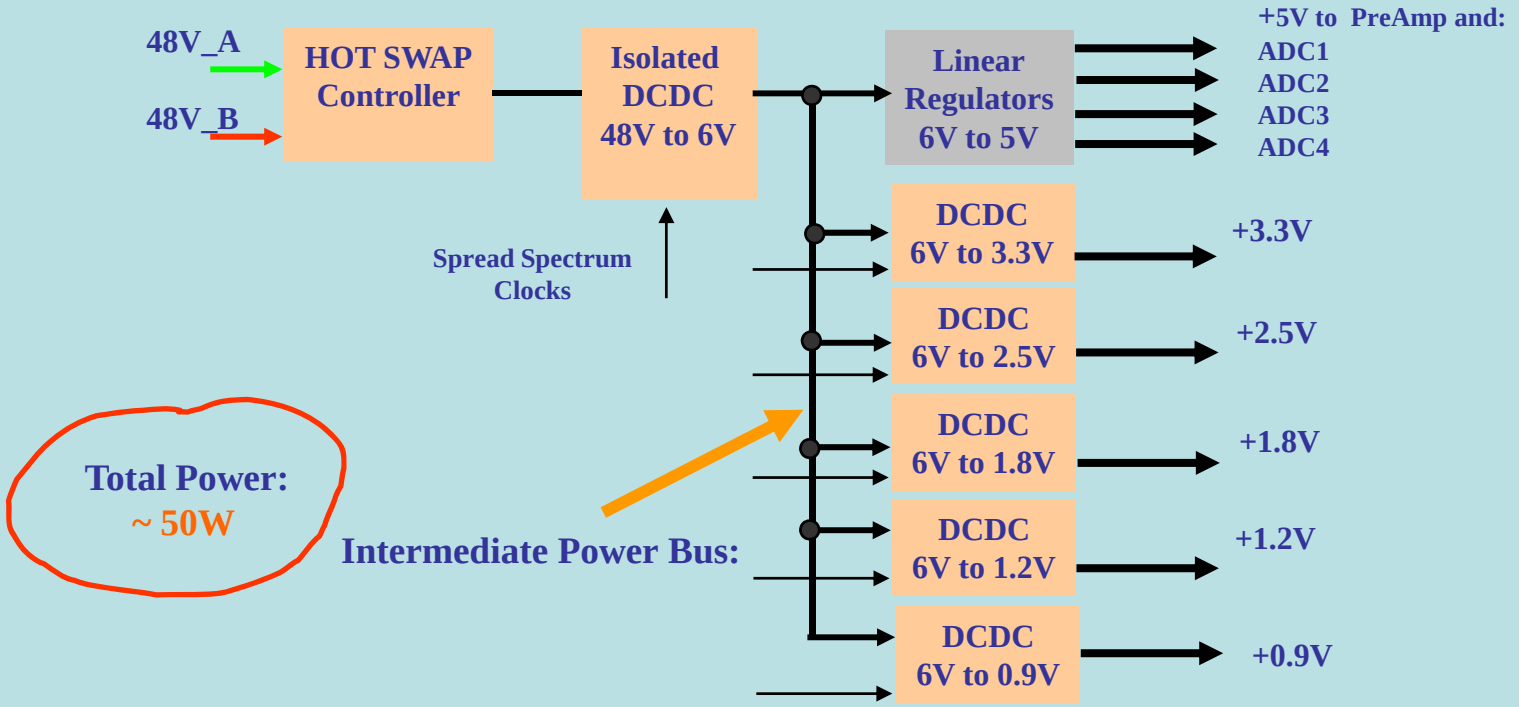


Amplitude Error vs. Clock Jitter

Project Critical Point #3:

- ***How to reduce EMI from ATCA – 48V DC-DC Power Converters?***

Power Distribution



Project Critical Point #3:

- ***How to reduce EMI from ATCA – 48V DC-DC Power Converters?***

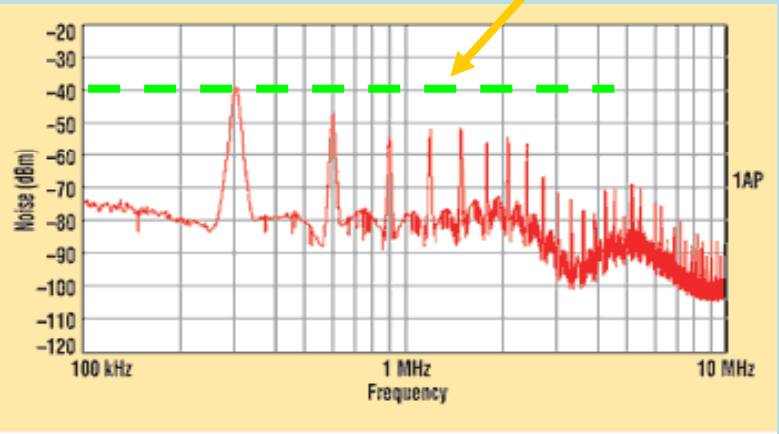
  - ✓ ***Spread-Spectrum Clock for DC-DC ?!***

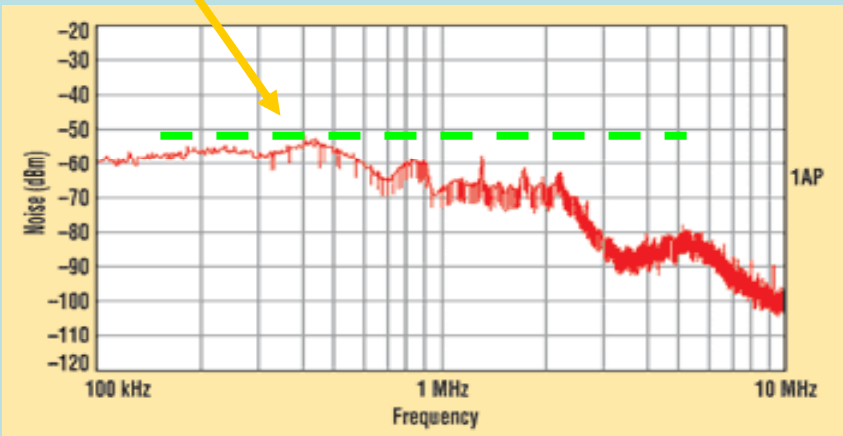
  - ✓ ***Slew Rate Controlled MOSFET Switches?!***

Project Critical Point #3:

- ***How to reduce EMI from ATCA – 48V DC-DC Power Converters?***
  - ✓ ***Spread-Spectrum Clock for DC-DC !***

40 dBm vs 55 dBm

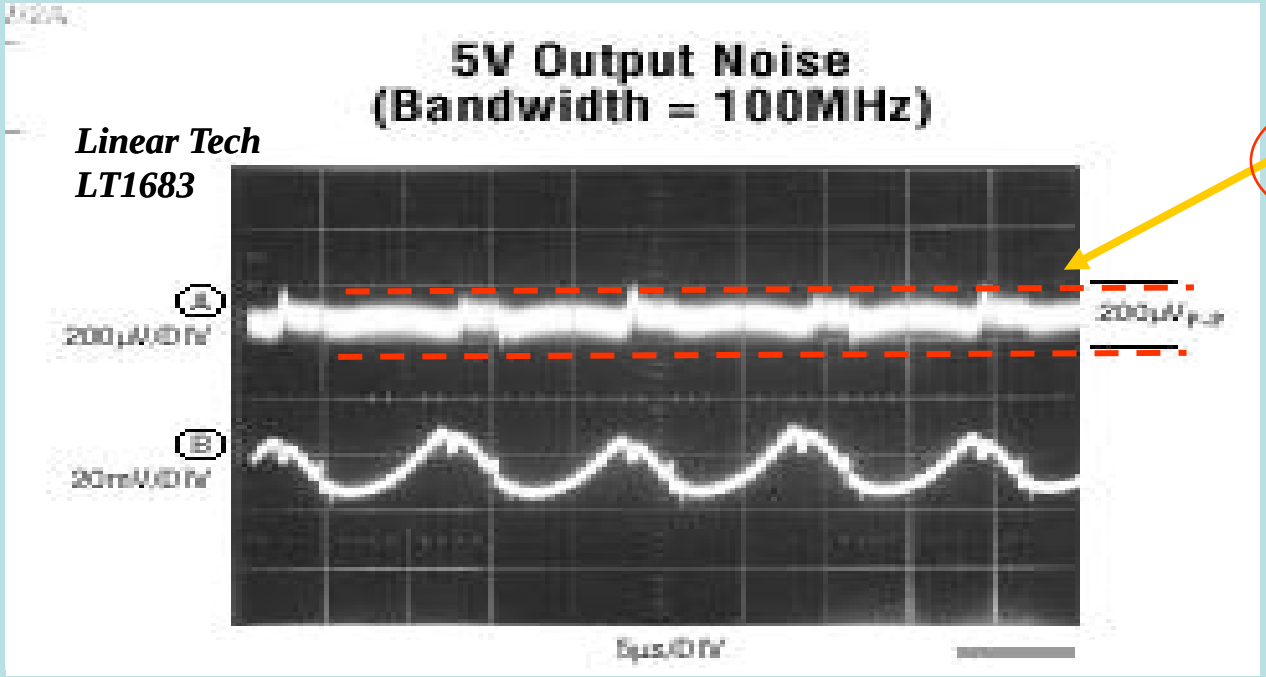




Output spectra demonstrate that a conventional fixed-frequency clock produces considerably more noise than does the spread-spectrum technique.

Project Critical Point #3:

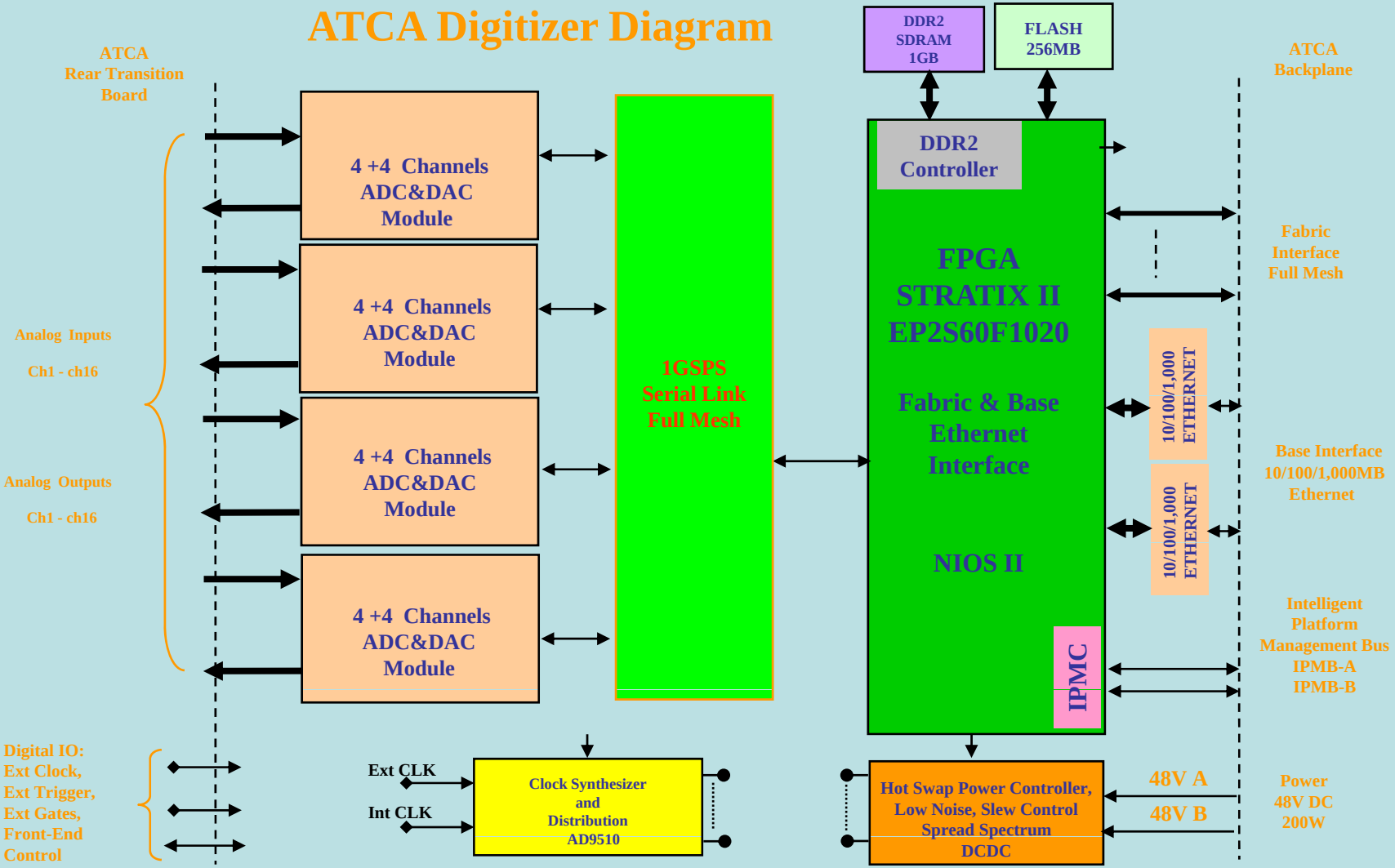
- ***How to reduce EMI from ATCA – 48V DC-DC Power Converters?***
  - ✓ ***Slew Rate Controlled MOSFET Switches!***

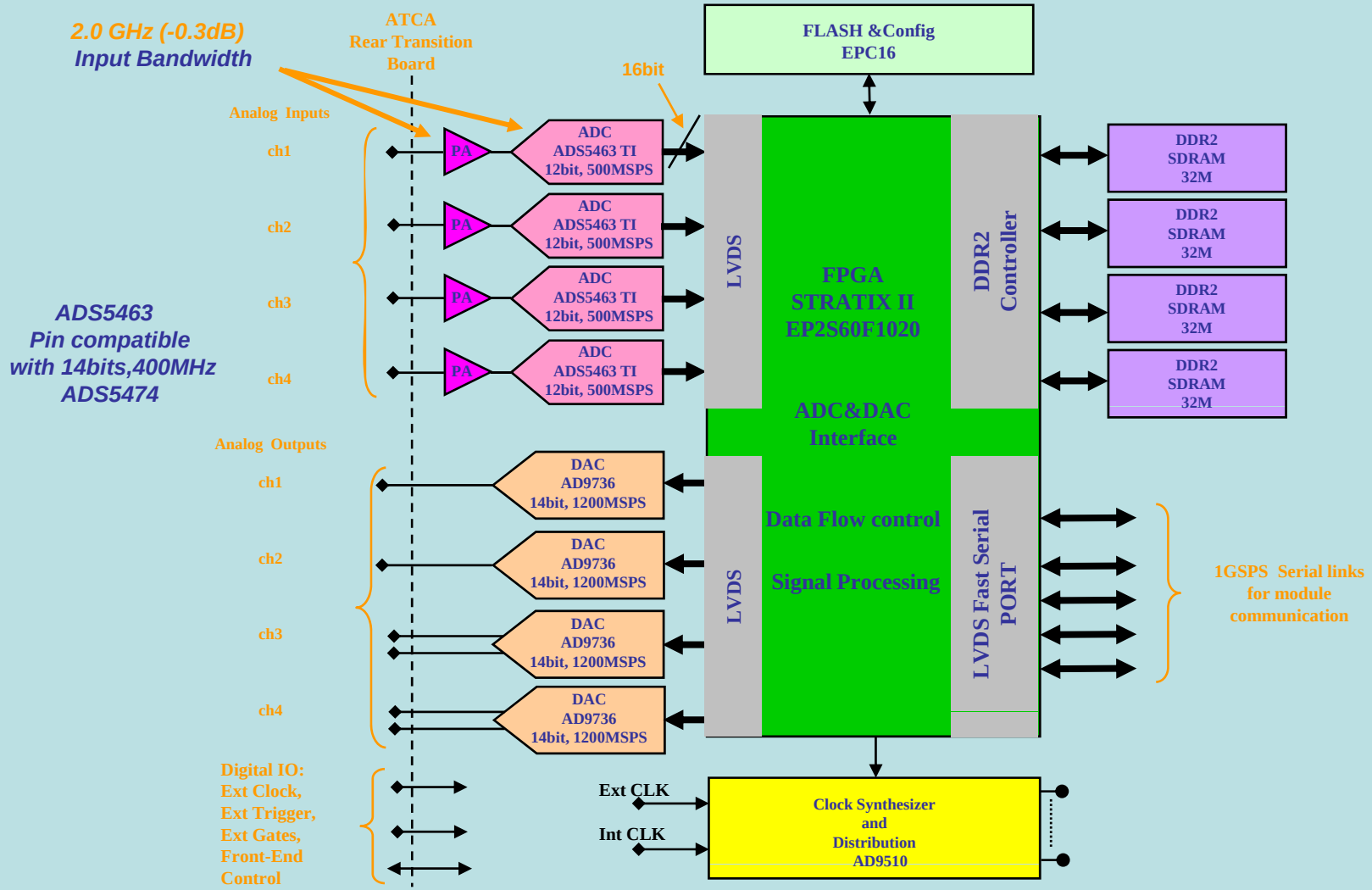


~40 dB reduction
~ 200µV !

LT1683 (Linear Tech) DCDC controller reduce conducted and radiated EMI by controlling the voltage and current slew rates of external MOSFET switches

ATCA Digitizer Diagram



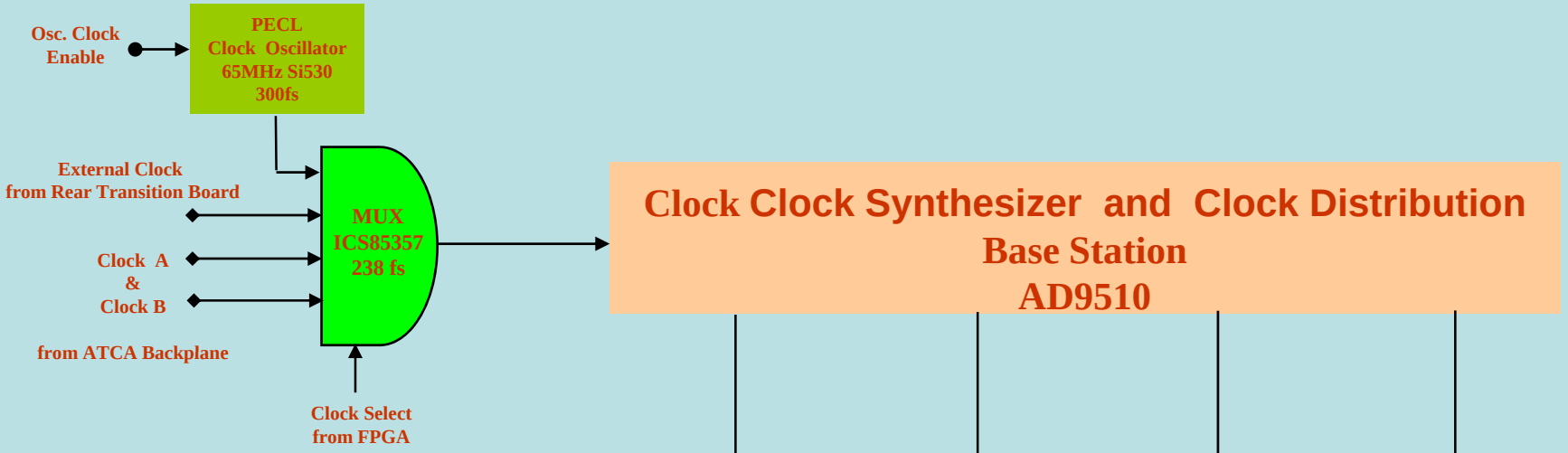


10/31/2007

Alexey Semenov, Manfred Wend
ATCA Digitizer

ADC & DAC
4 channels Module

Clock Synthesizer and Clock Distribution Tree



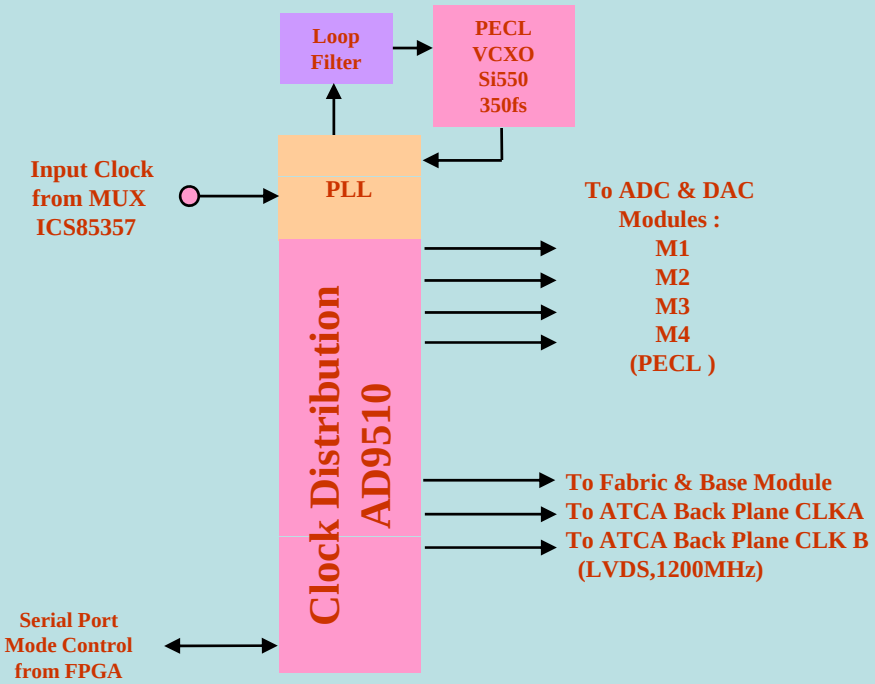
Based on AD9510 (Analog Device):

- ✓ *Additive output jitter 275 fs RMS*
- ✓ *Input reference frequencies to 250MHz*
- ✓ *4 independent 1.2 GHz LVPECL clock outputs*
- ✓ *4 independent 800MHz LVDS clock outputs*
- ✓ *Programmable divider for each output*
- ✓ *Fine delay adjust for two LVDS output*
- ✓ *Serial mode control port*

AD9510:

- ✓*Additive output jitter 275 fs RMS*
- ✓ *Input reference frequencies to 250MHz*
- ✓ *4 independent 1.2 GHz LVPECL clock outputs*
- ✓ *4 independent 800MHz LVDS clock outputs*
- ✓ *Programmable divider for each output*
- ✓ *Fine delay adjust for two LVDS output*
- ✓*Serial mode control port*

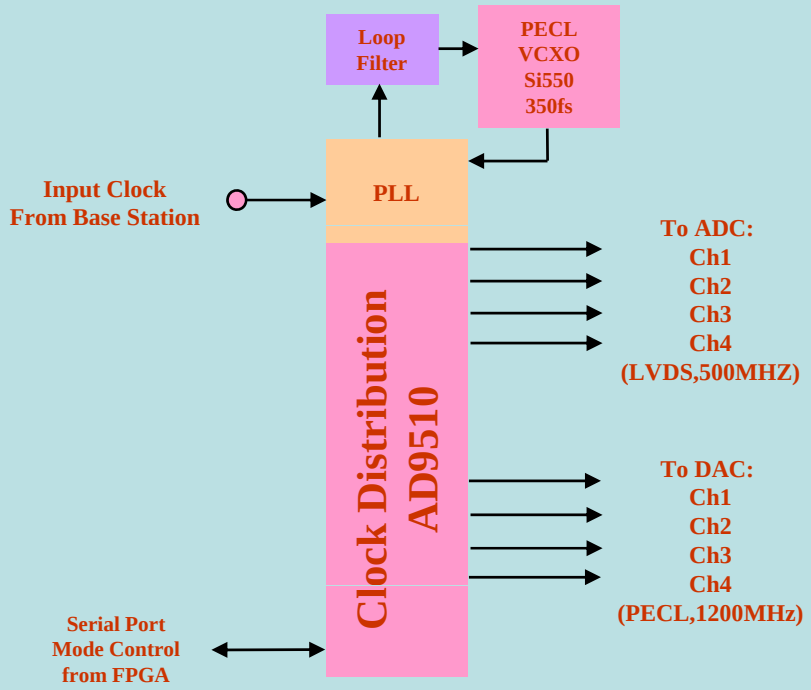
Clock Base Station



AD9510:

- ✓*Additive output jitter 275 fs RMS*
- ✓ *Input reference frequencies to 250MHz*
- ✓ *4 independent 1.2 GHz LVPECL clock outputs*
- ✓ *4 independent 800MHz LVDS clock outputs*
- ✓ *Programmable divider for each output*
- ✓ *Fine delay adjust for two LVDS output*
- ✓*Serial mode control port*

ADC&DAC Synthesizer and Clock Distribution (4 identical Station)



Digitizer Layout (in progress)

Summary
Project Hardware Status

- ✓ **Digitizer Schematic – *done***
- ✓ **Board Layout – *in progress…* *December 2007***
- ✓ **FPGA VHDL code – *in progress…* *May 2008***