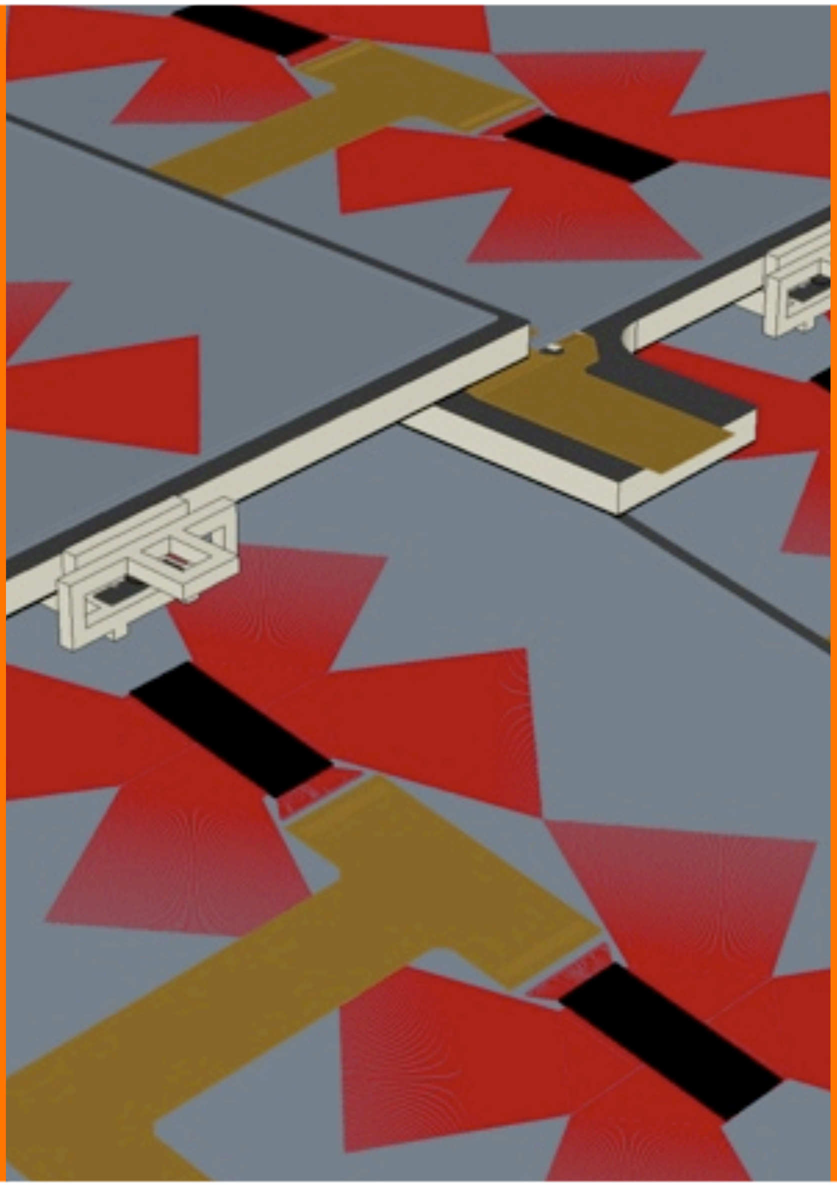


Tracking with Silicon

Tim Nelson - SLAC

ALCPG07

FNAL - October 24, 2007

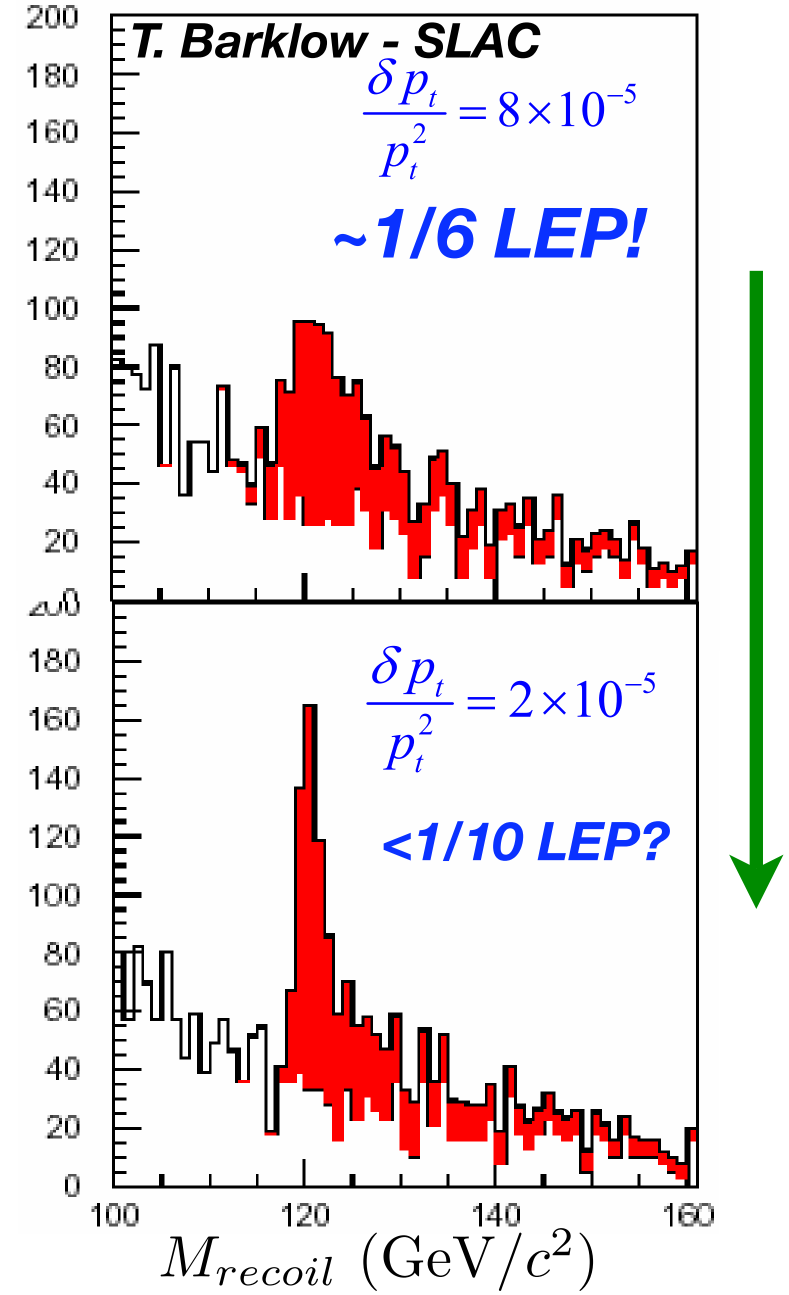
Why Silicon?

- Allows emphasis on phi resolution:
  - Superior asymptotic P_T resolution for given B-field and Δr
  - A prime ILC example:

$$e^+e^- \to Z^0H^0 \to \mu^+\mu^- + X$$

$$\text{Given } \sqrt{s}, M_Z, M_{\mu\mu} \Longrightarrow M_H$$

- Fast response allows single-bunch timing:
  - *Si*D: # of voxels / bunch train > typical TPC
- Sensors required are technologically mature
- Robust against aging and beam accidents

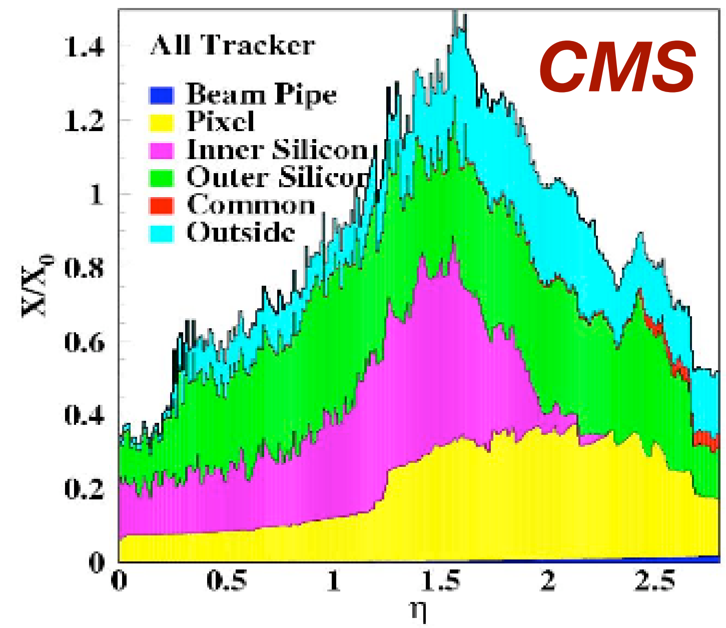


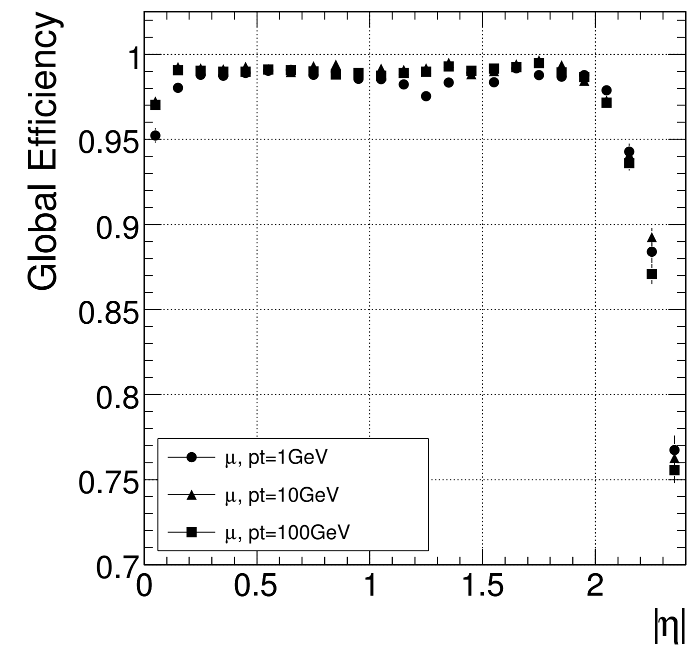
Key R&D Drivers

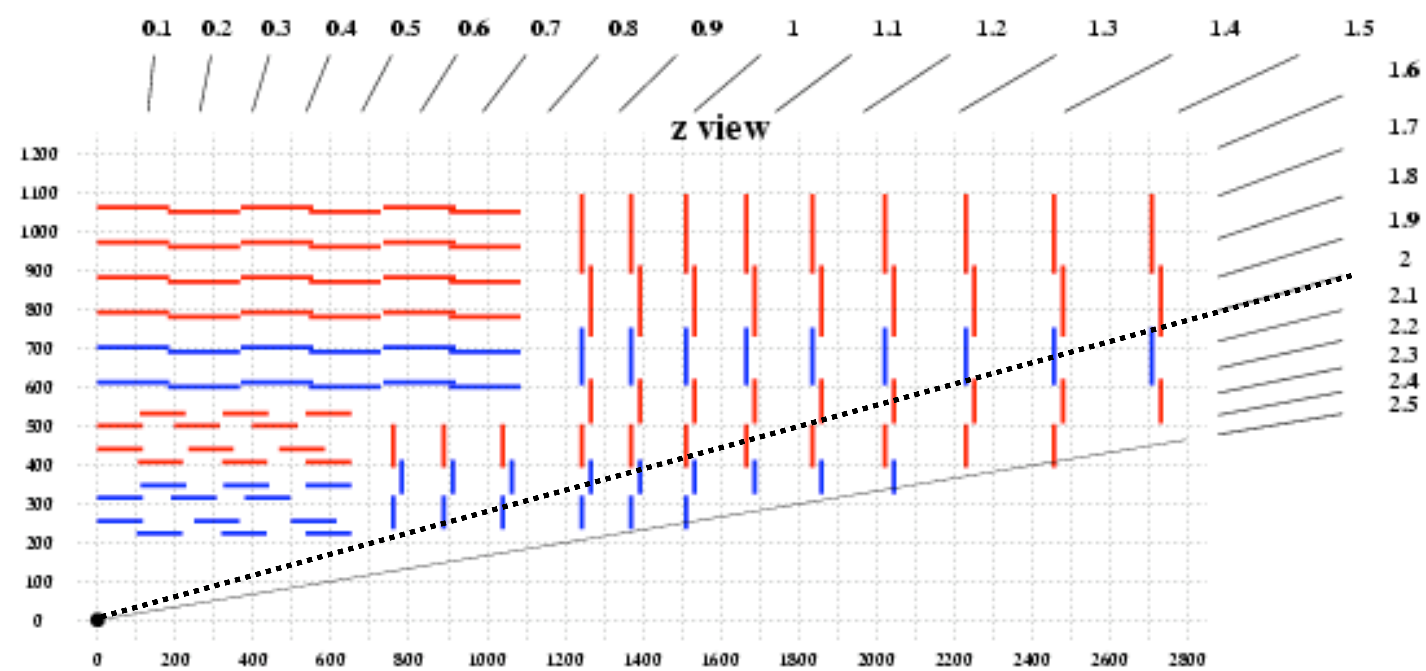
Where is the R&D challenge?

- Large silicon trackers (ATLAS, CMS) have been too massive
- Excellent forward tracking has eluded previous efforts
- Some tracks (e.g. non-prompt) can pose difficulties

These are the key issues to be resolved by the R&D program

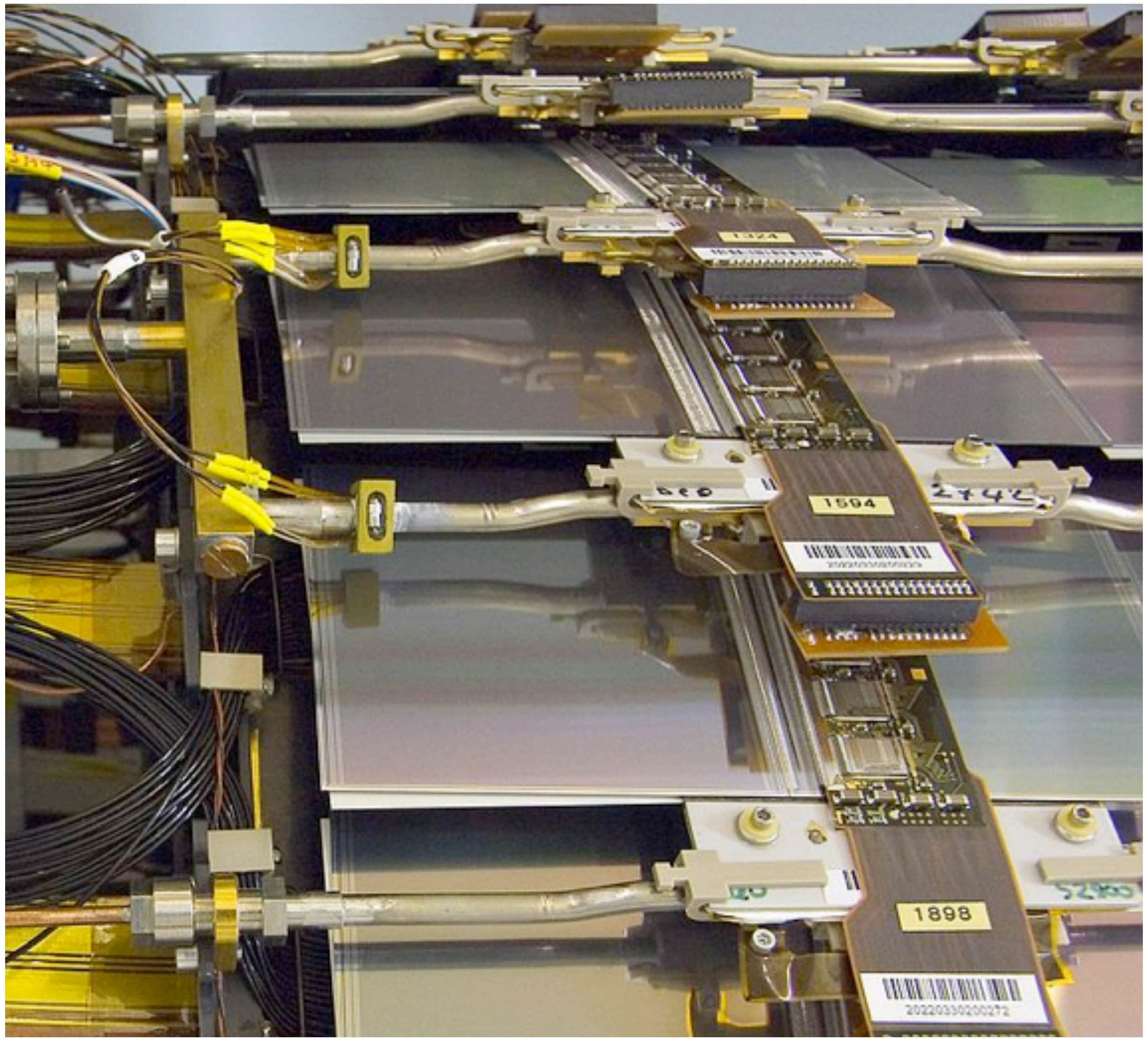






Reducing Material

- Cooling: eliminate
- Readout / Power: reduce
  - Chips
  - Hybrids
  - Cables
- Support: minimize
- Sensor: thin?



Eliminate Liquid Cooling

- Pulsed operation of front end results in ~100X reduction in power
- Tracker designs under consideration can be gas cooled

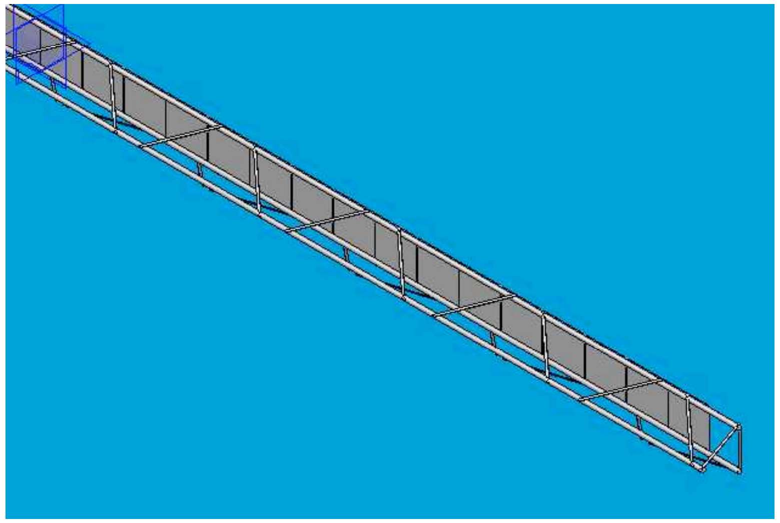
Pulsed power is a common element of ILC readout efforts, in particular:

- Long Shaping Time Front End (LSTFE) - *SCIPP/UCSC*
- SiTR - *LPNHE/LAPP* (SiLC Collaboration)
- *KPiX* (also Si-W ECal) - *BNL, UC Davis, Oregon, SLAC*

These efforts differ primarily in approach to reducing readout material

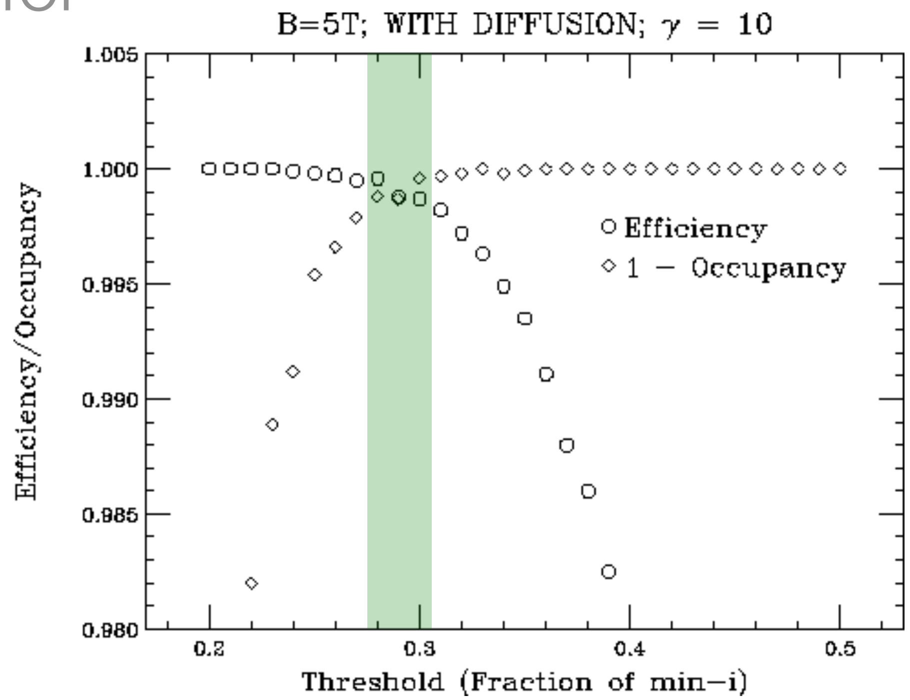
LSTFE

SCIPP/UCSC

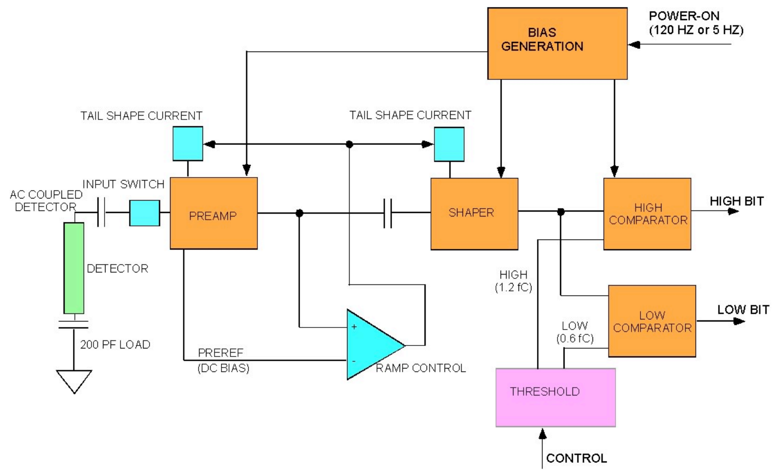


Simple approach: dilution of readout material

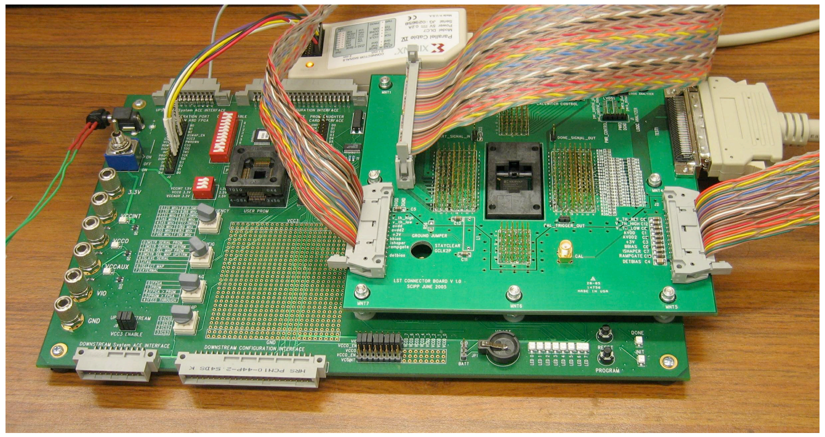
- Design tracker with long daisy-chained strips
- Goal: ladders 1/2 length of SiD barrels (up to 1.7m)
- Simulation indicates a feasible operating point.
- Requires carefully designed front end, optimized for low noise in this regime: long shaping time



LSTFE



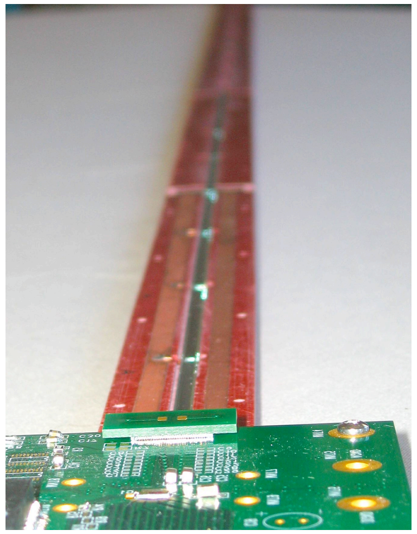
FPGA-based digital section

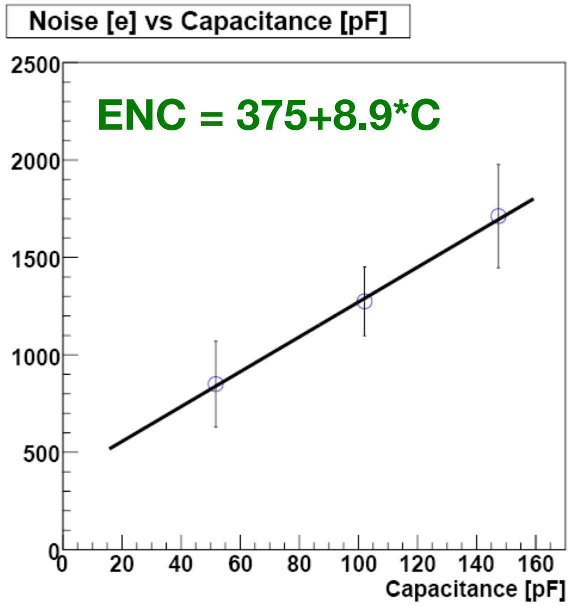


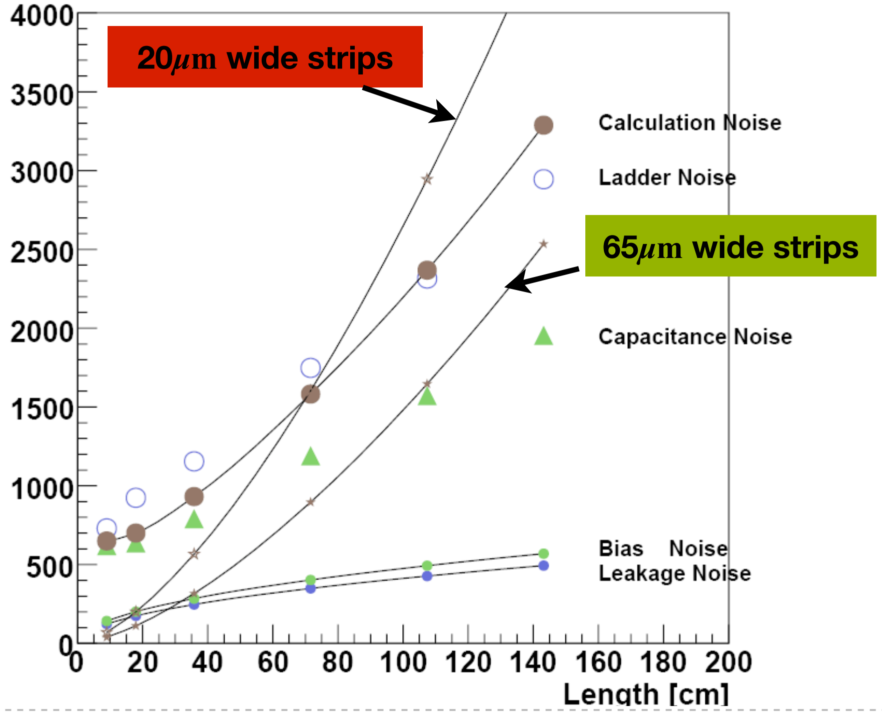
LSTFE

SCIPP/UCSC

- Tests with long strips of GLAST sensors: noise performance of front end is excellent.
- Challenges remain for ultra-long ladders
  - Manufacturing/handling/installation
  - Series resistance of narrow strips
  - ➡ ***targeting 80cm for long ladder approach***
- Narrow-strip test-ladders (CDF L00 sensors: 8μm)
- Delivery of 128-channel LSTFE-2 in ~1/08
  - Improved power cycling
  - Increased dynamic range ($\geq 50 \times$ min ionizing)
  - Improved time-over-threshold precision





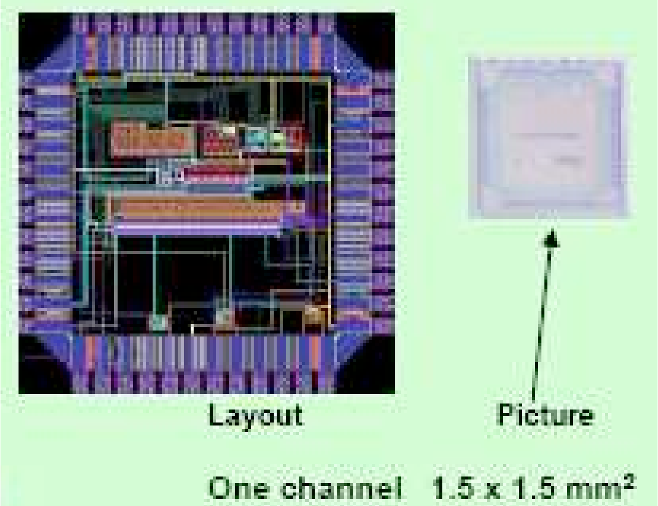


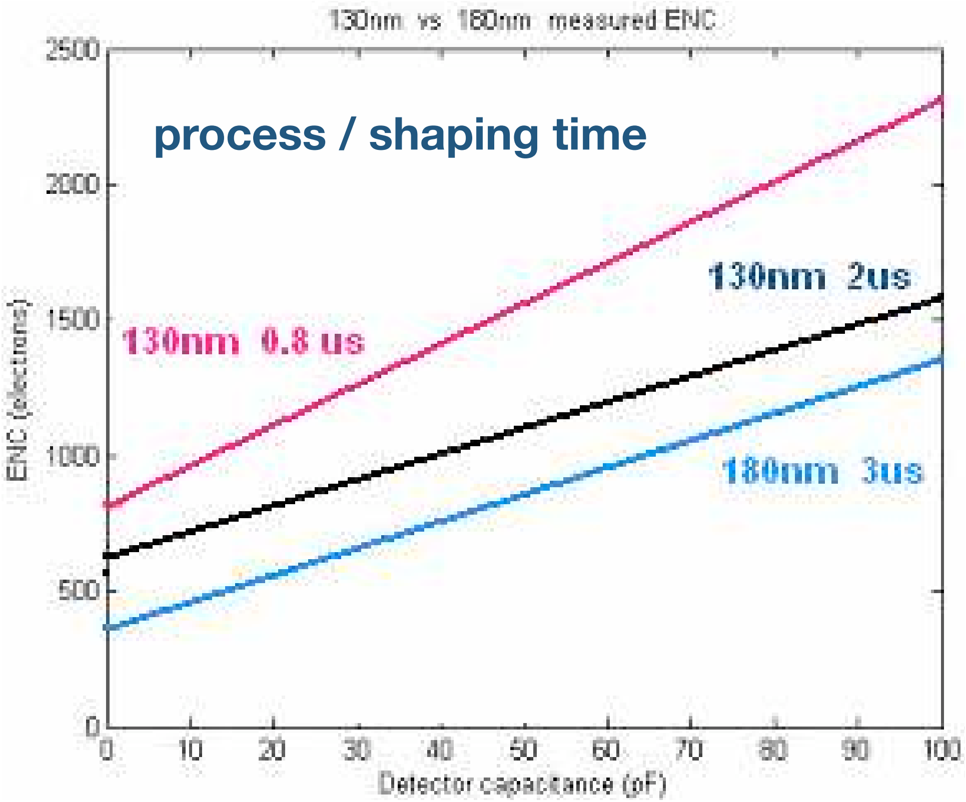
SiTR

LPNHE, LAPP (SiLC)

- Also optimized for long ladders
  - preamp/shaper w/ 2.5μs shaping time
  - “analog” charge measurement (instead of TOT)
- Pushing to smaller process sizes
  - Currently 130 nm: noise appears manageable
- More function currently integrated on-chip
  - trigger/sparsifier, buffering, digitization, calibration
  - no power cycling yet
- Next chip Q1 2008: 128 channels, power cycling
- Investigating various “traditional” ladder concepts: also considering more extreme alternatives...

SiTR-130_v2





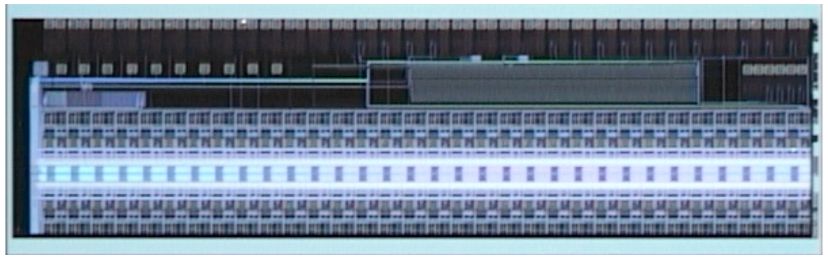
KPiX

BNL, UC Davis, Oregon, SLAC

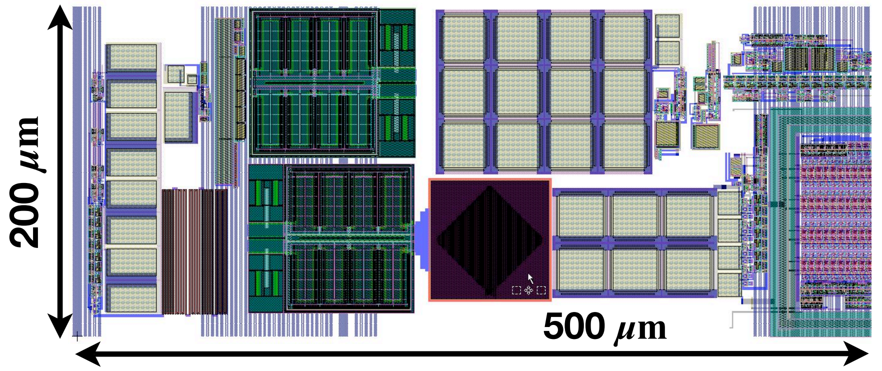
More radical approach: elimination of components

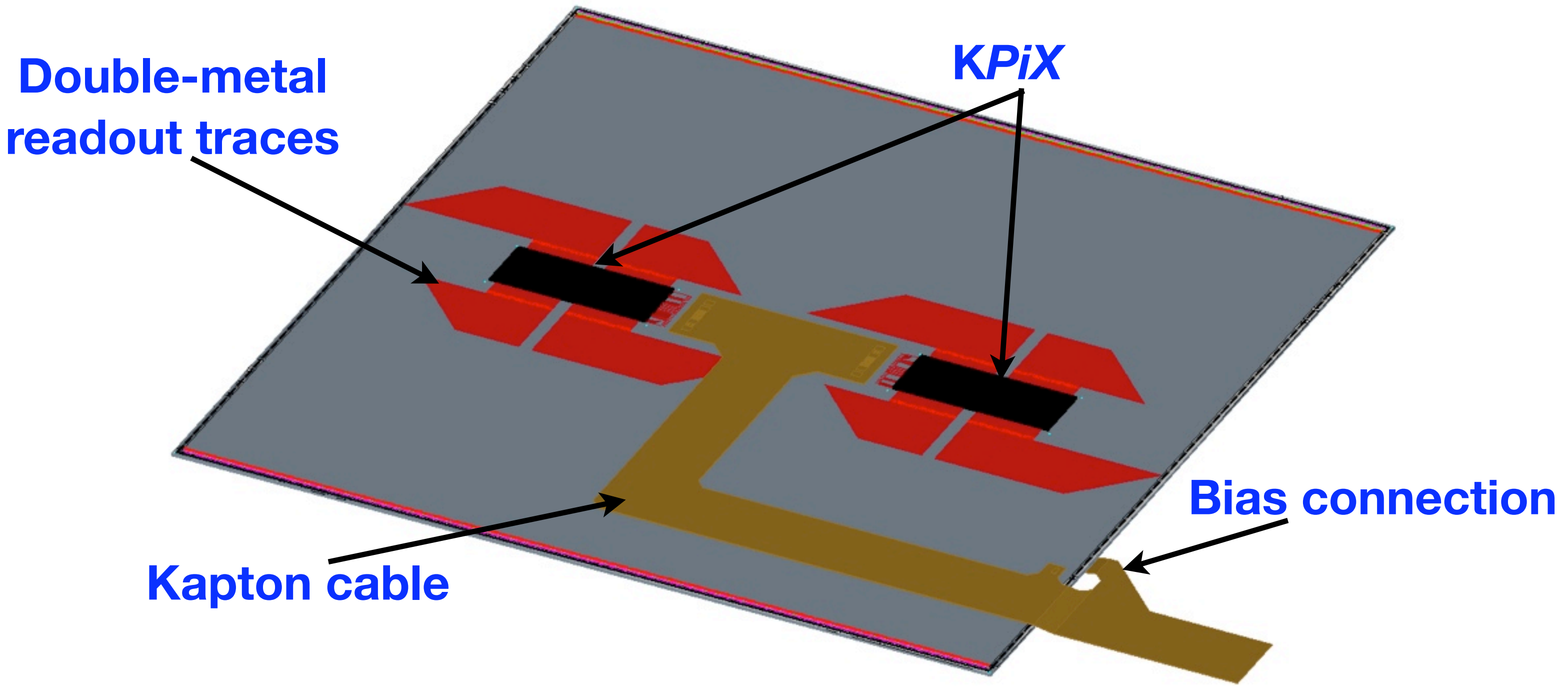
- Store signals in 4 analog buffers, digitize/read out between trains: quiet operation during acquisition
- Chip bump-bonded to sensor: eliminates hybrid
- Read out through double-metal traces, low-mass cable
- New progress on gold-stud bump bonding

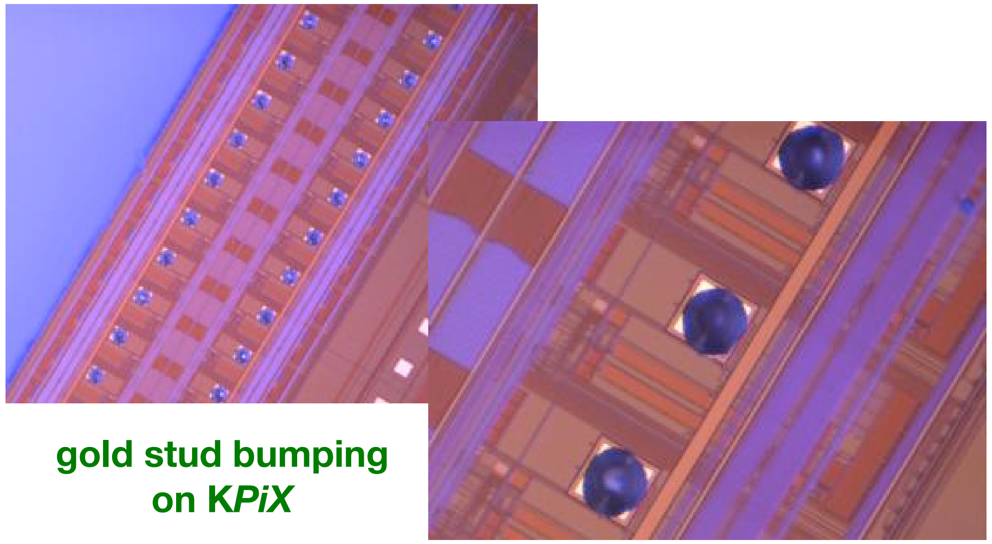
2×32 KPiX64



a single cell of KPiX







gold stud bumping on KPiX

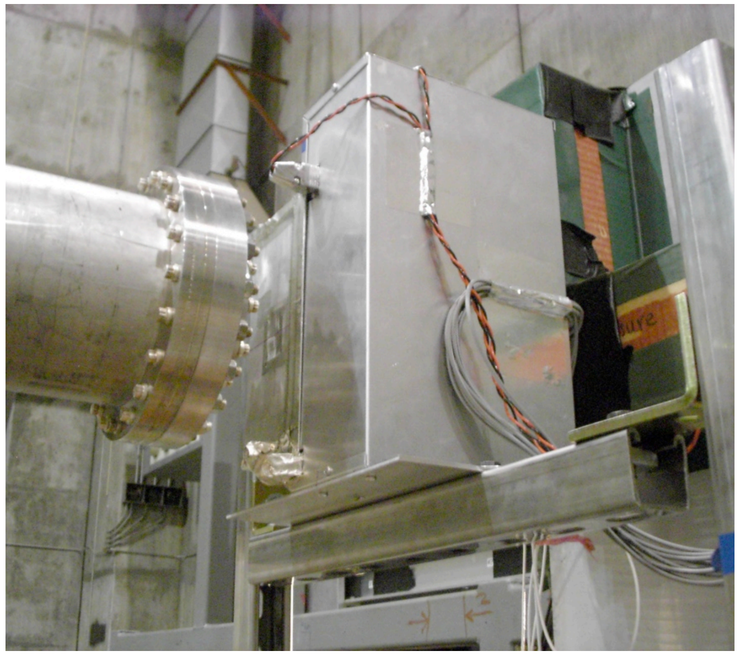
KPiX

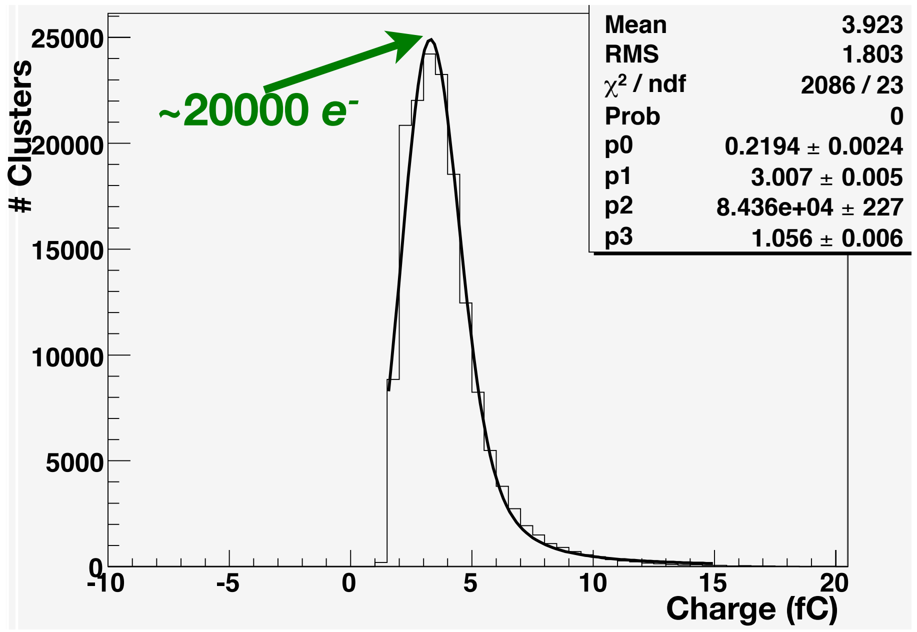
BNL, UC Davis, Oregon, SLAC

- 64-channel prototype, *KPiX*64-4 has undergone extensive testing
  - All major features working
  - Noise in trigger branch and from ADC is larger than expected: under investigation
  - SLAC-ESA beam test in August with CDF L00 sensors
  - *SiLC*: SiTR-130 just completed beam test using prototype modules with CMS sensors
- *KPiX*64-5 received and under test, *KPiX*64-6 submitted with several improvements

KPiX readout is the current SiD baseline:

Proving feasibility of bump-bonded readout is critical



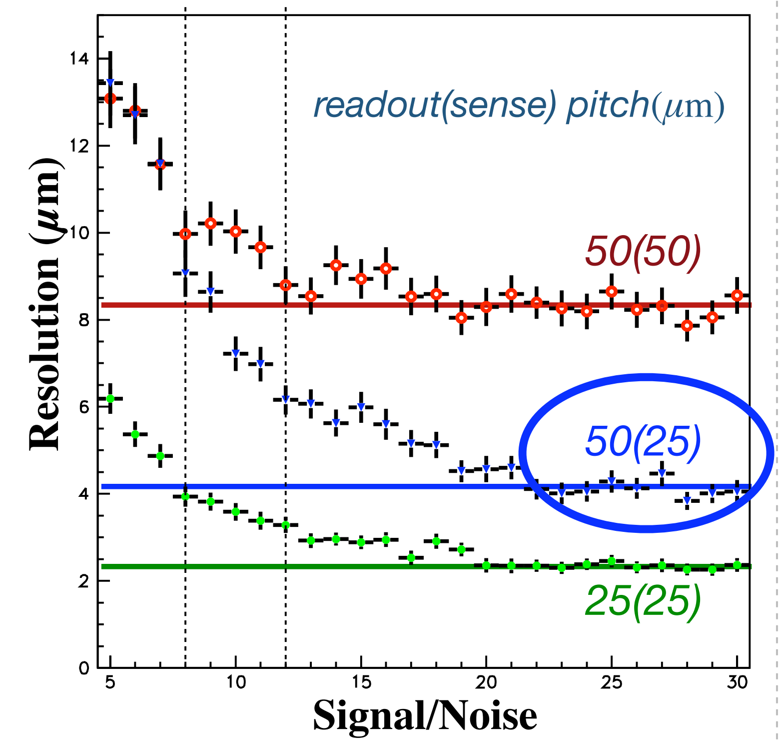


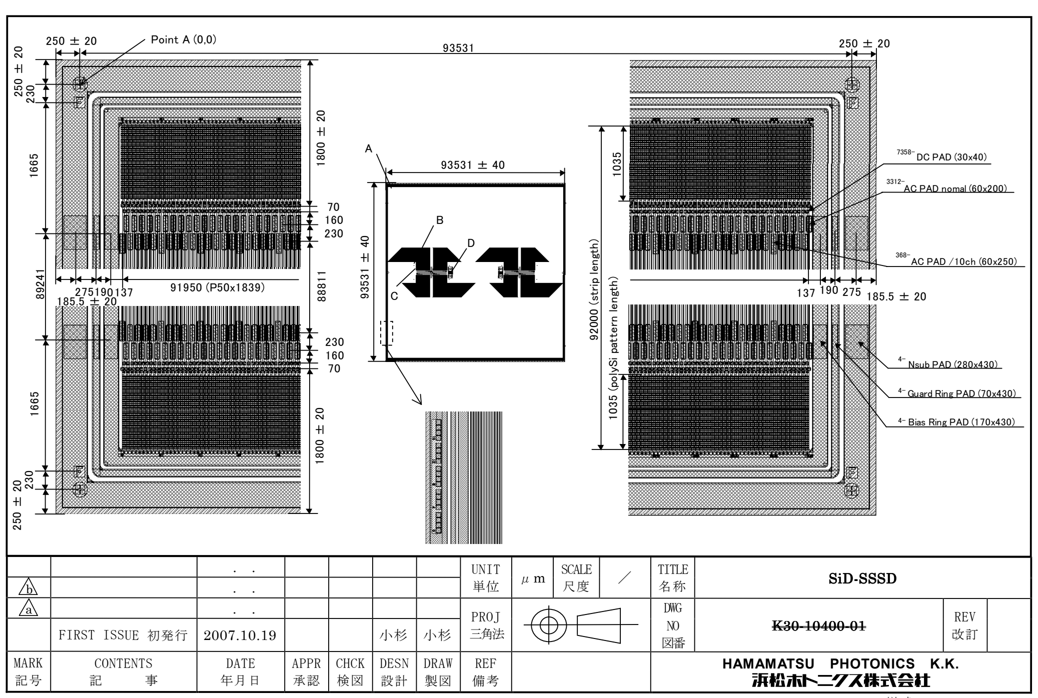
Barrel Sensors

FNAL, SLAC

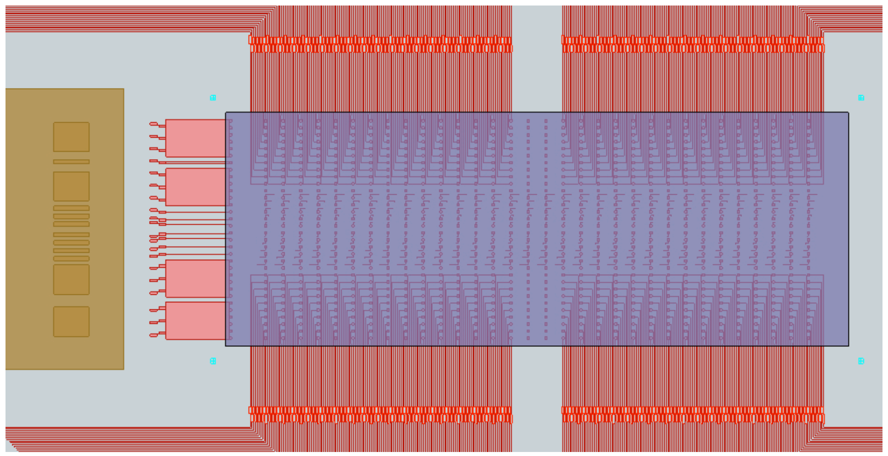
Double-metal prototype sensors submitted to HPK

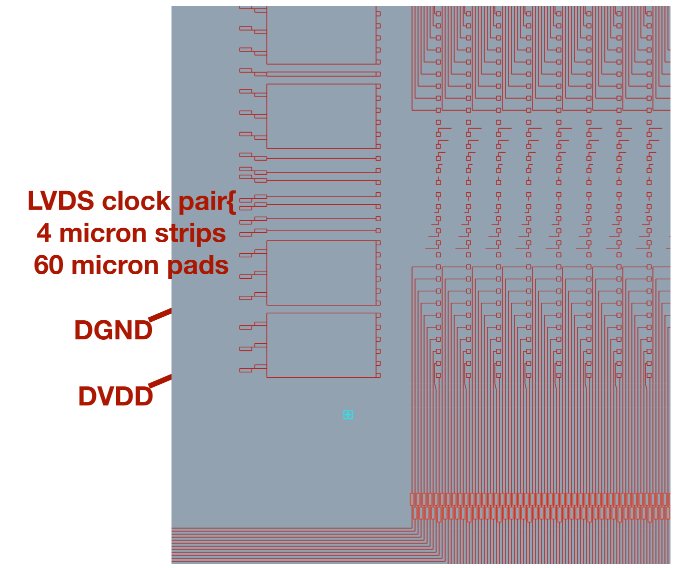
- Should achieve 5μm resolution for short modules
- Configured for both bump-bonding and wirebonding
- *Purdue* group is successfully thinning similar sensors: 200 μm silicon should not compromise resolution
- *SiLC:* HPK sensors w/ laser alignment windows, thinning





Q1 2008 delivery



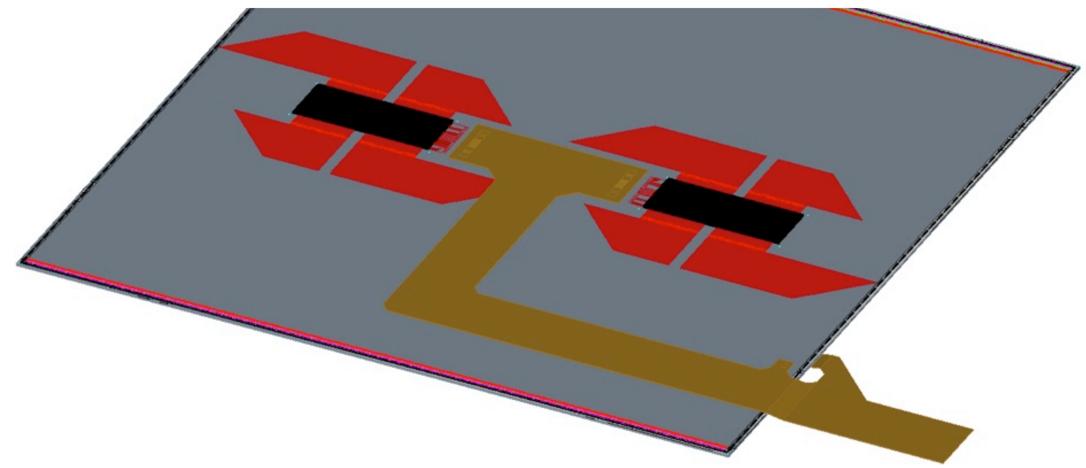


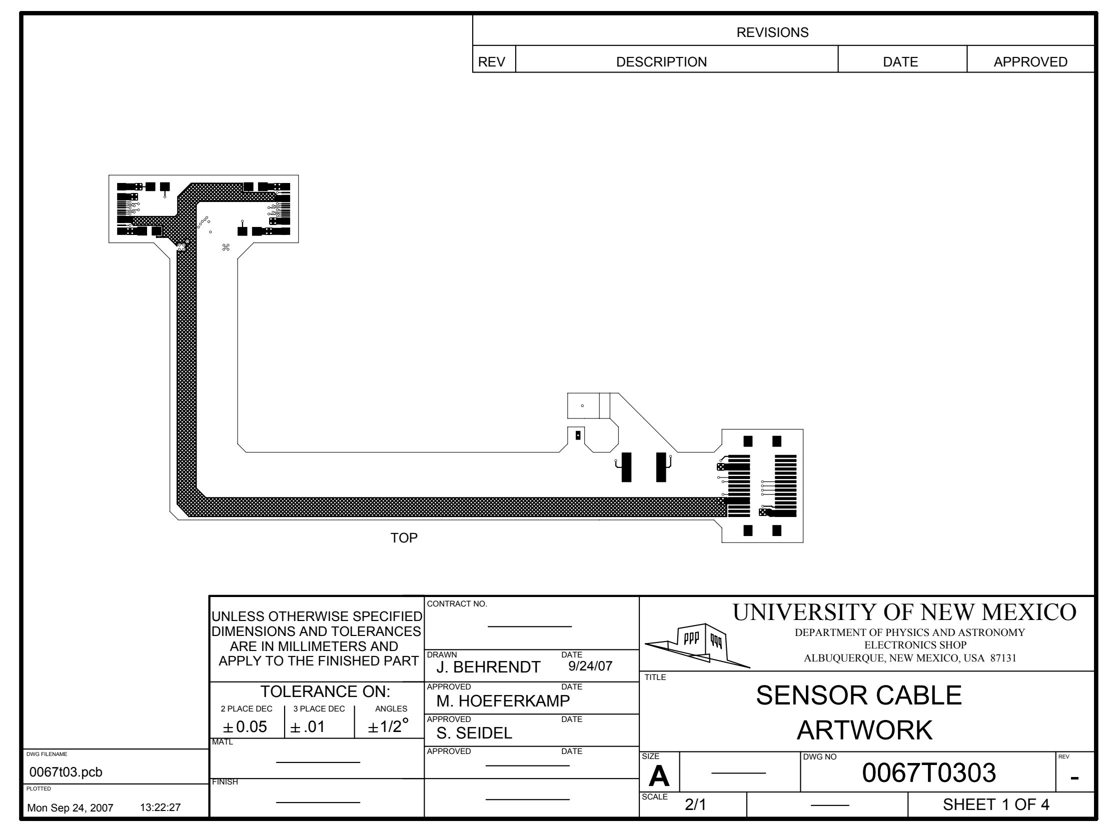
Pigtail Cable

UNM

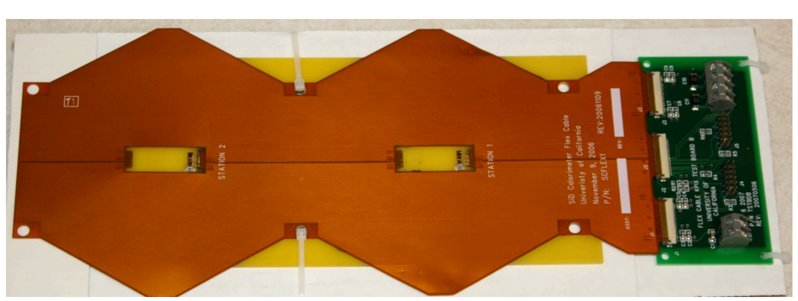
Design for pigtail prototype completed

- ¼-ounce copper on 50μm Kapton
  - 2 power+ground pairs <0.5Ω/trace
  - 8 narrow control/readout lines
  - HV pair for sensor bias
  - ➡ cable width 8mm
- ready for review, fabrication
- deliverable on same timescale as prototype sensors





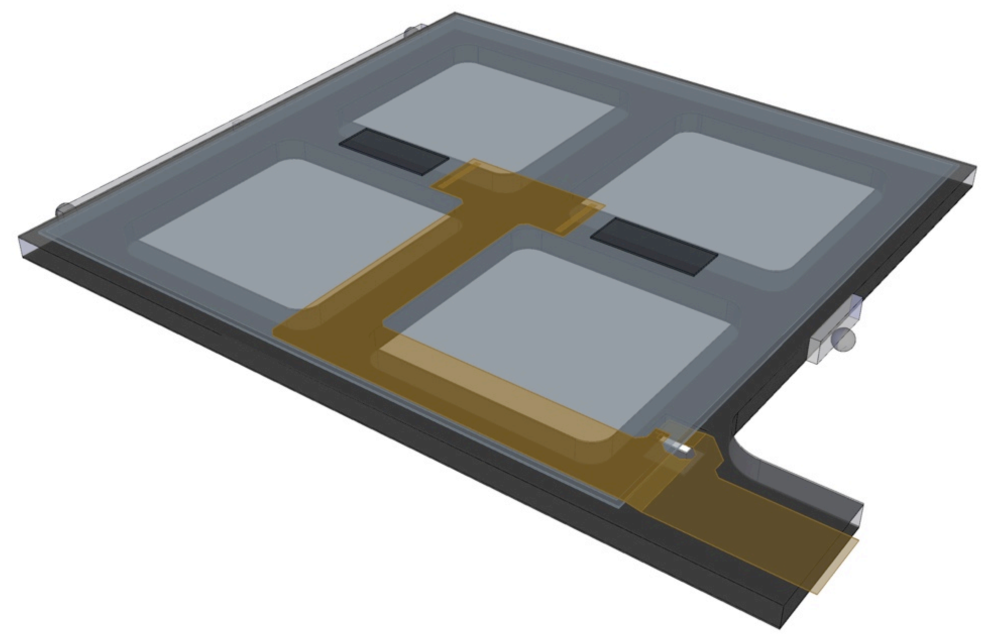
ECal *KPiX* cable (UC Davis)

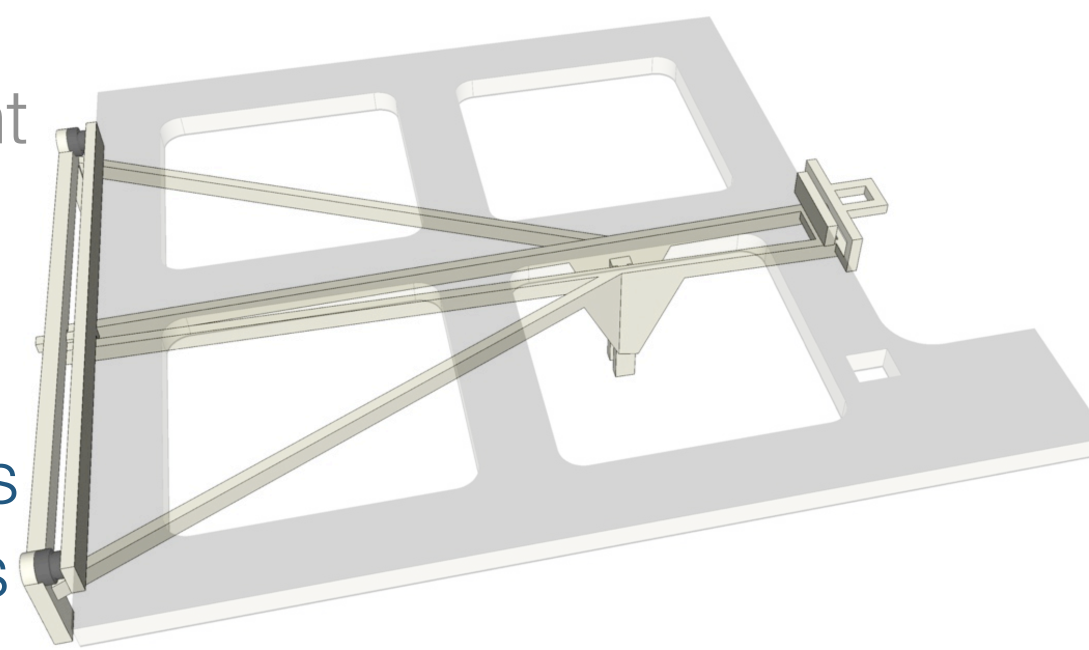


*S*i*D* Barrel Module Design

FNAL, SLAC

- Support frame is minimal: holds silicon flat and provides precision mount
  - CF-Rohacell-Torlon frame w/ ceramic mounts
  - CF-Torlon clips glue to large-scale supports
- Designed for mass-producibility, ease of assembly, handling, installation/replacement
- Can be made double-sided (stereo) with addition of same silicon on back side
- Submission soon for rapid prototyped parts to test concept, for first test beam modules



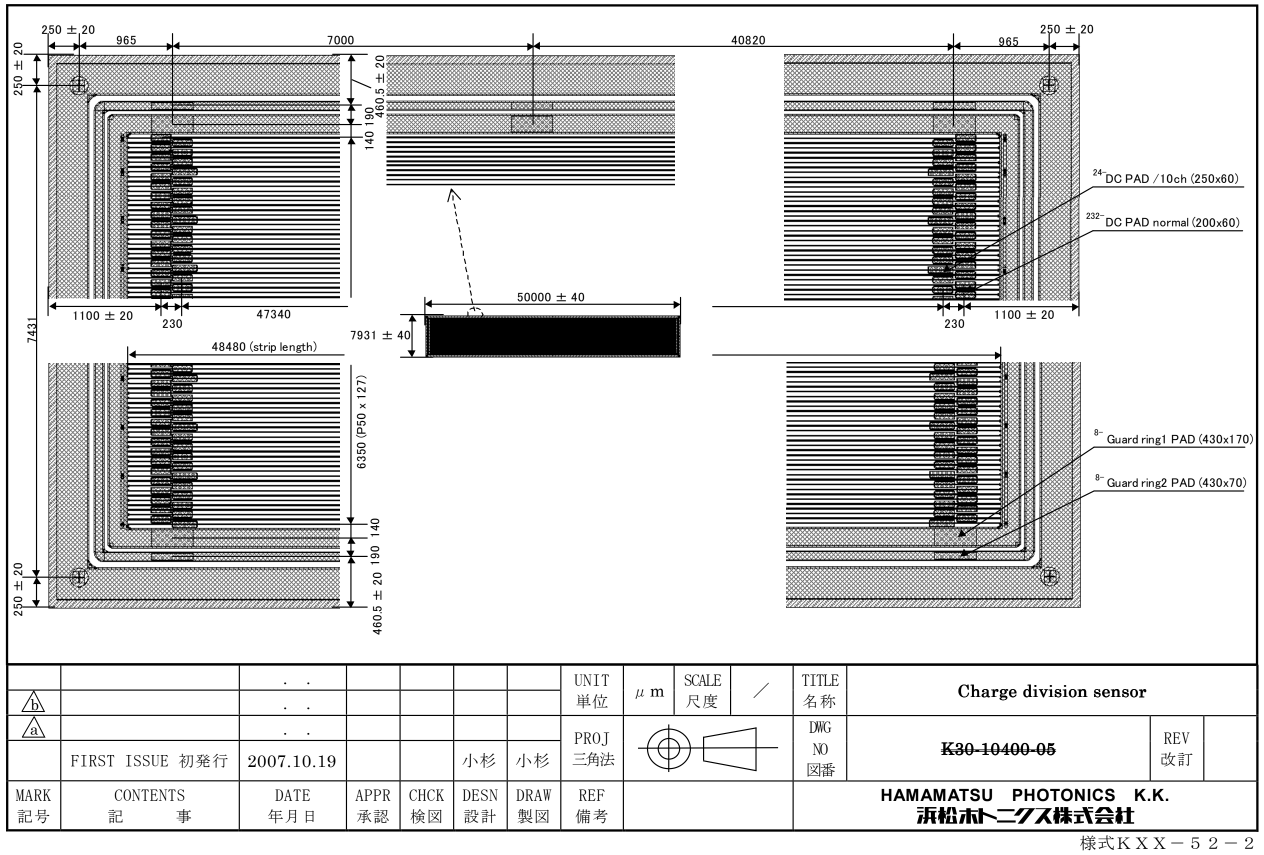


Charge Division Readout

Brown, SCIPP/UCSC

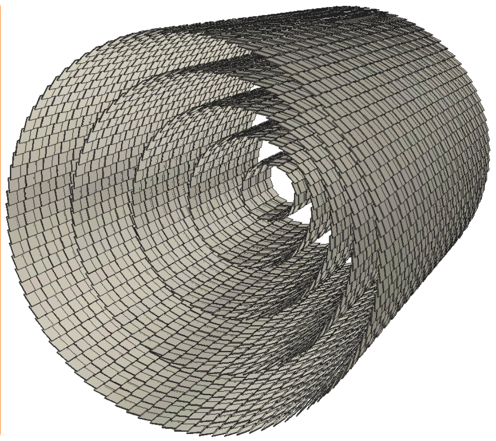
Obtain 3-d measurement by instrumenting both ends of strip

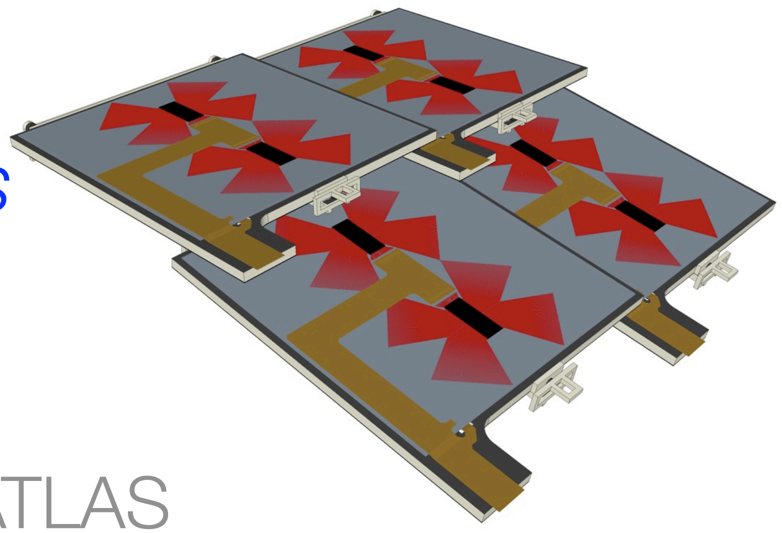
- Like double-sided modules, could be used forward, barrels if necessary
  - Single sensor: less material, cost
  - Somewhat less precision: theoretical limit is ~5mm
- Test sensor included with double-metal sensor submission
- Design of prototype readout chip to begin soon

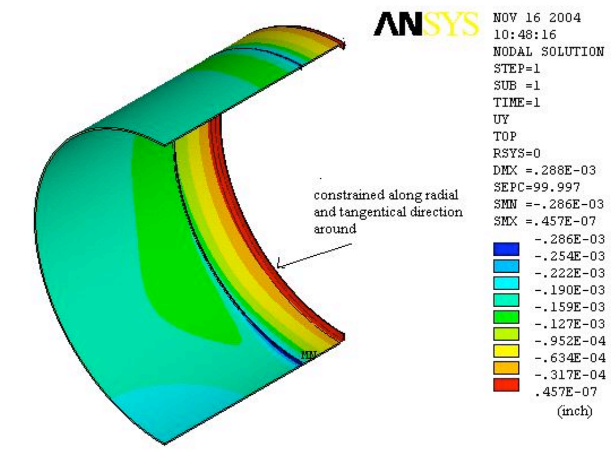


*Si*D Barrel Tracker Design

FNAL, SLAC



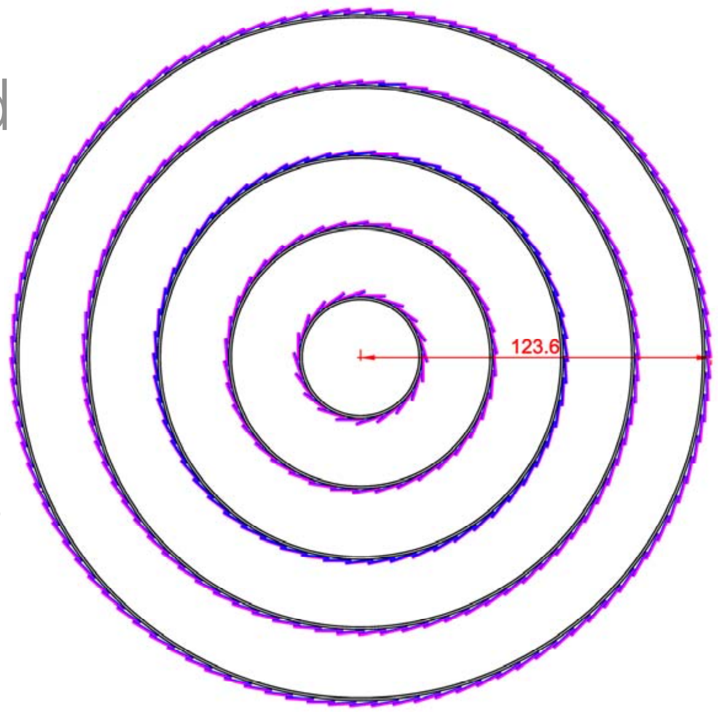




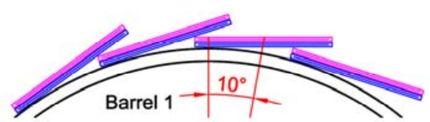
Vertical deflection with a 16mm x 7.5 mm carbon ring and 48 mm x 7.5 mm endring radial and tangencial direction has been constrained around the endring to simulate a very rigid endring.

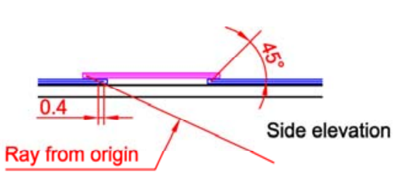
Modules tile CF-Rohacell cylinders

- Module tilt corrects for Lorentz drift
- Similar cylinders fabricated for D0, ATLAS
  - FEA results: 7um deflection fully loaded
  - 0.3% X_0 for solid cylinders: could be made up to 50% void
- More engineering and, ultimately, full scale prototypes will be required



Sensors:
Cut dim's: 9.35 cm x 9.35 cm
Active dim's: 9.20 cm x 9.20 cm
Modules:
Outer dim's: 9.65 cm x 9.65 cm x 0.3 cm
Support cylinders:
OR: 21.5, 46.5, 71.5, 96.5, 121.5 cm
Number of phis: 20, 38, 58, 80, 102
Tilt angles: 6.6 to 10 degrees
Radii normal to silicon (mm):
Barrel 1: 2.175, 2.215 cm
Barrel 2: 4.675, 4.715 cm
Barrel 3: 7.175, 7.215 cm
Barrel 4: 9.675, 9.715 cm
Barrel 5: 12.175, 12.215 cm
Blue and magenta sensors are at different Z's to provide longitudinal overlap.
Within a given barrel, cyan sensors overlap in phi, as do magenta sensors.



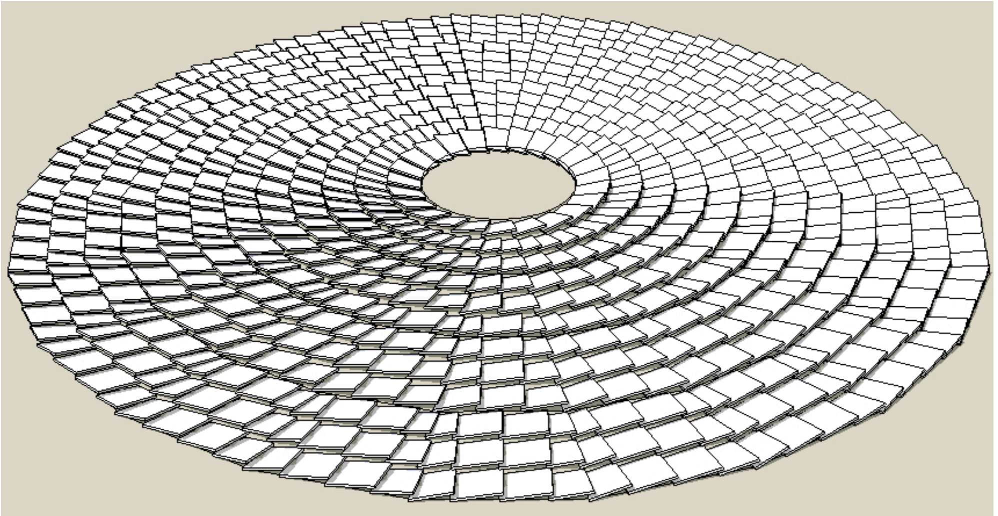


S*i*D Forward Tracker Design

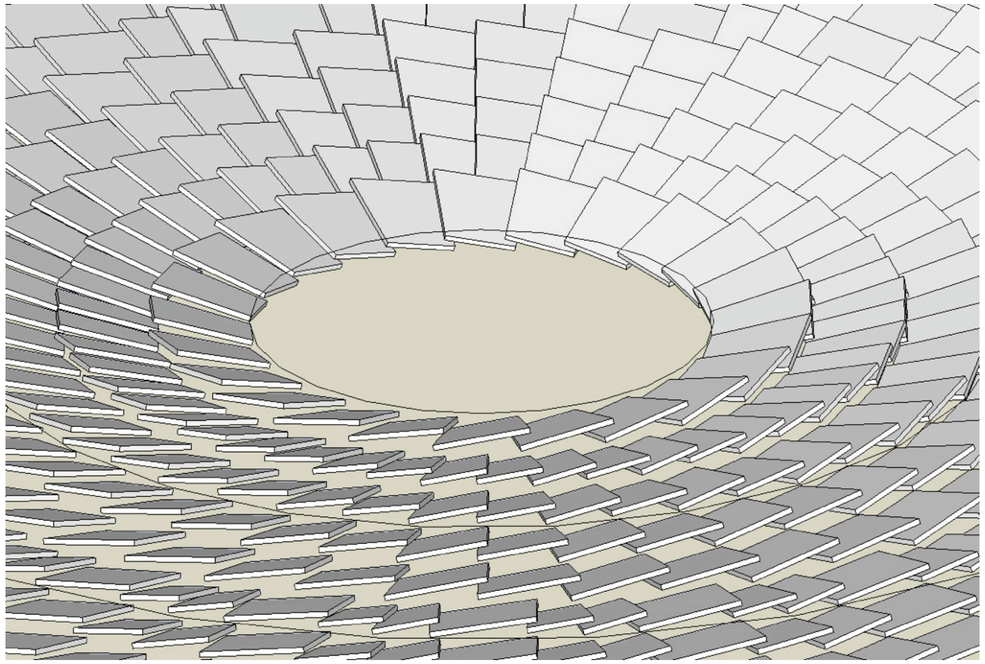
SLAC

Barrel cylinders closed by forward disks

- Straw man mechanical layout for wedges : squares, hexagons also being considered
- Issues demanding module R&D largely independent of shape
    - Short module accommodates many choices: designed with double-sided modules in mind
    - Long-module mechanics may exclude some tiling options



10 sensor designs

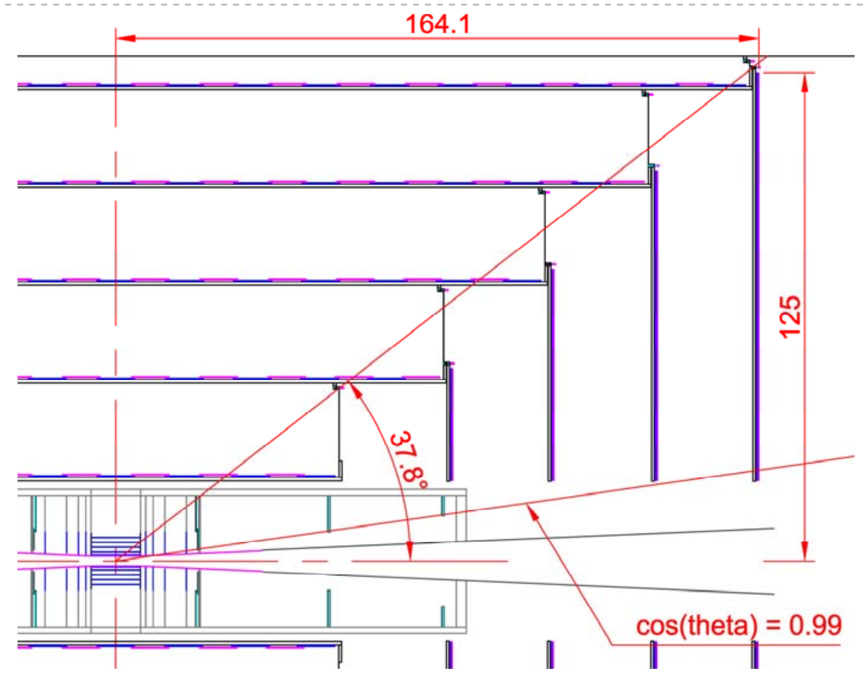


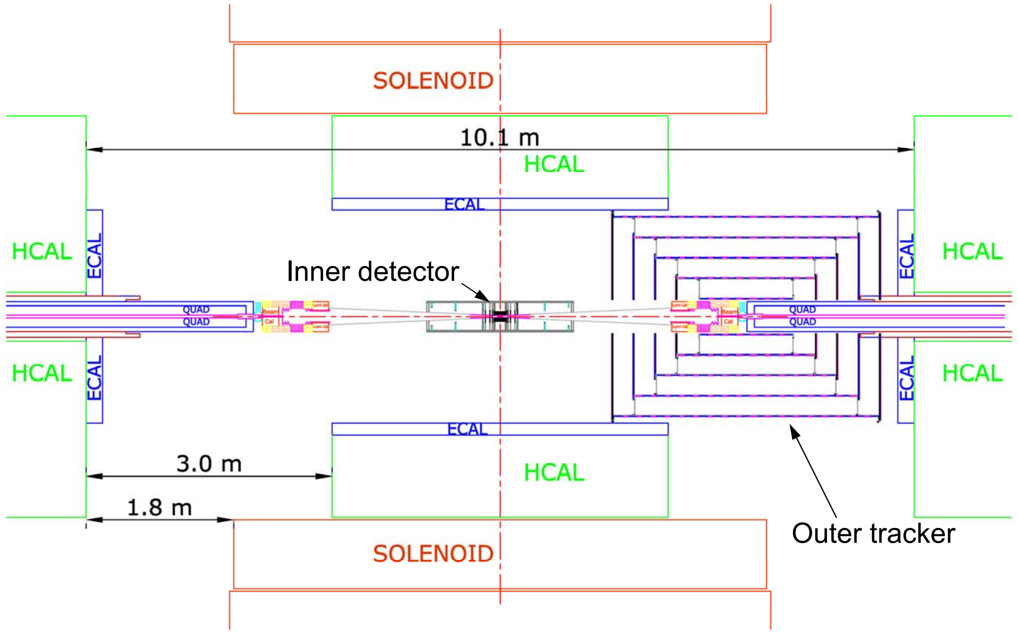
SiD Tracker Design

FNAL, SLAC

Nested cylinders supported by annular rings

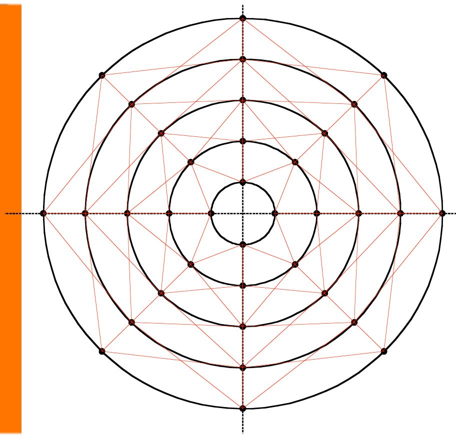
- Inner portion of disks supported with VTX to allow servicing
- Support rings also host power distribution and data concentrators:
  existing optical transceivers can easily meet our requirements
- DC/DC conversion or serial powering assumed to reduce cable plant
  - Peak current for tracker is 5000 amps
  - Lorentz forces could be problematic



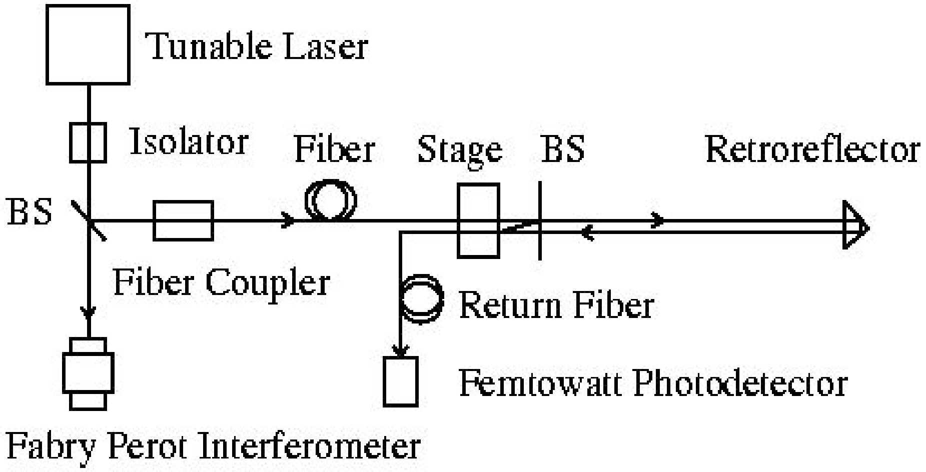


Dual Laser FSI

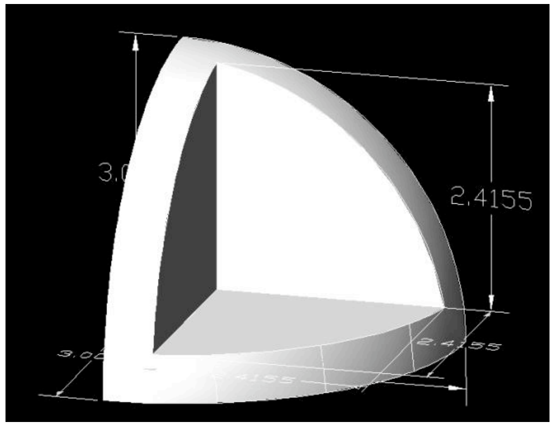
U. Michigan

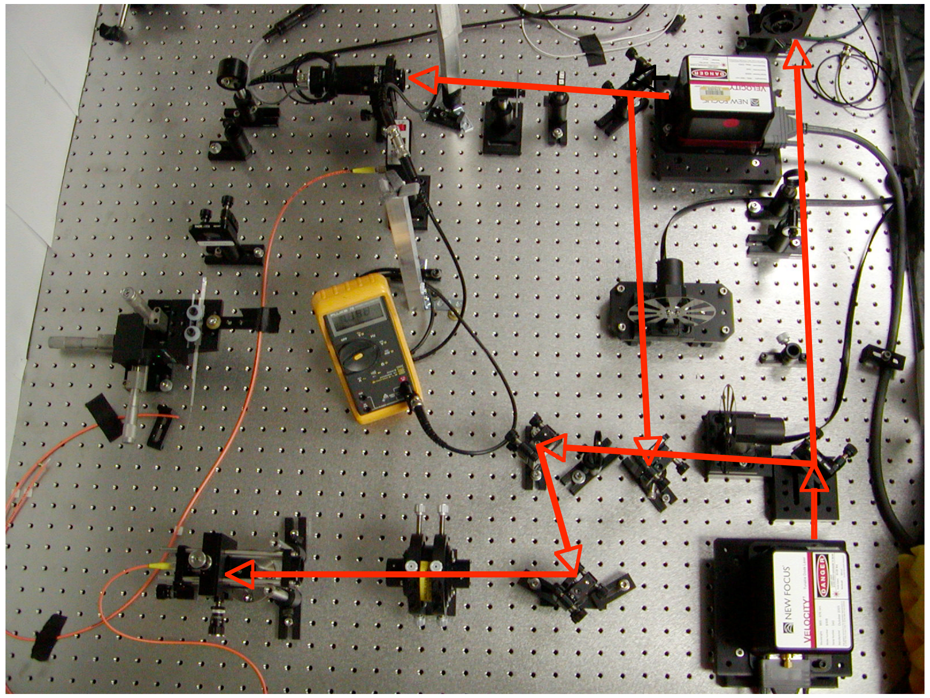


Aggressive material trimming, pulsed-power and push-pull may create need for alignment monitoring



- Absolute distances measured to ~200nm in real-world conditions with commercial optics
- Working on miniaturization: initial testing achieved 70nm precision with corner cube array
- Simulations of resolution degradation due to tracker distortions underway

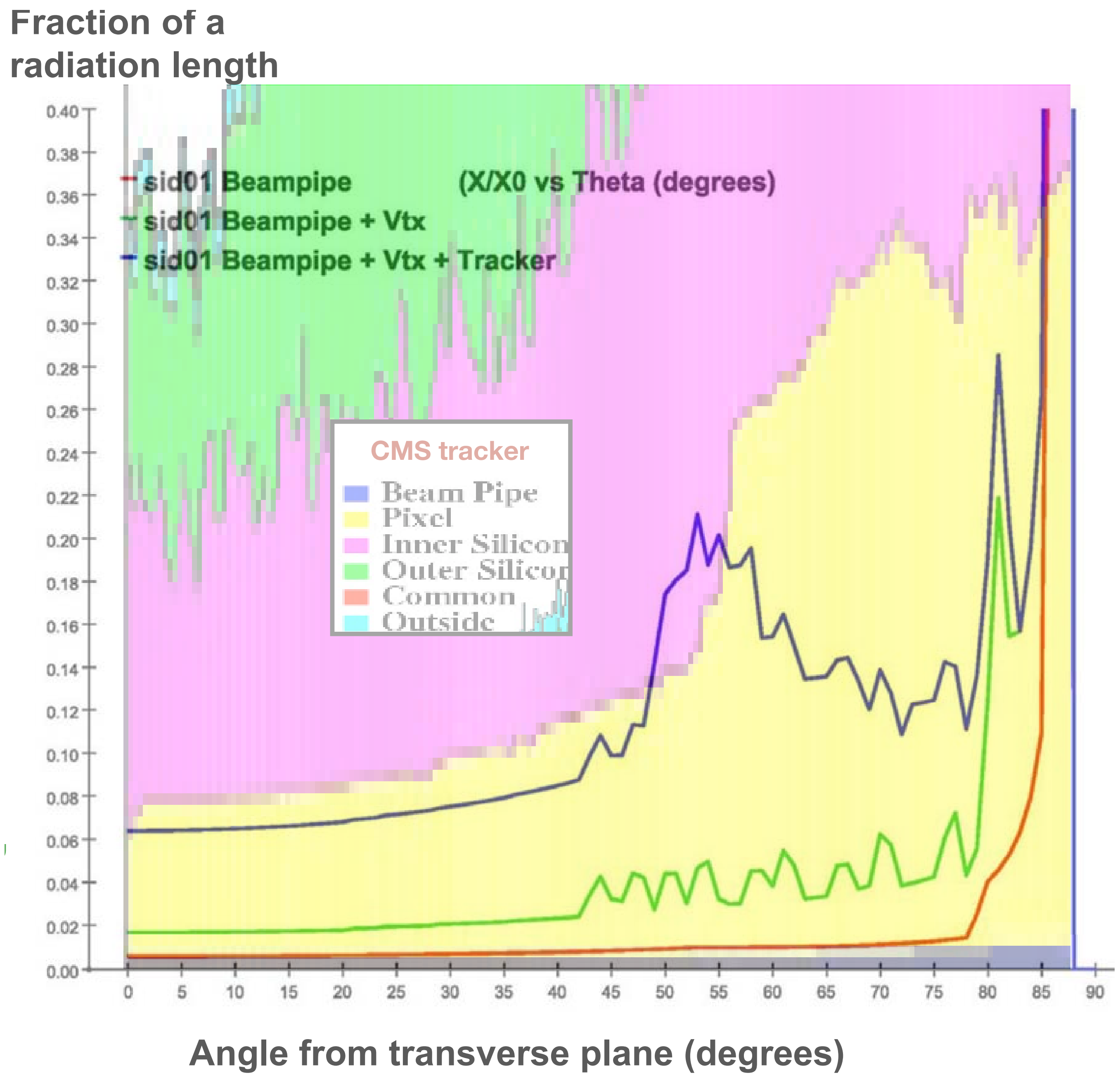




SiD Material Estimates

Scrupulous attempt to account for material

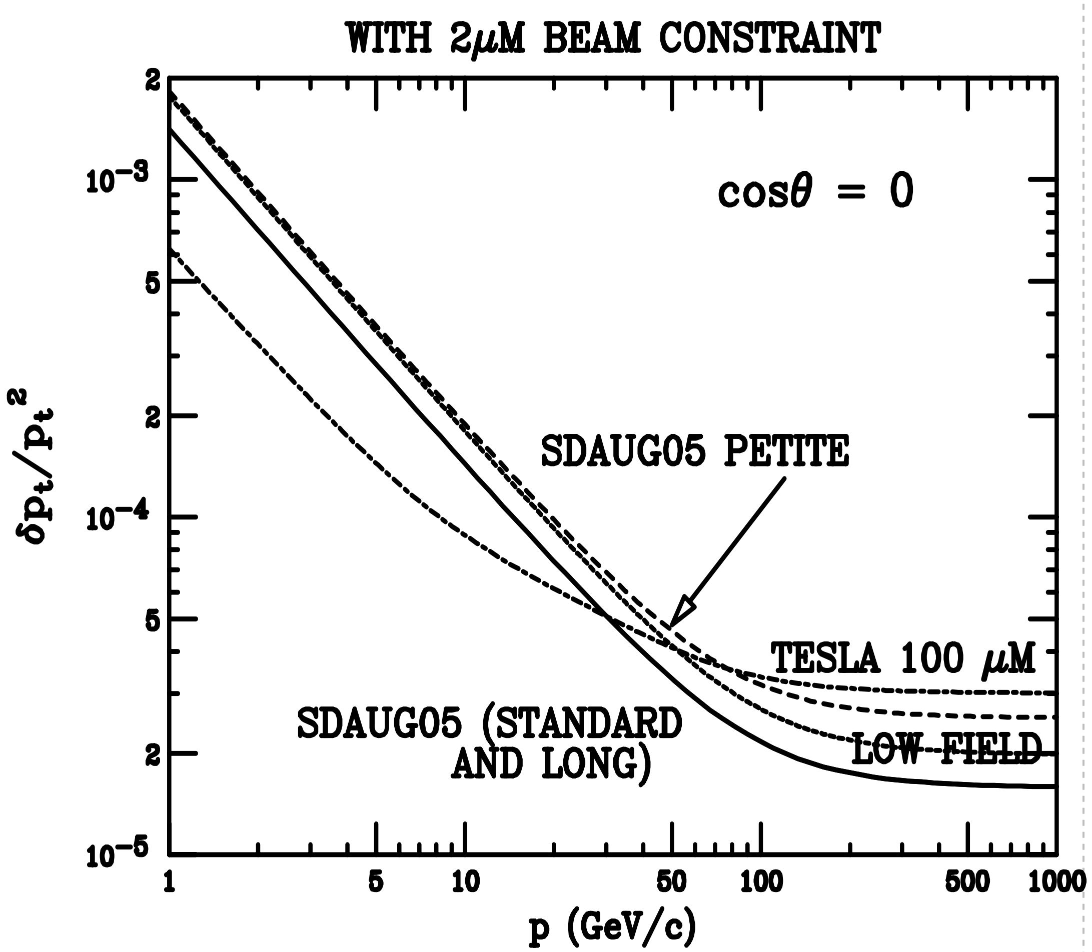
- Included in GEANT: sensors, chips, cables, connectors, bypassing, glue, module supports, module mounts, overlaps, power distribution boards, DAQ for baseline design
- Not included: alignment monitoring, mounting to ECAL, voids in large scale support structures
- Goal 0.8%/layer, currently 0.92%/layer



Momentum Resolution

- Material and single-hit resolutions used to create parameterized model for org.lcsim FastMC
- This model used for physics studies and to benchmark track fitters for full Monte Carlo
- Significant new efforts in hit modeling and track fitting will improve level of reality for LOI studies
- How good does resolution need to be, especially for low-momentum tracks?
  - Where are diminishing returns at high p_T?
  - Do we care whether 10 GeV tracks are measured to ±9 MeV instead of ±15 MeV?
  - 1 GeV tracks to ±0.6 MeV instead of ±1.5 MeV?

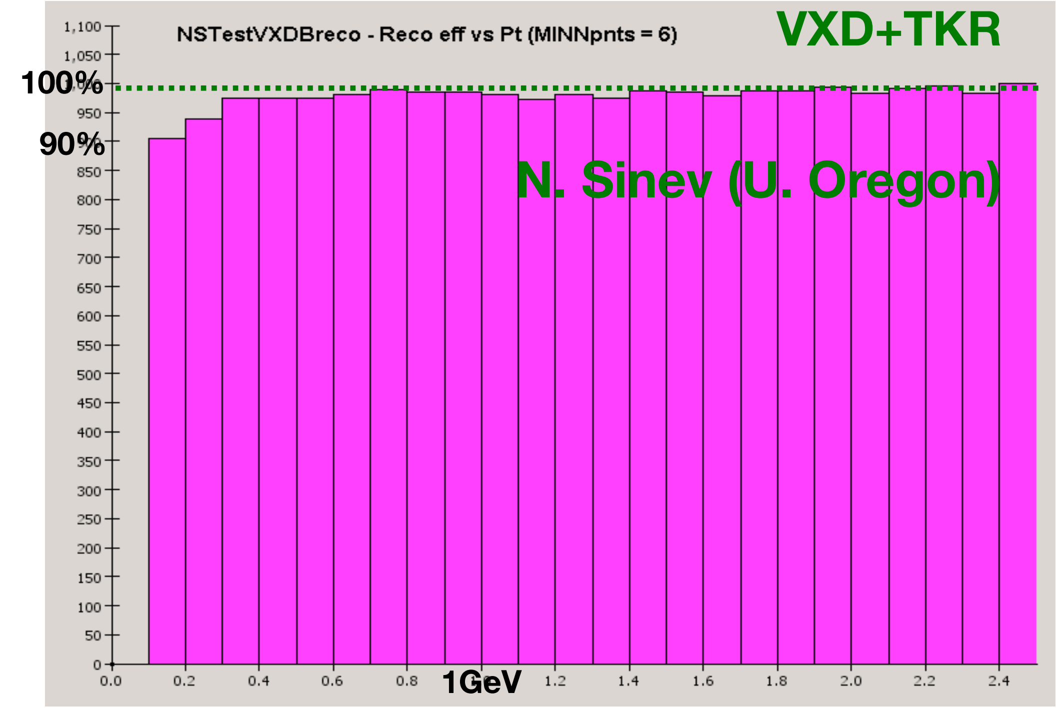
LCDTRK - B. Schumm (UCSC)

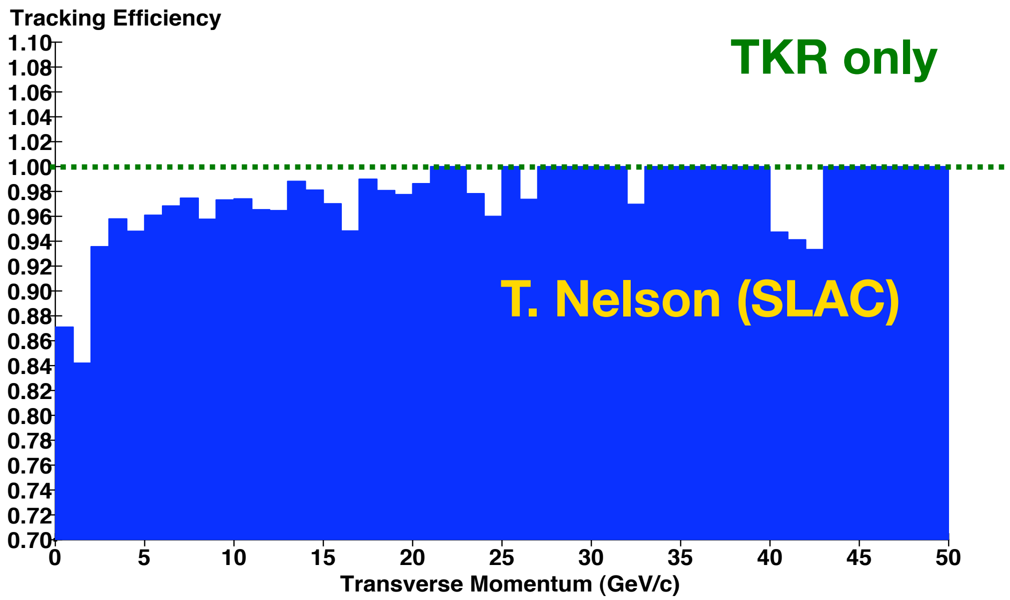


Tracking Efficiency

Realistic simulations, well-developed algorithms required for realistic estimates of efficiency

- A major push underway to fill this need, but some things we already know:
  - Efficiency and purity for prompt tracks is good even in absence of VXD
  - Performance for prompt tracks extends to the forward region if no ghost hits: the relevant case in the small module limit
  - *P_T* < 200 MeV (VTX-only) difficult in presence of full backgrounds
- Is there physics that demands highly efficient tracking below 200 MeV?





Non-prompt Tracks

- The vertex detector is important for pattern recognition in SiD concept: *How well can SiD reconstruct non-prompt tracks?*
- How important are non-prompt tracks for vertex reconstruction and PFA performance?
- Is there physics that demands reconstruction of non-prompt tracks for successful detection?

$Z \rightarrow qq$ at the Z pole

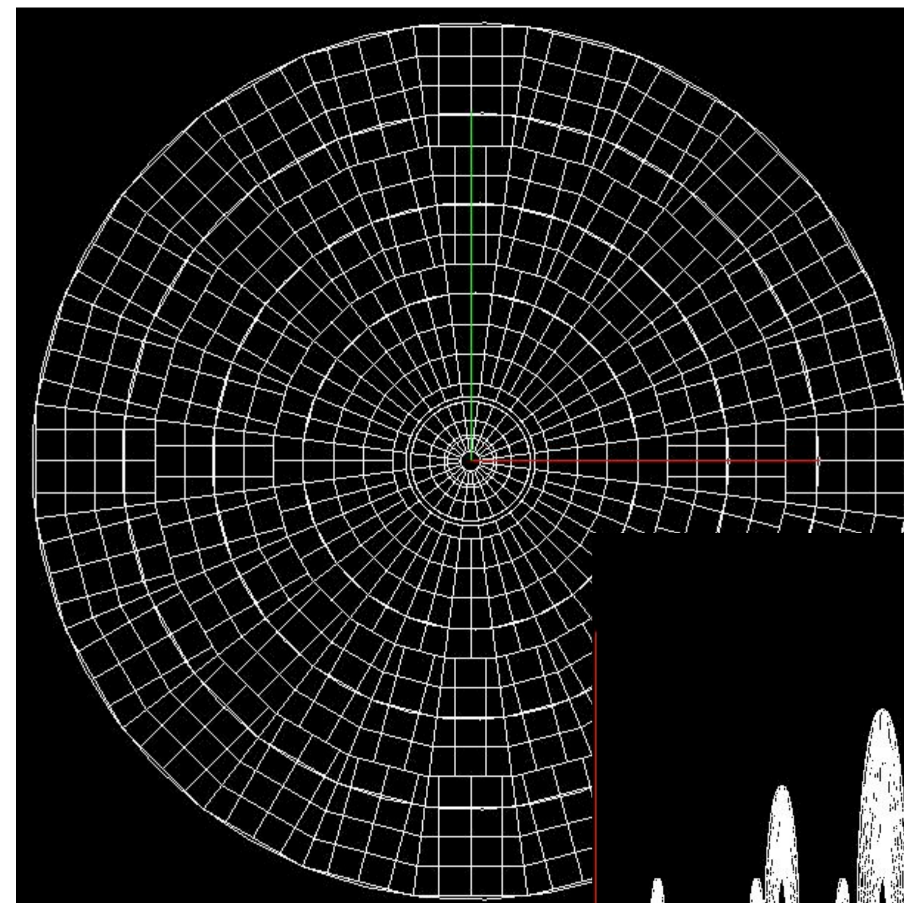
Meyer, Rice, Schumm, Stevens (UCSC)

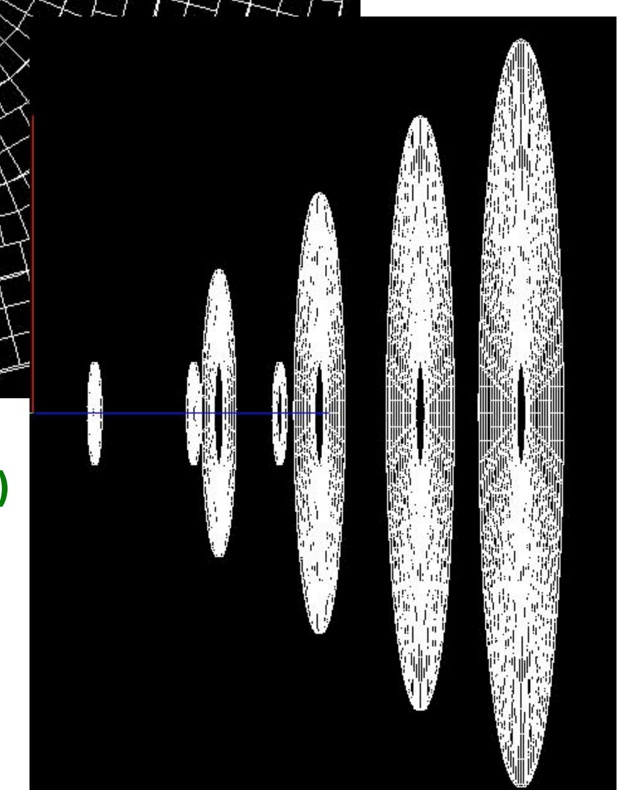
Radius of origin	Fraction of MC Particles	eff (purity) TKR Only	eff (purity) TKR+CAL
$R_{CAL} > r > R_{VTX}$	0.05	81% (90%)	83% (90%) or 73% (100%)
$R_{L1} > r > R_{VTX}$	0.032	94% (100%)	94% (100%) or 84%(100%)
$R_{L2} > r > R_{L1}$	0.012	86% (70%)	93% (71%) or 80%(100%)
$R_{L3} > r > R_{L2}$	0.007	---	70% (78%)
$r > R_{L3}$	0.0026	---	---

- **Event Thrust > 0.94**
- **P_T > 750 MeV**
- **Path length > 500 mm**
- **Barrel only**

Forward Tracking

- Tools for full simulation of forward strips with ghosts near completion
  - Silicon simulation, digitization and clustering
  - Representation of 2d silicon hits in segmented tracker
- Complete wedge design for forward tracking in simulation
- Beyond efficiency for multi-particle final states, is there physics that is only accessible in forward region?



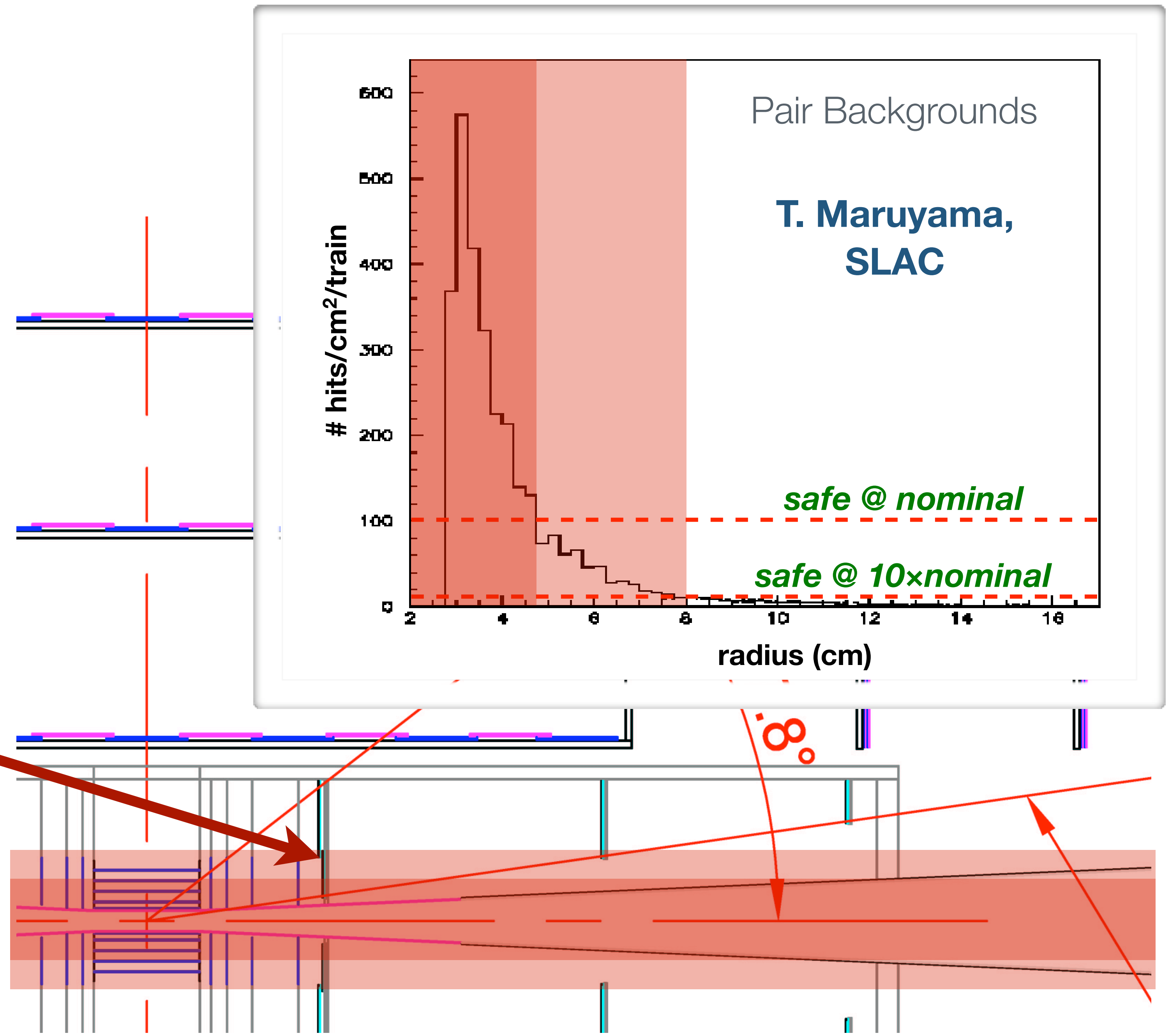


J. McCormick, T. Nelson (SLAC)

Endcap: 10 sensor designs
Forward: 4 sensor designs

Background Occupancy

- Occupancies at smallest radii are quite large
- Pair background dominate for silicon tracking
  - photon conversions ~10%
  - others are negligible
- One small forward piece problematic for 4-buffer *KPiX*
- Simplest solution is to turn this into another pixel vertex disk



Summary: Towards an LOI

- *Hardware:*
  - Develop concept for lightweight silicon tracker that passes “laugh test”
  - Demonstrate that proposed technical approaches meet our requirements
- *Simulation:*
  - Demonstrate that concept is light enough
  - Demonstrate that concept provides efficient tracking (w/ VXD, CAL)
  - Demonstrate that concept performs well in forward region

We are making good progress along this path, but there is much left to do.

We need input to help us understand the physics requirements: come to tomorrow’s signature session and help us define them!