High Availability Electronics R&D Program FY06-07

DOE/NSF ILC Americas Program Review
FNAL April 4-6 2006

Ray Larsen SLAC
For Controls, Instrumentation & Power Systems Collaborators

HA Electronics Topics

- 2.2.2 Control System Design
- 3.2.1 Power Supply Systems w/ ATF
- 3.2.2 Damping Ring Kicker w/ ATF
- 3.2.3 Diagnostic Processor for Power Systems
- 3.2.4 Controls & Instrumentation Standards
- 3.2.5 Universal Accelerator Parser*
- 3.2.6 Radiation Hard 500 MHz Digitizer**
- 3.2.7 Radiation Damage Studies Electronics**

*LBNL-Cornell Collab. ** University based Programs

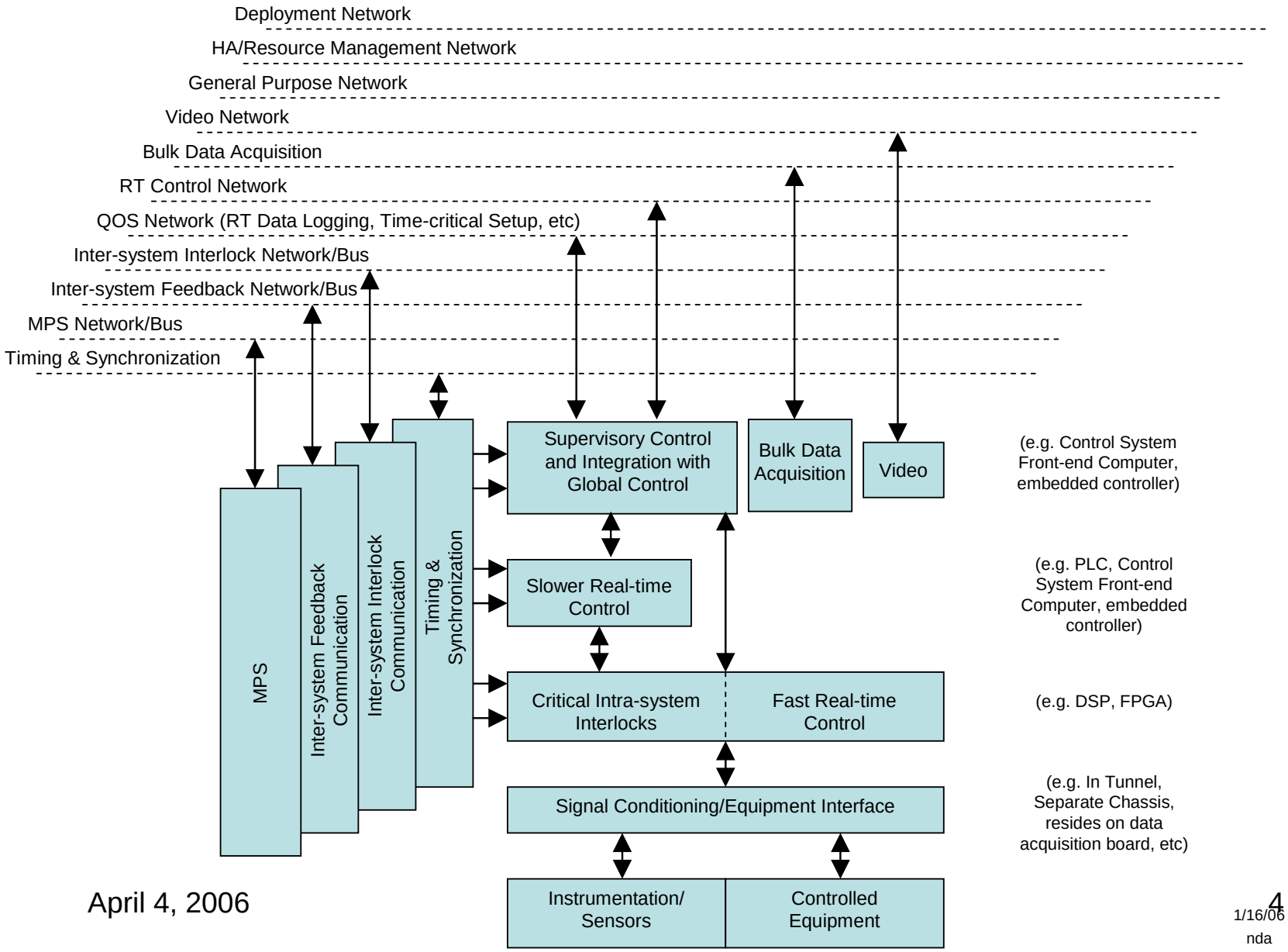
2.2.2 Control System Design

[Argonne, SLAC, FNAL, LBNL, DESY, KEK, Universities]

- Description
  - Evaluate High Availability designs for central computing, remote nodes, multi-gigabit serial communication systems based on dual redundant star configurations
  - Develop hardware, software models for top level, intermediate (sector) nodes and front-end applications
- Motivation
  - Controls BCD calls for High Availability design of hardware, software, networks, timing, RF reference, LLRF system for ILC to meet uptime goals.

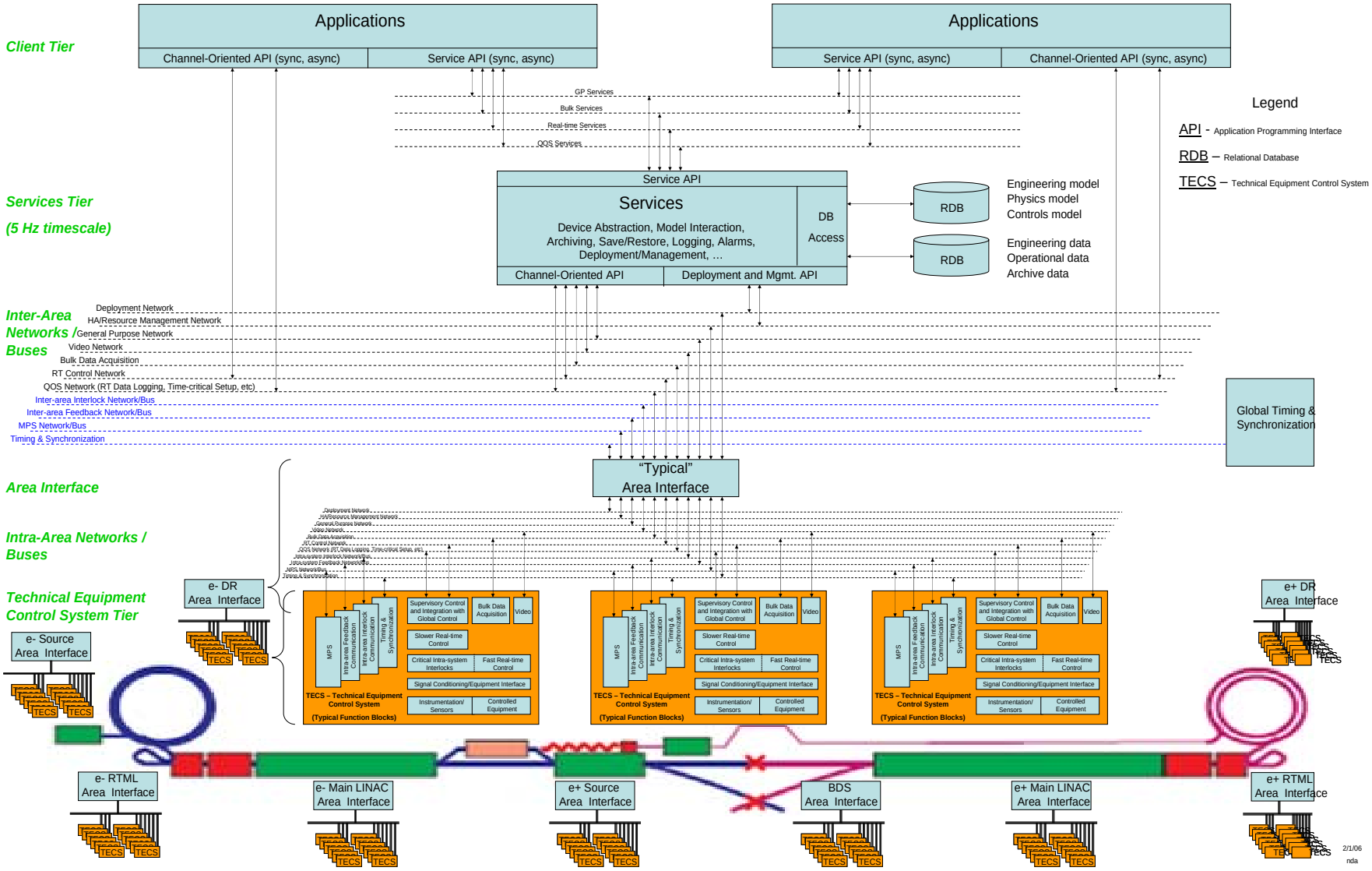
Controls Functional BD

Typical Function Blocks of a Technical Equipment Control System

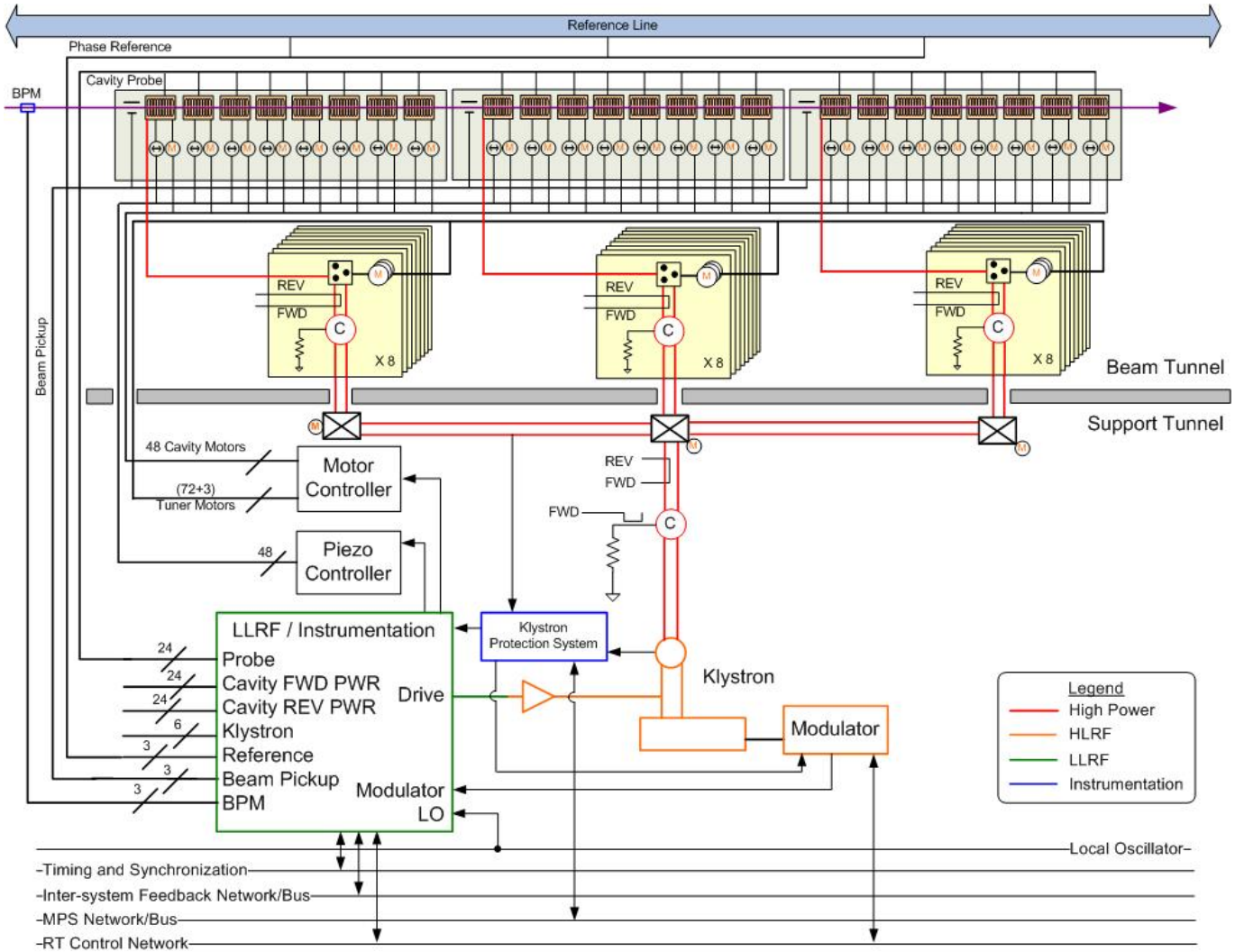


Controls Integrated System BD

ILC Integrated Control System (Functional View)



LLRF System BD



2.2.2 Progress in FY06

- Strong C&I collaboration established
- Controls lead at Argonne, LLRF lead at DESY & FNAL, Instrumentation lead at SLAC
  - Architectures studied versus block models of control system, LLRF, BPM, timing & RF reference applications
  - ATCA is platform for HA cost model; ATCA kits, memberships in PICMG (Standards Org.) purchased
  - Multi-tier software architecture development led by ANL
  - Planning in progress for cost modeling, estimates for RDR
  - Weekly Webex meetings with participation by ANL, FNAL, SLAC, DESY, KEK, Universities
- FY06 Budget
  - 0.8 FTE, 132K$, funds available.

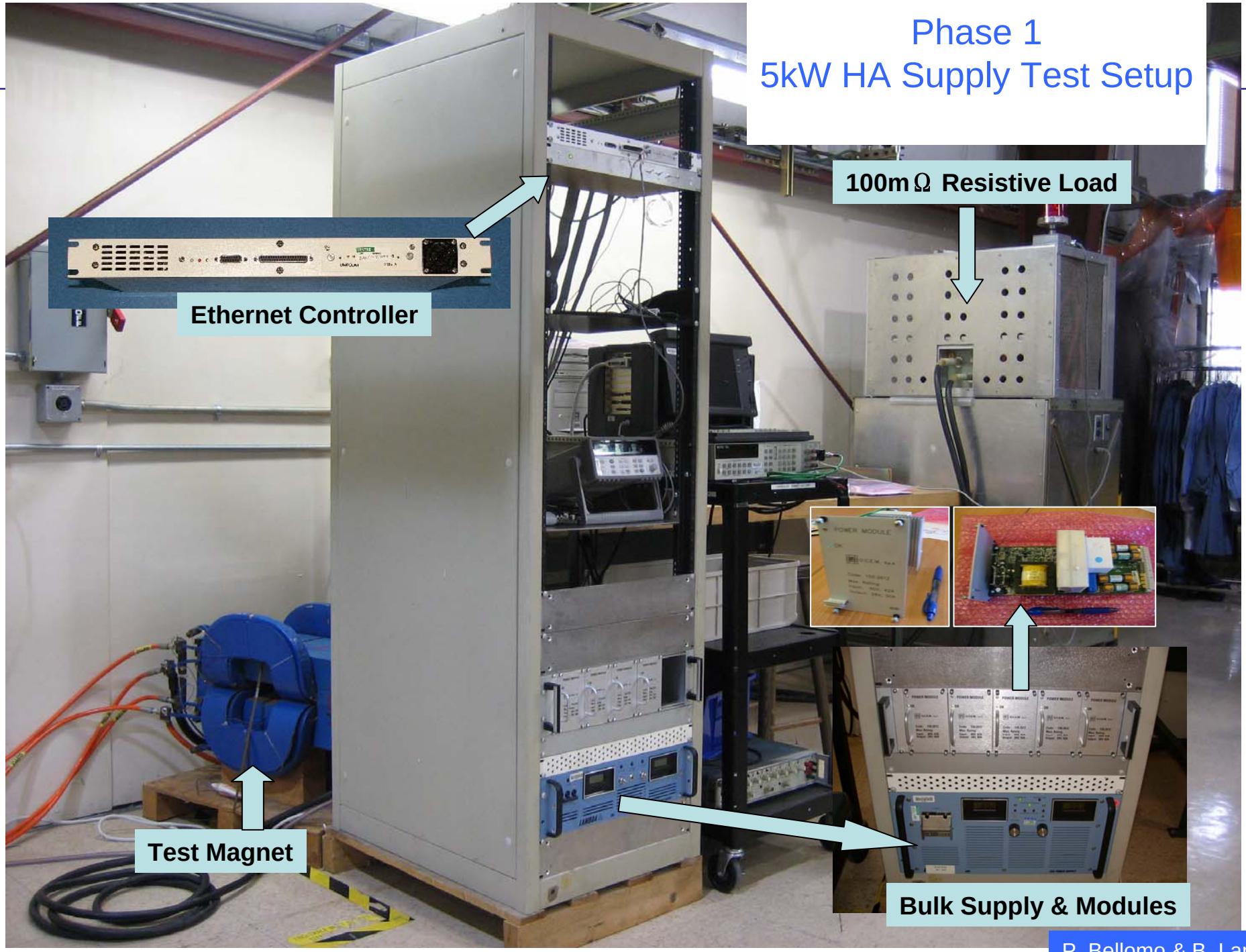
2.2.2 Summary Plan

			FY06			FY07				FY08				FY09		
			Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3
	3.1	*Controls Prototyping*														
	ANL Lead	Procure OS, test soft		•	•											
	ANL Lead	Procure ATCA mods t		•	•											
	ANL Lead	Install dual star network 2.4 GHz			•	•										
	ANL Lead	Demonstrate Shelf Manager, hot swap				•	•									
	ANL Lead	Demonstrate node performance w/ simulated data					•	•								
	ANL Lead	Develop Timing network				•	•	•	•							
	ANL Lead	Demonstrate timing protoype performance							•	•	•					
	ANL Lead	Develop RF Ref prototype				•	•	•	•							
	ANL Lead	Prototype computer farm nodes, demonstrate								•	•	•	•	•	•	•
	ANL Lead	Demonstrate RF Ref performance							•	•	•					
	3.2	*Controls Software Collaboration*														
	ANL Lead	Develop Test Platform for Hardware devmt				•	•	•	•							
	ANL Lead	Procure licenses, develop RT test software				•	•	•	•							
	w/ANL	Support Controls, Instrument developers				•	•	•	•							
	w/ANL	Deliver test platforms							•	•						
	w/FNAL/DE	Develop drivers for LLRF, BPM protos							•	•	•					
	w/Collab	Collaborate with high level arch. Design					•	•	•	•	•	•	•	•	•	•
		FY07 HA Controls Totals														

3.2.1 HA ATF2 Modular Power Supply System [SLAC, KEK]

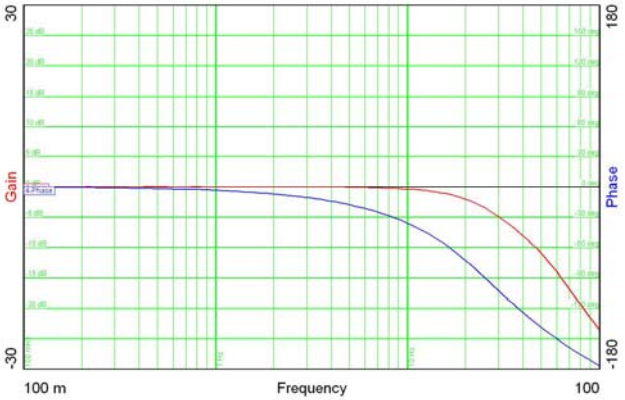
- Program
  - Phase 1 (FY06) – Demonstration Prototype
    - 4/5 prototype capable of A>0.99 for ILC, hot swap w/ATF
  - Phase 2 (FY06-07) - 40 Magnet System for ATF2
    - SLAC provides engineering, coordination, test
    - Parallel R&D on Redundant Bulk, Controller w/ failover
  - Phase 3 (FY08) – Installation & Training for ATF2
    - SLAC supports KEK installation, documentation, training
- Motivation
  - Non-HA Power Supplies chief source of downtime
  - Demonstration of technical, cost viability of HA design vital to achieving ILC up-time goals.

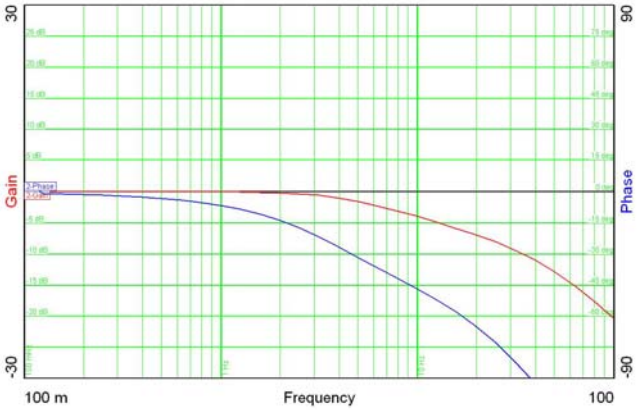
Phase 1
5kW HA Supply Test Setup



P. Bellomo & B. Lam

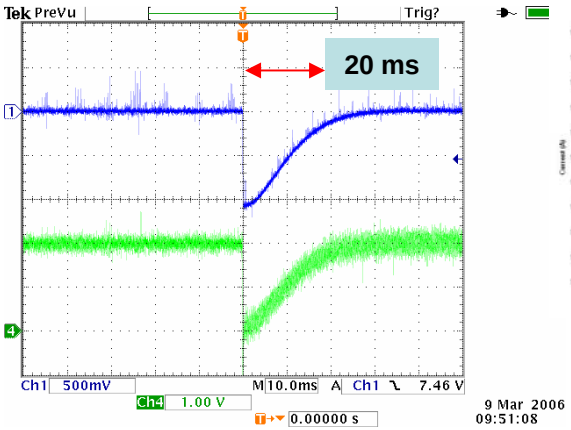
Frequency Response

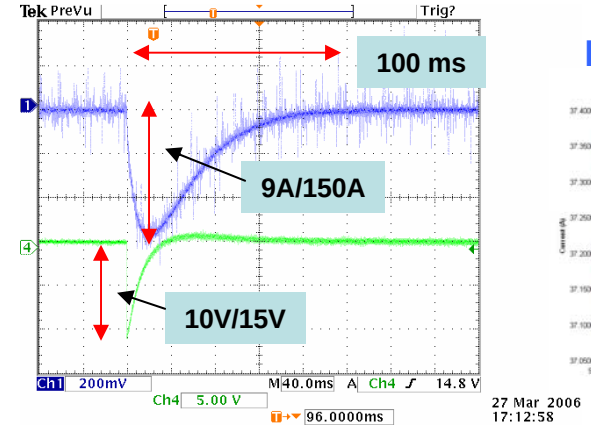




Top: Resistive Load, A, Φ
Bottom: Magnet Load + 100mΩ, A, Φ

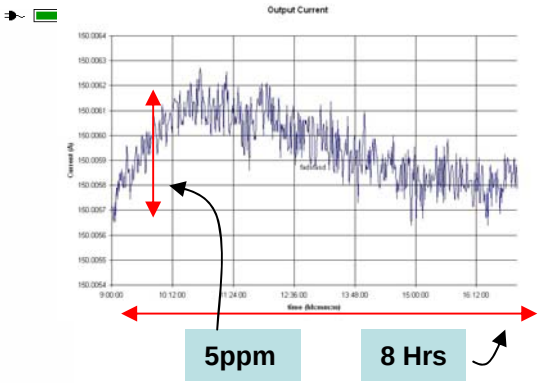
Transient Recovery
1 Module Switched Off



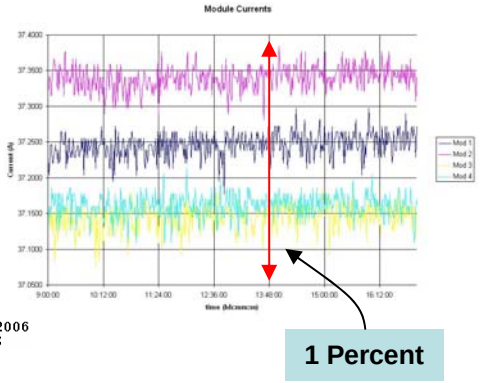


Top: Resistive Load, 10 ms/cm
Bottom: Magnet Load +100mΩ, 40 ms/cm

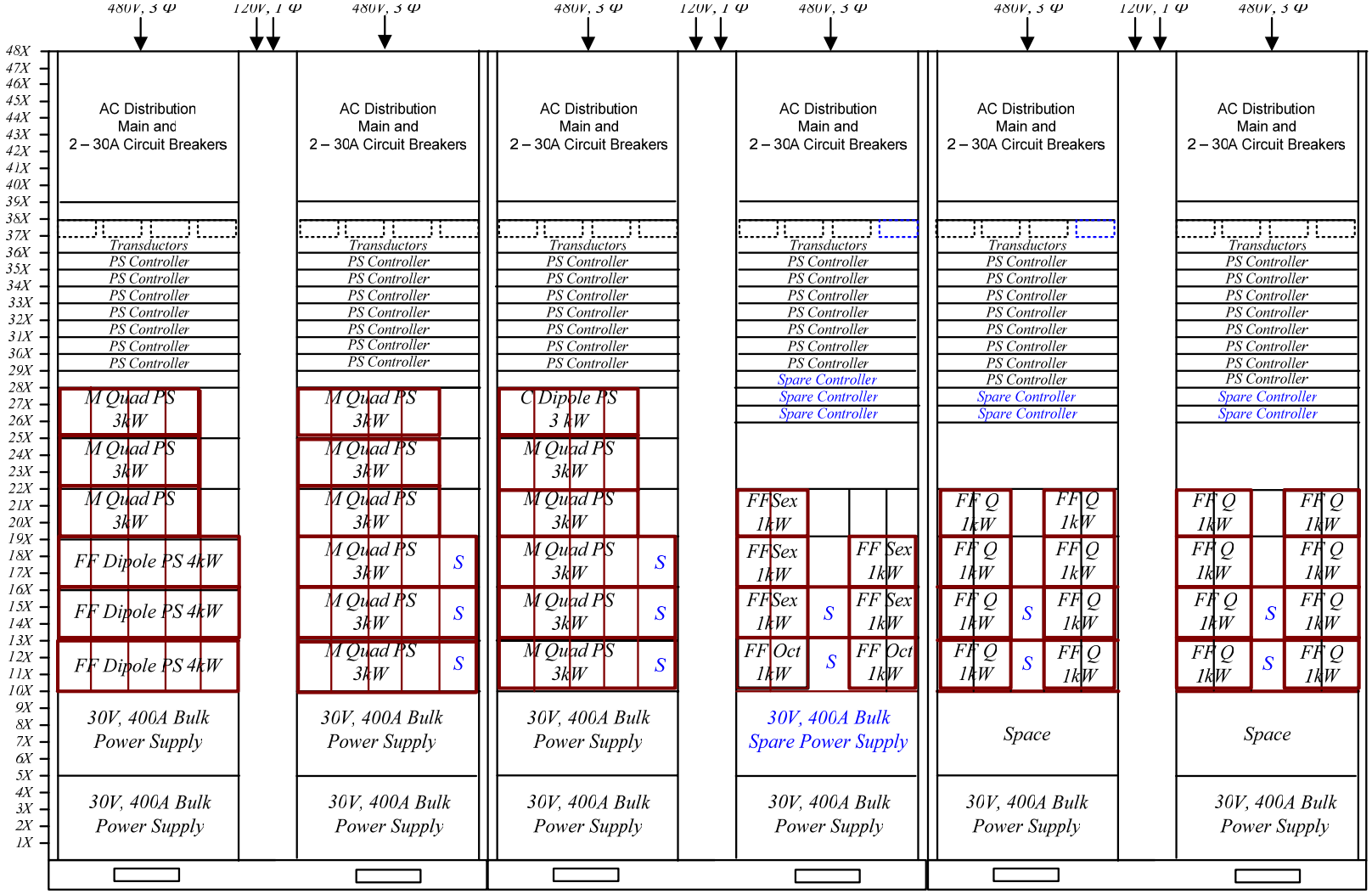
8-Hour Stability @150A



Module Current Sharing



System Architecture ATF2 Phase 2



P. Bellomo

3.2.1 Progress Summary

- Phase 1 initial tests successful, on budget, report in progress
  - Failure recovery of failed channel in 20 msec (resistive load) and 200msec (inductive load), stability over 8 hours 5 ppm
  - Hot swap feasible if needed.
  - Need to add diagnostics to power modules for failover, repair management
- Phase 2 development starting
  - 40-unit system proposal pending KEK decision
  - Continuing development of redundant bulk (easy) and controller (harder)
  - *4/5 Modules, A=0.88; add 1 of 2 Bulk, A=0.92; add 1 of 2 Controller, A=0.99*
- Budget
  - Phase 1 completed on budget [$30K]
  - Phase 2 beginning [$255K]

Larsen	3.2.1.Magnets	HA ATF2 Modular PS Sys Ph1	1111020	R&D	Materials & Service	11.303	10.000	-1.303
					Shop Services	0.067	0.000	-0.067
					SLAC Labor	18.953	20.000	1.047

CAM	Lvl-3	Charge	Chnum	FUND	Lsm	Kcst+Kcmt	Est.to cmplt	EstCstTot	Budgets	Remaining
		HA Mod PS Dev w/ATF2 Ph2	1110984	R&D	Materials & Service	0			200.000	200.000
					SLAC Labor	2.395			55.000	52.605

R&D Summary Proposal

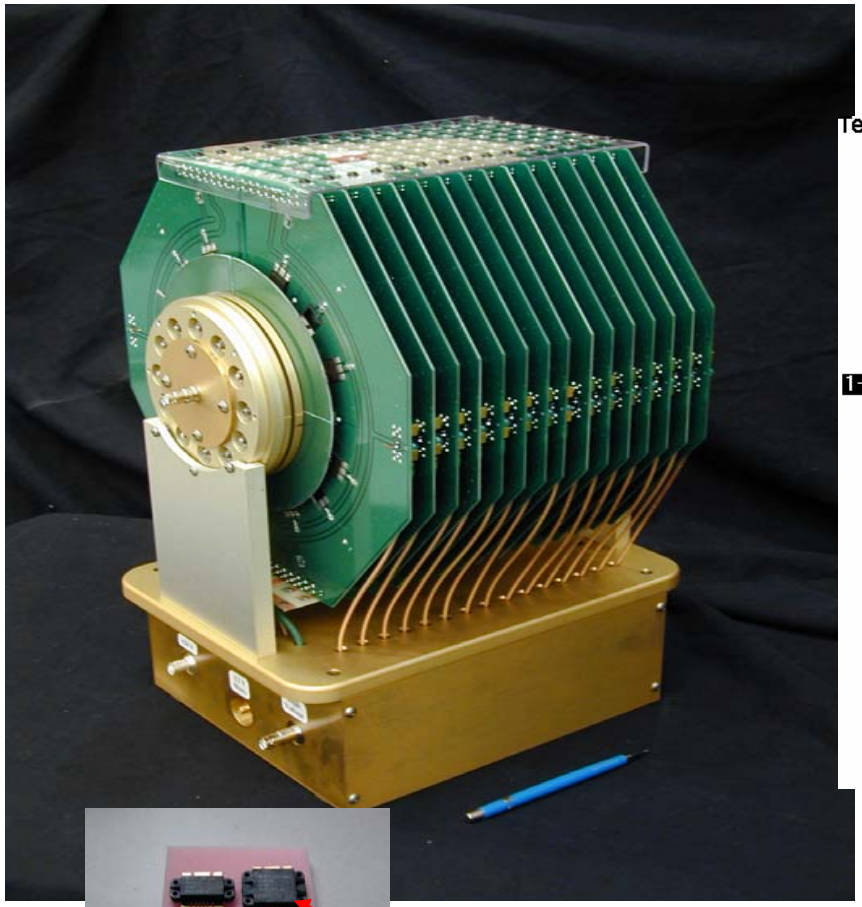
			FY06			FY07				FY08				FY09			
			Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
SLAC	3.2.1	High Availability Power Supply Systems															
	3.2.1.1	Construct, test ATF2 System w/subset HA	•	•	•	•	•	•									
	3.2.1.2	HA R&D Program															
	3.2.1.2.1	*Phase 1*															
		Demonstrate current share	•	•													
		Demonstrate hot swap 4/5 system		•	•												
		Test 4/5 on magnet load		•													
		Design, build redundant bulk supply		•	•												
		Design, build redundant Diagnostic Cntrlr		•	•	•	•	•									
		Design, test ATCA autofailover control				•	•	•	•								
		Design, build load monitor & interlocks		•	•	•											
	3.2.1.2.2	*Multiple Unit System (4) Phase 2, 3*															
		Construct, test full feature 4-up system					•	•	•	•	•						
		Design, build, procure magnet test loads						•	•	•	•						
		Construct, test ATCA auto-failover control						•	•	•	•						
	3.1.2.2.3	*HA Supply - Cold Magnets Phase 4*															
		Design HA system for Quad, Correctors							•	•	•	•					
		Build, test prototypes								•	•	•	•				
		Integrate Controls, test HA full features									•	•	•				
	3.1.2.2.4	*Industrialization*															
		Develop system generic specifications						•	•								
		Negotiate contracts								•	•						
		Procure 2 system units from 3 vendors										•	•	•			
		Demonstrate interoperability													•	•	•
		FY07 HA Power Supplies Totals															

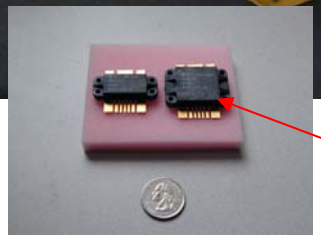
3.2.2 HA ILC Kicker w/ATF

[SLAC, LLNL/Bechtel, KEK]

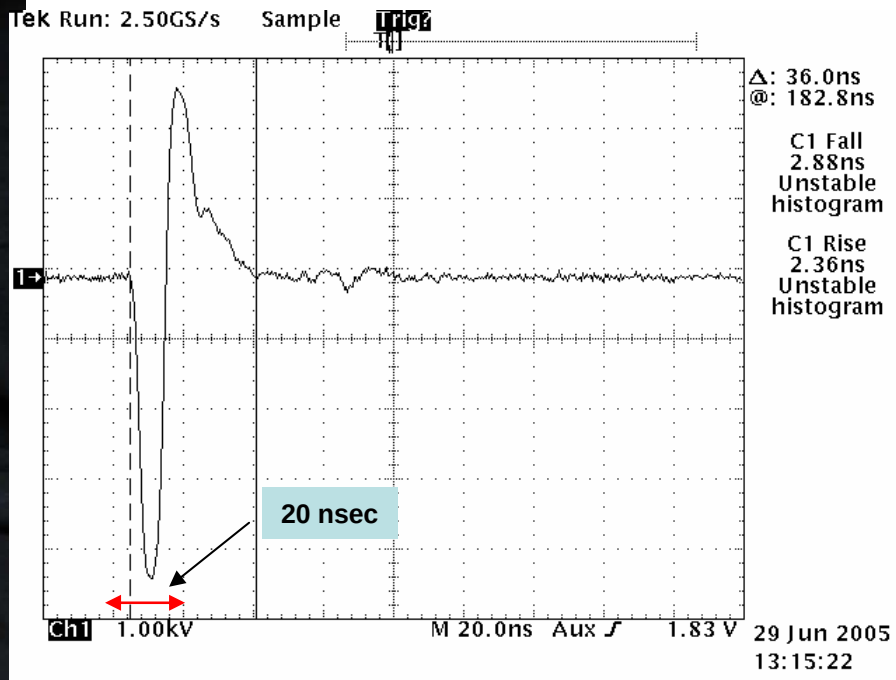
- Description
  - Demonstrate High Availability DR Kicker *System Architecture*
    - Multiple units, system control of timing, background calibration, fast diagnostics, reliability, failover
- Motivation
  - Many groups working on kickers to optimize pulse shape, but overall system problems need attention.
  - Reliability/Availability of System ~ 10-20 or more pulsers in series critical.
  - Induction modulator ideal balanced output (+/- 10kV) architecture but needs optimization for rise & fall time, impedance matching, stability of calibration, HA service features.

Original Prototype Tested at KEK





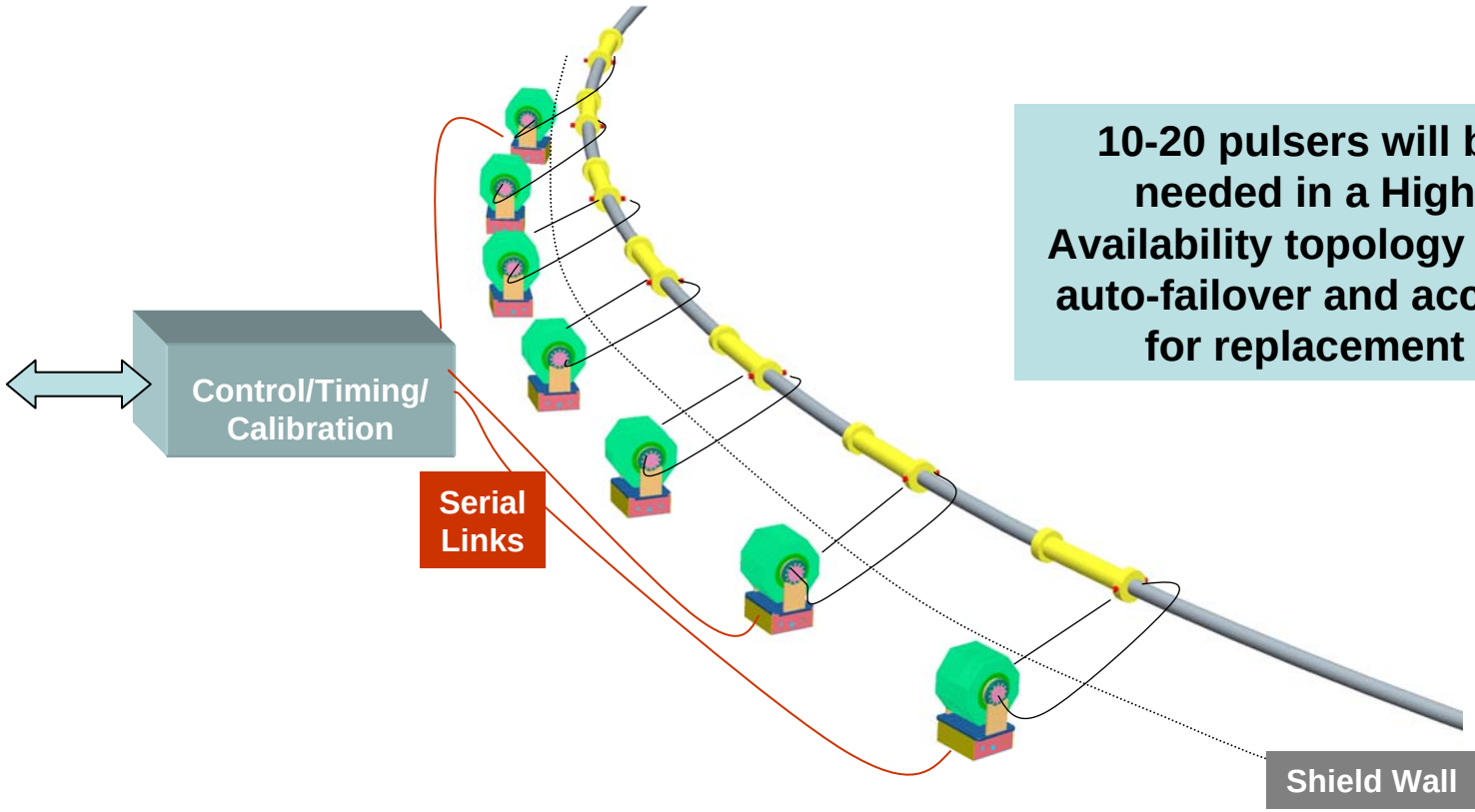
Integrated Driver & Power MOSFET



Pulse needs faster Tr, Tf, tail compensation

E. Cook LLNL

HA Kicker System Topology



10-20 pulsers will be needed in a High Availability topology with auto-failover and access for replacement

Program – Progress - Plans

- Program
  - FY06: Design 2nd prototype with 5 nsec pulse width for 6 km ring operating at 3 MHz (330 nsec bunch spacing for 1 msec every 5 Hz), +/- 10 kV balanced output.
  - FY07: Build 3rd prototype for full power 3 MHz operation; test ATF
  - FY08: Build multi-unit prototype system with control of precision timing, calibration, diagnostics; test at ATF2
- Progress in FY06:
  - Help with Marx 2nd order pulse flattening awaiting MOSFET-drivers
  - New Power MOSFET w/ drivers work starting
  - Higher voltage upgrade for KEK test in Fall 06

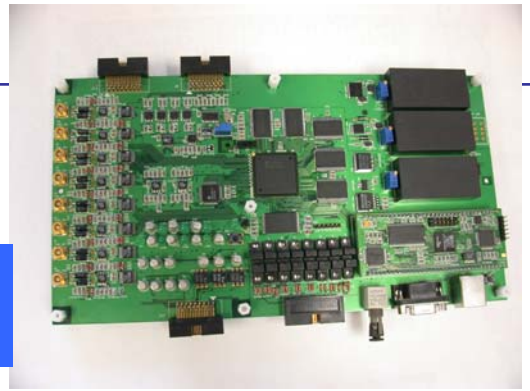
	A	B	C	D	F	G	Q	R	S	T	U
1											
2	CAM	Lvl-3	Charge	Chnum	FUND	Lsm	Kcst+Kcmt	Est.to cmplt	EstCstTot	Budgets	Remaining
6			HA ILC Kicker w/ATF	1110964	R&D	Materials & Services	124.125			250.000	125.875
7						SLAC Labor	28.922			55.000	26.078

3.2.3 Diagnostic Processor for Power Systems [SLAC, Pohang Accelerator Dept. (PLS)]

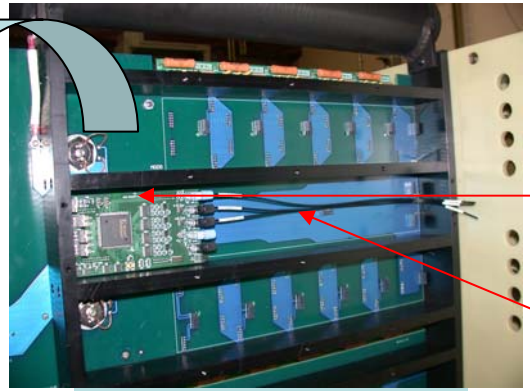
- Description
  - Generate trigger delays, pulse width for modulators, multi-phase rectifiers
  - Capture diagnostic waveforms via fast, slow ADC's, on-board memory for fault diagnosis, set trip points via precision DAC
  - Monitor interlocks, temperatures, pulsed and DC V,I levels
- Motivation
  - Experience with multi-cell solid state induction modulators showed need for *remote diagnostics and control* at the cell level.
  - Traditional manual methods inadequate for the ILC.
  - Diagnostics in control room can predict, take actions needed to protect boards, prevent unnecessary machine trips

Diagnostic Processors

Pohang Prototype

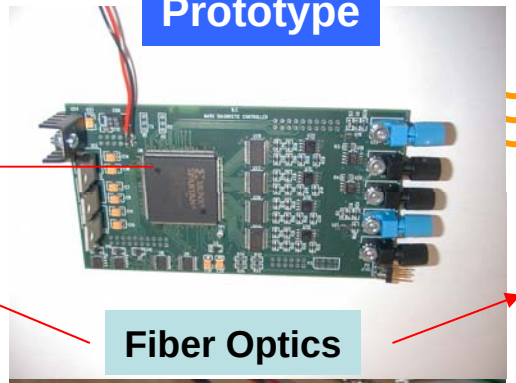


Marx Cell Front View 1 of 14

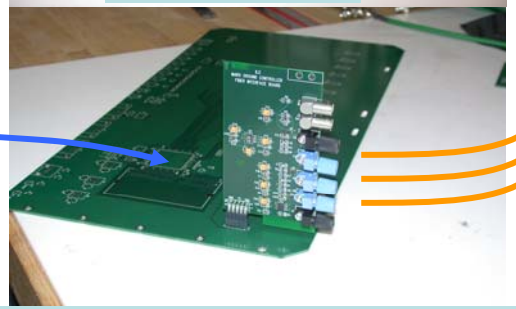


Marx Cell Rear View DP Mounting

Marx Prototype



Fiber Optics



Control Computer

Ground Control Station (16 Ch)

3.2.3 Diagnostics Progress in FY06

- First prototype designed, built to specifications; testing underway at PLS under MOU collaboration established 2005.
- SLAC refocused on Diagnostic Controller for Marx modulator
  - Cell voltages up to 120kV, very low power, small footprint
  - Marx units in production; firmware, testing underway; controls software engineer due to start in May.
- New Redundant Diagnostic Controller for HA power supplies
  - Conceptual design starting.

CAM	Lvl-3	Charge	Chnum	FUND	Lsm	Kcst+Kcmt	Budgets	Remaining
	3.2.3.Controls	Diagnostic Processor for PS	1110983	R&D	Materials & Service	10.100	60.000	49.900
					SLAC Labor	0.418	15.000	14.582

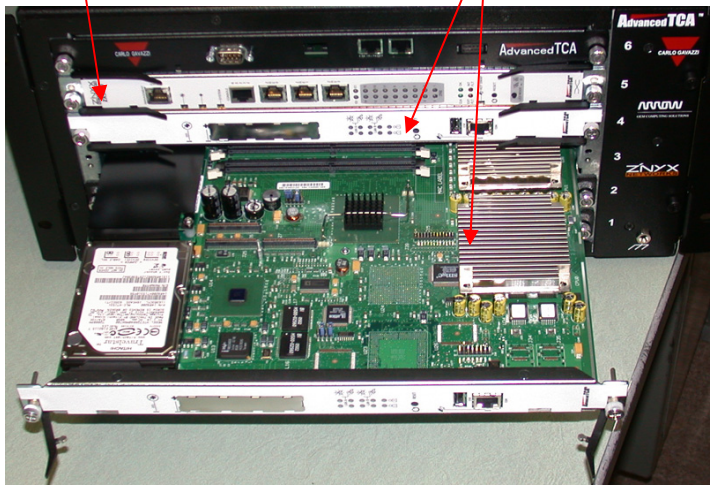
3.2.4 HA Instrumentation Standards

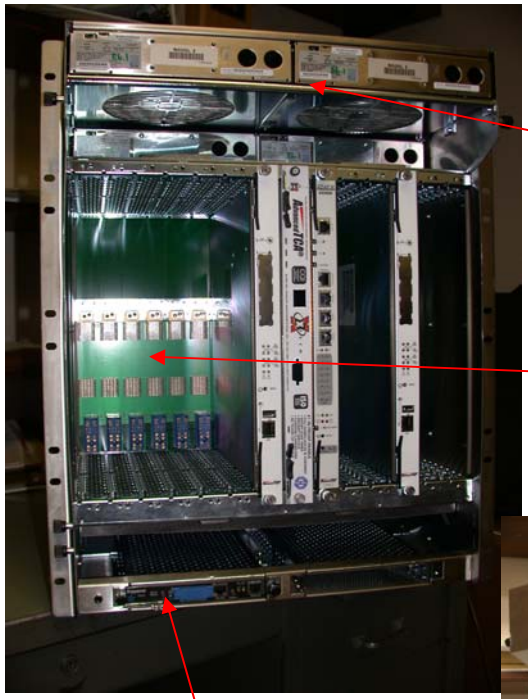
[Argonne, SLAC, FNAL, DESY, KEK, Universities]

- Description
  - Develop HA standard architectures for hardware and software, controls and front end instrumentation
  - Test critical features of hardware, applications software
  - Evaluate key applications, e.g. LLRF, BPMs, against candidate standard platforms
  - Main candidate: Advanced Telecom Computing Architecture (ATCA), A=0.999 at crate level.
- Motivation
  - Instrument standards essential for engineering, maintenance efficiency, low cost
  - New gigabit serial technologies provide opportunities to move designs to next generation technologies embraced by industry
- Progress
  - Working groups established, examining problems, opportunities for HA design in LLRF, BPM's. ATCA evaluations getting underway.

ATCA Starter Kits

5-Slot Crate w/ Shelf Manager
Fabric Switch
Dual IOC Processors

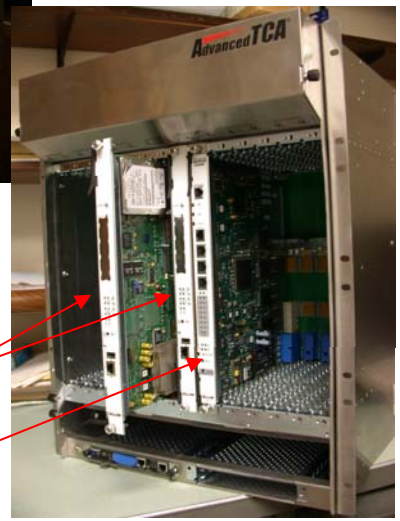




4 Hot-Swappable Fans

16 Slot Dual Star Backplane

Shelf Manager



Dual IOC's Fabric Switch

Dual 48VDC Power Interface

Rear View

3.2.4 Instrument Standards Plan & FY06 Budget

			FY06			FY07				FY08				FY09		
			Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3
	4.0	HA Instrumentation Standards														
	4.1	*ATCA Standard Evaluation*														
		Design/Procure develc	•	•		•	•									
		Procure Test Equipment for 2.5 GHz R&D				•	•									
		Evaluate for analog, d	•	•		•	•	•	•							
		Evaluate connectors,	•	•		•	•									
		Evaluate cbl-brd transitions, fiber-Cu intfces				•	•									
		Design, build channel protoypes LLRF, BPM				•	•	•	•							
	w/Collab	Demonstrate LLRF, BPMs integrated w/controls								•	•	•	•			
	w/Collab	Down-select all C&I systems standards												•	•	•

	A	B	C	D	F	G	Q	R	S	T	U
1											
2	**CAM**	**Lvl-3**	**Charge**	**Chnum**	**FUND**	**Lsm**	**Kcst+Kcmt**	**Est.to cmplt**	**EstCstTot**	**Budgets**	**Remaining**
12			**HA Instr Std R&D**	**1110985**	**R&D**	**Materials & Services**	**34.754**			**100.000**	**65.246**
13						**SLAC Labor**	**0.000**			**160.000**	**160.000**

Labor funds unused to date due to lab Engineering priorities.

3.2.5 Development of Universal Accelerator Parser, D. Bates, LBNL

- Develop tool for parsing lattice analyses data from different codes into standard format for information exchange. FY06 Budget $21K
- Program Goals (LBNL MOU Addenda, Collab w/Cornell)
  - Prototype converter to/from Accelerator Markup Language AML – March 06
  - Distribute Parser – Sept. 06
- Progress
  - AML Draft distributed Sept 05
  - MAD to AML translator developed
  - Project proposed to continue at same level in FY07

3.2.6 2_03: Design and Fabrication of a Radiation-Hard 500-MHz BW Digitizer Using Deep Submicron Technology, K.K. Gan, Ohio State U

- FY2006 Award: $75,000, FY07 Request $64,000
- Program: Develop 500 MHz BW 12 bit (11 Effective bit) 2 GS/s digitizer in deep submicron technology
- Pipelined approach four 3-bit stages with interleave
- Progress:
  - 3-bit cell designed and simulated
  - To date could not achieve 12 bits with rad-hard cells. Without correction limited to 6-8 bits. Hardware correction gets 10 bits precision. Calibration needed beyond. Continuing cell development.
  - Plan 1st silicon submission in 06, rework, 2nd run in 07.

3.2.7 2_09: Radiation Damage Studies of Materials and Electronic Devices Using Hadrons

David Pellet, UC Davis

- Hadron irradiation of NdFeB permanent magnets, electro-optical devices in detector readout, CCD's for vertex detector, accelerator control devices
- FY04-FY06 program; FY 2006 Award: $38,000
- Progress
  - Testing NdFeB 3-block sample field degradation, 3 manufacturers, 10kGy gammas & 1 kGy 1 MeV neutrons; series of 1 MeV neutron exposures
  - Starting electro-optics exposures - transmission vs. wavelength irradiated and standard samples
  - 7 runs done, 5 more planned for NdFeB next 6 months

RDR Status

- Controls & LLRF Converging on Cost Models
  - LLRF will draw from DESY, SNS design, cost experience
  - Cost, technical guidance needs to be prescriptive & clear
  - Standard worksheets
  - Main issue - Converge quickly on *new* models for HA hardware, software; select cost strategies
- Power Systems Cost Models
  - HLRF – Have firm manufacturing models for klystrons, modulators.
  - Distribution - Problematical to optimize manufacturing assemblies to avoid expensive off-the-shelf components
  - Power Supplies – HA models with industry quotes or actual pricing on key components.
  - Controls - Unique adaptation of existing Ethernet control designs.
  - Kickers – Use induction model.

RDR Plans, Resources

- Roadmap to RDR
  - Each subsystem group develops cost models
  - Data collected by standard rules, formats for WBS rollups
  - DCB designated team does top-level rollup
  - Additional key people assigned subsystem writing tasks for RDR
- Resources
  - RDR support drawn from high-level engineers in Technical Systems & Global Groups
  - Will impact R&D work
  - *Not specifically called out as line items in budgets*
  - Estimate 1 FTE per major system
- Regional Differences
  - Assume Region-specific comprehensive estimates with communication, sharing of information between Technical, Global groups. However must agree on BCD models.

Summary

- R&D Programs for FY06 on track for most important cost drivers – Modulators, power supplies
- Lagging in applying resources for controls and instrumentation standards
  - In-house help promised soon
  - Exploring outside university collaboration assistance
  - Need close support of additional people in Controls architecture & software. New resources in FY07 proposal for this purpose.
- RDR Roadmaps being developed for major systems
  - Models still under development; guidelines still in development, no costing started.
- *Meeting RDR fast track costing very challenging, needs tight collaboration & will impact key R&D resources*.