Vertex Detector R&D

Ronald Lipton, Fermilab

Contents:

- Physics Requirements
- Technical Challenges
- R&D Efforts
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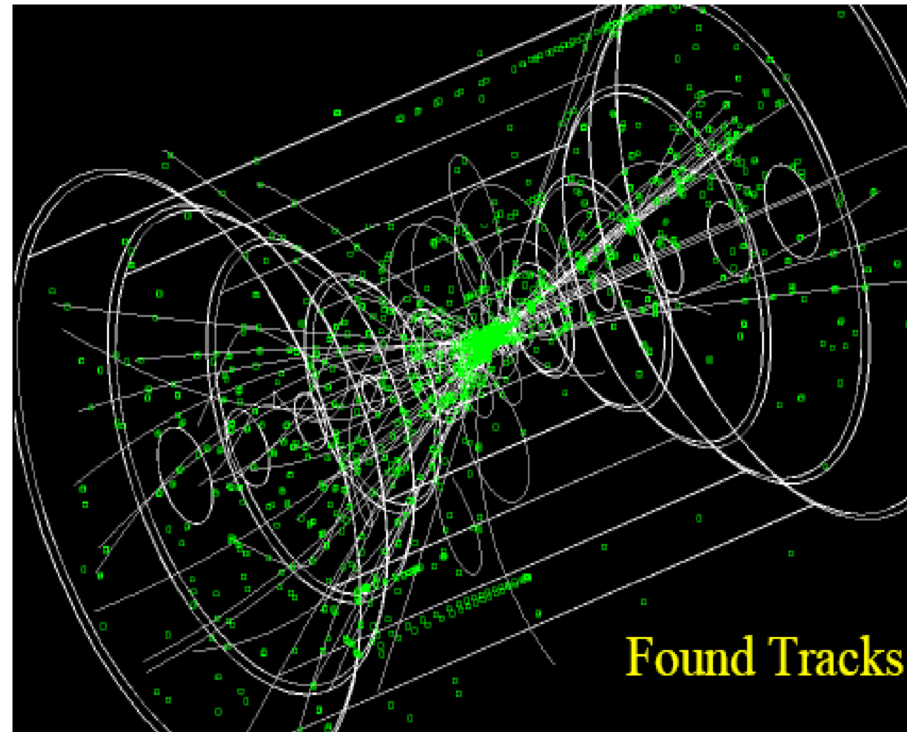
- Summary



Physics Needs

ILC is designed to do precision physics:

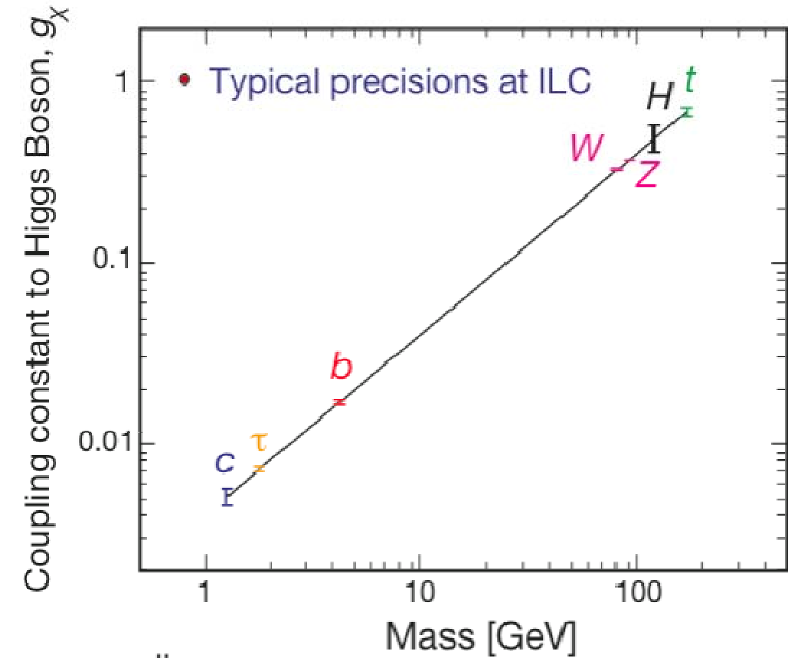
- Higgs couplings
  - Requires excellent separation of b/c/light quark vertices
- Higgs self coupling (potential):

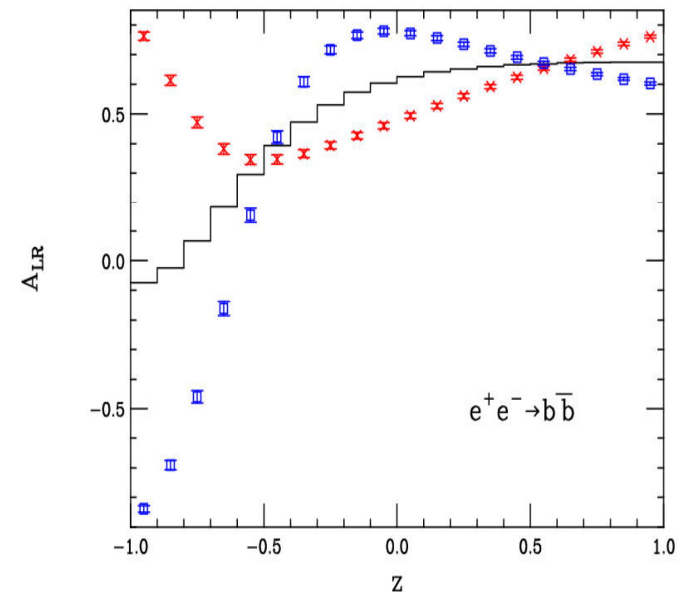
$$e^+e^- \to Z^0H^0H^0 \to qqbbbb$$

$$backgrounds : tt \to bb\,csc\,s, ZZZ, ZZH$$

  - B quark ID within jets
- Forward-backward asymmetry
  - Flavor tagging
  - Vertex charge
  - Forward tracking

All of these (and many more) depend on precise tracking and vertexing. The ILC environment allows the deployment of a vertex detector of unprecedented power.



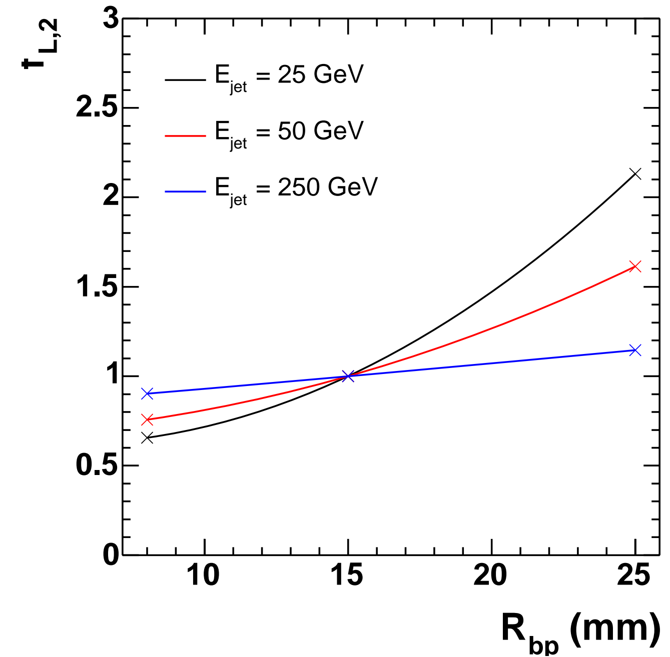


KK graviton exchange with jet-charge info $\sqrt{s}$ = 500 GeV, Λ = 1.5 TeV, 500 fb^{-1} (Hewett)

Optimizing Vertex Performance

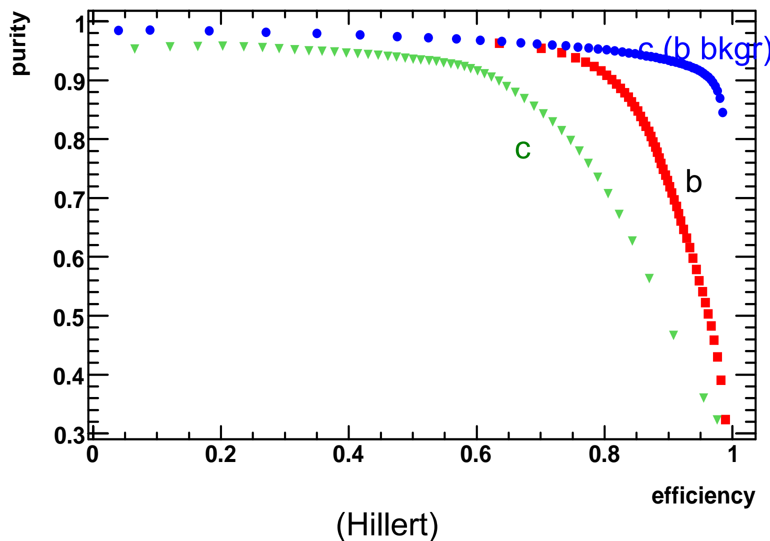
Optimizing vertex performance has major impact on physics capabilities

- Inner radius
- Material
- Position resolution (<5 microns)
- Forward tracking



Luminosity factor as a function of radius for processes requiring vertex charge for 2 jets

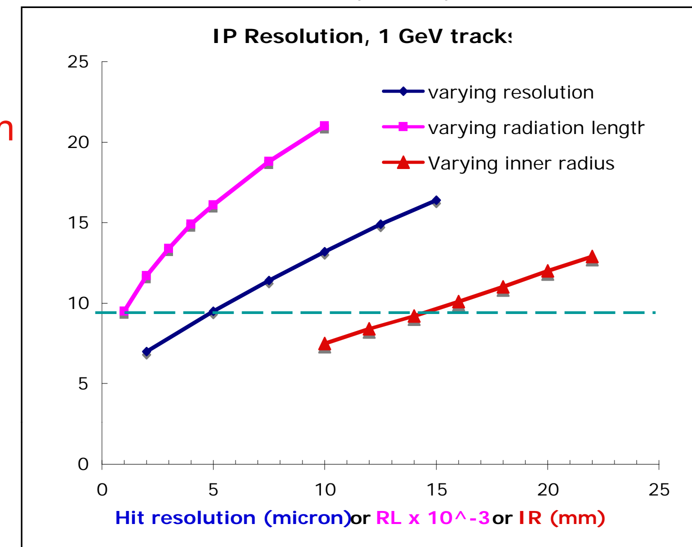
(Hillert)



(Hillert)

Parametric simulation assuming:
- 0.1% RL per layer
- 5 micron resolution
- 1.4 cm inner radius

Varying each parameter



Ronald Lipton LCDRD review
June 19,2007

Detector Goals

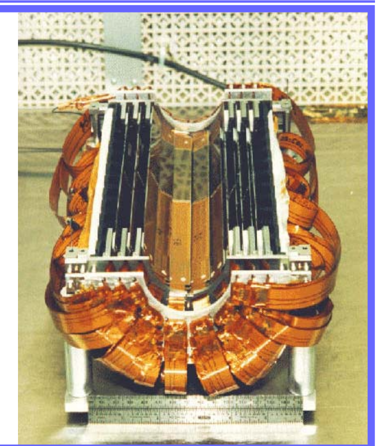
- Good angular coverage with many layers close to IP, pattern recognition
- Excellent spacepoint precision (< 5 microns)
- Superb impact parameter resolution ($5\mu m \oplus 10\mu m/(p \sin^{3/2}\theta)$)
- Transparency (~0.1% X_0 per layer)
  - Average power constraint based on air cooling with minimal mass (< 50 Watts)
- Integration over <150 bunch crossings (45 μsec)
- Electromagnetic Interference (EMI) immunity
- Moderately radiation hard (<1 MRad)

These goals require an unprecedented combination of high resolution, low mass & precise timing from the vertex detector.

Made possible by rapid advances in semiconductor technology.

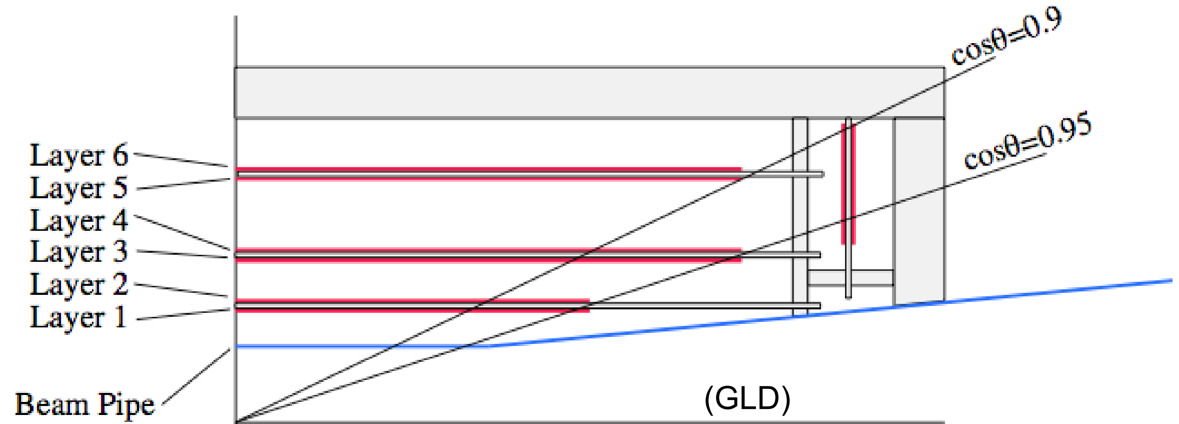
SLD VXD3

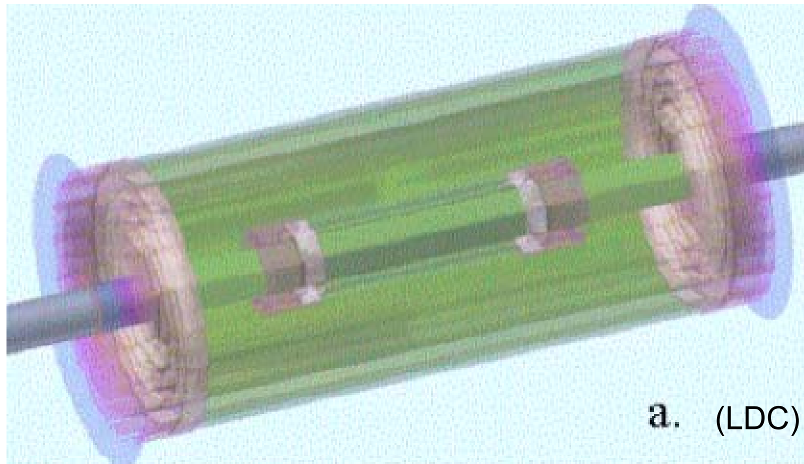
307 Mpixels
5 MHz ⊗ 96 channels
0.4% X_0 / layer
~15 watts @ 190 K
3.9 μm point res.

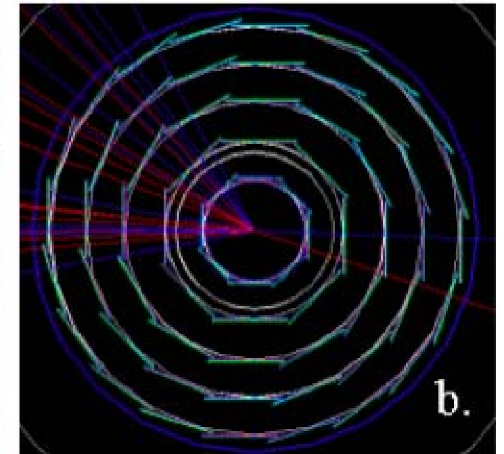


Design Features

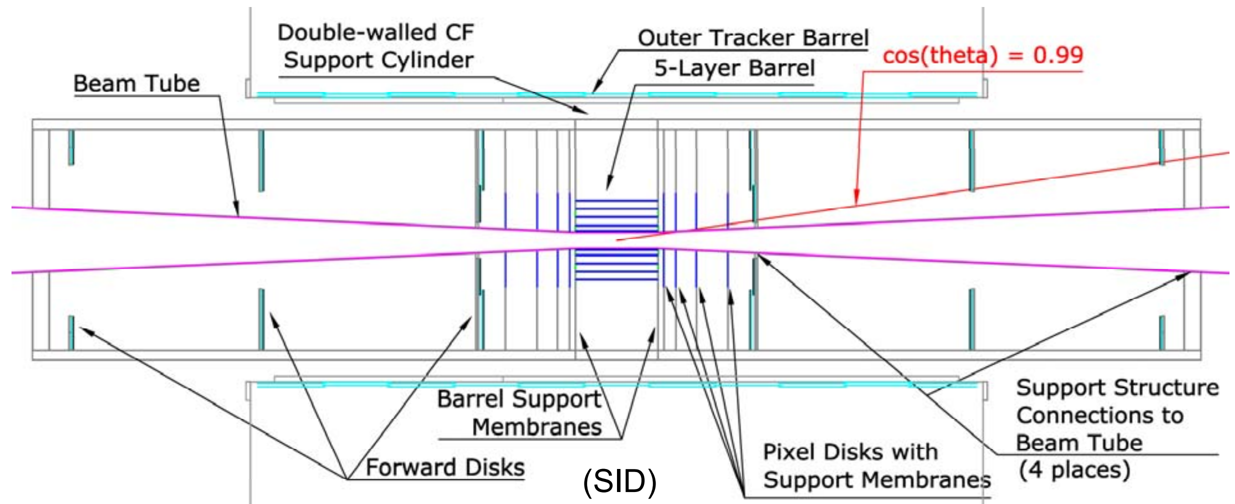
- Outer radius ~ 6 cm
- Barrel length ~ 14 cm
- Ladder widths 1-2 cm
- Disks to cover forward region







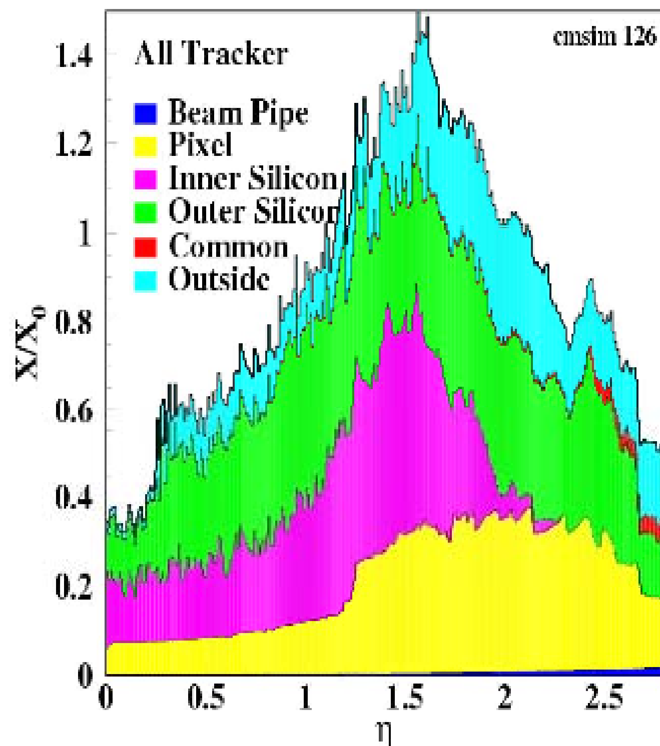
A bit larger than this

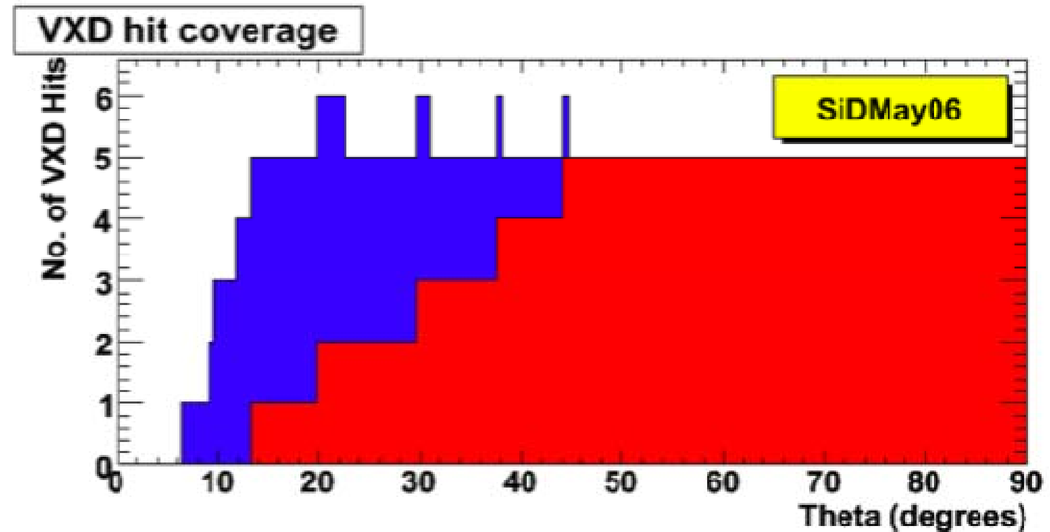


Material

- To achieve ILC goals we must improve RL/layer by ~20 x
  - *Low power*
  - Thin detectors

LHC





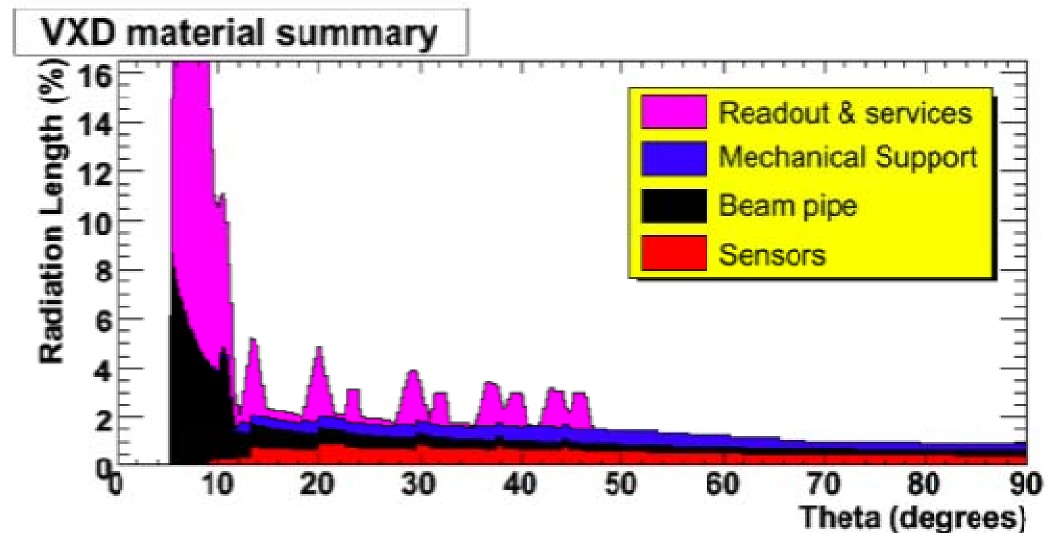
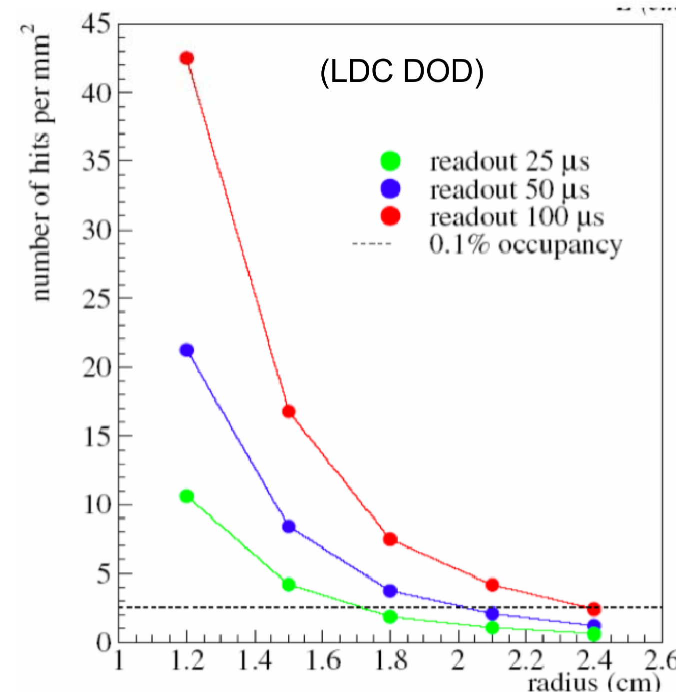
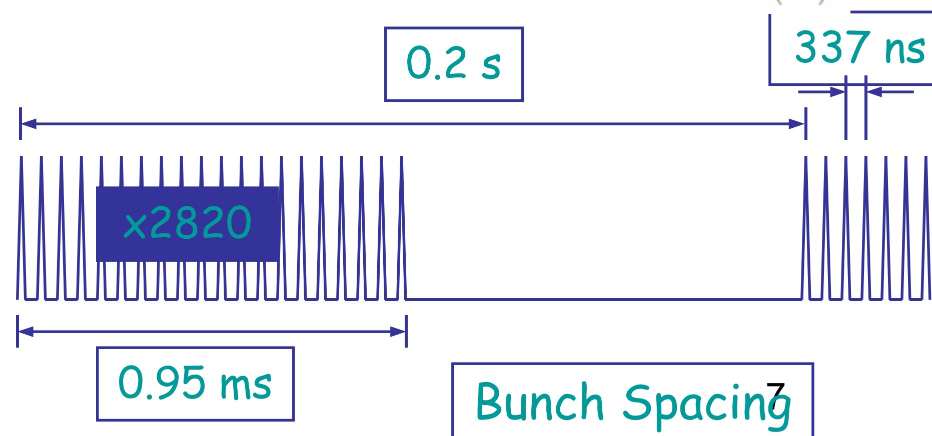


Figure 33 VXD hit pattern and material summary as a function of polar angle.

Integration Time

- The sparse nature of the physics events and time structure of the ILC bunch trains allow readout of ALL of the hit information in a vertex detector
- Integration time needs set by inner layer beam-based occupancy - how many crossings do we integrate over?
- Better than 50μs resolution generally agreed (the more precise the better)
- Time is power (FE current, more clock cycles …)
- Read out during or after bunch train
- Architecture differs by technology
  - Rolling shutter
  - Multiple analog samples
  - Explicit time stamps
  - Buffers per pixel

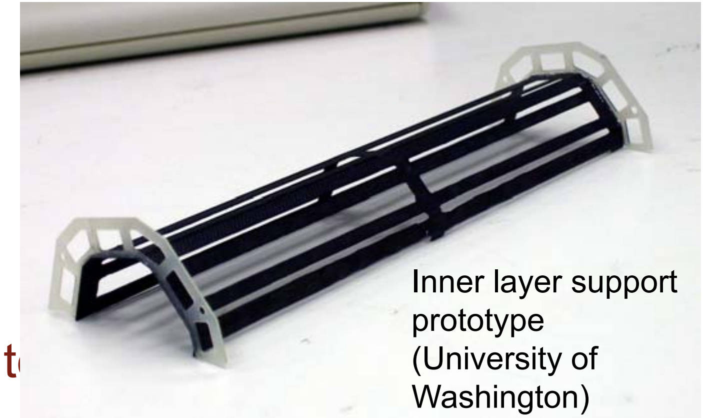




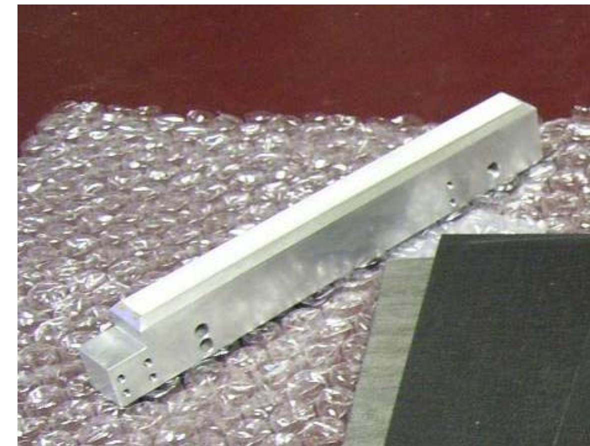
Mechanical Support

U. Washington/Fermilab

- U. Washington/Fermilab are investigating carbon fiber-based structures
  - Develop techniques for fabricating and handling thin-walled carbon fiber structures
  - Prototypes of carbon-fiber support structures
  - Various tooling for attaching support membranes t support structure and mounting silicon wafers on support structure
  - FEA analysis of mechanical and thermal behavior
  - Measurement of material properties (CF CTE)
- Fabricated and delivered to Fermilab
  - Three prototype half-shell structures for evaluation, testing and developing silicon mounting procedures
  - Assembly mandrel, end ring glue fixture and vacuum chuck for precision placement of silicon

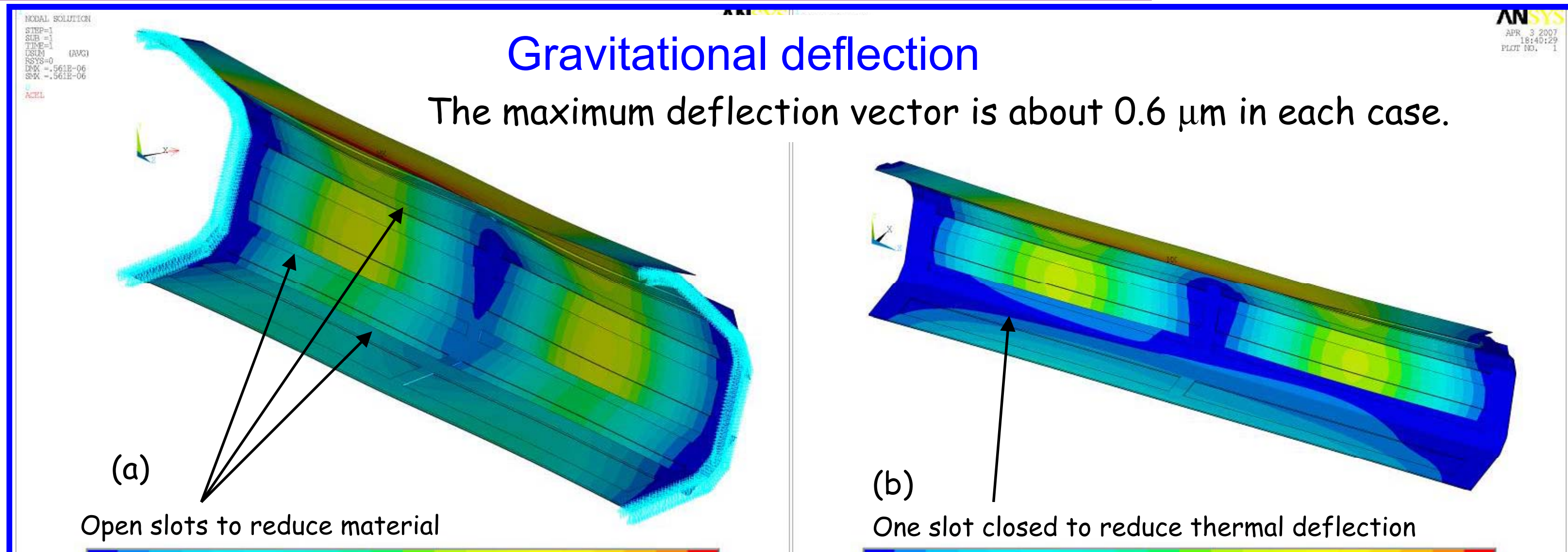


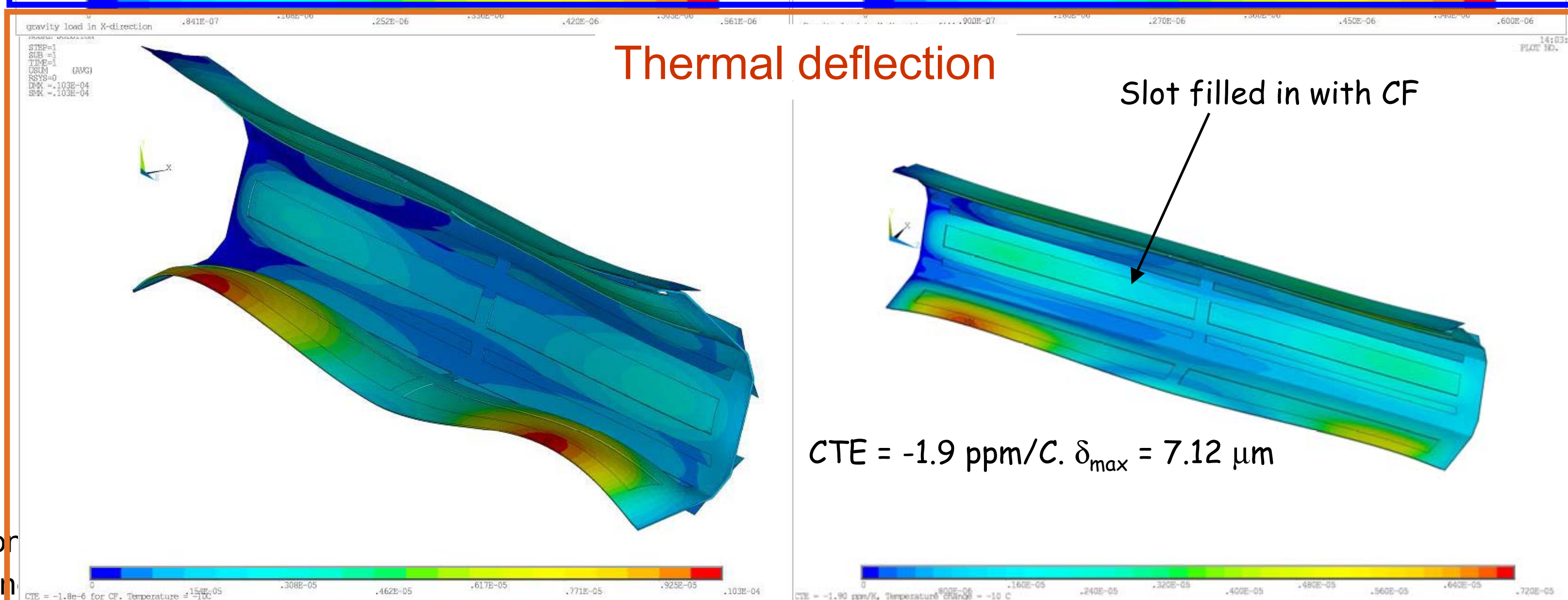
Inner layer support prototype (University of Washington)



Support FEA Studies

U. Washington



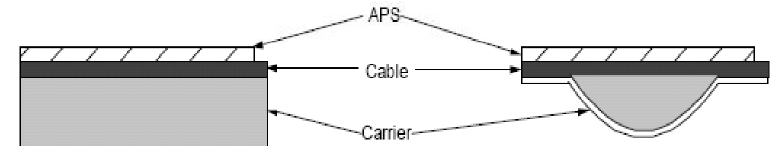


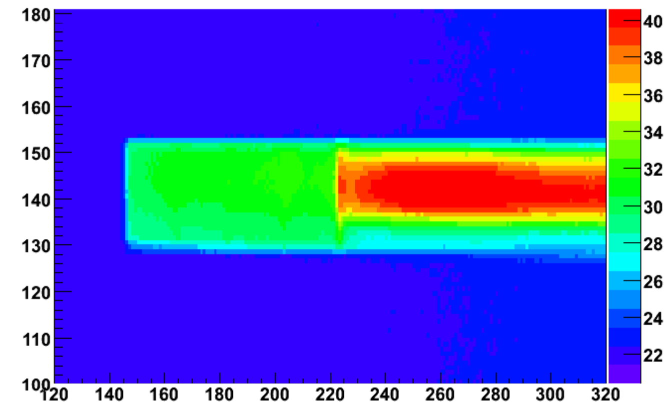
VTX Ladder Design & Testing

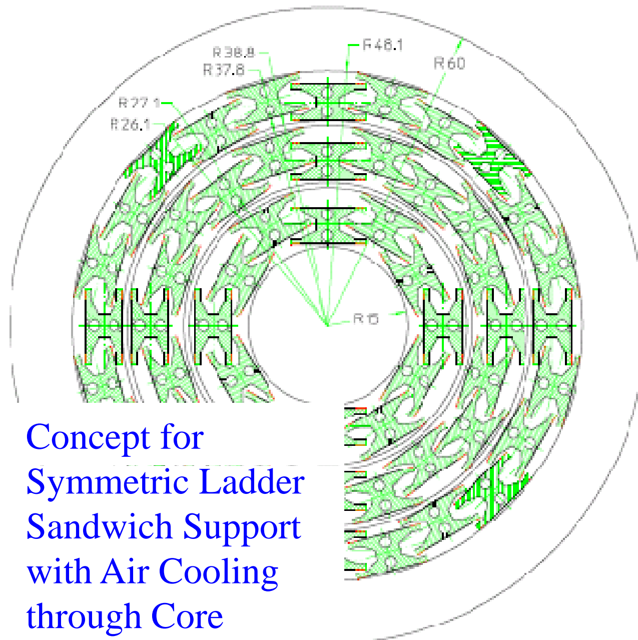
LBL

Design, construction and characterization of a full ladder equipped with back-thinned CMOS pixel sensors in collaboration with STAR.

- STAR carrier: 50µm CFC+3.2mm RVC+50µm CFC (=0.11%X_0)
- Mechanical and thermal characterization of STAR prototype, study of heat removal using low-speed airflow







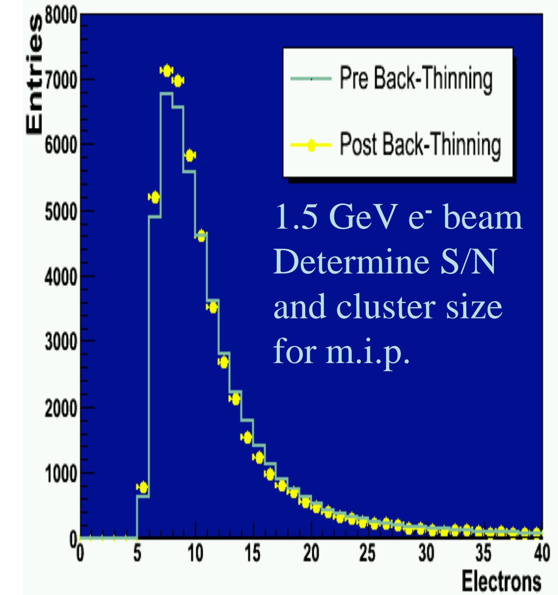
Concept for Symmetric Ladder Sandwich Support with Air Cooling through Core

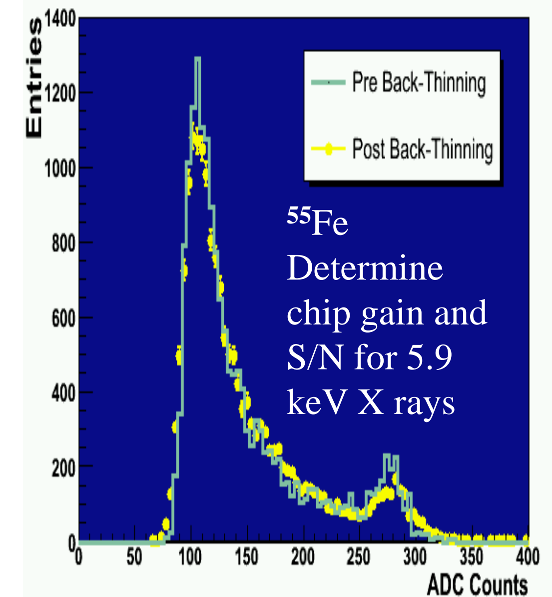
- FEA of prototype structures: (core-cooled Si/CF/RVC sandwich, Si/Al/RVC sandwich, CVD coated CF) in progress using data from surveys of 40 and 50 mm thin chips, first results promising, test of prototype in 2008

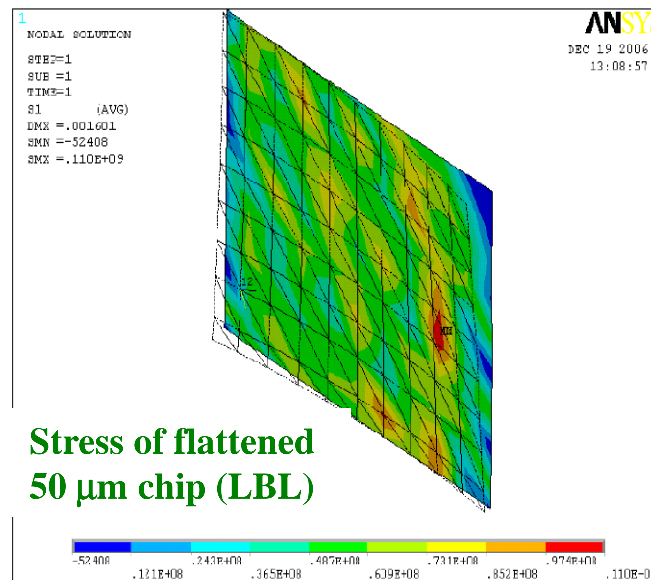
Thinning

LBL, Fermilab

- LBL has thinned over 15 Mimosa CMOS MAPS chips,yield of functional chips~90%, Process reliable down to 40 μm
  - Study charge collection and S/N before/after back-thinning: MIMOSA 5 sensors
  - These sensors will be used in beam telescope
- Fermilab has thinned BTeV Fpix readout chips to 15 μm with ~75% yield, FPIX wafers to 20 μm





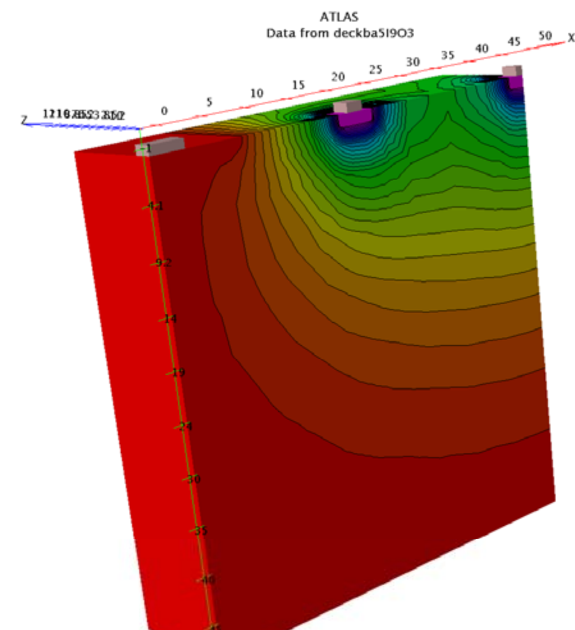


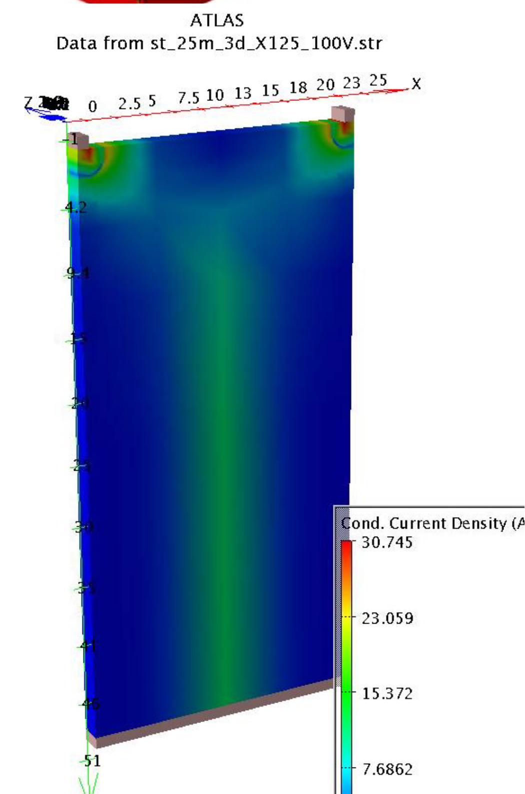
Stress of flattened 50 μm chip (LBL)

Sensor Technology

- Technologies being developed by the semiconductor industry are directly applicable to ILC vertex detectors
  - Thinning (standard for many applications)
  - Integrated sensors and CMOS (digital camera)
  - Focal plane sensor development - “edgeless” sensors
  - “Virtual Wafer Fab” simulation software
  - Access to CMOS processing variants

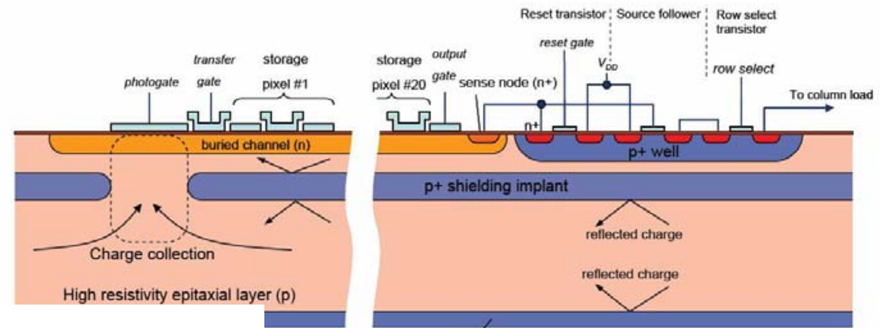
- We can engineer detectors in ways we never could before.





Candidate Technologies

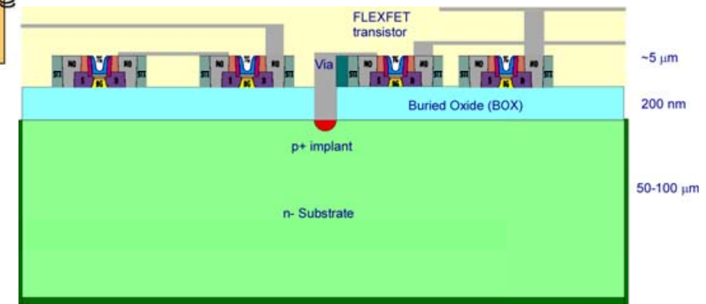
- CCDs
  - Column Parallel
  - ISIS
  - Split Column
  - Fine Pixel
- CMOS Active Pixels
  - Mimosa I-XII
  - INFN
  - LCRD 1-3 (LBNL)
  - CAP1-4 (Hawaii)
  - Chronopixel (Oregon/Yale)
- SOI
  - American Semiconductor/FNAL
  - LCRD-SOI (LBNL)
  - CAP5 (Hawaii)
  - KEK
  - SUCIMA
- 3D
  - VIP1 (FNAL)
- DEPFET



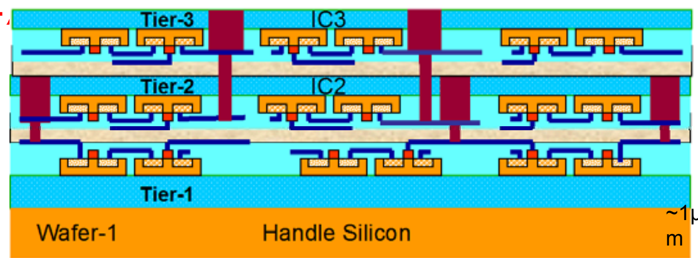
CCD

NMOS PMOS NMOS Detector (V= 2.5) NMOS PMOS NMOS
P-Well N-Well (V=1.8) P-Well N-Well Deep N-Well P-Well N-Well (V=1.8) P-Well
Depleted P-epi
Undepleted P-epi
7um
V = 0
P++ Substrate
Charged Particle or laser

CMOS Active Pixels

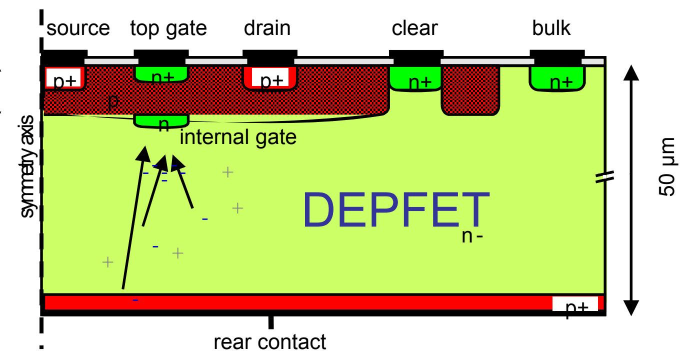


SOI



3D

US work in red



Ronald Lipton LCDRD review
June 19,2007

Architectures

	CMOS MAPS	CCD	DEPFET	SOI	3D
Rolling Shutter	Mimosa 1-N LDRD1,2	Normal CCD		LDRD-SOI	
Column (row) Parallel	Mimosa 8 LDRD3	CPCCD	DEPFET/ CURO/ SWITCHER		
Pipelined Storage	FAPS, Mimosa12 CAP	ISIS		CAP5	
Time Stamp	SLIM5, Chronopixel			ASI SBIR	VIP1

US Efforts

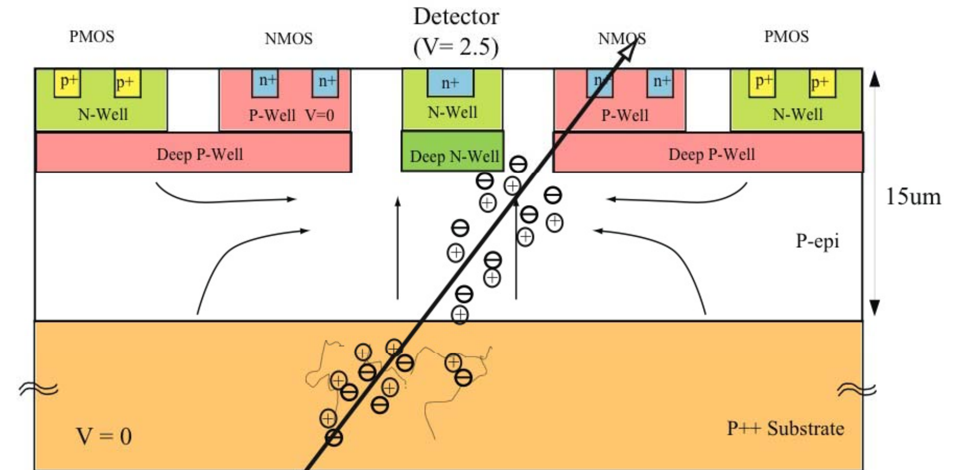
Chronopixel

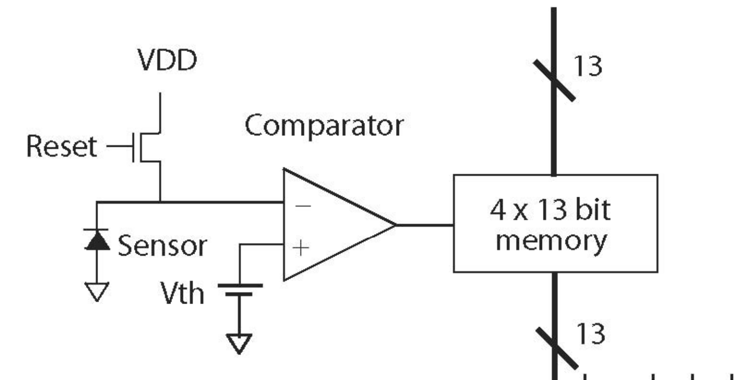
Yale/Oregon/Sarnoff

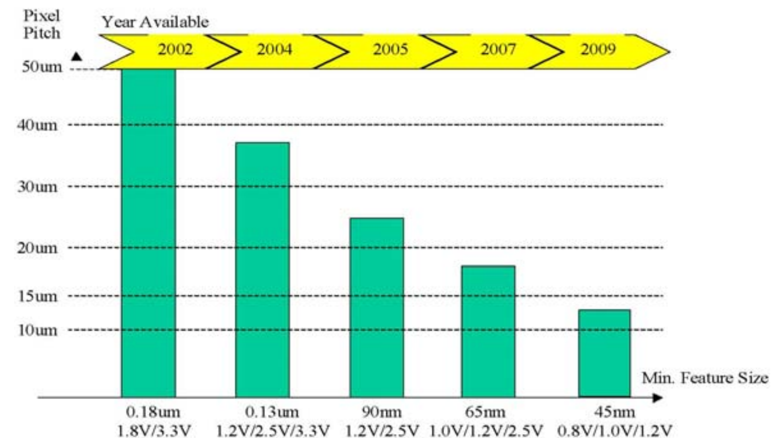
Variant of CMOS active pixel

- Charge collection in thin (5-20μm epitaxial layer)
- Design Goals
  - Single bunch time stamp
  - 4 buffers/pixel
  - Deep depletion
  - Deep p-well to direct diffusion charge
  - Digital readout
- Depends on available technology

  50 μm pixels now - scales to <20 μm in 45 nm technology.
  Thickness and resistivity of available epitaxial layers



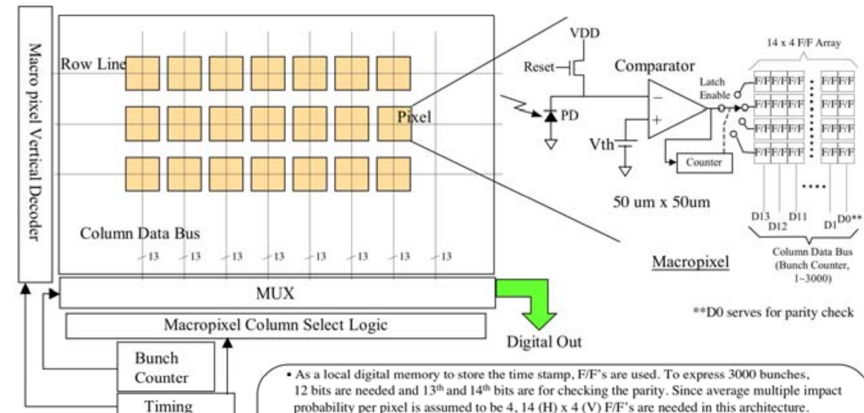


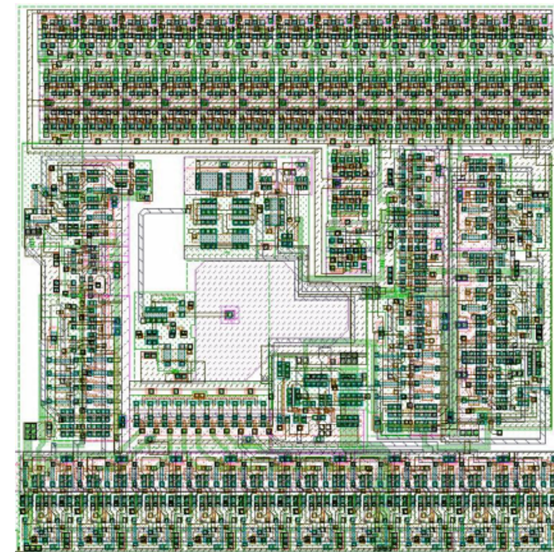


Chronopixel

Yale/Oregon/Sarnoff

- Completed Macropixel design last year
  - Key feature – stored hit times
  - 645 transistors
  - Spice simulation verified design
  - TSMC 0.18 mm => ~50 mm pixel
  - Epi-layer only 7 μm
  - (Talking to JAZZ (15 mm epi-layer))
  - 90 nm => 20-25 μm pixel
- January, 2007
  - Completed Chronopixel design
  - 2 buffers, with calibration
  - Deliverable – tape for foundry
- This year
  - Fab 50 μm Chronopixel array
  - Demonstrate performance
  - Then, 10-15 mm pixel (45 nm tech.)





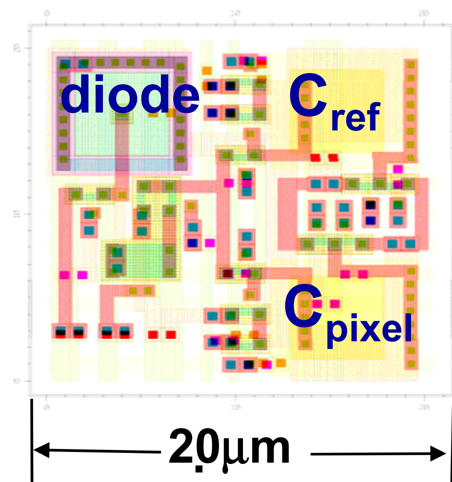
563 Transistors (2 buffers +calibration)

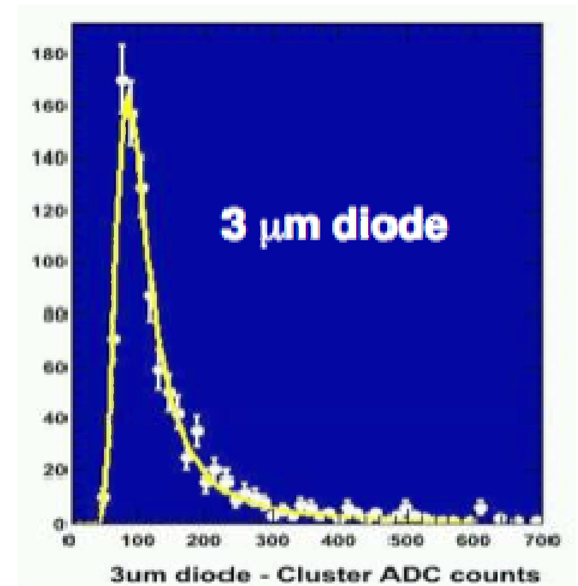
50 μm x 50 μm

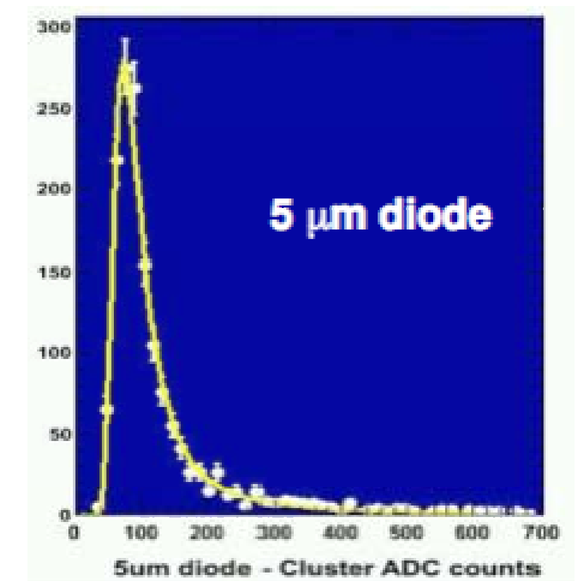
CMOS MAPS

LBL

- Set of chips designed to explore pixel and electronics design variants
- LDRD1: First LBNL test structure
  - AMS 0.35 μm OPTO, 14 μm epilayer
  - Simple 3T pixels, serial analog output
  - 3 matrices with 10x10 μm^2, 20x20 μm^2 and 40x40 μm^2 pixels
- LDRD-2: second prototype chip
  - AMS 0.35 μm OPTO, 14 μm epilayer
  - 20×20 μm^2 pitch with in-pixel CDS: signal and pedestal level stored on pixel capacitors
  - 3×3 μm^2 and 5×5 μm^2 diodes
- LDRD-3: next prototype in AMS 0.35 μm OPTO, to be submitted in June/July
  - In-pixel CDS
  - 5-bit successive approximation, fully-differential ADCs @ 300 MHz at the end of each column







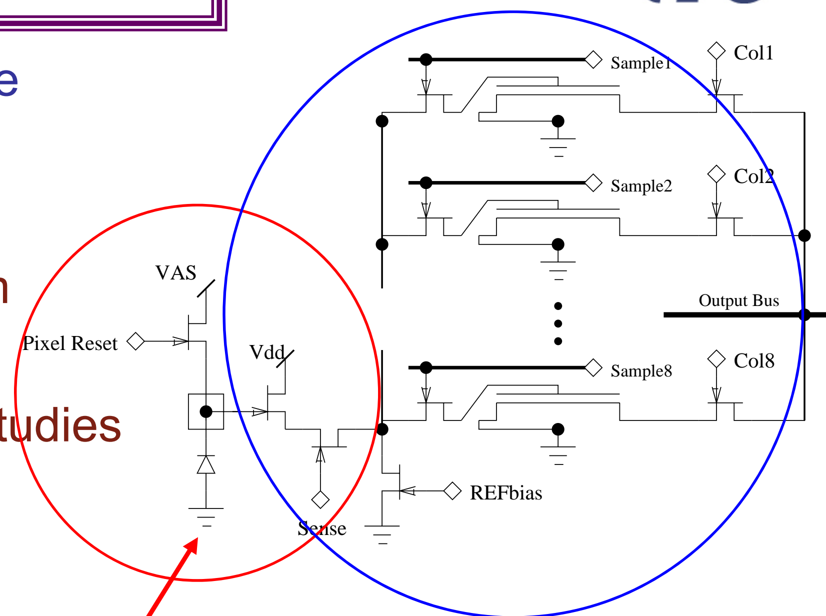
CAPS CMOS Pixels

Hawaii

Part of development also aimed at super Belle

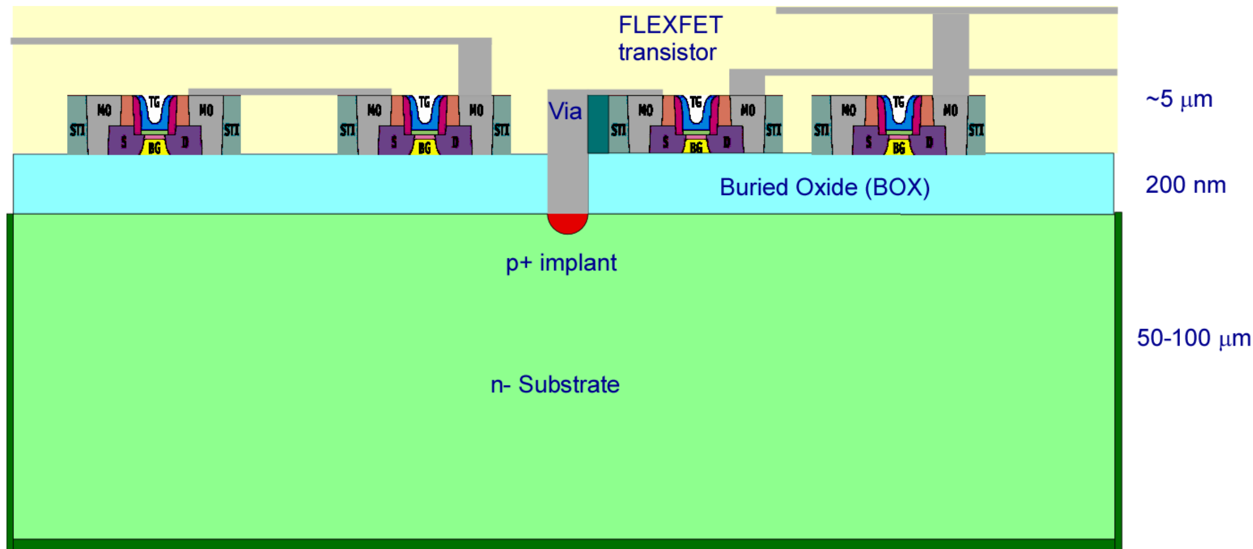
In-pixel charge storage/time sliced

- CAP1/2 [MAPS technology] Studies
  - Characterization of CAP1 in test beam
  - Study of radiation hardness/storage
  - Storage density/max. pipeline depth studies
- CAP3 "full size" Detector
  - Development of laser scan system for systematic studies
  - Systematic scan and study of transfer rate and signal uniformity
  - Non-uniformity and transfer limitations observed
- CAP4 AMS 0.35um Opto
  - Study of new analog storage/readout – evaluation started



SOI

Fermilab, LBL, Hawaii



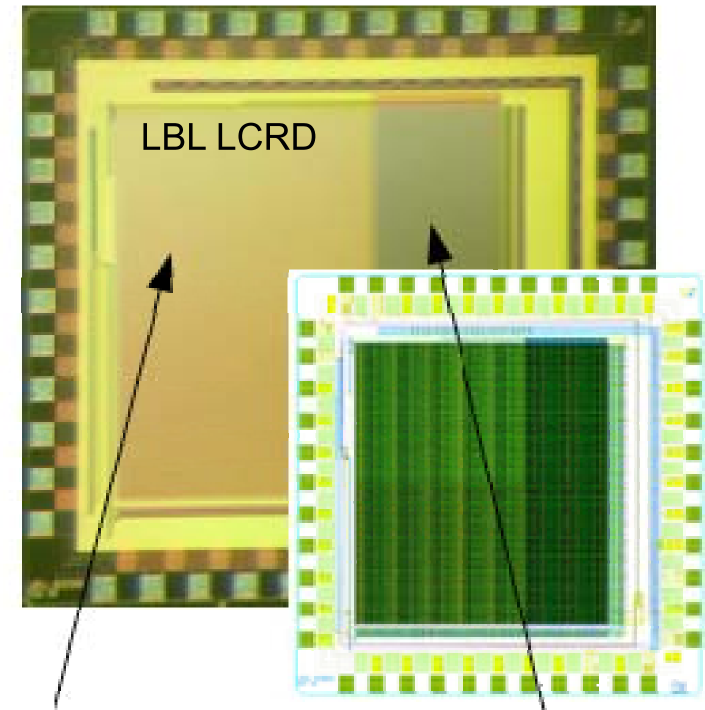
- SOI is based on a thin active circuit layer on an insulating substrate. Modern technology utilizes ~200 nm of silicon on a “buried” oxide (BOX) which is carried on a “handle” wafer.
- The handle wafer can be high quality, detector grade silicon, which opens the possibility of integration of electronics and fully depleted detectors in a single wafer with very fine pitch and little additional processing.
- Two processes available: OKI (through KEK), and American Semiconductor (SBIR, Cypress)

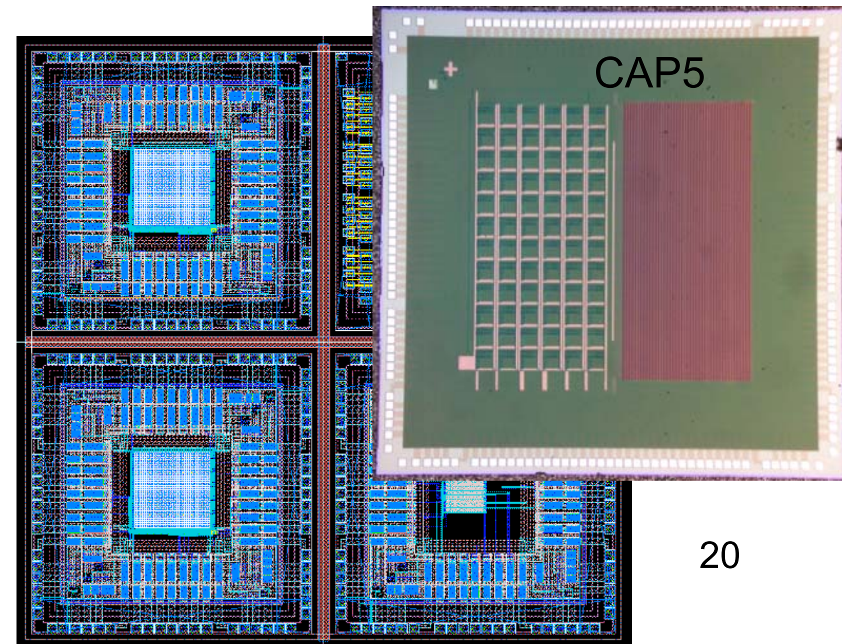
SOI

Fermilab, LBL, Hawaii

Several submissions based on OKI/KEK 0.15 micron SOI process

- LBL has designed binary and analog 10 μm pixels in the OKI 0.18 micron process.
  - Variety of diode sizes, transistor types.
- Hawaii - CAP5
  - Debugged process for non-Japanese
  - Problems with backside bias (back gate problem)
- Second CAP submission
  - 4x larger die
  - Study process spread
  - Evaluate space-time correlation

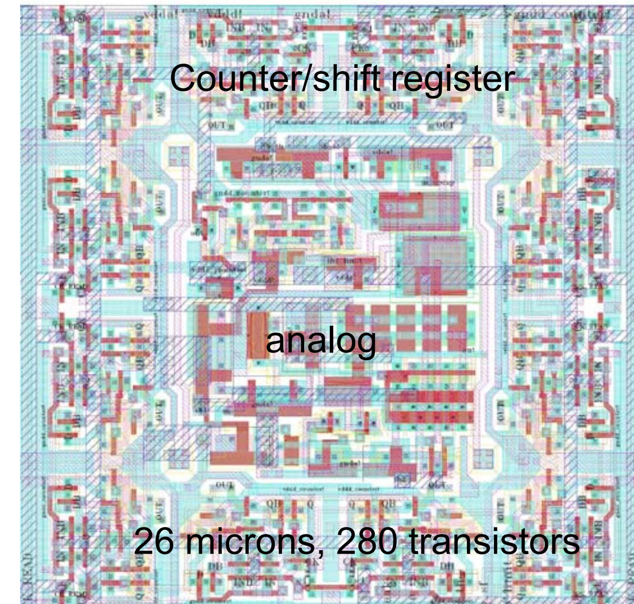


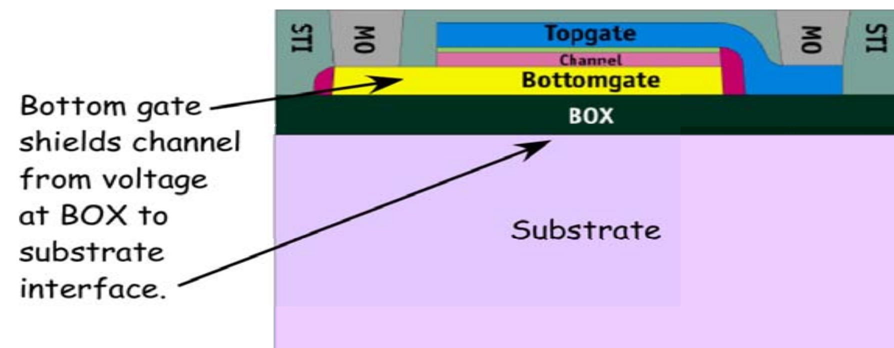


SOI

Fermilab

- FNAL has designed a 12 bit 26 μm pitch imaging chip in the OKI process
  - Back and being tested
- FNAL has designed a 20 μm pitch ILC vertex chip in the ASI 0.18 μm process (SBIR funded)
  - Single bunch analog/digital time stamp
  - Immunity to back gate, analog-digital coupling and radiation effects due to dual gated “Flexfet” transistor and pinning layer
  - Fabrication depends on phase II SBIR

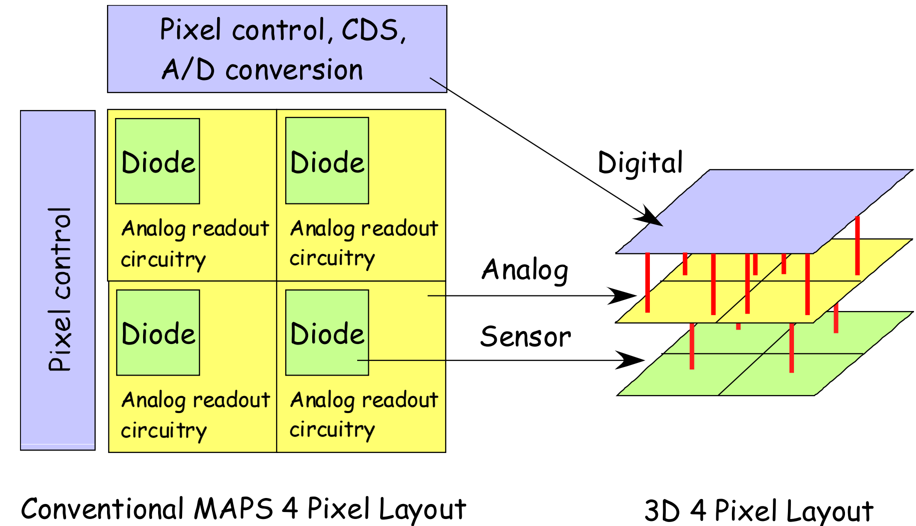




3D Circuits

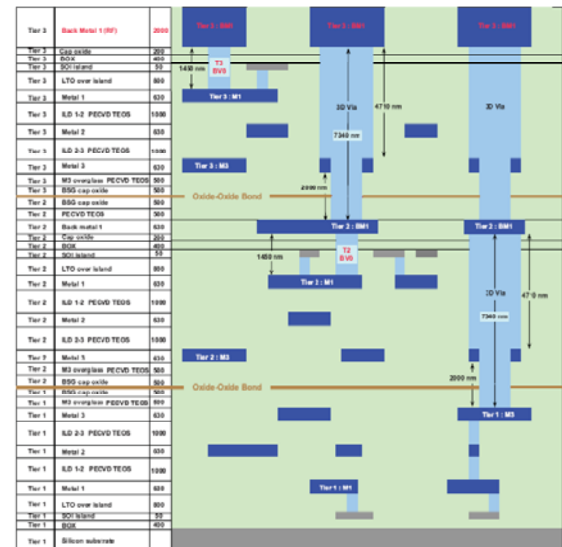
Fermilab

- A 3D chip is generally referred to as a chip comprised of 2 or more layers of active semiconductor devices that have been thinned, bonded and interconnected to form a "monolithic" circuit.
- The layers can be fabricated in different processes.
- Industry is moving toward 3D to improve circuit performance.
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power and crosstalk
- Utilizes technology developed for Silicon-on-Insulator devices



Conventional MAPS 4 Pixel Layout

3D 4 Pixel Layout

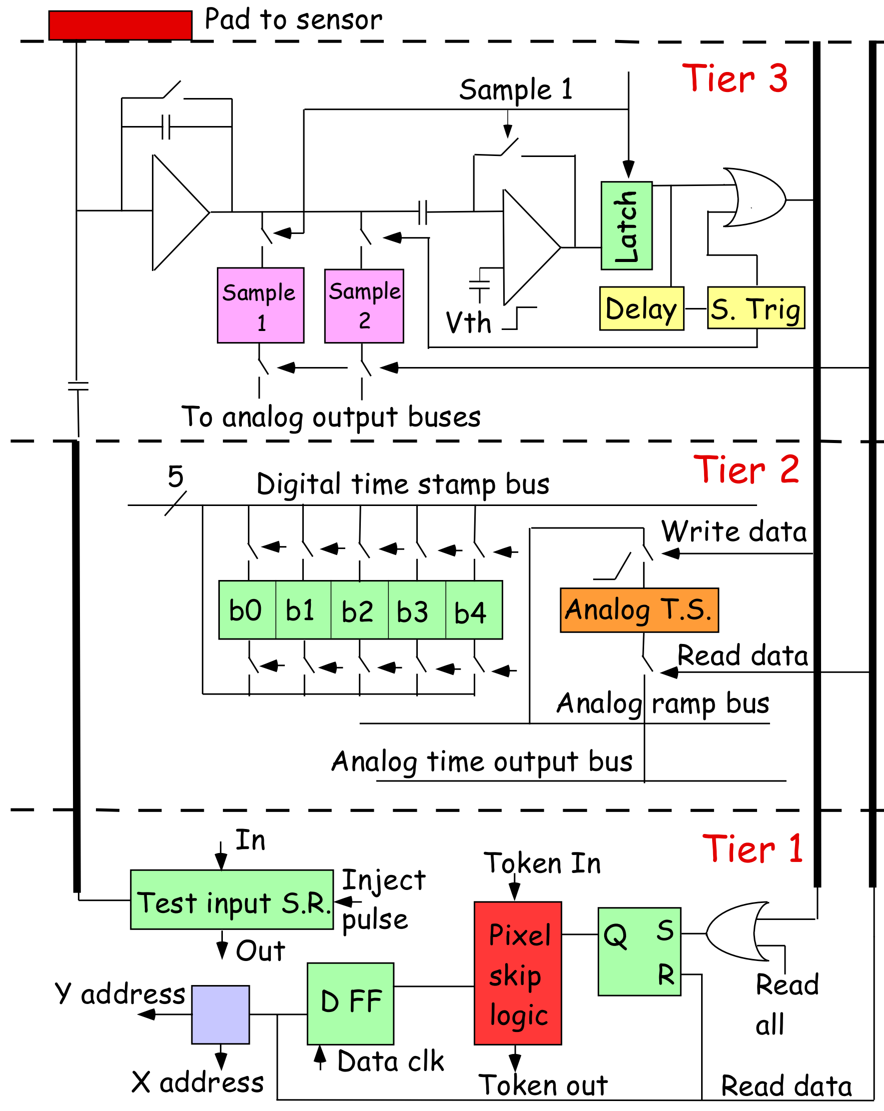


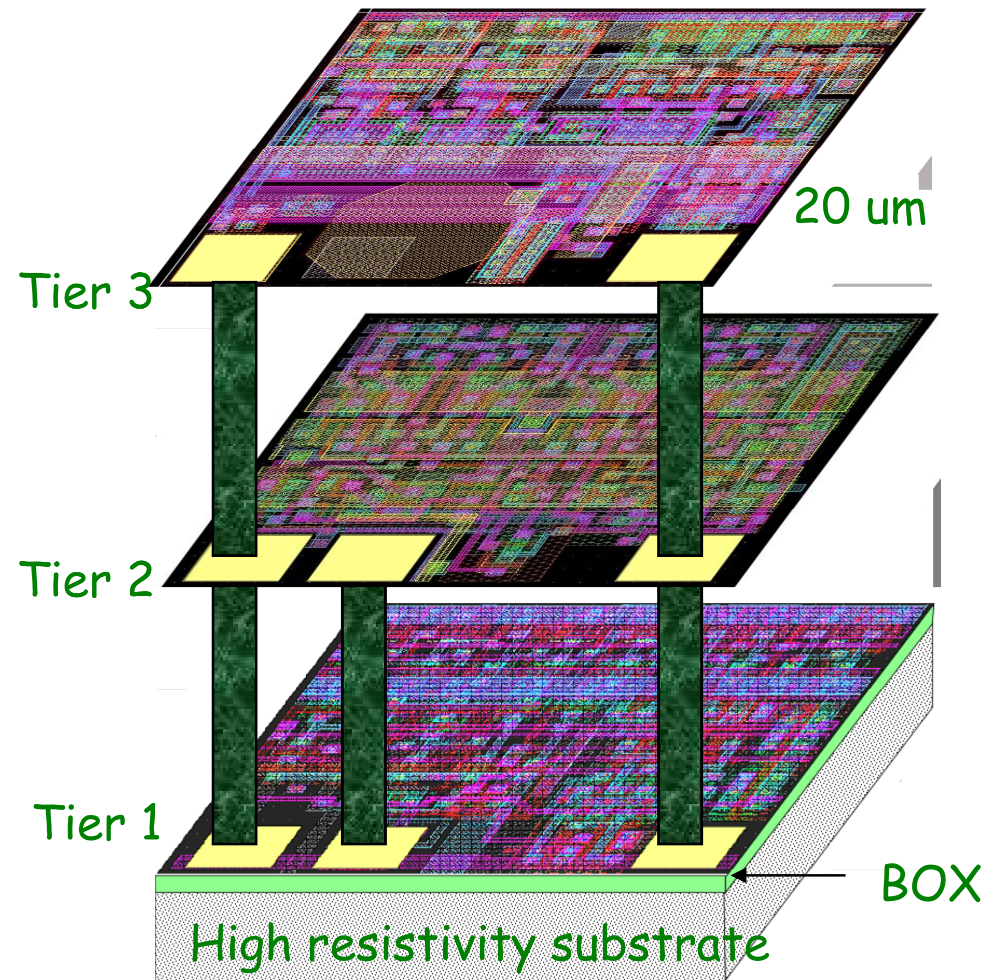
MIT-LL 3D Process: Three levels of transistors, 11 levels of metal in a total vertical height of only 22 μm.

3D chip VIP1, submitted to DARPA funded MIT-LL 0.18 micron 3D process due back August

Key features: Analog pulse height, sparse readout, high resolution time stamps.

Front end power ~ 1875 μW/mm^2 (before cycling), 175 transistors in 20 μm pixel.



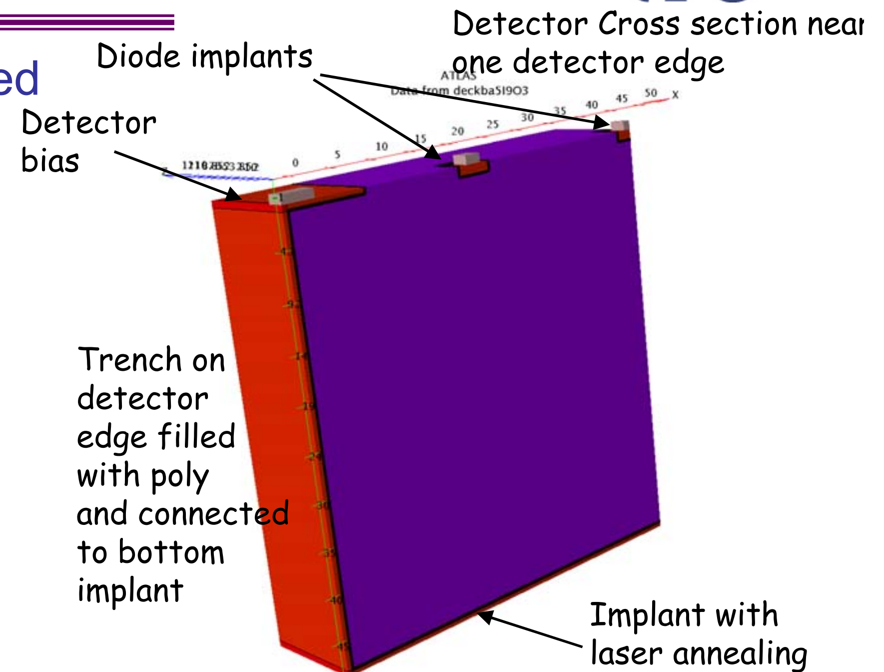


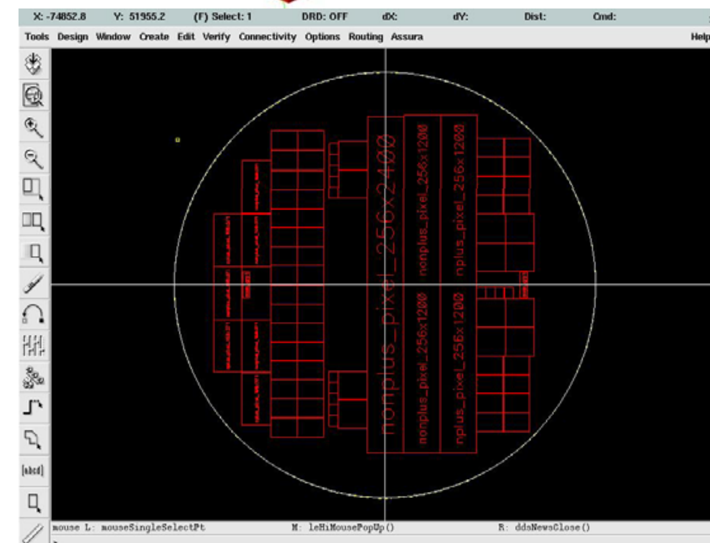
Thinned, Edgeless Sensors

Fermilab/Cornell

Sensors sensitive to the edge can be fabricated by a combination of trench etching, thinning, and laser annealing

- Produce a set of detectors thinned to 50-100 microns at MIT-LL for beam and probe tests.
  - Validate process
  - Understand performance
  - Measure the actual dead region in a test beam
- Parts available for prototype vertex structures
- Masks designed at FNAL
  - Strip detectors (12.5 cm and ~2 cm)
  - FPiX2 pixel detectors (beam tests)
  - Detectors to mate to 3D chip
  - Due back September
- Laser annealing studies at Cornell

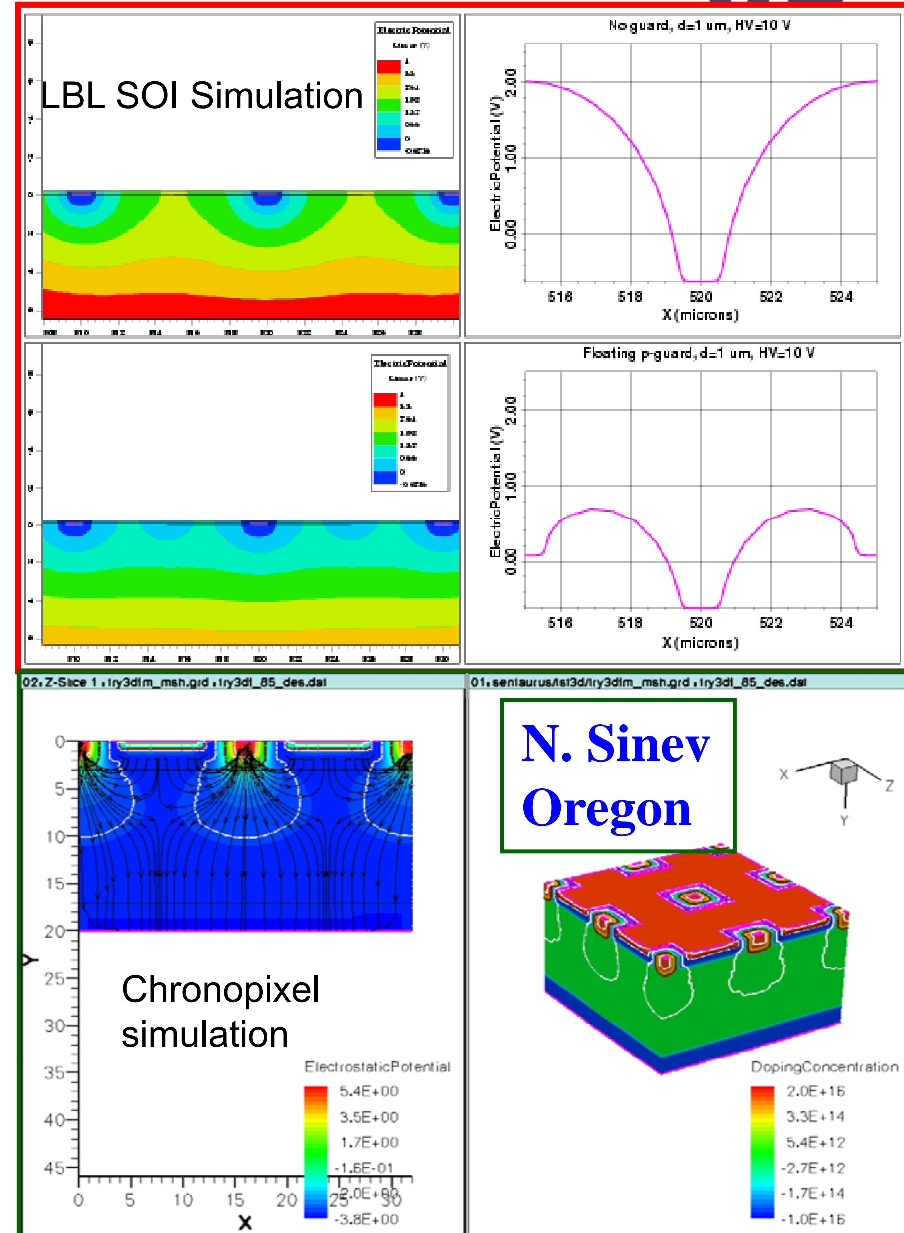


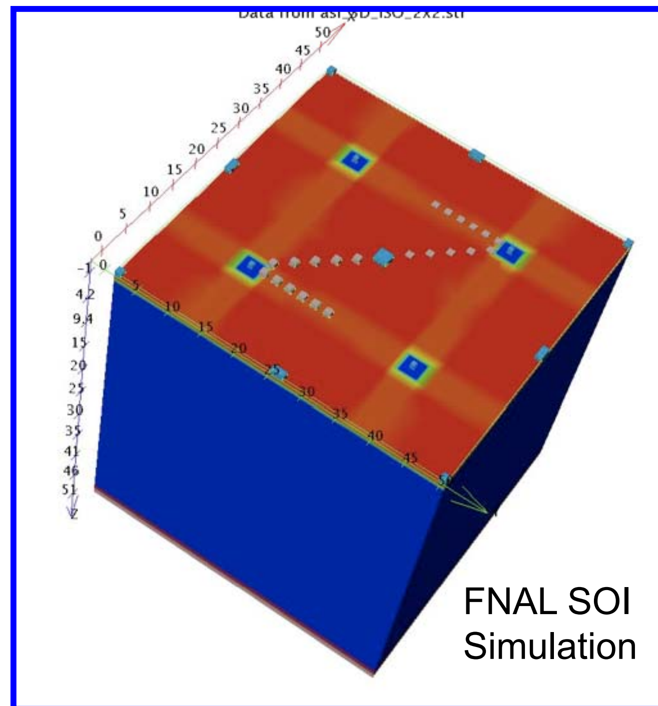


TCAD Simulation

Crucial to understanding sensor tech.

- LBL - back gate effects in SOI
- Oregon - depletion of complex 3D structure
- FNAL analog-digital coupling in SOI

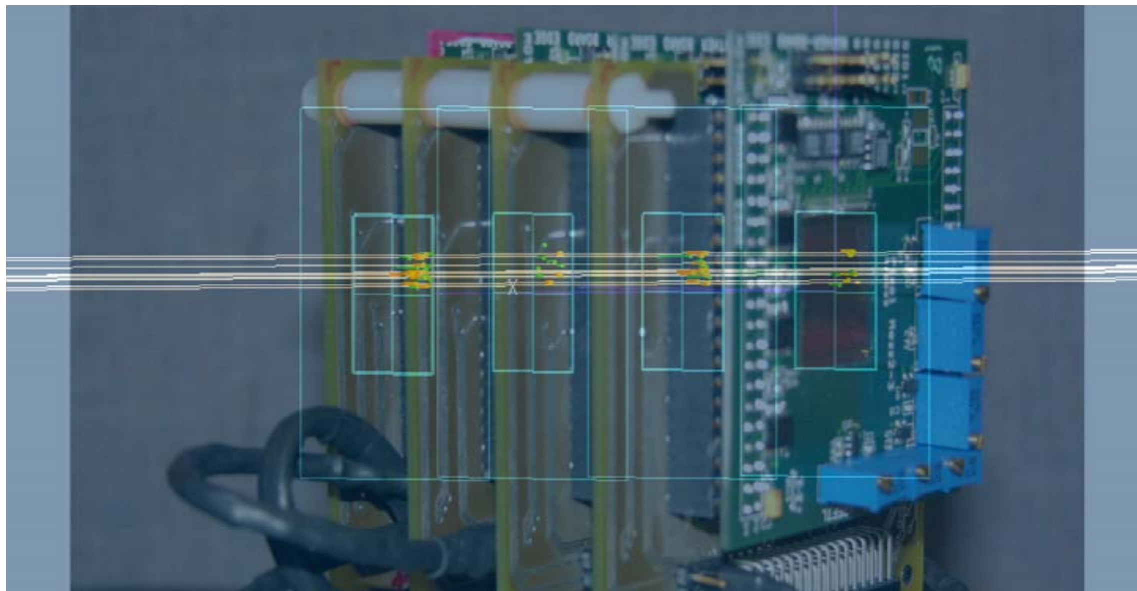


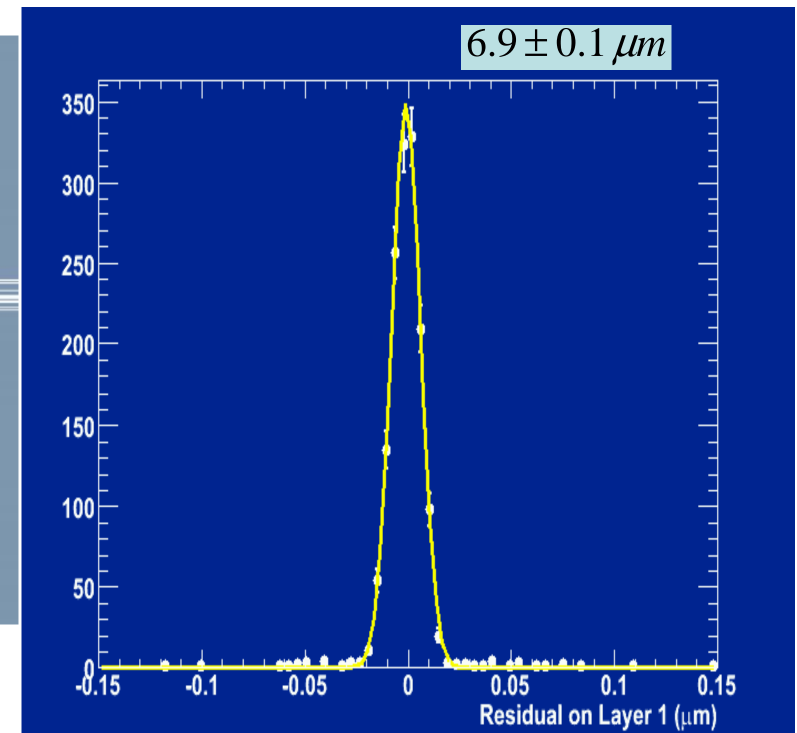


Test Beams

LBL

- The LBNL Thin Pixel Pilot Telescope
  - Layout: 3 layers of thin Mimosa 5 sensors (17μm pixels) (40μm + 50μm + 50μm) + reference detector
- Beam: 1.5 GeV e- from ALS booster at BTS - simulate ILC track density
- First beam telescope based on thin pixel sensors
- Prototype for proposed FNAL MBTF telescope & T966
- System test of multi-M pixel detector in realistic conditions.

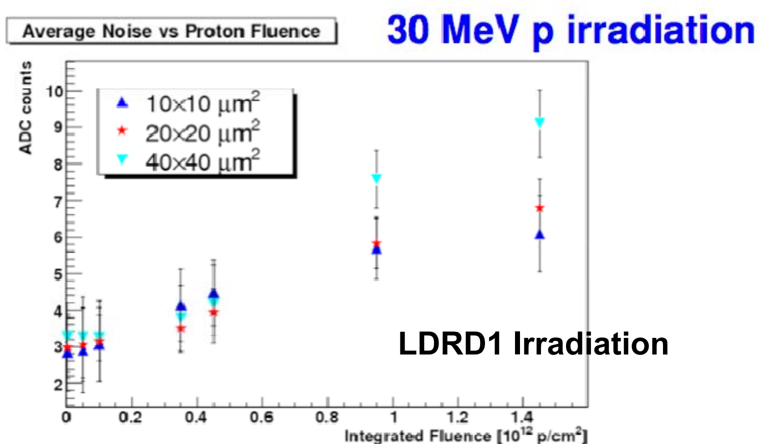


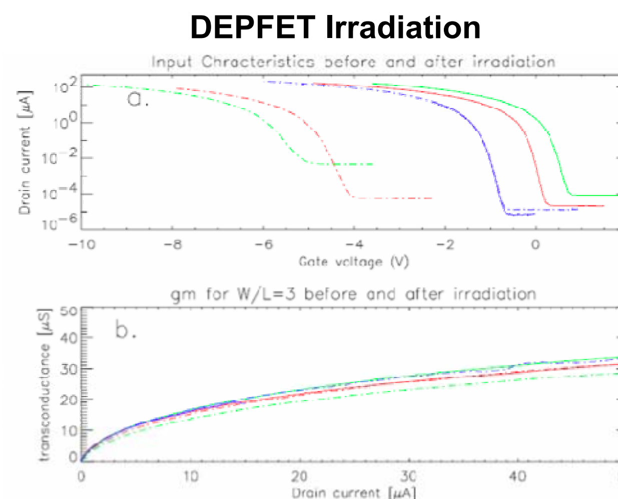


Test Beams and Irradiation

Beam Test at FNAL MBTF 120 GeV p beam-line (T-966) (UC Berkeley /LBNL/INFN Padova/Purdue U Collaboration)

- Deploy two pixel beam telescope:
  - TPPT-2 telescope: 4 layers of 50μm thick MIMOSA-5 sensors,
  - LDRD telescope: 4 layers of LDRD-2 sensors,
  - ILC-like geometry, extrapolation resolution on 1st plane ~ 1mm
- T943 (Varner) - measure CMOS MAPS





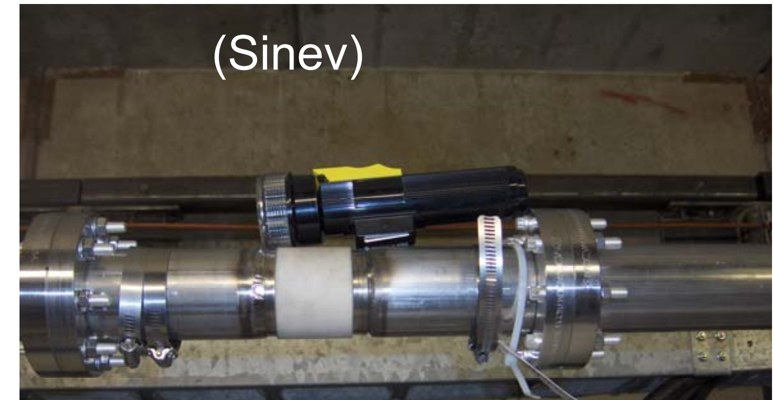
- Radiation Hardness tests @ 88" Cyclotron:
  - 30 MeV p up to 1.45x10¹² p/cm²
  - 1-20 Mev n, no change up to 2x10¹¹ n/cm²

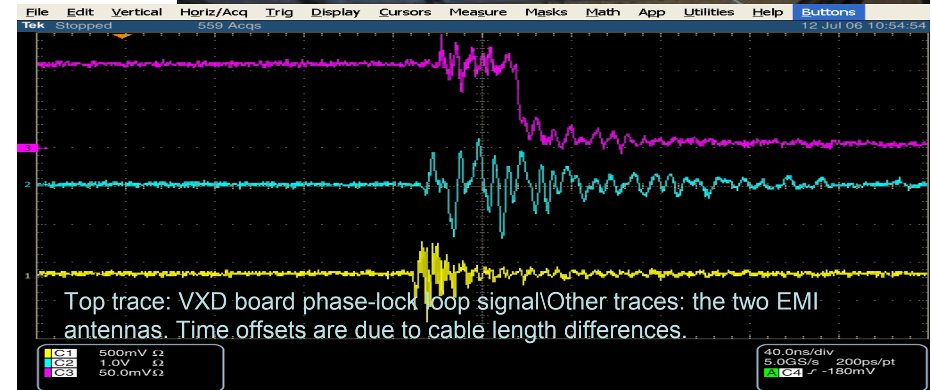
irradiation	TID / NIEL fluence	ΔV_{th}	g_m	I_{Leak} in int. gate at RT(*)
gamma ^{60}Co	913 krad / ~ 0	~-4V	unchanged	156 fA
neutron	~ 0 / 2.4x10¹¹ n/cm²	~ 0	unchanged	1.4 pA
proton	283krad / 3x10¹² n/cm²	~-5V	~ -15%	26 pA

Test Beams - EMI Studies
(SLAC/Oregon)

SLD saw significant electromagnetic interference associated with the SLC beam crossings

- amplifiers saturate, PLL lost lock
- This can have a major effect on vertex (and all electronics) design
  - Better to read out between bunches
  - Avoid active electronics during train





End Station A study of beam-induced EMI

- Antennas placed near (~1 m) gaps observed pulses of EMI in the high MHz range with strengths up to ~20 V/m.
- The pulse amplitudes varied in proportion to the bunch charge, independent of the bunch length.
- A single layer of 5mil aluminum foil placed over the ceramic gap and clamped at both ends reduced the signal amplitude by >x10 (eliminated?)
- A 1 cm hole in the al was enough to cause the PLL to fail, failures stopped at .6 cm

Horizontal and Vertical Collaboration

- Internationally, there are a number of groups focusing on sensor technology
  - Most tend to work independently on each technology
  - Non-US groups had a head start - but we are catching up (passing?)
- These same groups collaborate on more general aspects of the problem
  - General mechanical meetings (FNAL/UW/LCFI/MPI/Valencia/LBL…)
  - Overlapping technologies
    - 3D development at FNAL/MPI
    - SOI development at FNAL/LBL/Japan
    - CMOS MAPs work at LBL/IRES/INFN/…
    - Work on detector concepts - many groups collaborate on SID, LDC vertex design.

All groups feel strongly that promising technologies should continue to be developed until a solution is demonstrated.

There is substantial spinoff potential for X-ray, electron microscopy, imaging and sLHC. Drives many of the overall lab efforts.

Accomplishments

- Mechanical
  - Completed prototype support structures which meet ILC goals
  - Initial studies of ladder design and cooling
  - Design of vertex air cooling within the SiD concept
  - Silicon thinning and handling studies
  - Inter-regional vertex design meetings
  - Measure CF CTE
- Sensors
  - Completed chronopixel design
  - CMOS MAPs test devices (LDRD, CAPs)
  - First SOI-based devices from OKI, SOI design for American Semiconductor
  - First 3D designs
  - Demonstrated laser annealing of thinned sensors
  - *Conceptual sensor designs which meet ILC power, position and time resolution goals*
- Test Beam
  - Improved understanding of EMI sources and effects
  - Built telescopes based on CMOS MAPS sensors
  - Beam tests at ALS
  - Beam tests at FNAL

Near Future Goals

- Mechanical
  - Populate and test support structures
  - Understand sensor flatness requirements and solutions
  - Air cooling studies
  - Study interconnection issues
- Sensors
  - Chronopixel prototype testing
  - CMOS MAPs test devices
  - Test SOI-based devices, second round of SOI submissions, ASI SBIR?
  - Test 3D chips integrated with thinned sensors, second round of MIT-LL chips
  - Complete laser annealing process development
- Power
  - Begin to study serial powering and DC/DC conversion - Serial power chip
  - Study pulsed power design issues
- Test Beam
  - Final round of EMI tests at SLAC
  - Beam tests of prototypes at FNAL

Conclusions

- Although the US community has come into this work later than our European counterparts we are making our mark
  - New technologies (SOI, 3D)
  - Mechanical and infrastructure expertise
  - Increasing sophistication
- We need to maintain this momentum with the next generation of devices going to test beams next year.
- The next steps will include integration of sensor, support, and power delivery technologies aimed at demonstration of prototype modules that meet ILC goals by 2010-2012.

There is great excitement in the US vertex community based on the promise of new vertex detector technologies and ILC physics.
I hope I have conveyed some of this.