The DHCAL DIF and the DIF Task Force

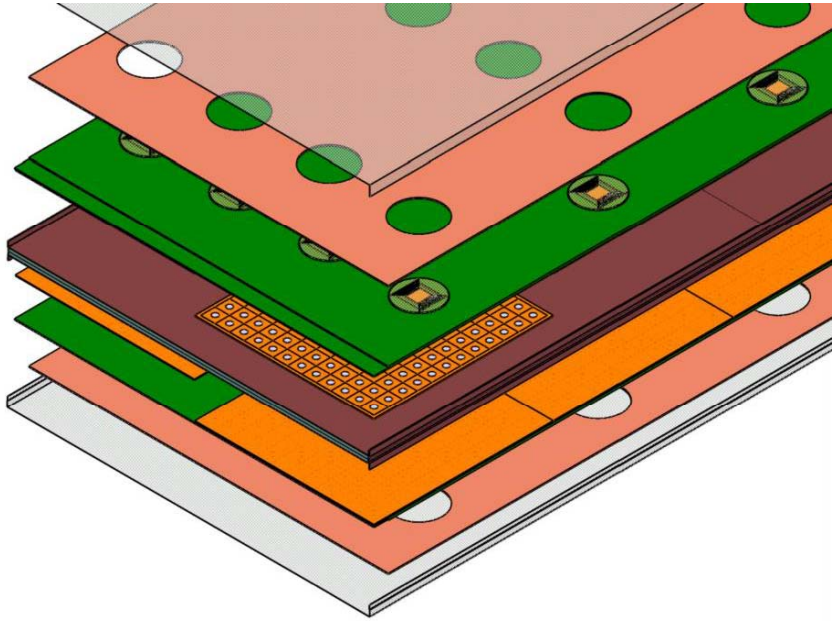
Julie Prast, LAPP, Annecy

The DHCAL board

- First detector with 2nd generation ASICs and 2nd generation DAQ.

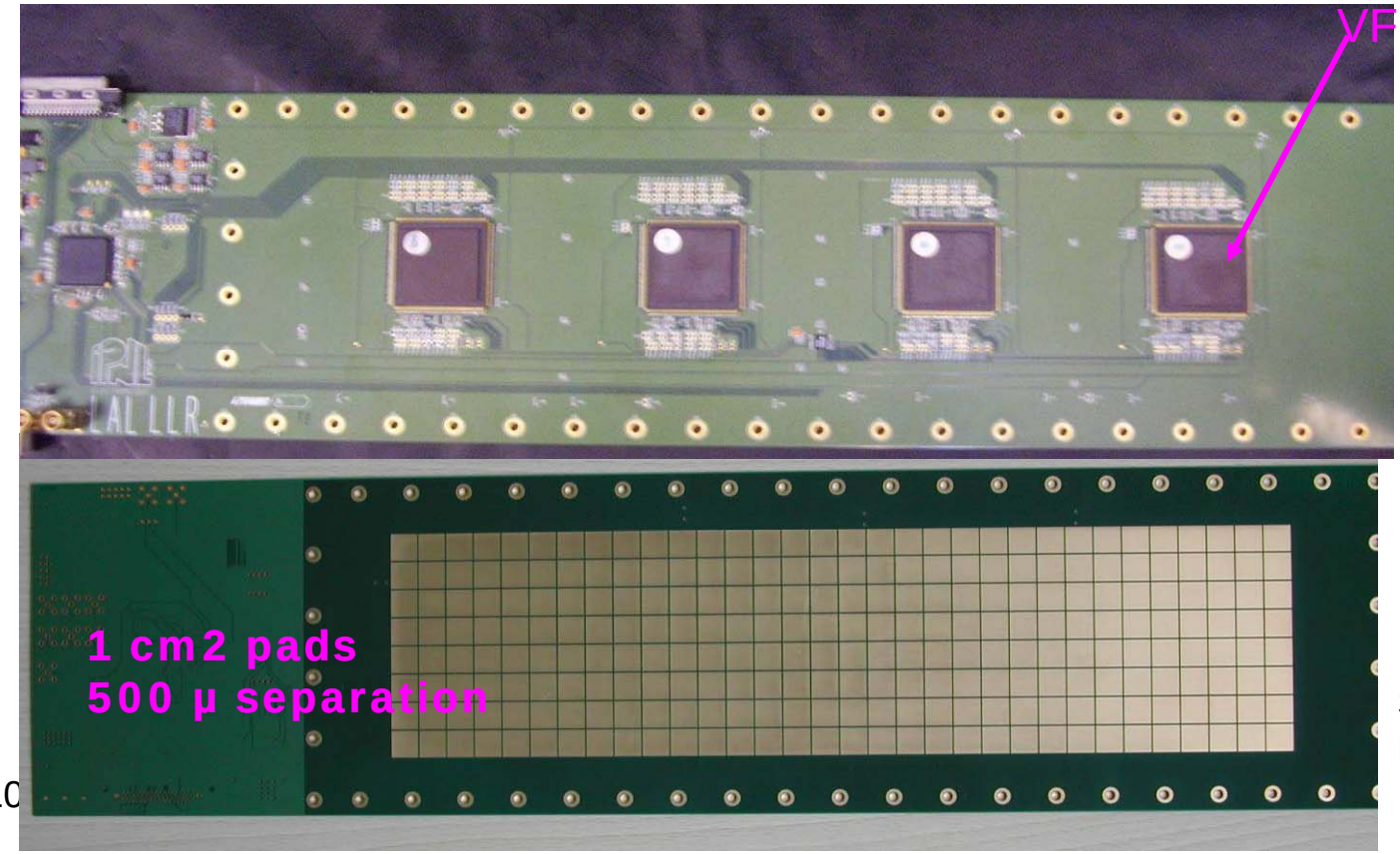
- Front-end ASICs are embedded in detector
  - High level of integration, low PCB thickness
  - Ultra-low power with pulsed mode
- All communications via edge
  - Minimal access and room
- Large scale technological prototype optimized for the ILC concept.
  - Essential to demonstrate detector feasibility

Low Cost and industrialization are the major goals

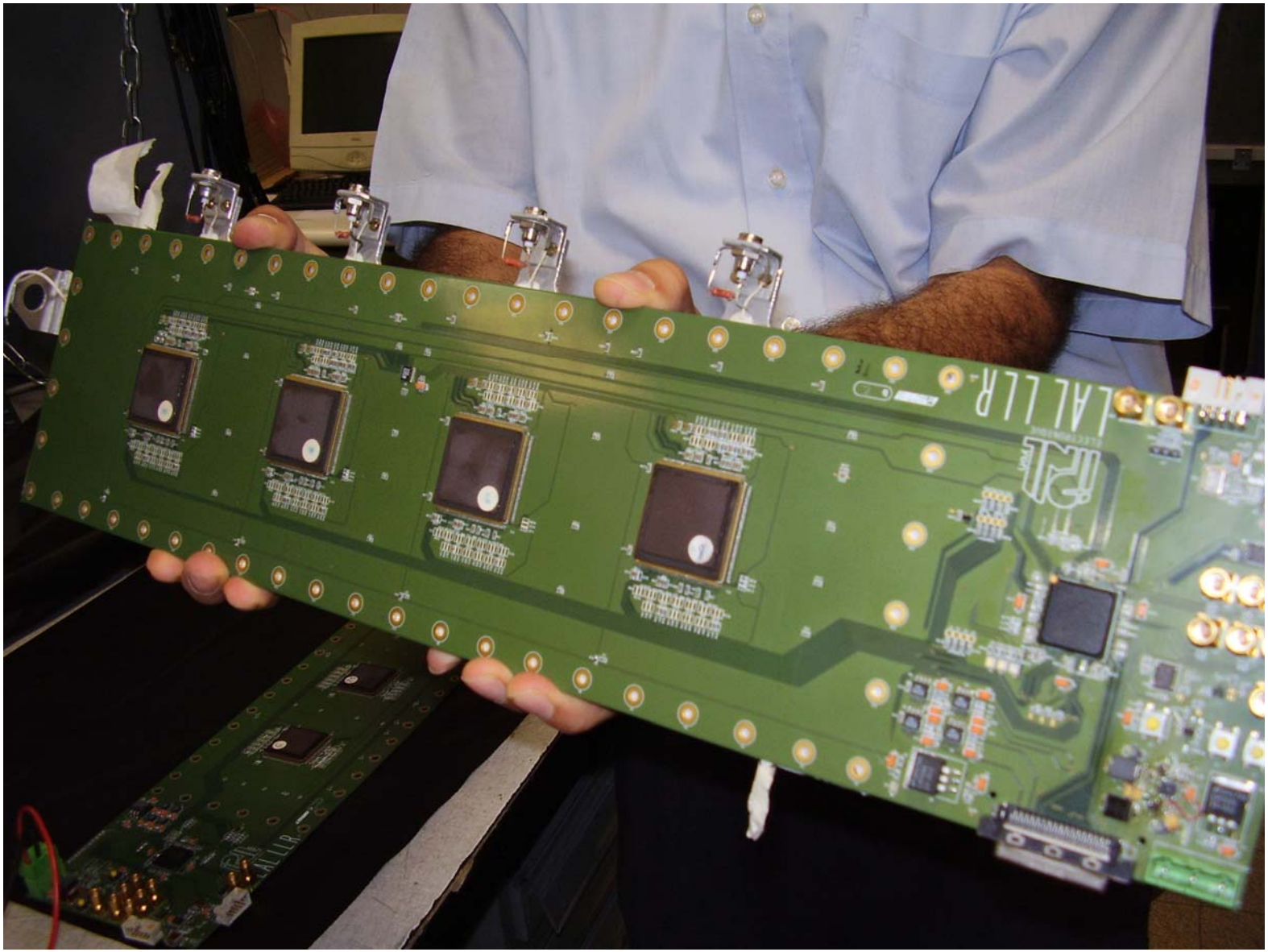


The DHCAL board

- First detector with 2nd generation ASICs and 2nd generation DAQ
  - 8X32 pads RPC detector, 8 layer PCB optimized to reduce crosstalk and compatible with MicroMEGA detector
- Board received in june 07. First tests are encouraging.

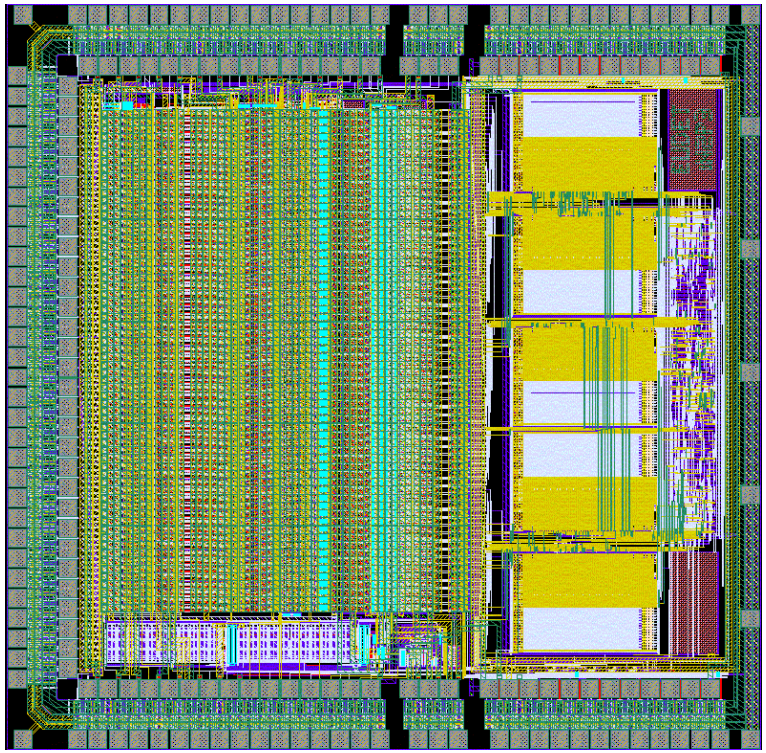


Slide from Imad Laktineh, IPNL


LALLLR

HaRDROC chip for DHCAL

Hadronic Rpc Detector Read Out Chip (AMS SiGe 0.35µm, Sept 06)
LAL IPNL



64 inputs, **1 serial output @ 5 MHz**

•Multiplexed **analog charge output** (debugging)

•**A 128 deep digital memory**: store all channels and BCID for every hit : 20k data transferred during interbunch.

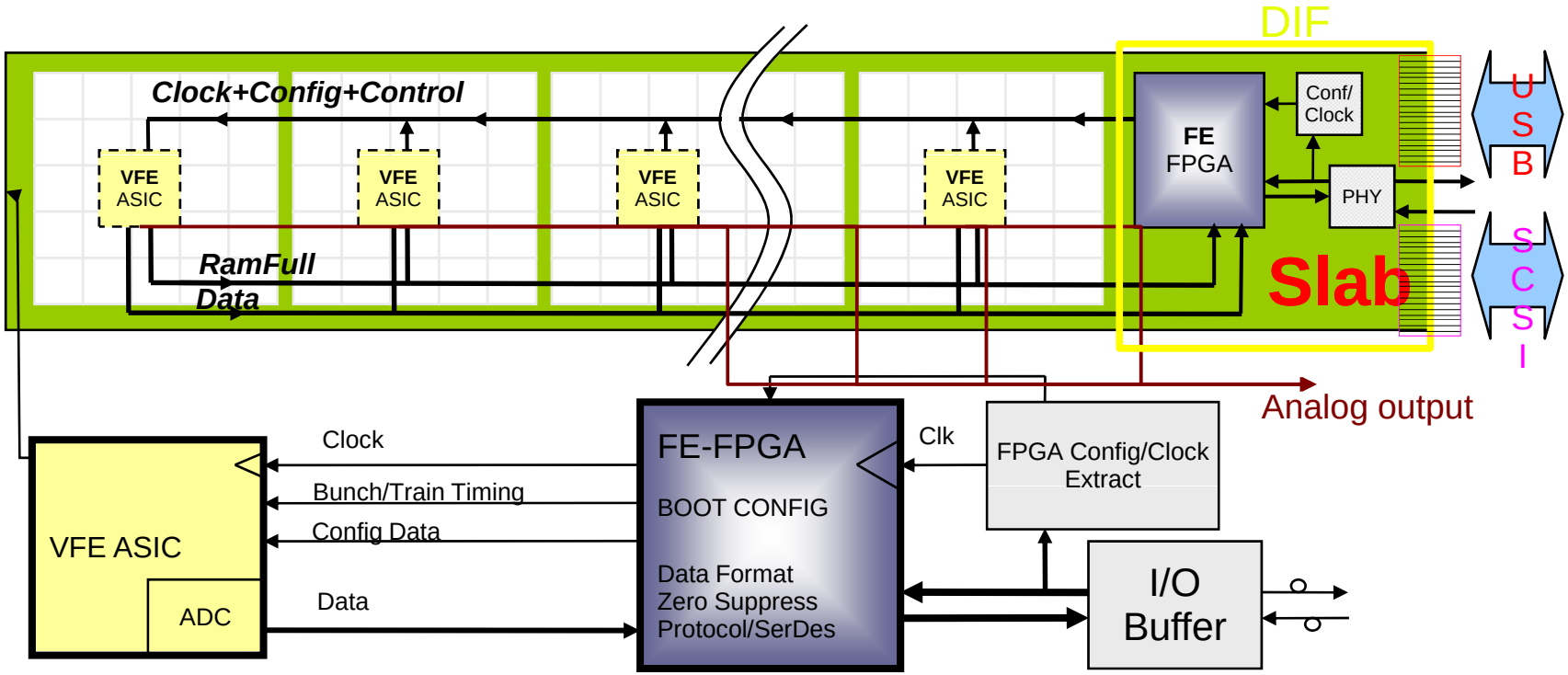
•**ASICs embedded** inside the detector for compactness and **daisy chained** to minimize output lines on the detector.

•**Full power pulsing**

•**1700 chips** to be produced in 2007 for **1m^3 DHCAL prototype**.

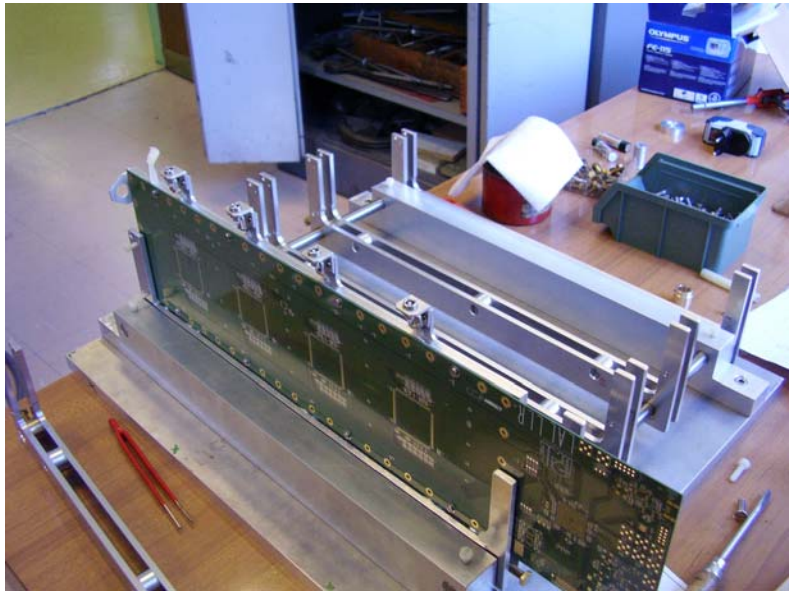
HaRDROC digital part

- Chips are embedded and daisy chained to minimize number of output lines on the detector.
- FPGA based readout
- DAQ communication through USB



Next steps

- Perform cosmics test at Lyon and beam test at Desy this fall.
  - Using both RPC and MicroMega detectors
  - Setup: Almost done with the possibility to host few detectors
- Build a large area detector (>1m2) with an extensible scheme
  - Separate Slab and DIF for more flexibility
  - Stitchable PCBs to get long structure
  - Work in collaboration with the DIF task force



Setup for the Cosmics and beam tests

DIF Task Force

- Many similarities between the 3 subdetector ASICs (SPIROC, SKIROC, HARDROC) and between the 3 DIFs.
  - The 3 ASICs have been mostly developed by LAL and have a lot of common features, in particular the digital interface :
    - Daisy chain, power pulsing, …
  - DIFs have also some identical functions:
    - Slow control, readout, interface with the DAQ, …

- To avoid duplication (triplication) of work, a small working group of 4 people has been created, with one people from each subdetector and one from the DAQ :
  - Remi Cornat (Clermont) : ECAL
  - Mathias Reinecke (DESY) : AHCAL
  - Julie Prast (Annecy) : DHCAL
  - Bart Hommels (Cambridge) : DAQ

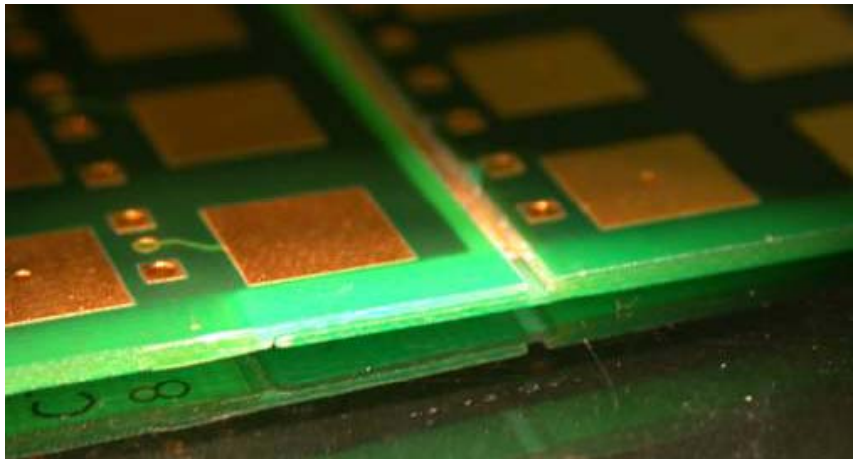
- We will work in collaboration with all the people working on the different subdetectors, on the DIF or on the DAQ.

Aim of the task force

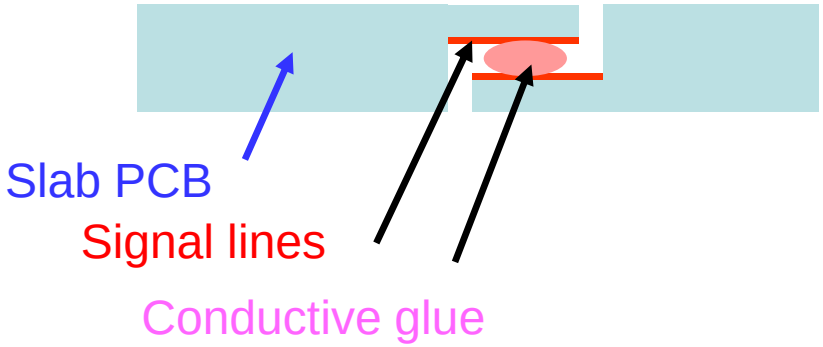
- Define the interface between SLABs and DIF
  - Connector pinout
  - Electrical signals and levels
  - Underlying what is common and detector specific
- Define the DIF architecture : common blocks and detector specific blocks, interface to DAQ and USB.
- Define the slab to slab interface.
- Define common VHDL libraries.
- Try to standardize developments (Altera, Xilinx, …)

- Summarize everything in a common document for the end of this year.

SLAB Long Structure



ECAL PCB



- Which technique to get the long structure (2 m) ?
- Gluing as for ECAL ?
- Other scenario ? See C. Combaret's Prague's talk
- Aim : manufacture standard sized PCBs : lower cost designs

- The SLAB/SLAB interface will be an essential parameter for the definition of the SLAB/DIF interface as it will impact the number of signals to consider.
  - Max 4 etches / cm ?

Pictures from Peter Göttlicher, DESY

Towards a generic SLAB/DIF interface

Category	Signal	Function	I/O for slab	Validation	ECAL (SKIROC)	DHCAL (HARDROC)	AHCAL (SPIROC)
operation control							
	reset*	global reset of complete ASIC	I	low	LVCMOS	LVCMOS	LVCMOS
	RST_counter	Reset for the BCID counter	I	high	LVCMOS	LVCMOS	LVCMOS
	Digital_pwr_on	power-cycling control for the digital part	I	high	LVCMOS	LVCMOS	LVCMOS
	Analog_pwr_on	power-cycling control for the analog part	I	high	LVCMOS	LVCMOS	LVCMOS
	DAC_pwr_on	power-cycling control for the DAC part	I	high	LVCMOS	LVCMOS	LVCMOS
	ADC_pwr_on	power-cycling control for the ADC part	I	high	LVCMOS		LVCMOS
	StartAcqt	start data acquisition	I	high	LVCMOS	LVCMOS	LVCMOS
	start_conv_DAQ	start ADC conversion	I	high			LVCMOS
	no_trig	erase active analogue column	I	high			LVDS
	Val_Evt	external validation of event	I	high	LVDS	LVDS	LVDS
	trig_ext	external trigger	I	high	LVCMOS	LVCMOS	LVDS
	RAZ_Chn	reset for internal RS flip-flops (discriminator outputs)	I	high	LVDS	LVDS	
slow control							
	clk_sc	slow-control shift-reg. clock 1MHz	I	rising	LVCMOS	LVCMOS	LVCMOS
	srin_sc (D_SC)	data input of slow control shift-reg.-chain	I	high	LVCMOS	LVCMOS	LVCMOS
	srout_sc (Q_SC)	output of slow-control shift-reg.-chain	O	high	LVCMOS	LVCMOS	LVCMOS
	load_sc	latch-command for slow control data	I	high			LVCMOS
	srin_sc_byp	bypass input of slow-control reg.	I	high			LVCMOS
	srout_sc_byp	bypass output of slow-control reg.	O	high			LVCMOS
readout							
	start_readout	token input of resul data	I	high	LVCMOS	LVCMOS	LVCMOS

From Mathias and the Task Force group

Towards a generic SLAB/DIF interface (2)

		readout					
	end_readout	token output of result data readout	O	high	LVCMOS	LVCMOS	LVCMOS
	CK_5M	5MHz/1MHz clock readout	I	rising	LVDS	LVDS	LVDS
	CK_40M	40MHz clock for state machine	I	rising	LVDS	LVDS	LVDS
	TransmitOn	data readout is active	O	high	open coll	open coll	open coll
	Dout	output of result data	O	high	open coll	open coll	open coll
	SCASat	analogue pipeline full	O	high			open coll
	RamFull	digital RAM full	O	high	open coll	open coll	
	RamFull_ext	stops current acquisition if an HC RAM is full	I	high		LVCMOS	
	bypass_in	bypass for token signal for readout	I	high			LVCMOS
	bypass_out	bypass for token signal for readout	O	high			LVCMOS
debugging							
	hold_ext (hold)	external channel trigger	I	high		LVCMOS	LVDS
	clk_probe (clk_R)	debug register clock	I	rising		LVCMOS	LVCMOS
	srin_probe (D_R)	readout probe reg. input	I	high		LVCMOS	LVCMOS
	srout_probe (Q_R)	readout probe reg. output	O	high		LVCMOS	LVCMOS
	srin_read	operates the analogue debug outputs	I	high			LVCMOS
	srout_read	read register chain output	O	high			LVCMOS
	flag_tdc_ext	debug: external charge or time SCA select command	I	high			LVCMOS
	start_rampb_¶ adc_ext	debug: external start signal for ADC ramp	I	low			LVCMOS
	start_ramp_tdc_ext	debug: external switch 'Ramp1 to Ramp2' signal	I	high			LVCMOS
	analog_output (Out_q)	SCA analogue test output	O	-	analogue	analogue	analogue
	analog_probe_output	analogue test output	O	-			analogue
	digital_probe1	digital probe output (debug)	O	high	open coll		open coll
	digital_probe2	digital probe output (debug)	O	high			open coll

From Mathias and the Task Force group

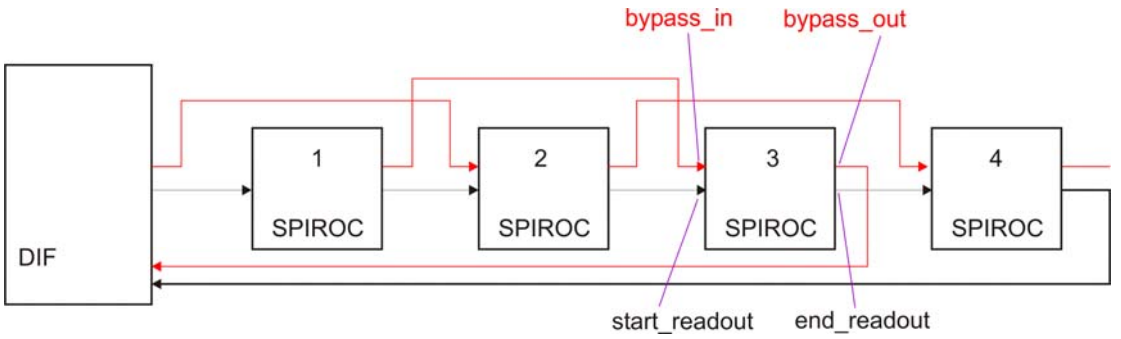
Towards a generic SLAB/DIF interface (3)

	Spare1						
	Spare2						
	Spare3						
	Spare4						
Power							
	positive supply	+3.5V (digital + analog)	I	-	power	power	power (?)
	Analog power supply	+3.5 V	I			power	
	additional supply	+5V (DAC)	I	-			power (?)
	common ground	GND	I	-	power	power	power (?)
	detector bias	HV	I	-	power	power	power (4)
Calibration and Monitoring							
	Sensor_Power	Power for temperature monitors	I	-			power (1)
	Temp	output of temperature monitors	O	-			analogue (6?)
	Trigger_Power	power for trigger logic	I	-			power (2)
	Charge_Power	power for charge injection circuits	I	-			power (2)
	LED_Power	power for light calibration system	I	-			power (2)
	VCALIB	analogue level of calibration signal	I	-			analogue (1)
	Trigger	fast trigger of calibration system	I	rising			LVDS
	CTest	charge injection	I	-	analogue	analogue	

From Mathias and the Task Force group

SLAB/DIF interface: Main questions

- **Low power:**
  - 4 Power cycling signals**:** DAC, Analog, ADC, digital.
  - Use token for digital PS to switch off the preceding ASIC in the readout chain.
  - No clock during interbunch.
- **Reset signals:** merge all ?
  - Slow control and BCID resets to be discussed.
- **Clocks**: generate the 40MHz clock from the 5MHz clock with a PLL ?
- **External trigger** has priority to the internal one during calib and test.
- **Reliability of the daisy chain**
  - Add signals to strap one asic in case one is broken ?



Scheme from Mathias Reinecke

- **Mechanical aspects :**
  - Number of connections, Density of the connector, Low height connector, reliability

Conclusion

- DHCAL is the first detector with 2nd generation ASICs and 2nd generation DAQ.
- Next steps are beam test and 1 m^2 prototype.
- New developments in particular on the DIF architecture and SLAB to DIF interface are done conjointly with the DIF working group.
  - Already some progress on the Slab to DIF interface (see previous tables)
  - Slab to Slab interface is an important parameter.
  - Inputs are very welcome.