MANCHESTER 1824

The University of Manchester

LDA and DIF Link

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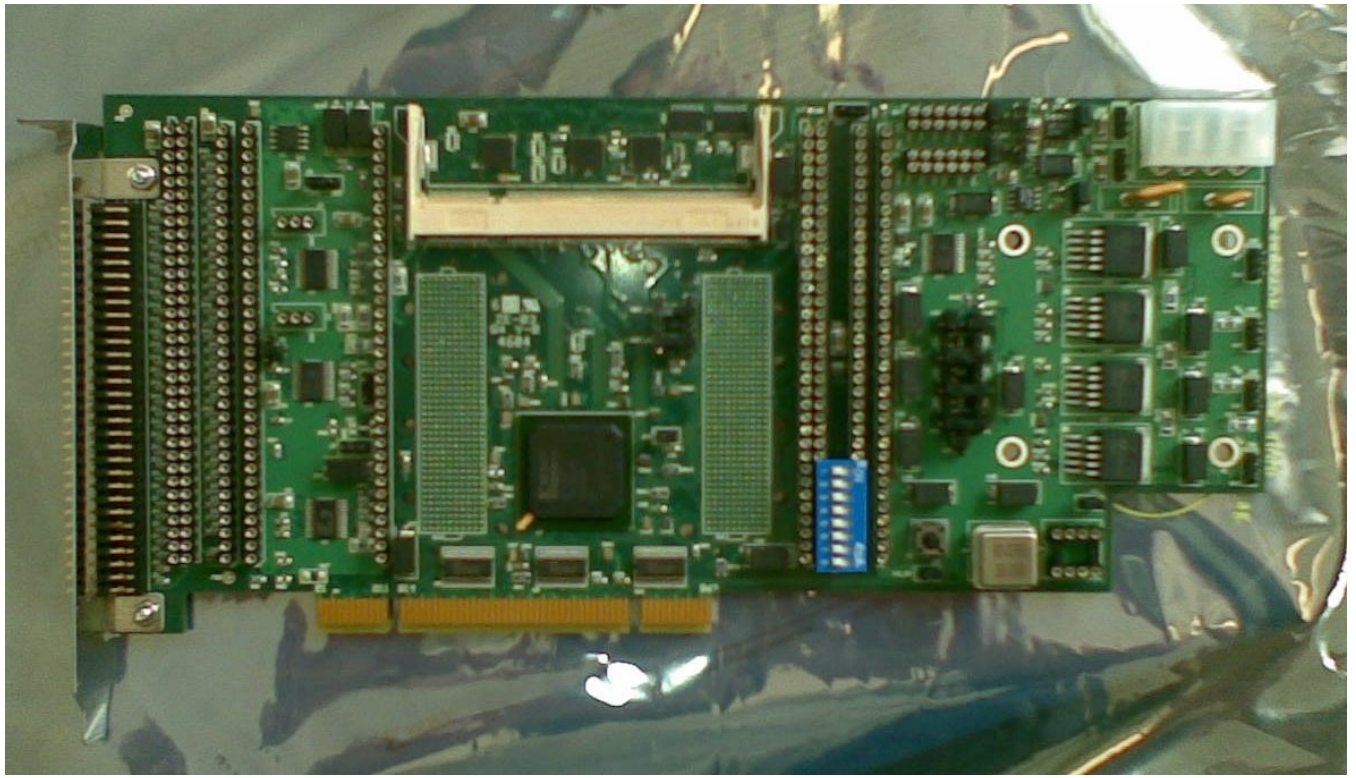
Prototype LDA Design

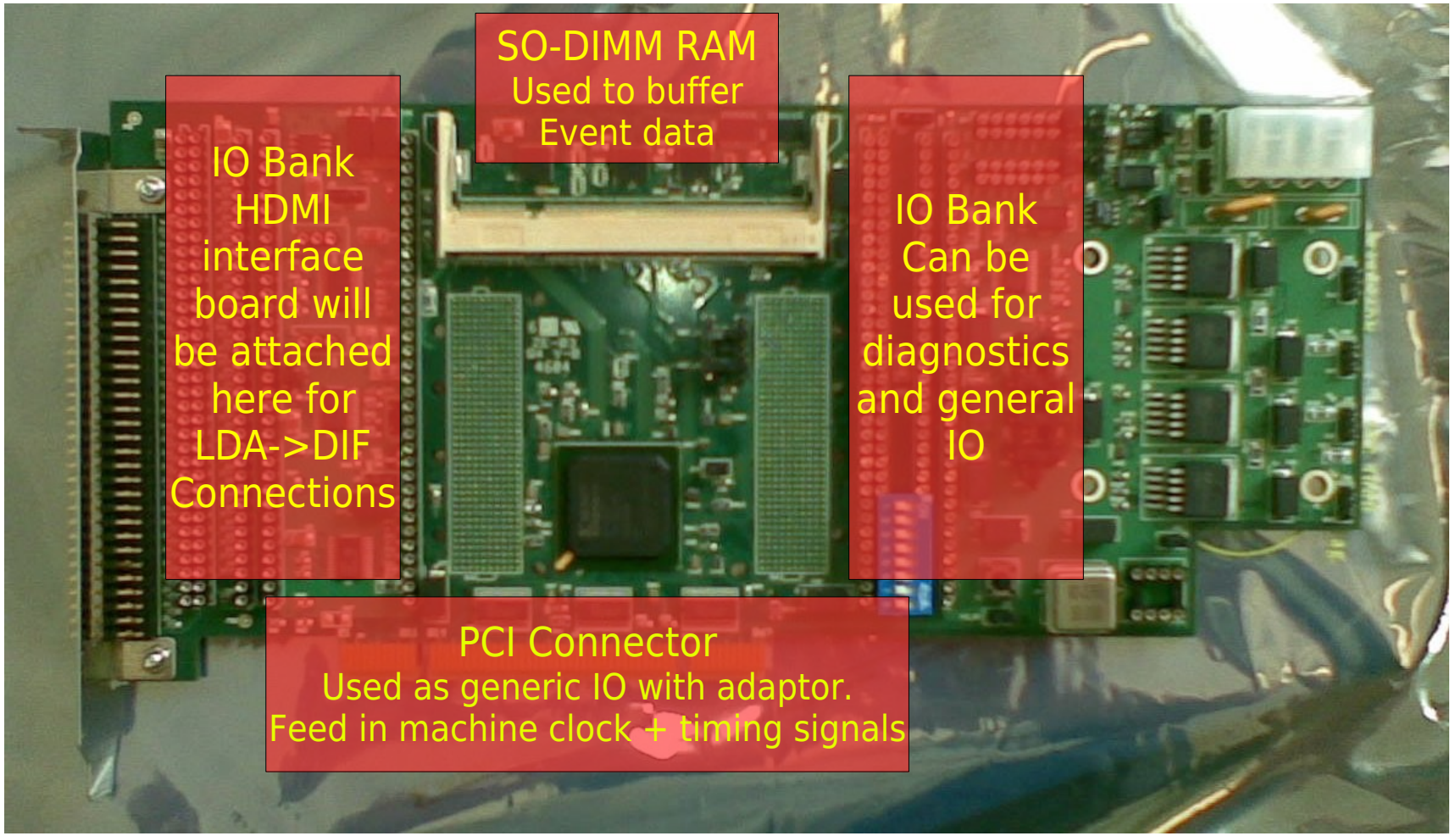
Based on a commercial Spartan 3 FPGA development board. S3-2000 FPGA installed.



Board has DDR2 SO-DIMM socket, allowing us to install ram for event buffering.
The size of the ram needed is currently not determined.

External IO to be used to drive add-on boards for LDA-DIF and LDA-ODR links. Spare IO to be used for debugging and also for a possible Clock & Control input into the system.

Add-on boards (Front)



Prototype LDA Design

- *LDA-DIF* link.
  - Will use HDMI based system.
  - Type-A connectors, as used in HDTV. Consists of 4 sets of twisted pairs, plus some control lines, in a nice easy to use format.
  - Available in various lengths. 2m is ~4 GBP. Up to 20m available reasonably cheaply.

  - Designed to handle data rates of ~350 Mbits/sec per pair in HDMI 1.3 Spec.

LDA-DIF Link details

- 1 TX pair for "Machine Clock". (Expected Freq?)
- 1 TX pair for LDA -> DIF data.
- 1 RX pair for DIF <- LDA data.
- 1 TX pair for Control channel.
- 1 RX pair for slow monitoring/misc side band data. (This pair is NOT designated a high bandwidth pair in the HDMI spec. SAMTEC makes cables where this pair is UTP however. Tests with off the shelf HDMI cables need to be done.)
- TX and RX data is expected to be Encoded with 8B/10B or similar balancing scheme.
- Clock recovery is not expected to be used in the current prototype, a multiple of the "Machine Clock" will be used to clock the data.

LDA-DIF Link details

- LDA design will have 10 HDMI connections on it, giving fairly good connectivity.
- It is know that people were asking/expecting ~20-30, however for this quick prototype we been limited by time and engineer effort.
- To run larger detectors, use more than 1 LDA.
- A cheap/quick way envisioned for this is to use a passive PCI backplane and use that to feed clock & control signals into ~5-6 LDAs.
- A method to do this via the ODR link will be investigated as well.
- Future redesigns of the LDA could have more DIF links, but these would be 100% custom designs, costs and required numbers need to be considered.

Add-on boards (Back)

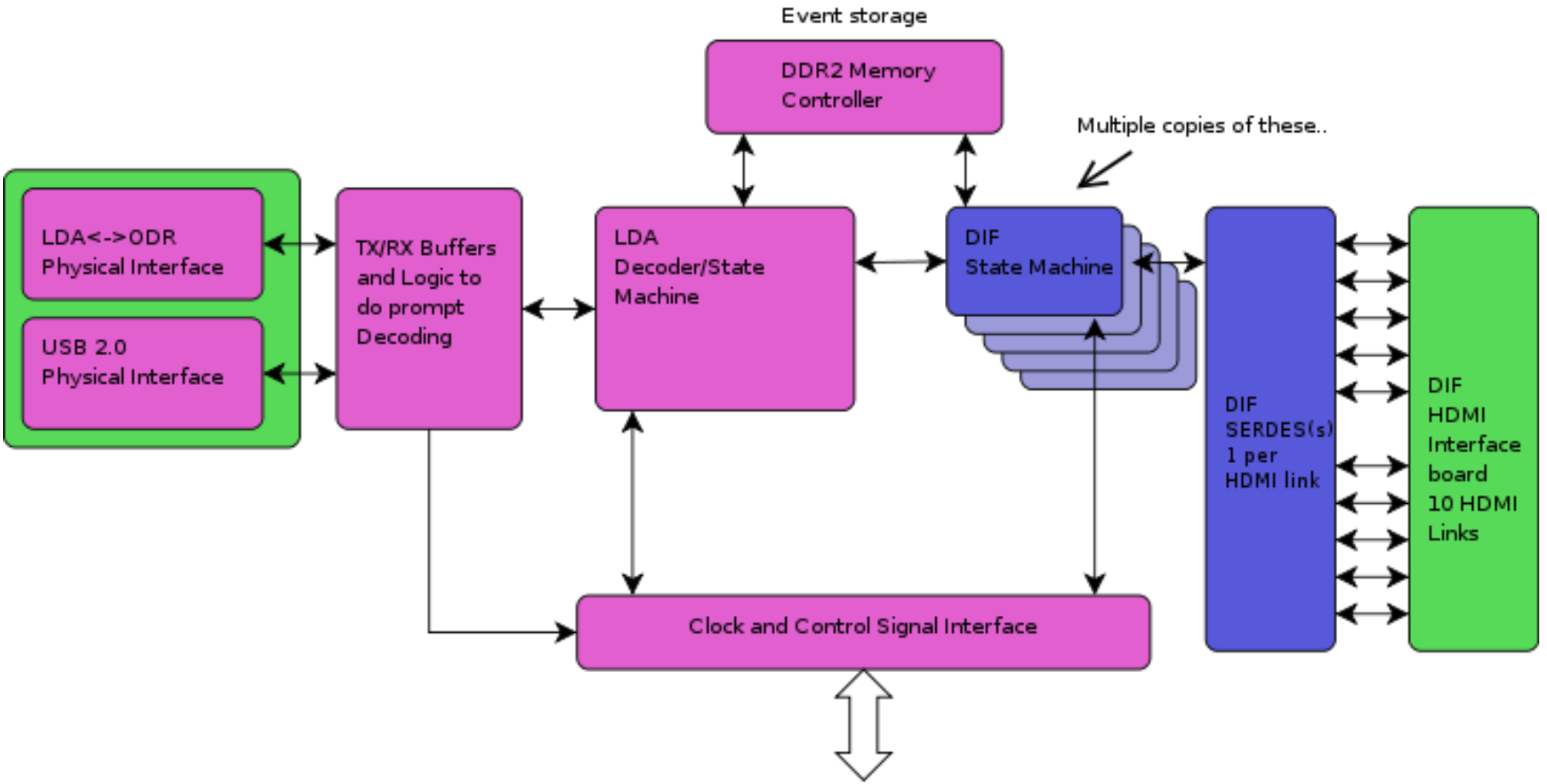
Prototype LDA Design

- *LDA-ODR* link has two current options. Both via SFP cages, allowing choice of fibre or cable.
  - **Gigabit Ethernet**. This has been tested and demonstrated to be easy to achieve with FPGAs. It is cheap, and can be fed into a switch to aggregate multiple LDAs output into a single ODR. However has issues for clock and control uplink from ODR, due to variable latency etc.
  - **TLK 2501 chipset**. Used in a lot of DAQ equipment, is a generic 16:1 SERDES chipset that uses 8B10B encoded data streams to work at 1.25 -> 2.5 Gbit/sec. Has better, more controllable latency, and a link with this could do both data and clock & control.

Prototype LDA Design

- *USB* interface
  - Intend to provide some kind of USB interface that allows testing and debugging of the LDA+DIF without the use of an ODR.
  - The plan is to duplicate the functionality of the ODR link as much as possible from the software's point of view.
  - Seen as a method of bench testing multiple DIFs using a single LDA using a generic laptop/desktop PC.
  - The chipset to be used is the **Cypress CY7C68014**.

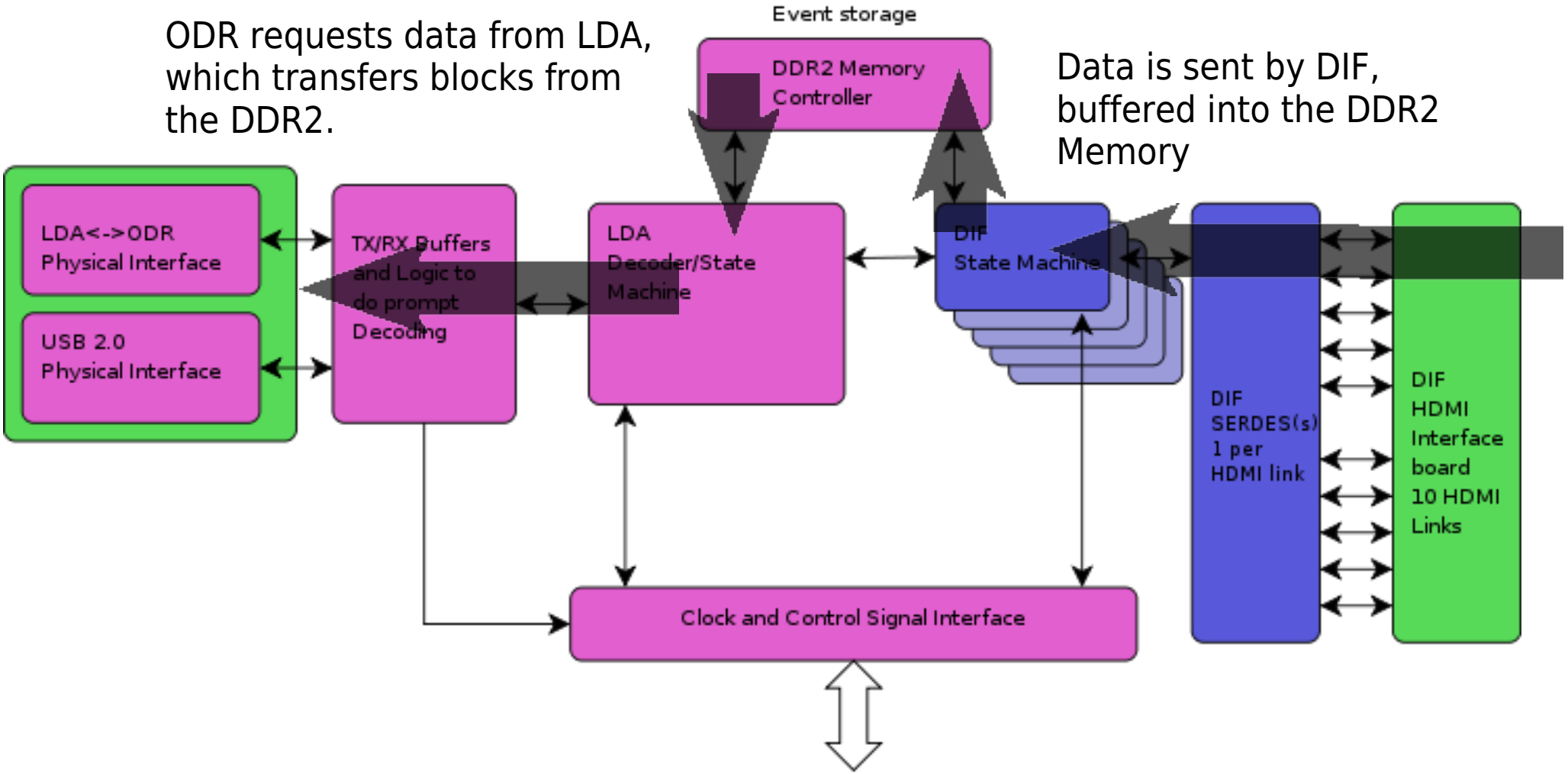
Rough first pass at some form of diagram



Data Path for Event Readout

ODR requests data from LDA, which transfers blocks from the DDR2.

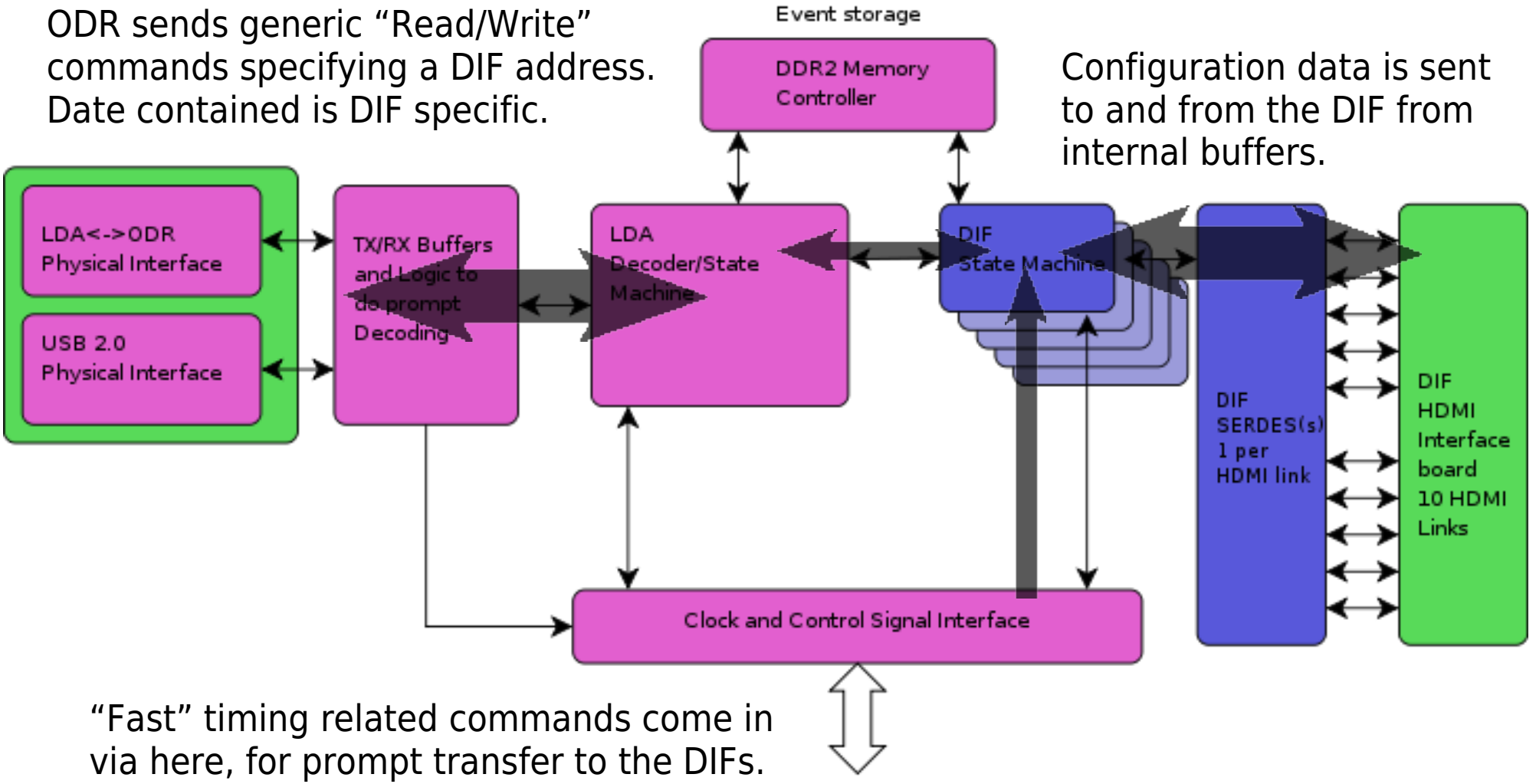
Data is sent by DIF, buffered into the DDR2 Memory



Control and Configuration Path

ODR sends generic “Read/Write” commands specifying a DIF address. Date contained is DIF specific.

Configuration data is sent to and from the DIF from internal buffers.



“Fast” timing related commands come in via here, for prompt transfer to the DIFs.

LDA Status (Hardware)

- Hardware has been quoted for by an external company, comes to about 140 GBP for the HDMI interface, and 400 GBP for the Gigabit interface. You can convert that to EUROS based on what ever the exchange rate is. Carrier Board (BroadDown2) is ~150-300 GBP's based on which Spartan3 size is required.
- Delivery of first prototypes is 4-6 weeks for design and a further 4-6 for production. Delivery by end of year is possible.
- Ordering 10 HDMI and 5 GigEthernet.
- Further BroadDown2 carrier boards are in stock, and available at fast turnaround.
- Would be nice to know how many LDA-DIF and LDA-ODR boards would be required in next 3-6 months.

LDA Status (Firmware)

- Need to fill in all the blocks from previous diagram.
- Work has been done on the initial LDA-DIF SerDes blocks, these will be used to do basic HDMI cable bit error testing once the first boards arrive.
- It is anticipated that the firmware is not overly “smart”. It does not inspect any of the data going to/from the DIF. Just does “packet” transfer to get the data to/from place to place.
- Event readout based on packets, where the DIF(s) send data tagged with an Identifier. The LDA buffers these and does a basic sanity check for sequences.
- The ODR can request event status and request the data blocks needed.