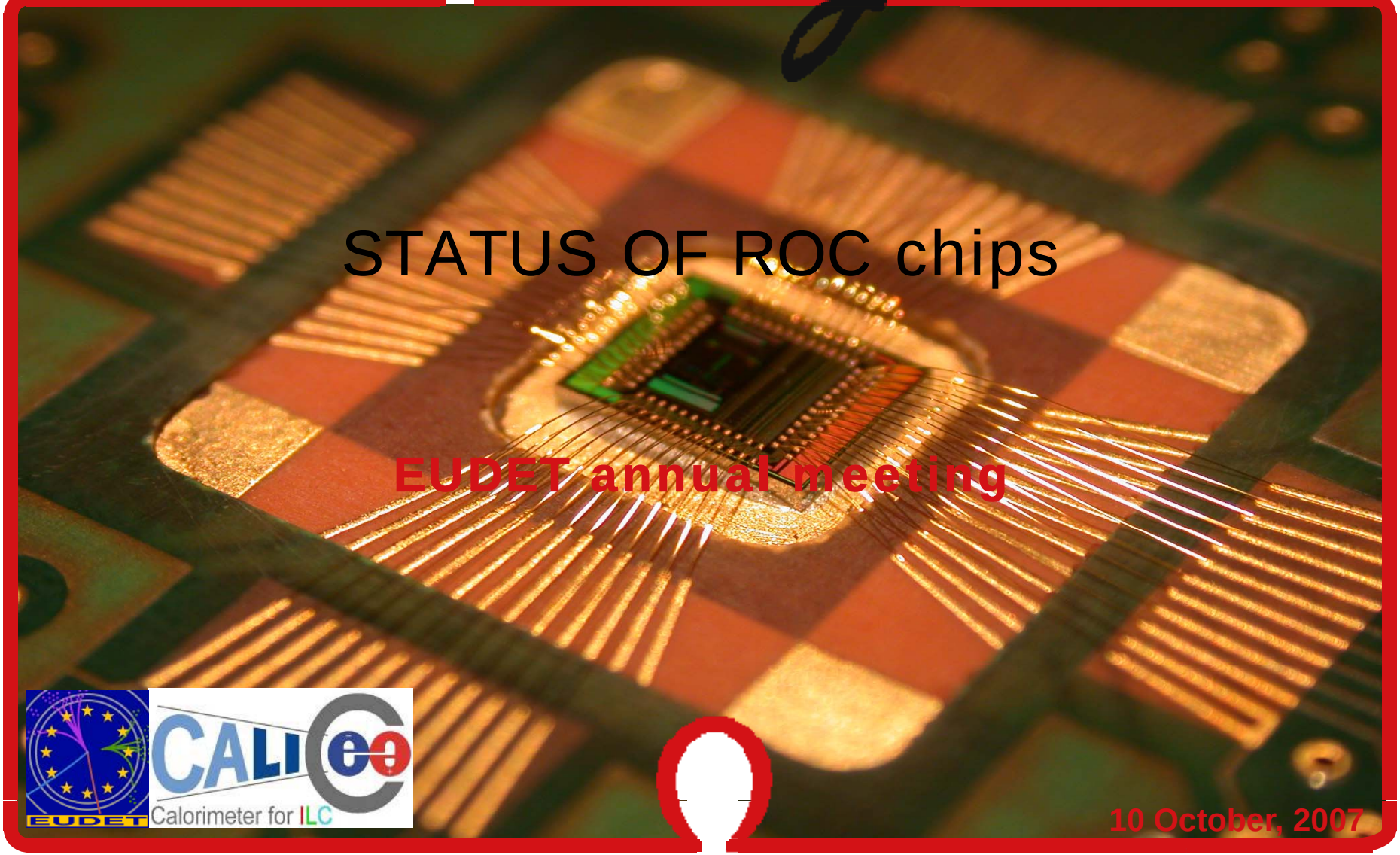
IN2P3

Omega

LAL LPNHE

STATUS OF ROC chips



EUDET annual meeting

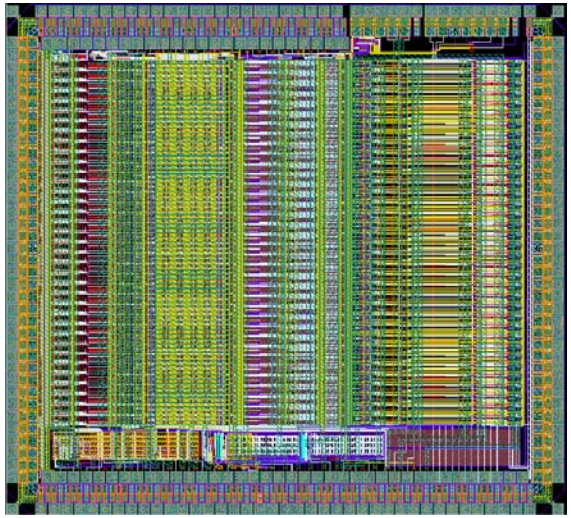
EUDET Calorimeter for ILC

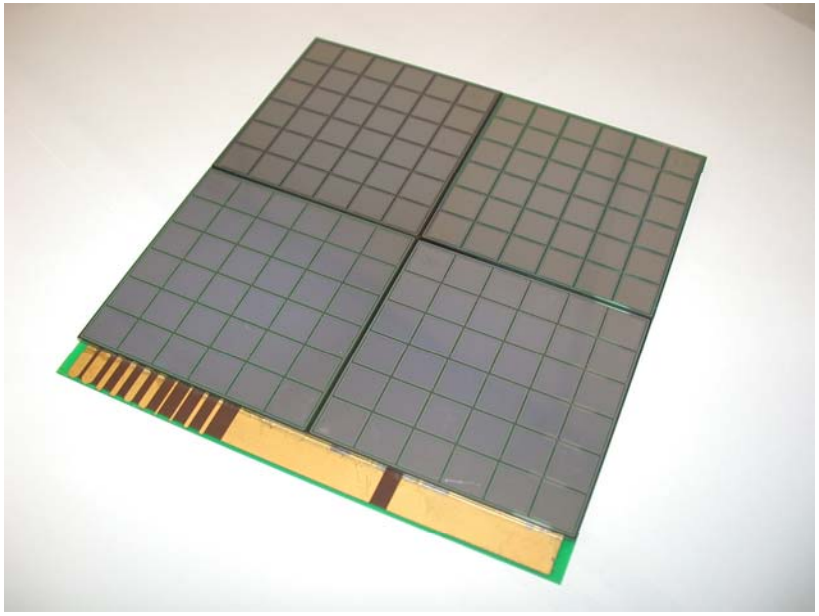
10 October, 2007

Orsay MicroElectronic Group Associated

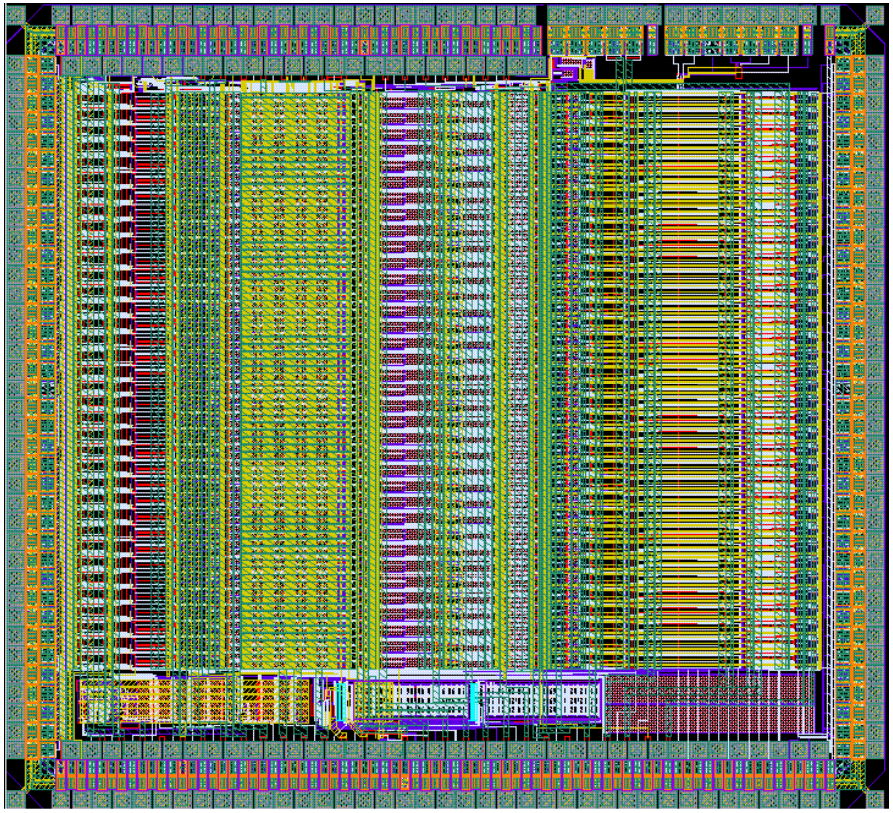
Plan

- ECAL : Skiroc presentation
  - A brief reminder
  - Preliminary results
- DHCAL : Hardroc status
  - The daisy chain read out
  - The power pulsing meas.
- AHCAL : Spiroc status
- Schedule & conclusion

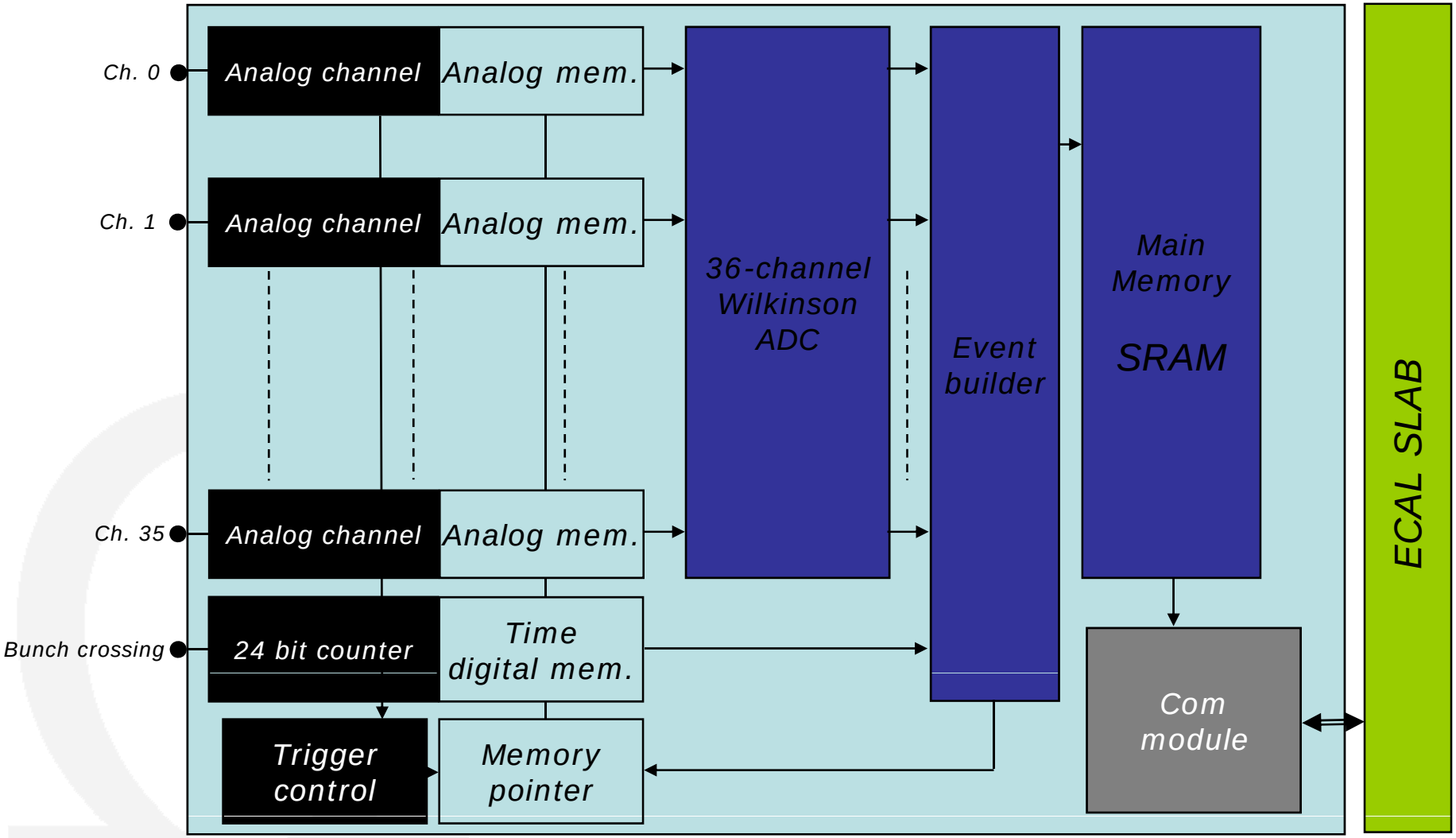




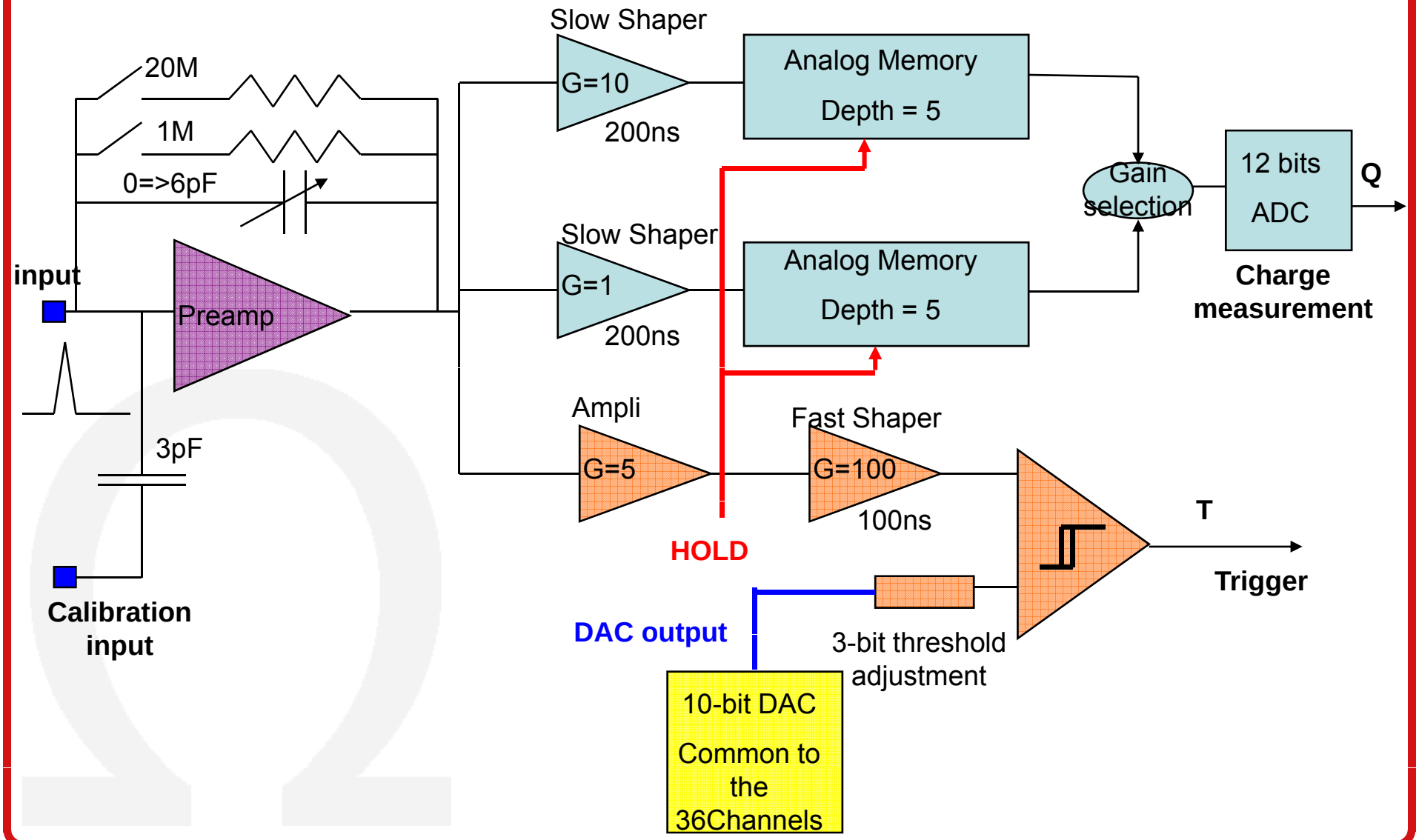
SKIROC STATUS



Reminder : Block scheme of SKIROC



Reminder : One channel



SKIROC : tested features

Preamplifier

- Preamp disable (DC coupled channel OFF – leakage to supply)
- Preamp low Rf (DC coupled degrated mode)

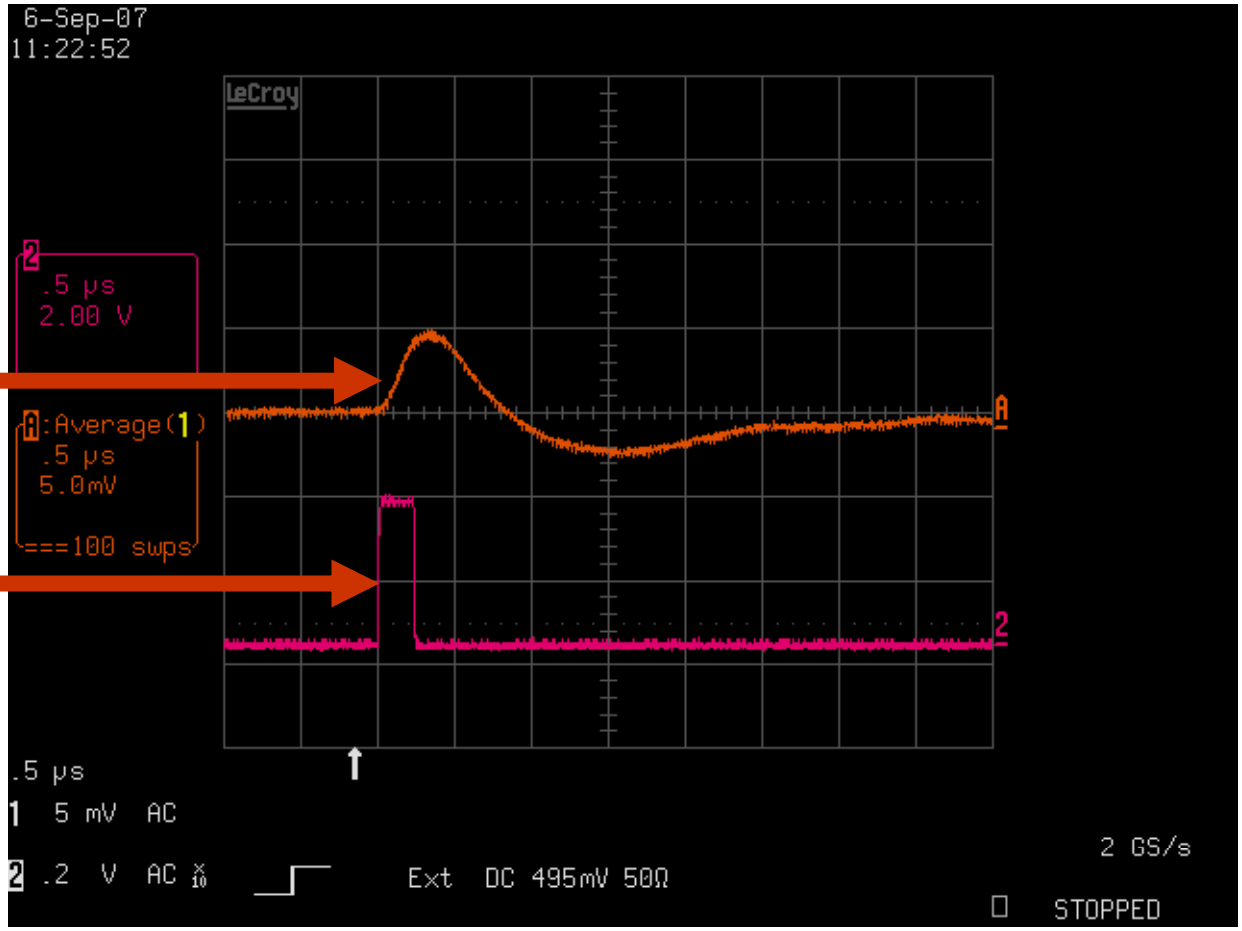
- Auto-trigger
  - Self trigger on a MIP observed in measurement

- Power pulsing
  - Programmable stage by stage
- Calibration injection capacitance
- Embedded bandgap for references
- Embedded DAC for trig threshold
- Serial analogue output
- Probe bus for debug

First measurement

Before any quantitative measurement, some qualitative results to get courage !

1 MIP in SKIROC



Charge measurement

Self trigger

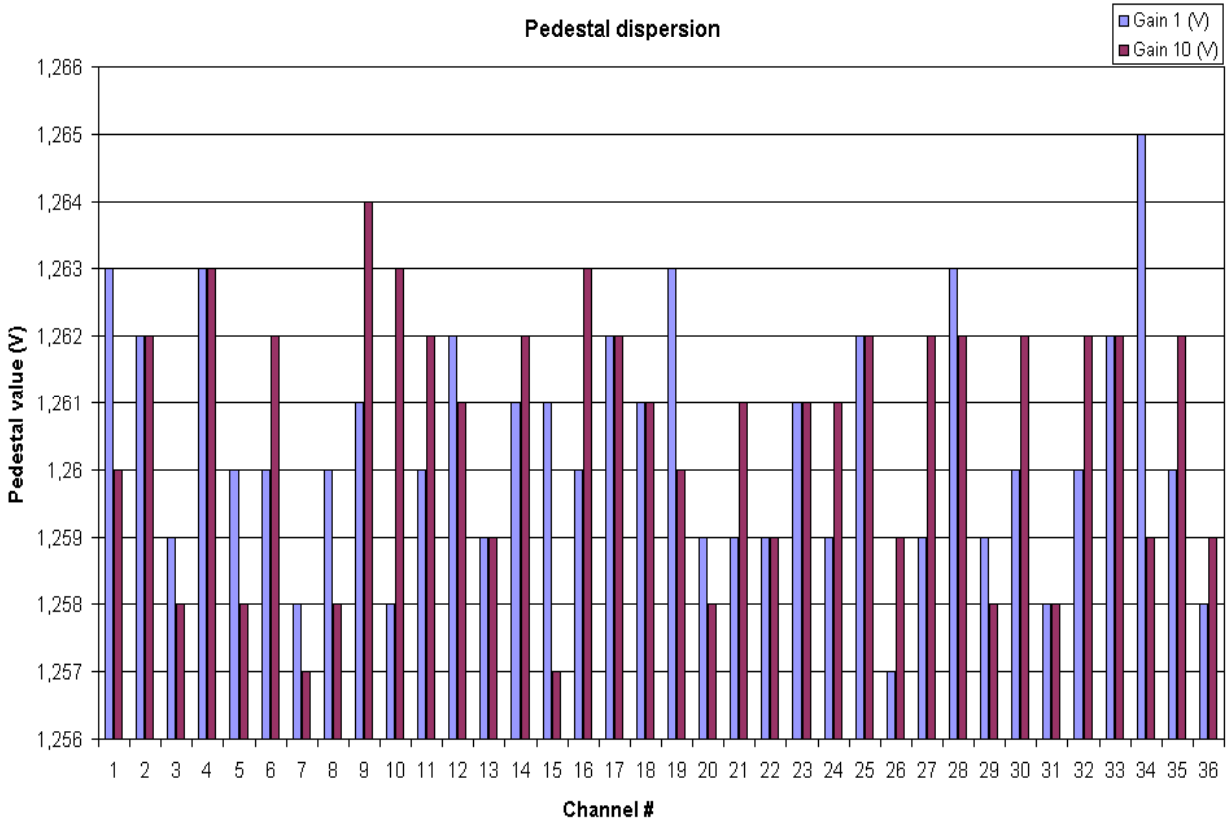
Pedestal dispersion

The pedestal measurement is coherent with what we expect :
-No pedestal pattern (random values according to statistical dispersion)
-Statistical dispersion equivalent to what we get with that technology

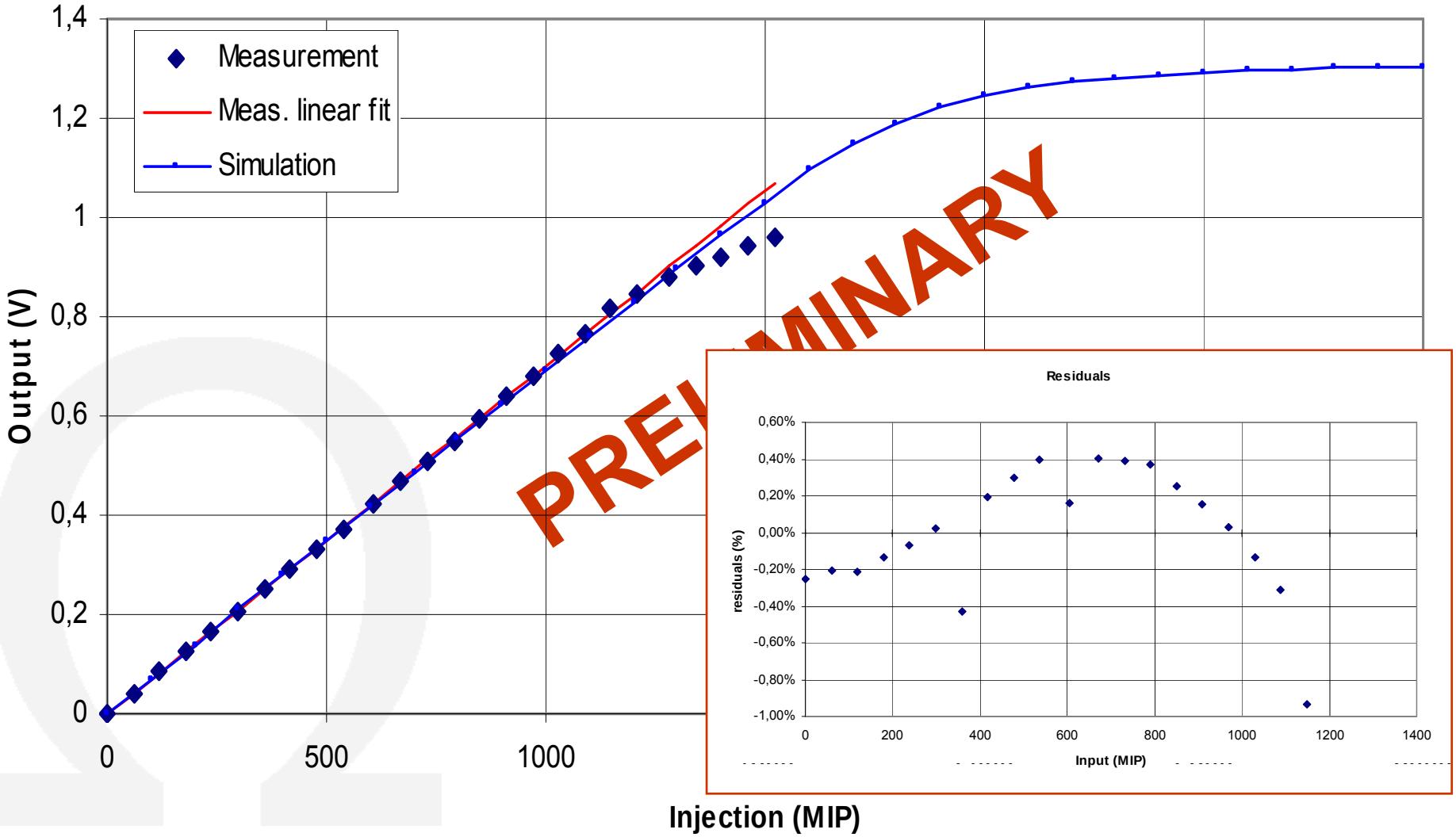
Standard deviation :

$\sigma_{Gain\ 1}$= 1.8mV

$\sigma_{Gain\ 10}$= 1.95mV



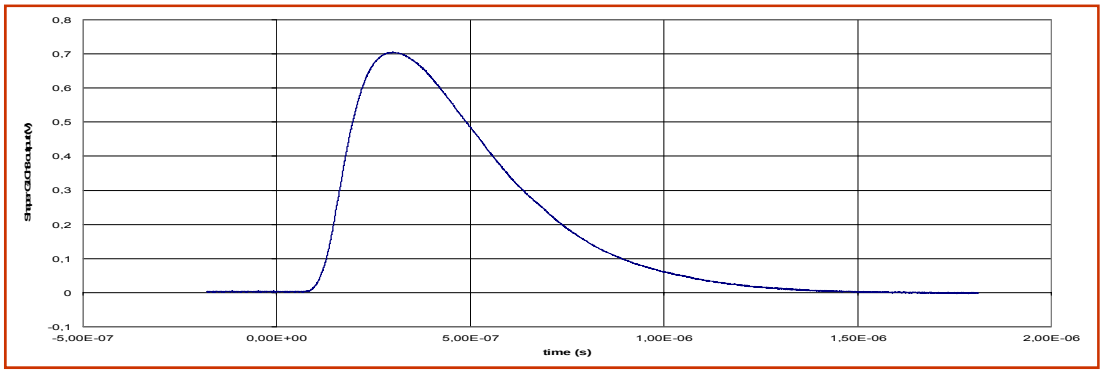
Linearity


SKIROC linearity results
Measurement
Meas. linear fit
Simulation
Output (V)
Injection (MIP)
1,4
1,2
1
0,8
0,6
0,4
0,2
0
0
500
1000
PRELIMINARY
Residuals
residuals (%)
Input (MIP)
0,60%
0,40%
0,20%
0,00%
-0,20%
-0,40%
-0,60%
-0,80%
-1,00%
0
200
400
600
800
1000
1200
1400

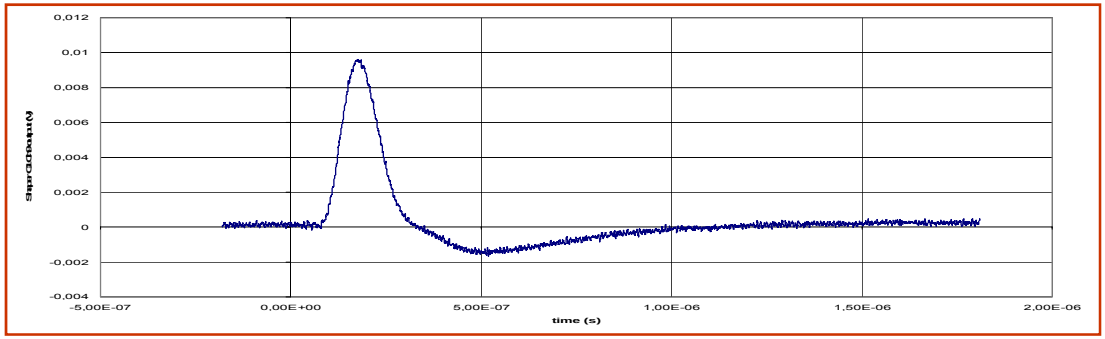
Crosstalk

Crosstalk :
-Neighboor <0.05%
-Long distance <0.02%

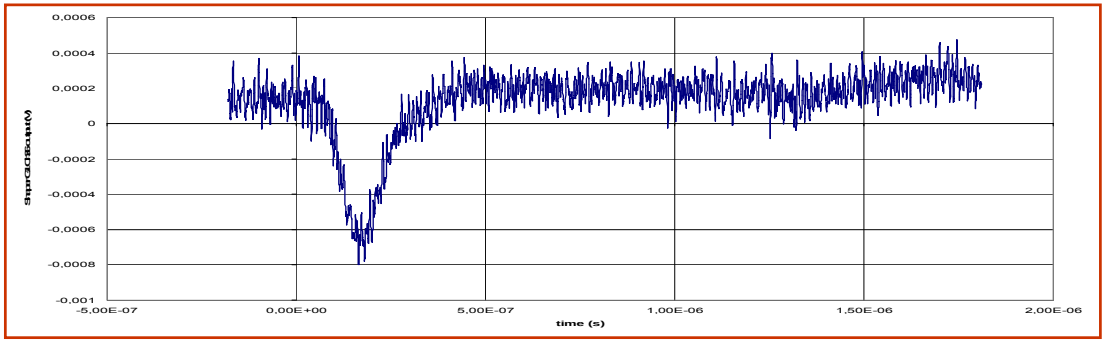
CH.8 – 1000 MIP



CH.9

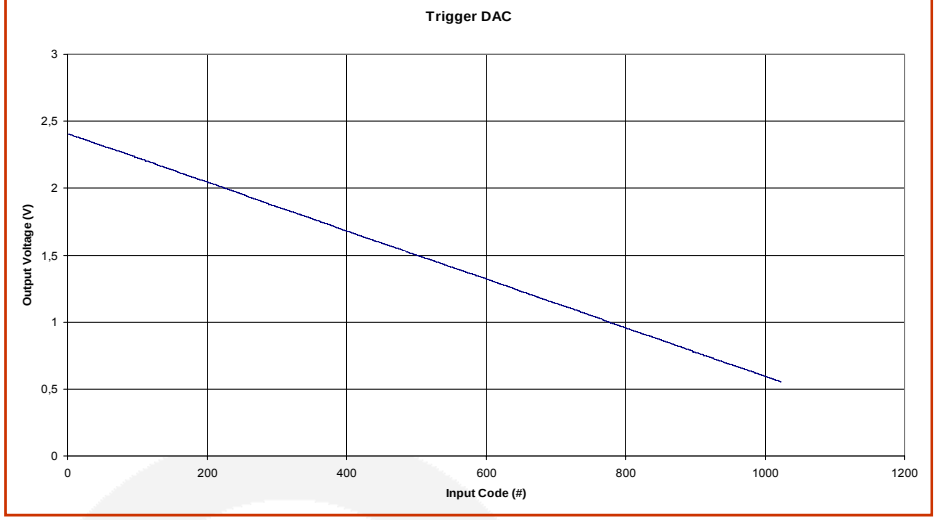


CH.36

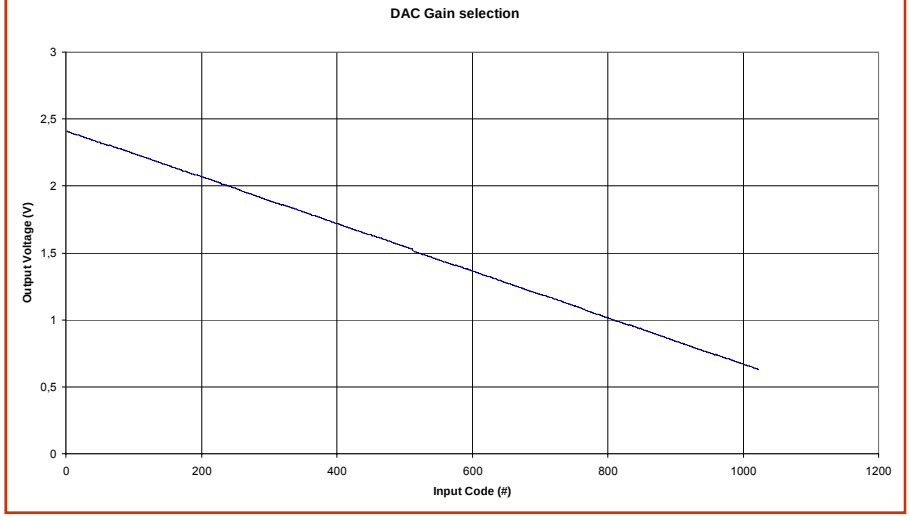


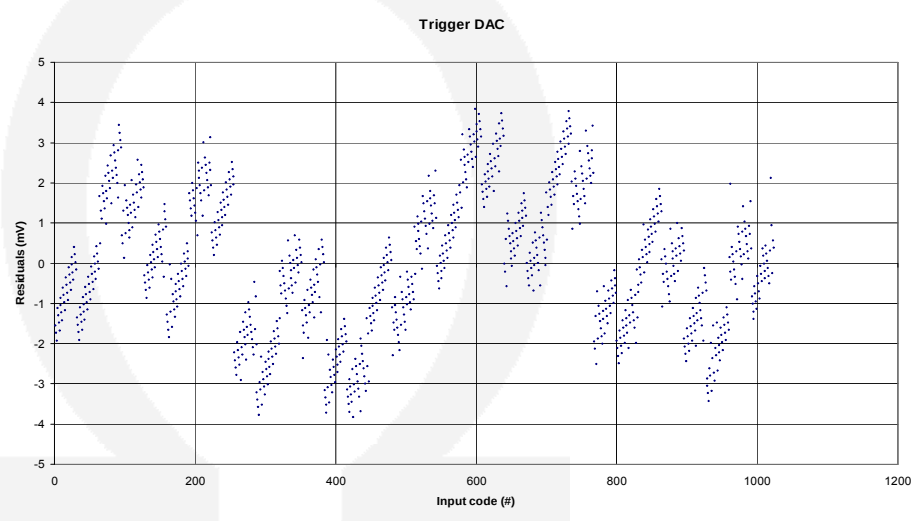
DAC measurement

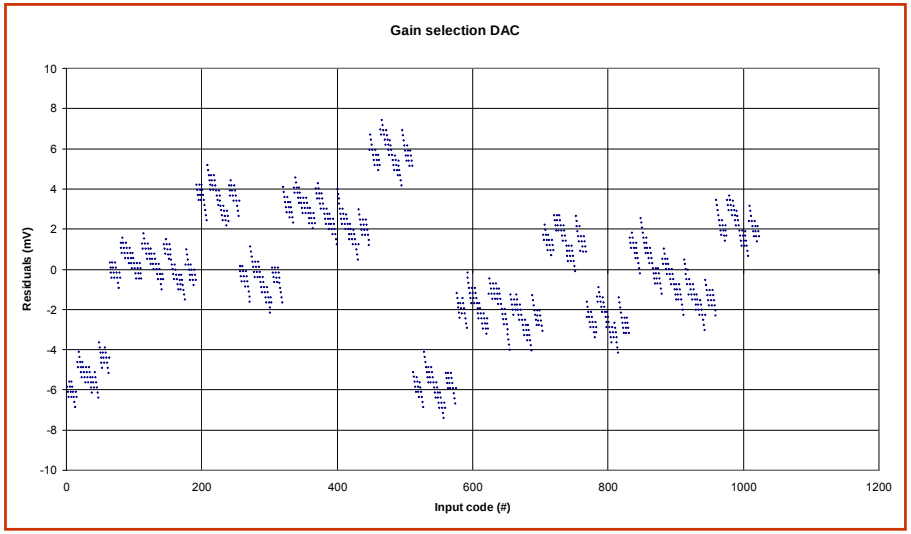
Trigger DAC. Step ~ 2mV
Precision : 9.5 bit



Gain select DAC. Step ~ 2mV
Precision : 8.5 bit

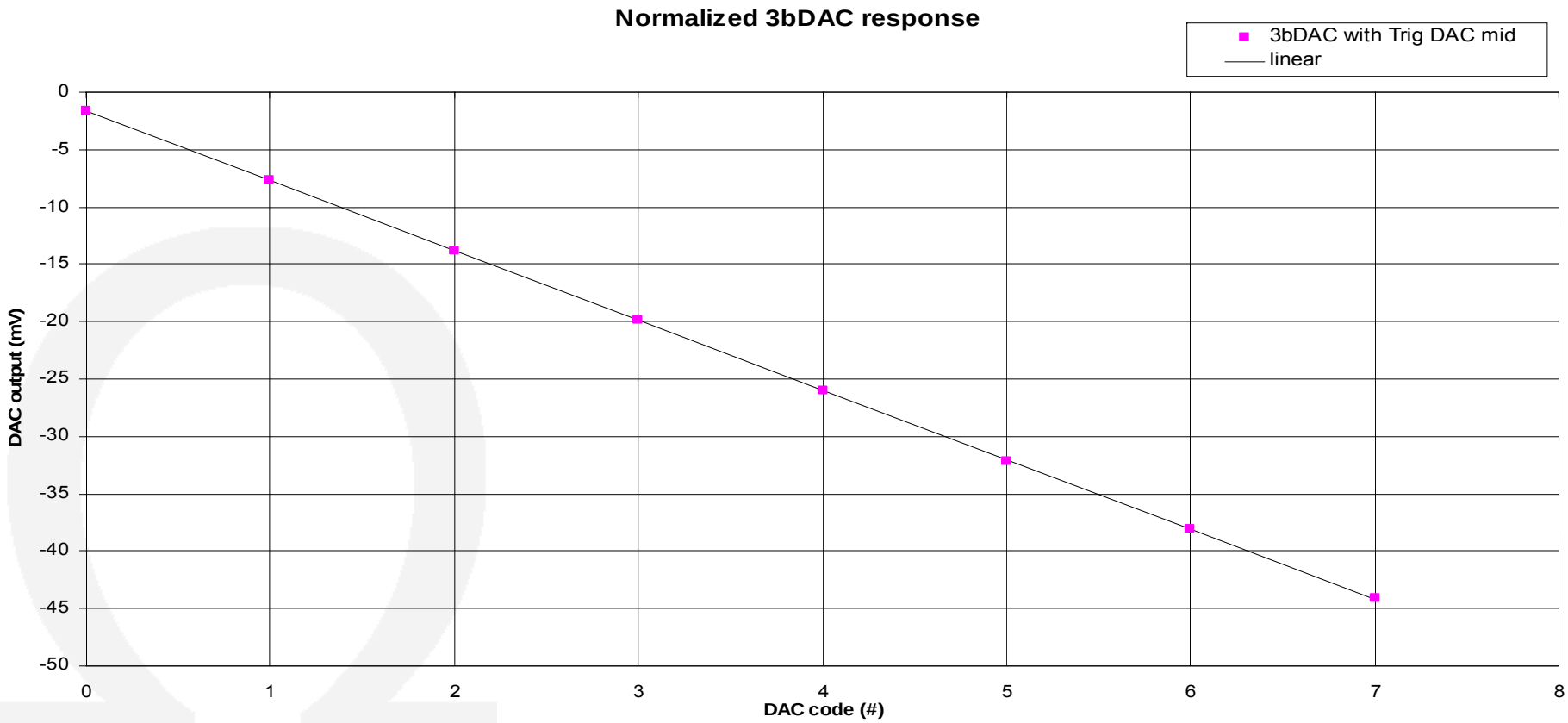






3 bit DAC adjustment

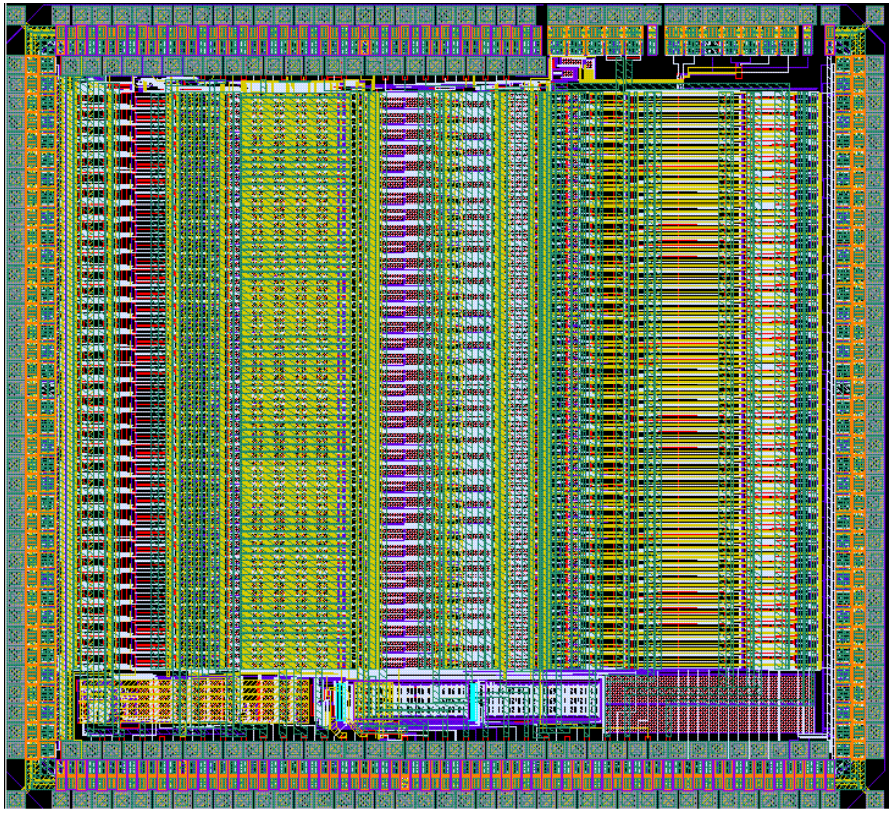
Trigger DAC. Step ~ 6mV
Precision : 8.1 bit



SKIROC : test to be performed

- Dynamic range
- Noise
- Trigger efficiency
- Stability
- Crosstalk
- ADC resolution
- Power pulsing & consumption
- DC coupling capability (leakage current swallowing)

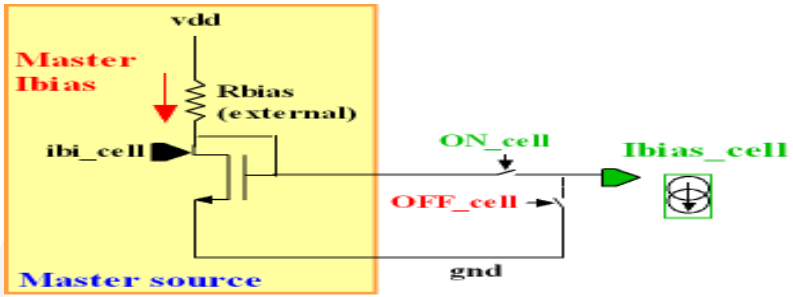
HARDROC STATUS



HARDROC POWER PULSING: Power dissipation (1)

- Maximum power available:
  - 10 µW/ channel with 0.5% duty cycle

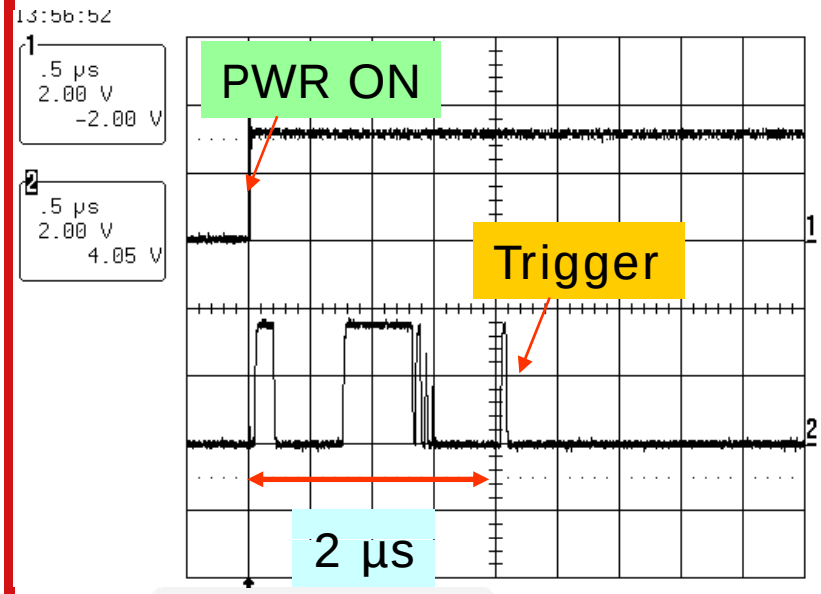
    => 640µW/3.5V=**180 µA** for the entire chip
  - **OFF**= Ibias _cell switched off during interbunch:

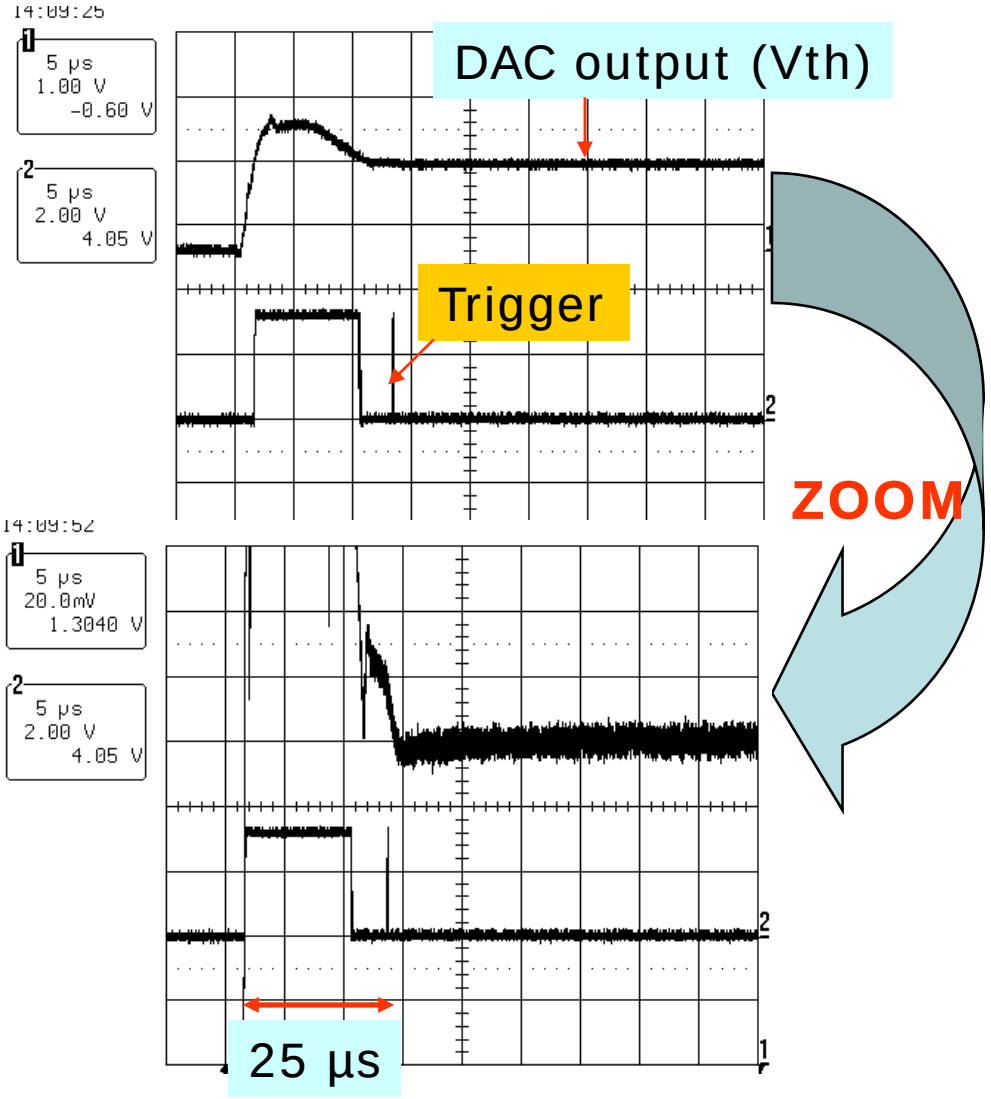


  - BUT a few forgotten switches...
    - Bandgap, some reference voltages not power pulsed
  - **Easy to fix in the production version**

	ON	OFF
Vdd_pad	0	
Vdd_pa	5.8 mA	5.6 µA
Vdd_fsb	4.9 mA	65 µA
Vdd_d0	2.8 mA	78 µA
Vdd_d1	2.7 mA	0
Vddd+ vddd2	3.3mA	200µA + 0 (Clk OFF)
Vdd_dac	0.77 mA	218 µA
Vdd_bandgap	5.05 mA	2.73 mA
Total (noPP)	25.3 mA	3.2mA
Total with 0.5% PP	125 µA	0 hopefully

HARDROC Power pulsing: « Awake » time (2)

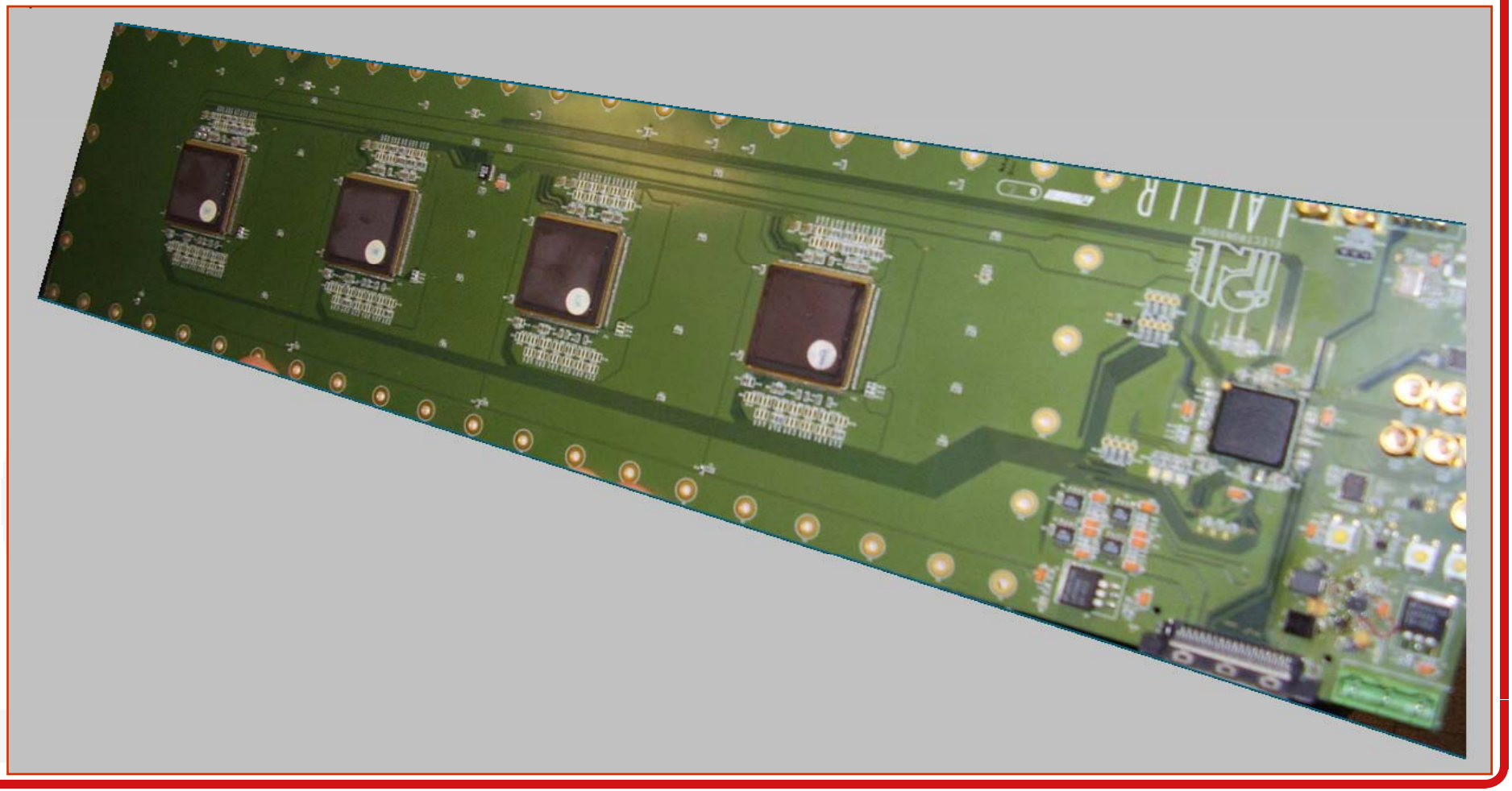




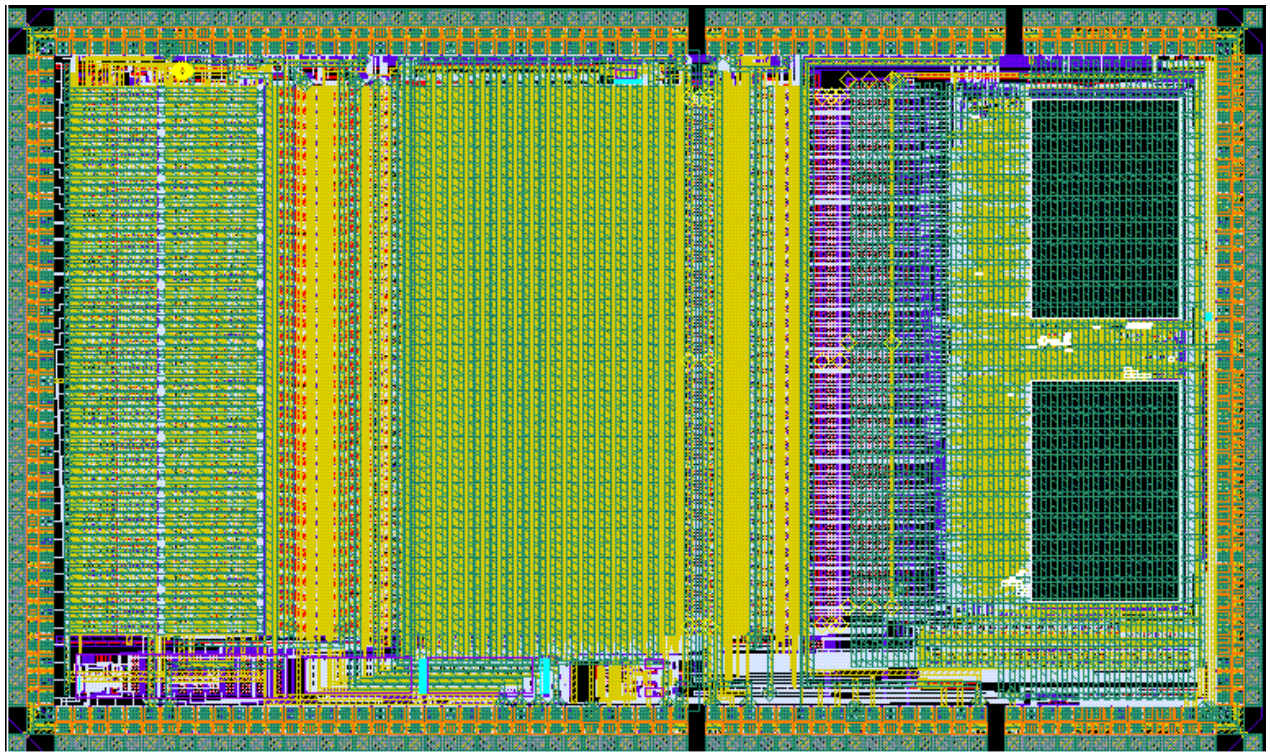
- PWR ON: ILC like (1ms,199ms)
- All decoupling capacitors removed
- PP of the analog part:
  - Input signal synchronised on PWR ON
  - Injection of 100fC, Threshold= 30fC
  - => **Awake time= 2 µs**
- Power pulsing of the DAC:
  - **25 µs (slew rate limited)**

Daisy chain measurement

- First measurement of four chips on the DHCAL prototype PCB (IPNL, LLR, LAL)



SPIROC STATUS



Summary

- PCB in hand (since last week)
- 2 first test boards assembled today
- Test firmware and software in design
- Still waiting for the chips (packaging)

Ludovic is writing the datasheet

Conclusion

- SKIROC :
  - Measurements in progress
  - So far so good, no bad surprise
  - Digital part in test (few bugs already corrected)
- HARDROC :
  - Guess what measurement in progress
  - Power pulsing OK
  - Digital chaining OK → common to the three ASICs
- SPIROC :
  - PCB in hand
  - Waiting for the ASICs