Electronics, common issues
NA2, JRA1, JRA2, JRA3

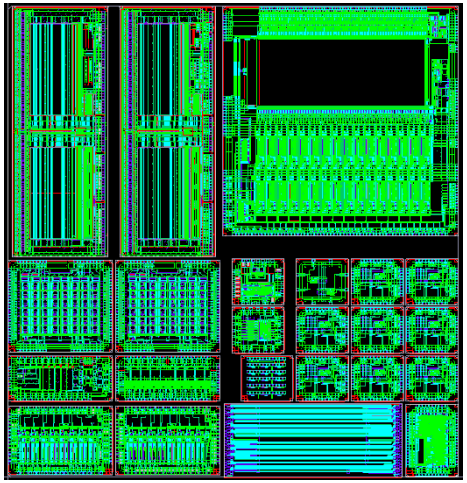
- Monday 8/10 16.30 hrs-18.00 hrs
- ~40 attendees

- NA2: News on the MICELEC microelectronics service; Michael Campbell for Alessandro Marchioro
- JRA1: The EUDET data reduction board and its application to the JRA1 pixel telescope; Concezio Bozzi
- JRA3: JRA3 developments; Christoph de la Taille
- JRA2: Requirements/ideas for a future gas detector readout device; Michael Campbell

NA2 contribution

EUDET-MICELEC
Status Report
October 2007

A. Marchioro / CERN-PH



Technology access

- **Foundry contract** for 130 and 90 nm CMOS and BiCMOS is available for all HEP community
- Present total demand from community is below threshold to organize **internal MPWs**
  - But mini-MPWs (10-25 mm^2) in 130 nm are organized through MOSIS for same foundry
- Proposal for **common 130 nm MPW run:**
  - **February 2008**
  - If interested, contact us asap !

Support services

- **Packaging** contract discussed with Europractice for ASE/Taiwan
  - Many standard and advanced products DIL, Quad, BGA, Flip-Chip etc.
  - If interested, contact us!
- CERN has acquired a **new advanced IC tester** (Credence Sapphire)
  - Users interested in accessing this service for professional IC characterization are welcome to contact us!

Tools and Training

- **Customized design kit** developed (partly) with EUDET funds to facilitate design of complex digital ICs
- Four **training courses** with 10 participants each (last in June 2007) organized to spread knowledge about utilization of advanced design tools. 5th Design course being prepared for late '07

Final remarks:

Community is warmly recommended not to spread (the thin resources) over different technologies!

Users are welcome to submit suggestions and comments on their wishes and needs

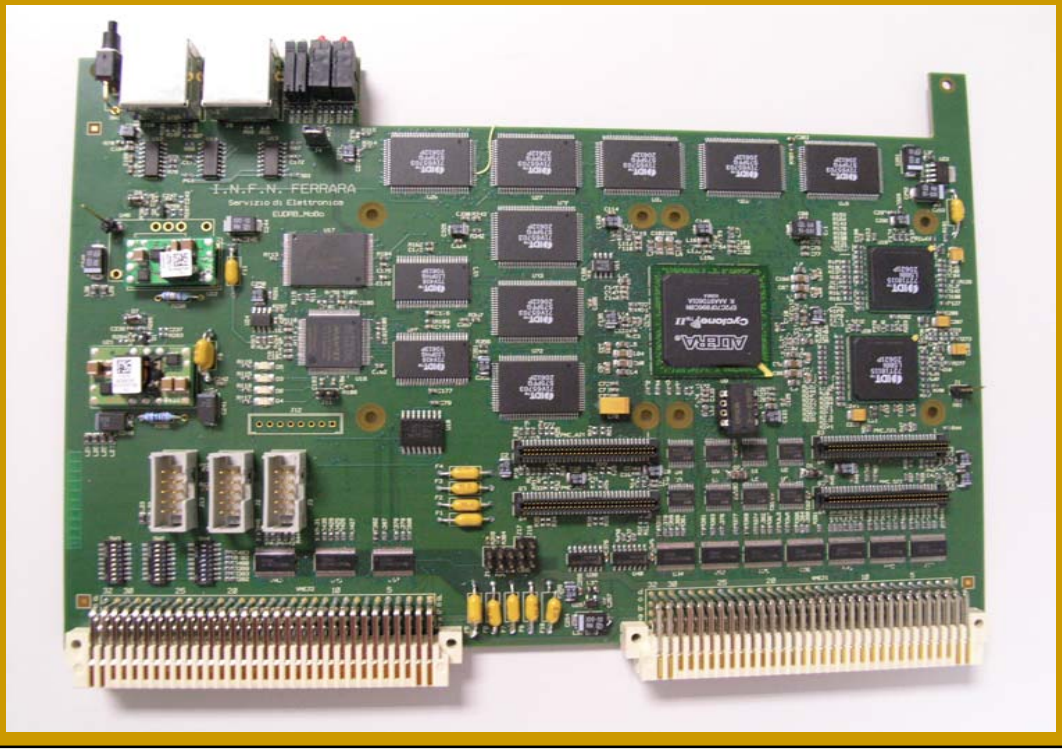
Contribution from JRA1

EUDRB: the data reduction board of the EUDET pixel telescope

Lorenzo Chiarelli, Angelo Cotta Ramusino,
Livio Piemontese, Davide Spazian
Università & INFN Ferrara

Presented by Concezio Bozzi

A VME64x/USB2.0-based DAQ card for MAPS sensors



Mother board built around an ALTERA CycloneII FPGA (clock rate: 80MHz)

NIOS II, 32 bit “soft” microcontroller (clock rate: 40MHz) implemented in the FPGA for

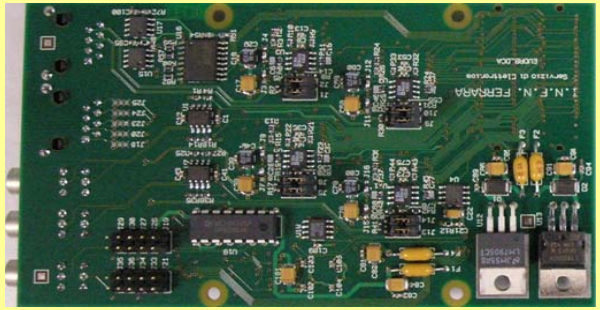
- on board diagnostics
- on-line calculation of pixel pedestal and noise
- remote configuration of the FPGA via RS-232, VME, USB2.0

Two readout modes:

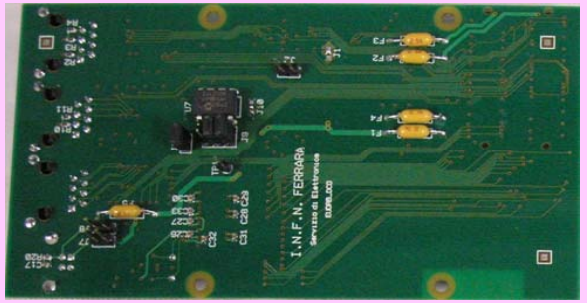
Zero Suppressed readout

Non Zero Suppressed readout

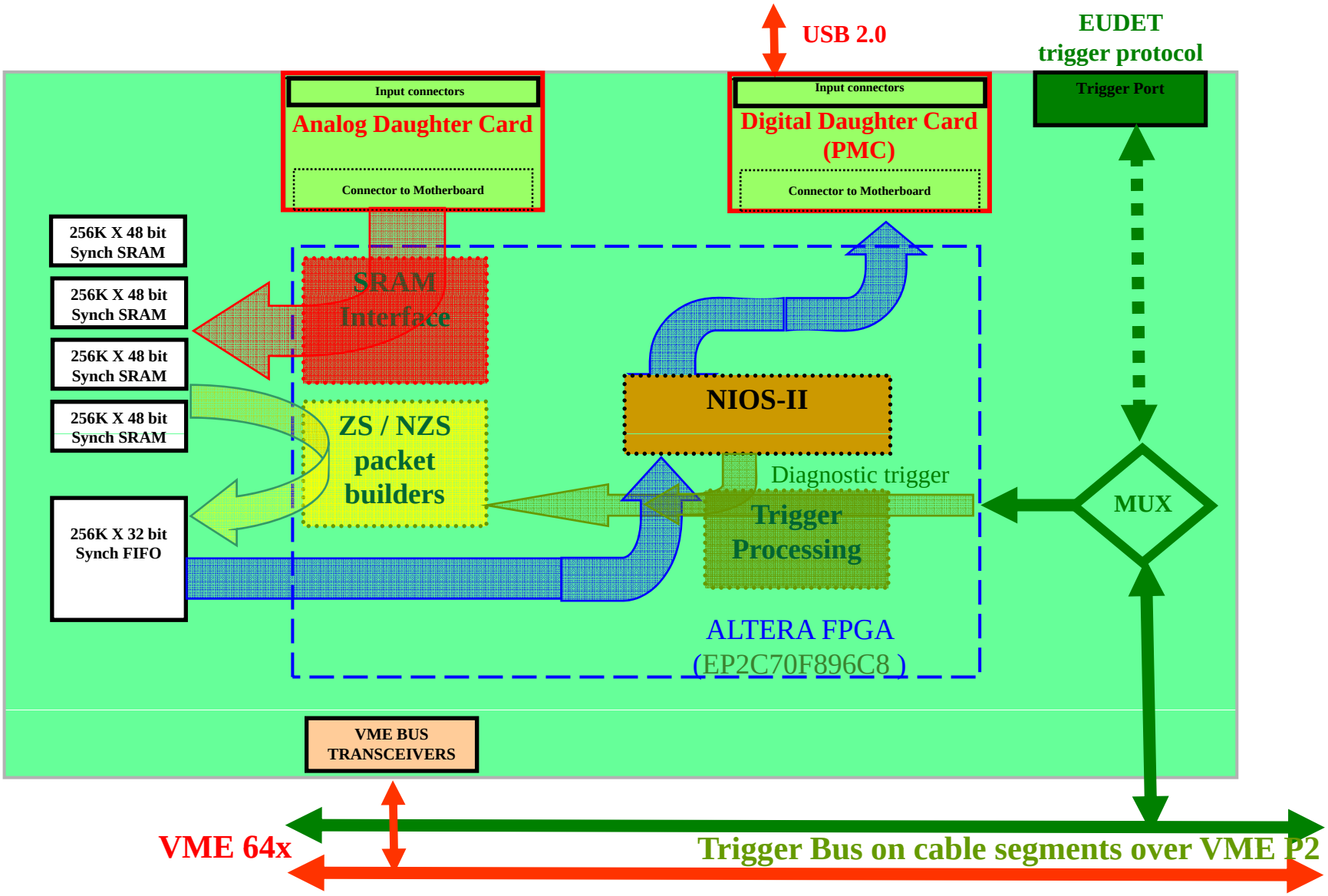
analog daughter card based on the successful LEPSI and SUCIMA designs



digital daughter card drives/receives control signals for the detectors and features a USB 2.0 link



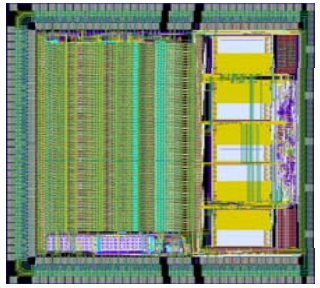
Data Flow for benchtop DAQ via USB2.0, and for data taking via VMEBUS



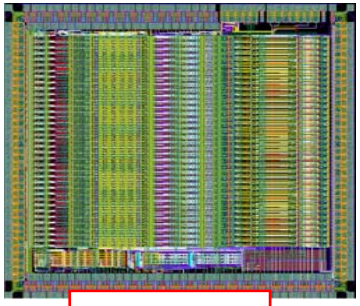
Conclusions

- EUDRB successfully used in beam tests at DESY (June, August) and CERN (September)
- Connected to MAPS sensor for demonstrator: MimoTEL, 256x256, 30μm x 30μm pitch
- Hunting for better performance:
  - VME CPU is the real bottleneck at the moment
  - Some improvements on the EUDRB side also possible

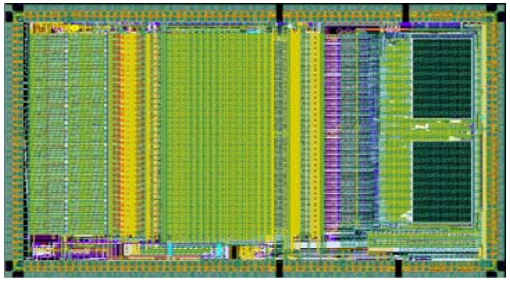
Once optimised, the EUDRB could be used in other Pixel read-out applications



HaRDROC



SKIROC



SPIROC

EUDET JRA3 Front-End electronics in 2007

IN2P3 Institut National de Physique Nucléaire et de Physique des Particules

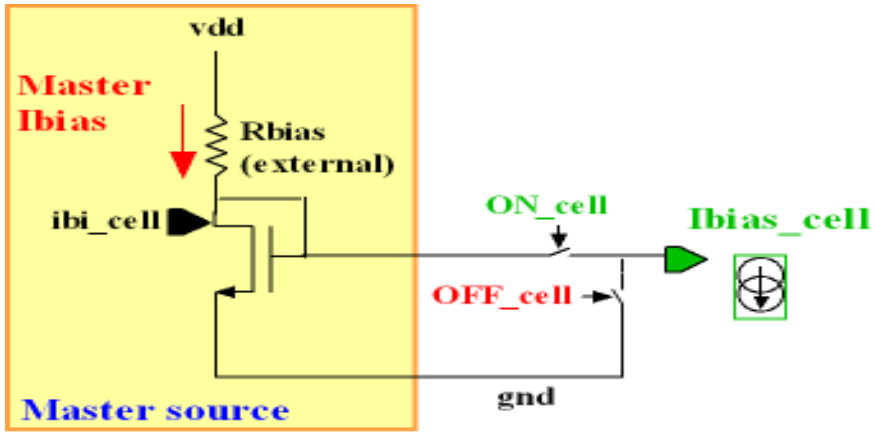
C. de La Taille

IN2P3/LAL Orsay

HARDROC POWER PULSING: Power dissipation

- Maximum power available:
  - 10 µW/ channel with 0.5% duty cycle

  => 640µW/3.5V=**180 µA** for the entire chip
  - **OFF**= Ibias _cell switched off during interbunch:



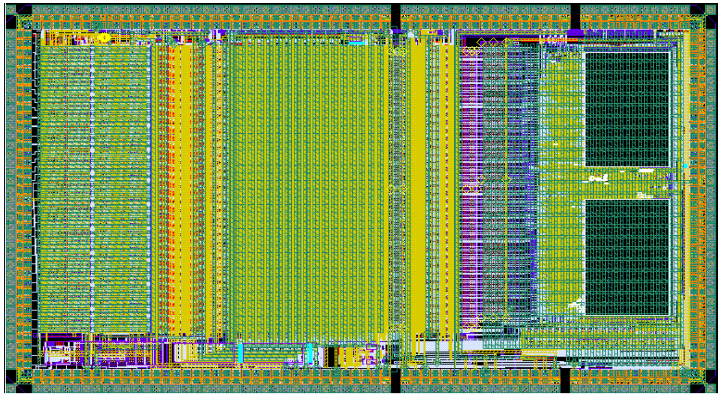
	ON	OFF
Vdd_pad	0	
Vdd_pa	5.8 mA	5.6 µA
Vdd_fsb	4.9 mA	65 µA
Vdd_d0	2.8 mA	78 µA
Vdd_d1	2.7 mA	0
Vddd+ vddd2	3.3mA	200µA + 0 (Clk OFF)
Vdd_dac	0.77 mA	218 µA
Vdd_bandgap	5.05 mA	2.73 mA
Total (noPP)	25.3 mA	3.2mA
Total with 0.5% PP	125 µA	0 hopefully

Common issues

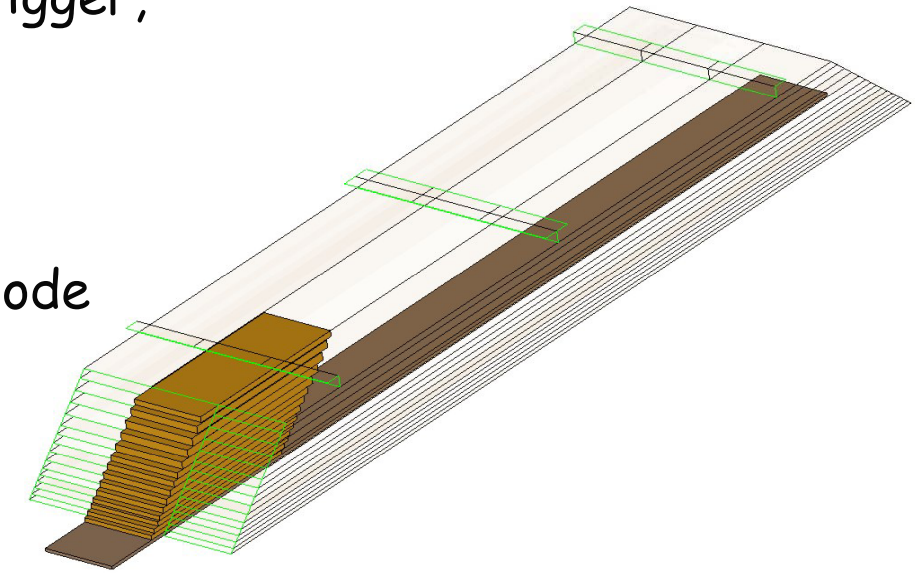
- Power pulsing studies
  - Power management and distribution
  - Stability,
  - Clock distribution
- DAQ
  - Zero suppressed data
  - Minimum number of lines
- ASIC technologies
  - « Analog friendly » technologies : now mostly 0.35µm AMS SiGe
  - Sharing blocks, MPWs : in2p3, Krakow….

Conclusion

- 3 major second generation ASICs for technological prototypes submitted
  - HARdROC submitted for DHCAL RPCs
  - SKIROC submitted for ECAL Si-W
  - SPIROC for AHCAL SiPM

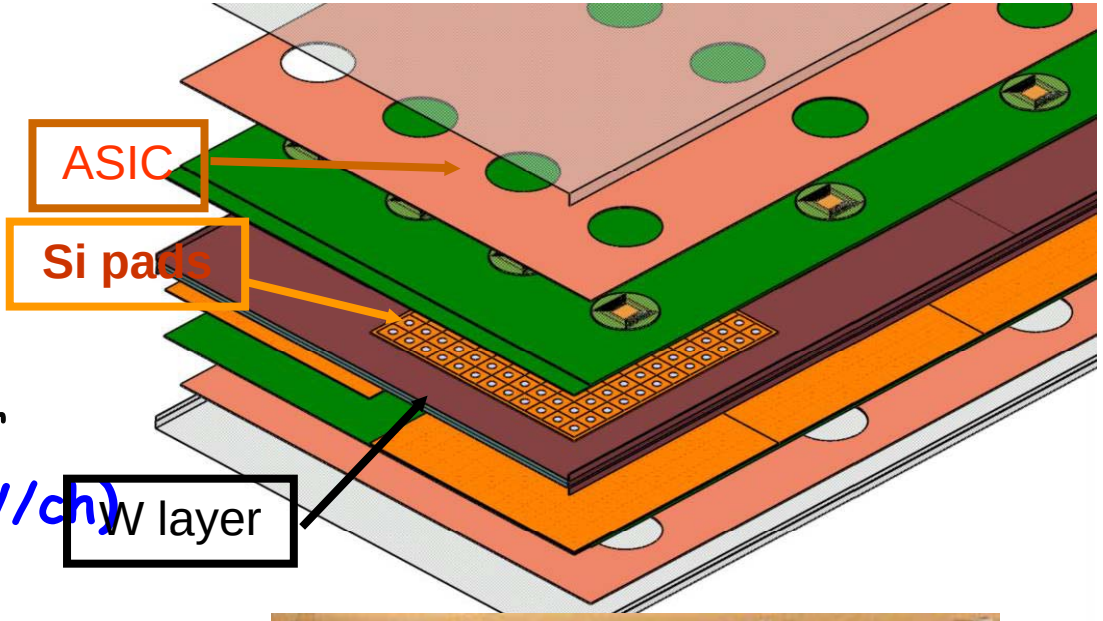


- System aspects now proceeding
  - Power pulsing, Zero-suppress, Auto-trigger, 2nd generation DAQ…
  - On detector boards
  - Connection to DAQ : task force
  - EUDET repository for shared VHDL code

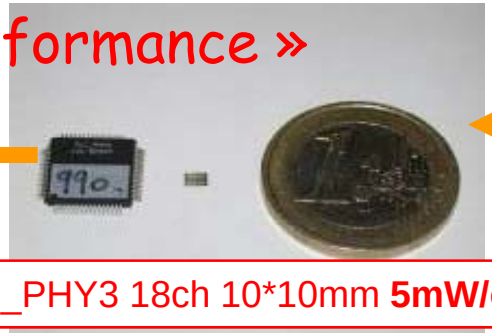


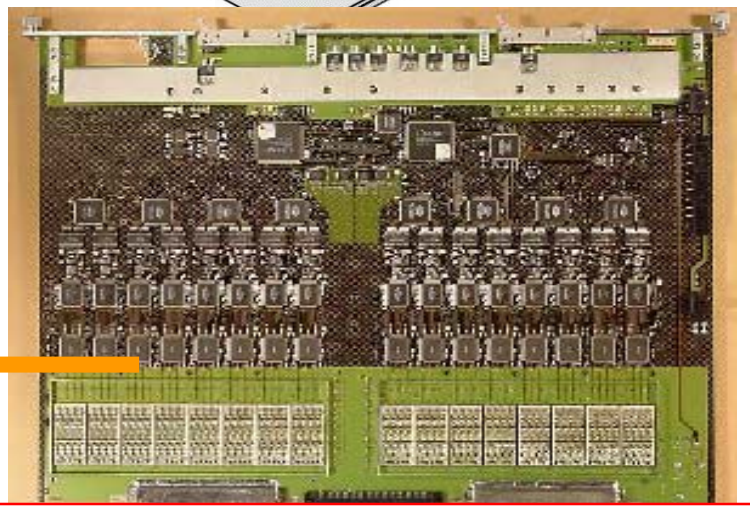
ILC Challenges for electronics

- Requirements for electronics
  - Large dynamic range (15 bits)
  - Auto-trigger on ½ MIP
  - On chip zero suppress
  - Front-end embedded in detector
  - **Ultra-low power : (« 100µW/ch)**
  - 10^8 channels
  - Compactness



- « Tracker electronics with calorimetric performance »

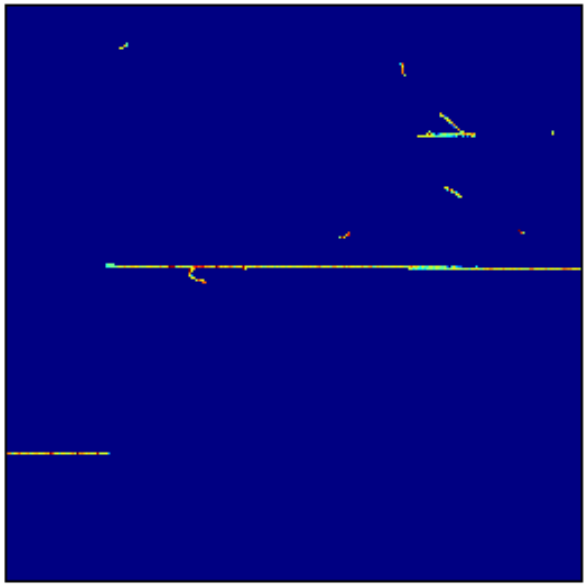




ILC : **100µW/ch**

FLC_PHY3 18ch 10*10mm **5mW/ch**

ATLAS LAr FEB 128ch 400*500mm **1 W/ch**



Contribution from JRA2

Pixel Readout Electronics - from HEP to imaging to HEP… Status, requirements, new ideas

M. Campbell, R. Ballabriga, E. Heijne, X. Llopart,
L. Tlustos, W. Wong
CERN
Geneva, Switzerland

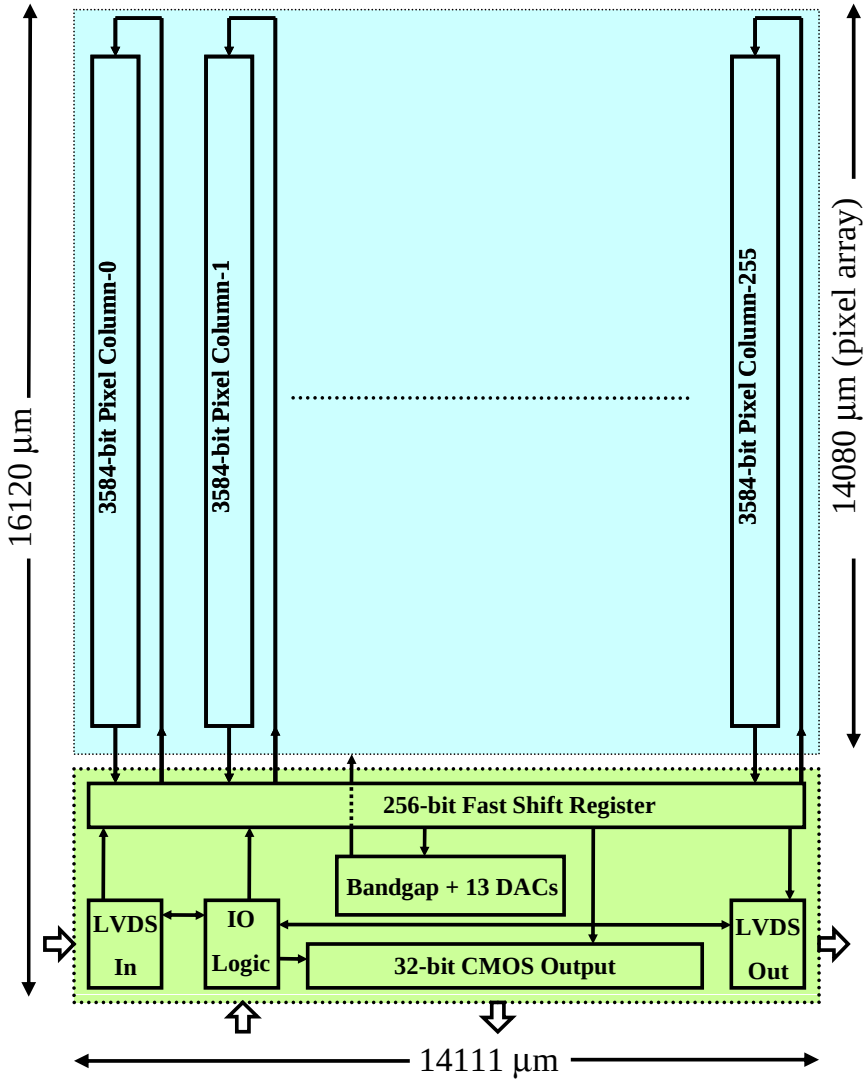
Timepix developed within JRA2

- Chip architecture almost identical to Mpix2MXR20
  - M0=M1=1 and Shutter ON -> FClock used as Ref_Clk
- 256x256 55µm square pixels
- Analog Power -> 440mW
- Digital Power (Ref_Clk=50MHz) -> 220mW
- Serial readout (@100MHz) -> 9.17 ms
- Parallel readout (@100MHz) -> 287 µs
- > 36M Transistors

Very successful development => JRA2 results

Room for further development

- Charge below threshold in shared events is lost in all modes
- Charge measurement near to threshold in TOT is imprecise
- Arrival time/TOT measurement range is limited by counter depth
- Chip is neither triggerable nor data driven
- There is no FAST-OR



Requirements for a general purpose gas and semiconductor readout chip

- Clean hit information
- Low and uniform threshold
- High spatial resolution
- Combined energy and arrival time information
- Include a FAST-OR

GasSiPix - Front end

***** Basic idea developed together with Ruud Kluit of NIKHEF *****

- Medipix3 or GOSSIPO-2 like
  - Suitable for semiconductors and gas readout?
  - Rise time 25ns?
  - Noise 100 e^- rms?
  - Minimum threshold 750e^-?
  - Power <1W/cm^2?
- For gas detectors include spark protection and SiProt shielding
  - Which A:Si thickness?
  - How many pC should it withstand?
- Use precision time tag unit from Nikhef (GOSSIPO-2 V. Gromov) in pixel to measure arrival time
  - 1-2ns precision for Vernier counter?
  - 15-bit clock tick counter?
- Use TOT for energy measurement and/or timewalk correction if charge summing not include
  - 8-bit TOT precision?

Gave rise to a lively discussion, with clear interest in the subject

Summary of Common electronics session

- There is a broad spectrum of electronics activities in EUDET
- ~20 talks on electronics during the parallel sessions on Monday
- Some of these were discussed at the Common electronics session, with a view of common use/developments and cross fertilisation
- Clear areas for use across the NA/JRA's were indicated as well as prime areas for development and future application of EUDET work