# Electronics Developments for SITRA

Silicon strips readout using
Deep Sub-Micron Technologies

**Jean-François Genat**

on behalf of

A. Comerma-Montells[3], W. Da Silva[1], J. David [1], M. Dhellot[1], D. Fougeron[2], D. Gascon [3], R. Hermel[2], J-F. Huppert[1], F. Kapusta[1], H. Lebbolo[1], T.H. Pham[1], F. Rossel[1], A. Savoy-Navarro[1], R. Sefri[1], S. Vilalte[2]

*[1] LPNHE Paris, [2] LAPP Annecy, [3] UEB Barcelona*

Work in the framework of the SiLC (Silicon for the Linear Collider), R&D Collaboration and the EUDET I3-FP6 European Project

**EUDET Annual meeting October 8-10th 2007 Ecole Polytechnique Palaiseau, France**

# Outline


- Detector data 2
- Technologies 5
- Front-End Electronics 7
- 4-channel 130nm chip 11
- 128-channel chip 30
- Conclusion 39

# Silicon strips detector

Assume:

- A few $10^6$ Silicon strips
- 10 - 60 cm long,
- Thickness 200–500 µm
- Strip pitch 50–200 µm
- Single sided, AC or DC coupled
- Strixels ?, 3D ?

Millions of channels:
Integration of k-scale channels readout chips

# Silicon strips data at the ILC

- Pulse height: Cluster centroid to get a few $\mu$m position resolution
  *Detector pulse analog sampling*
- Time: 150-300 ns for BC identification, 80ns sampling
  *Shaping time of the order of the microsecond*

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# Technologies

Silicon detector and VLSI technologies allow to improve detector and front-end electronics integration

Front-end chips:

- Thin CMOS processes 130, 90 nm available from Europractice (IMEC, Leuven)
- Chip thinning down to 50 µm

**More channels on a chip, more functionalities, less power**

Connectivity:

- On detector bump (stud)-bonding (flip-chip) 50-100 µm pads
- 3D interconnections even less…

**Smaller pitch detectors, better position and time resolution.**
**Less material**

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# Integrated functionalities

- Full readout chain integration in a single chip

  - Preamp-shaper
  - Trigger decision on analog sums : Sparse data scan
  - Sampling: Analog pipe-line
  - Analog event buffering: occupancy: 8-16 deep event buffer
  - On-chip digitization 10-bit ADC
  - Buffering and pre-processing:
    Centroids, Least square fits, Lossless compression and error codes
  - Calibration and calibration management
  - Power switching (ILC duty cycle)

- Presently 128 channels in 130nm CMOS under design at LPNHE/LAPP/UEB having in view 512-1024 channels

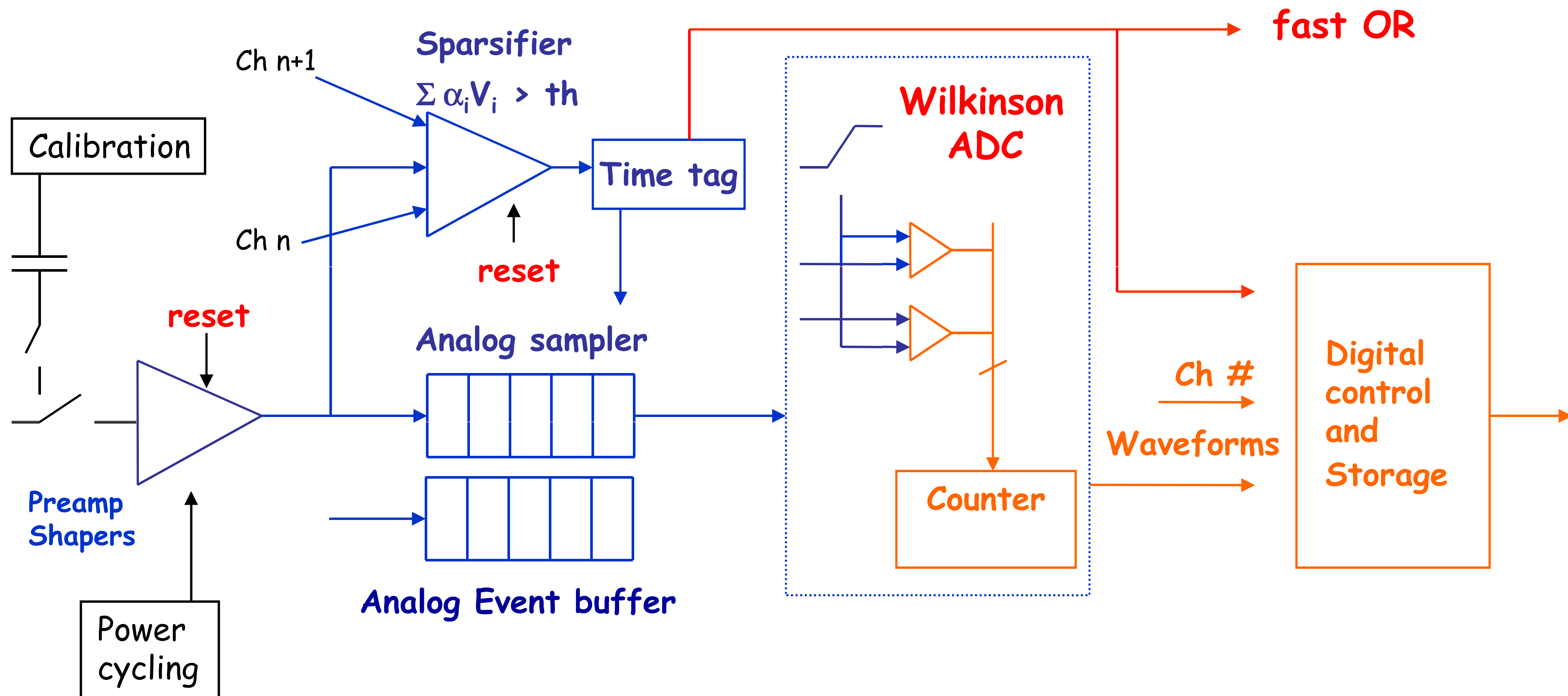
# Front-End Chip goals

- Integrate 512-1024 channels in 90nm CMOS:
  - Amplifiers: - 30 mV/MIP over 30 MIP range
  - Shapers: - Two ranges: 500ns–1µs, 1µs-3µs
  - Sparsifier: - Threshold the sum of 3-5 adjacent channels
  - Samplers: - 8 samples at 80ns sampling clock period
    - Event buffer 8-16 deep
  - Noise baseline:

    Measured with 180nm CMOS:
    375 + 10.5 e-/pF @ 3 µs shaping, **210µW power**
    S/N = 20 @ 90cm long strips
  - ADC: - 10 bits
  - Buffering, digital pre-processing
  - Calibration
  - Power switching can save a factor up to 200

ILC timing: 1 ms: ~ 3-6000 trains @150-300ns / BC
199ms in between

# Foreseen Front-end architecture




**Charge 1-30 MIP, Time resolution: BC tagging 150-300ns**
**80ns analog pulse sampling**

**Technology: Deep Sub-Micron CMOS 130-90nm**

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# History

| | | | |
|---|---|---|---|
| 2004-2006 | 180nm chip: | | OK with radio-active source |
| 2006-2007 | 130nm | 4-channel: | Beam tests this week at CERN |
| 2007 | 130nm | 1-channel: | Improved analog pipe-line, calibration |
| 2007-2008 | 130nm | 128 channels: | True mixed design<br>All analog blocks validated<br>Digital under design. |
| 2009 | k-channels chip | | |

# Front-end in 130nm

130nm CMOS:

- Smaller
- Faster
- Less power
- Will be (is) dominant in industry
- (More radiation tolerant)

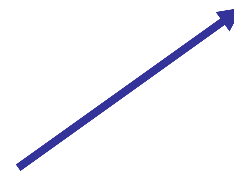
Drawbacks:

- Reduced voltage swing (Electric field constant)
- Noise slightly increased (1/f)
- Leaks (gate/subthreshold channel)
- Design rules more constraining
- Models more complex, not always up to date

Millions of channels:
Integration of k-scale channels readout chips

# UMC CMOS Technology parameters

| | 180 nm | 130nm |
|---|---|---|
| • 3.3V transistors | yes | yes |
| • Logic supply | 1.8V | 1.2V |
| • Metals layers | 6 Al | 8 Cu |
| • MIM capacitors | 1fF/mm² | 1.5 fF/mm² |
| • Transistors | Three Vt options | Low leakage option |



May be used for analog storage during ~ 1 ms

# 2006-7 Chips

130nm CMOS

Both under test

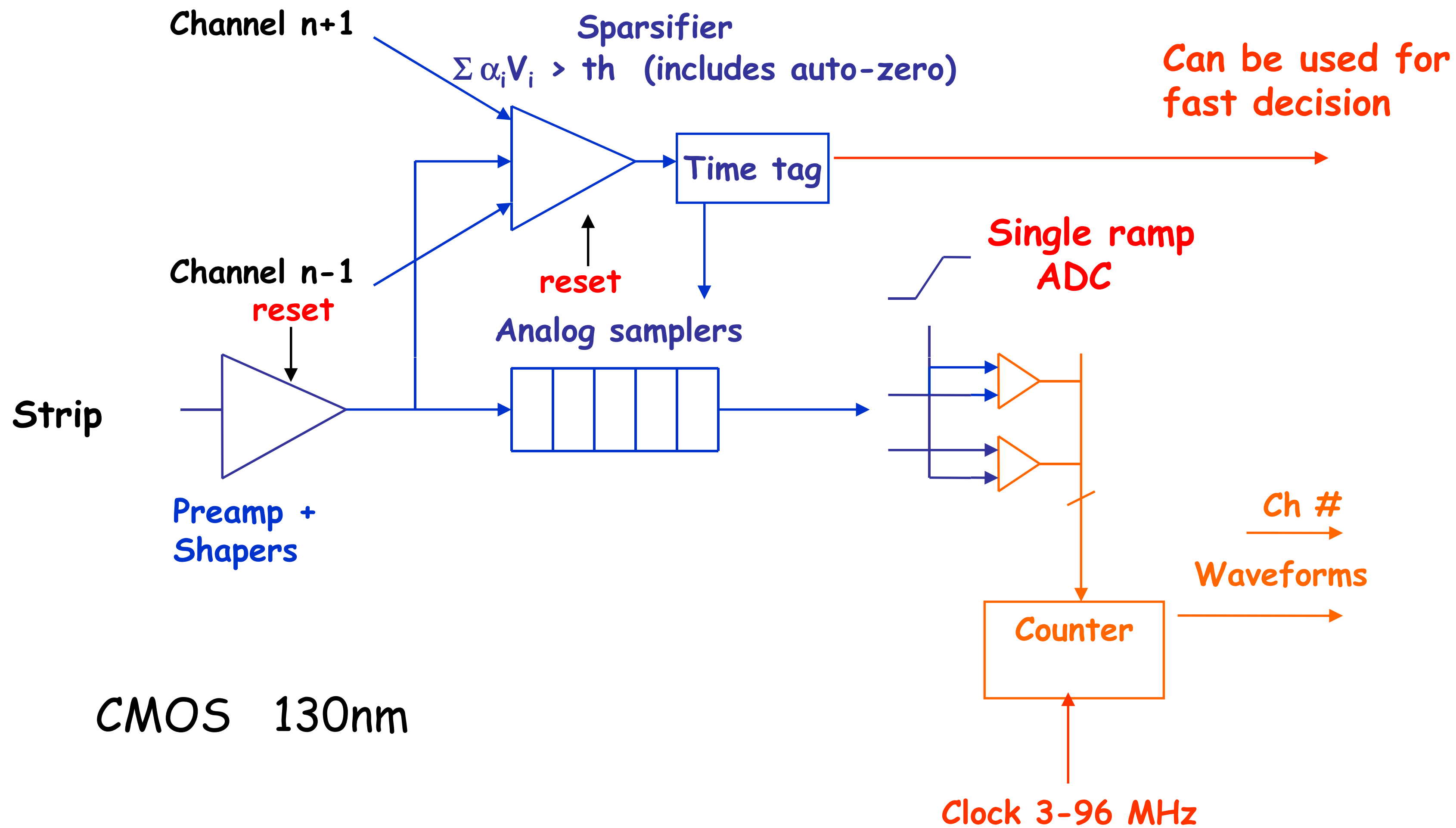
Chip -1 4 channels

- Preamp-shapers + Sparsifier
- Pipeline 1
- ADC
- Digital

Chip -2 One channel

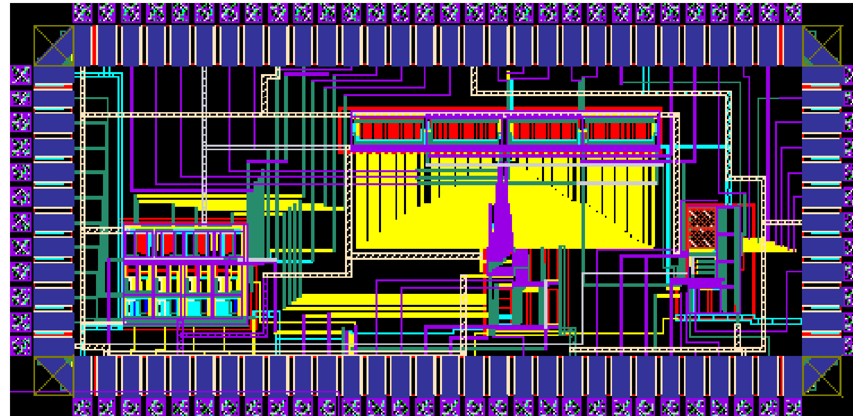
- Preamp-shapers + Sparsifier
- DC servo
- Pipeline 2 (improved)
- DAC
- Test structures: MOSFETS, passive

# 4-channel Chip

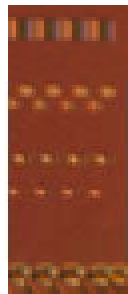


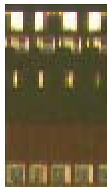

CMOS 130nm

# 4-channel 130nm Silicon

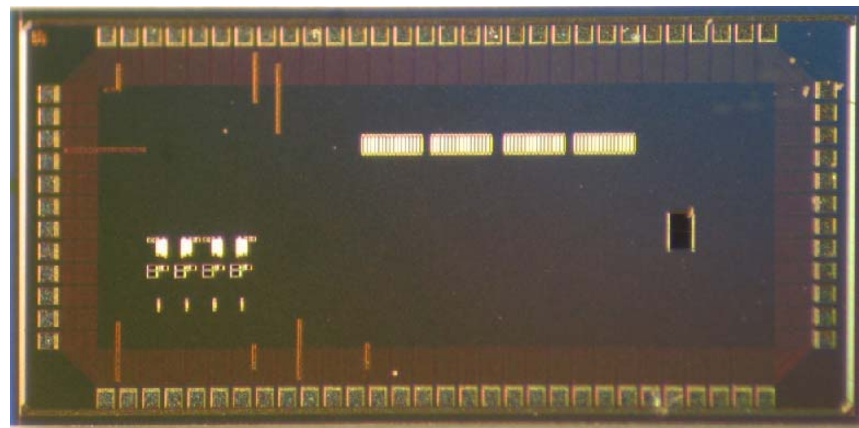


Layout of the 130nm chip including sampling and A/D conversion





180nm 130nm

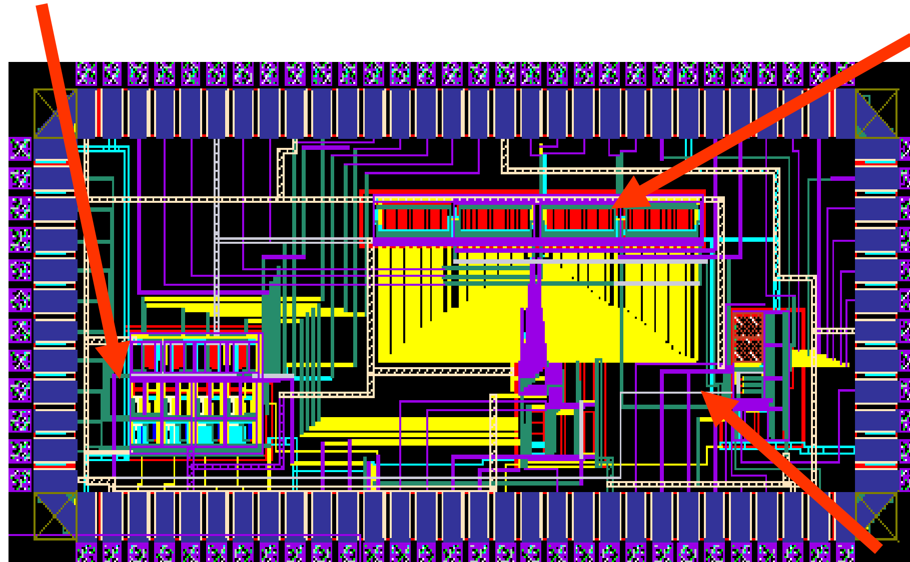


**Picture**

# 4-channel chip layout

Amplifier, Shaper, Sparsifier 90*350 μm²

Analog sampler 250*100 μm²



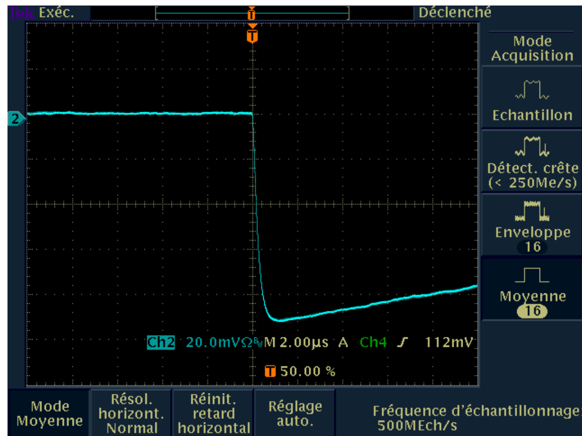
A/D 90*200 μm²

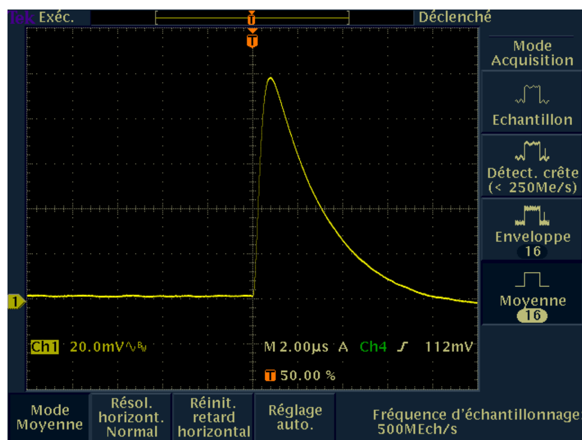
Layout of the 130nm chip including sampling and A/D conversion

# Results

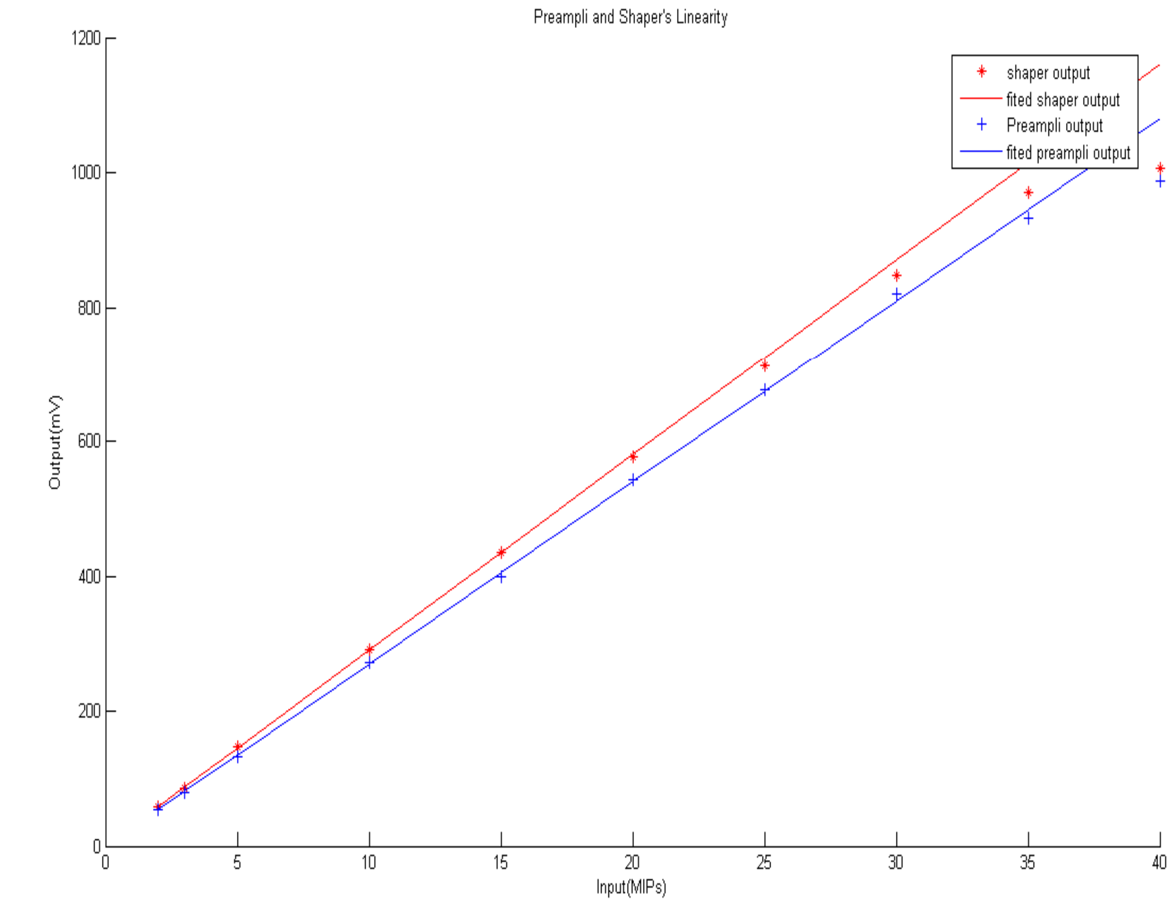
## Measured gain - linearities

Preamp output




Shaper output

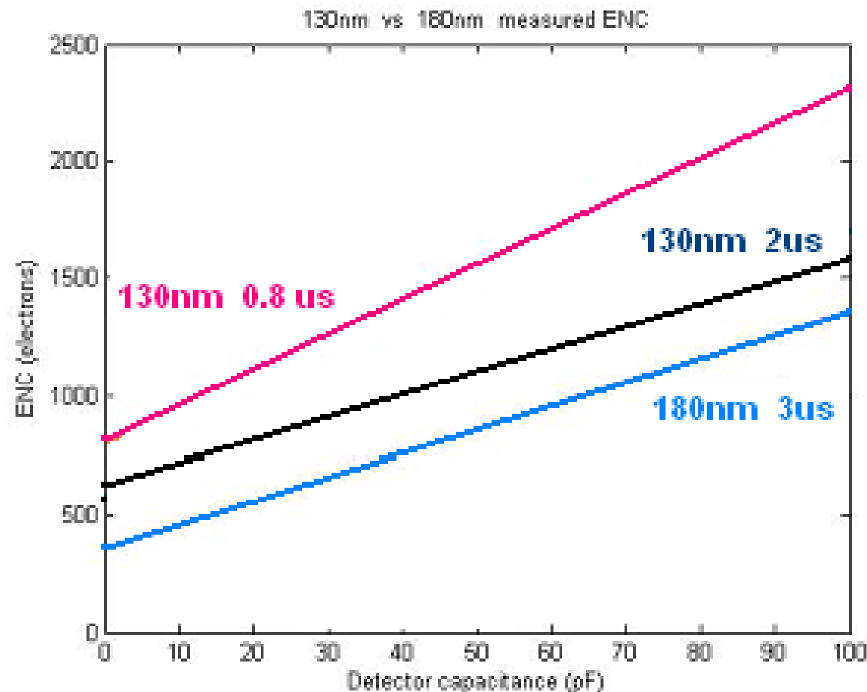



Preamp and Shaper:

Gain = 29mV/MIP
Dynamic range = 20MIPs 1%
30 MIPs 5%
Peaking time = 0.8-2.5µs / 0.5-3µs expected

# 130nm vs 180nm chip noise results

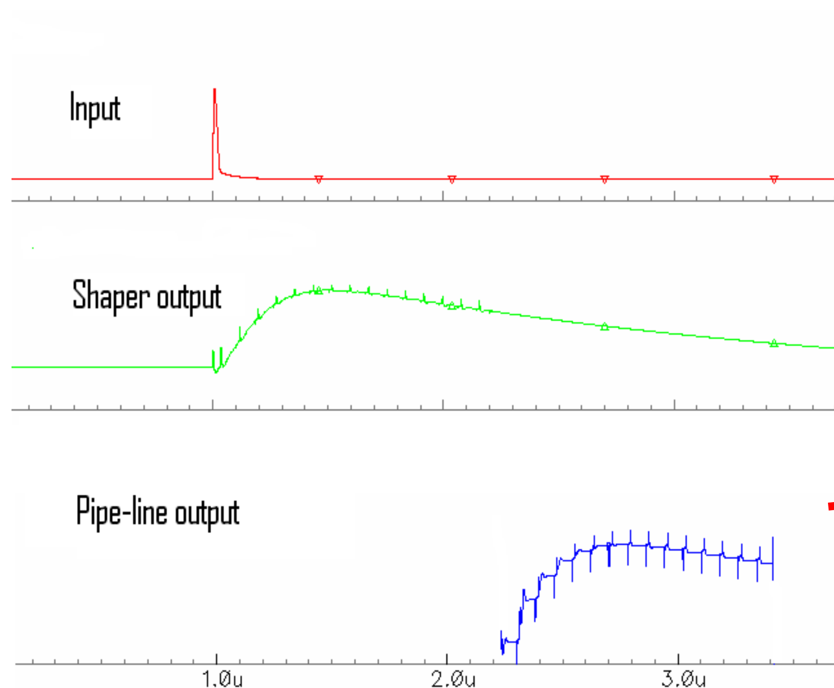
**Gain OK:** 29 mV/MIP OK
**Dynamics:** 30 MIPs @ 5%, 20 MIPS 1% OK
**Peaking time:** 0.8 – 2.5 µs (0.7 – 3 µs targeted)

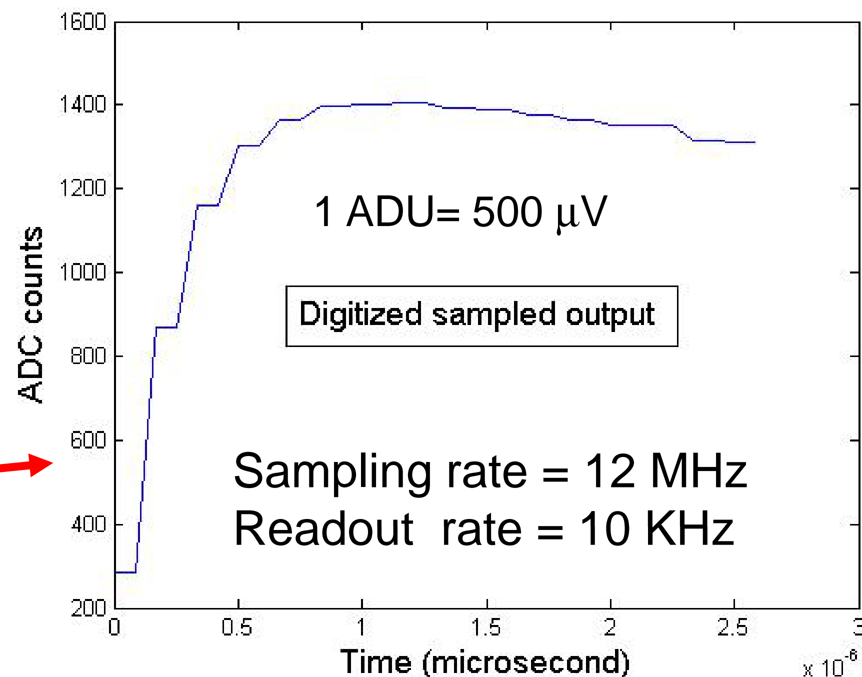



Power (Preamp+ Shaper) = 245 µW

| Noise: | 130nm @ 0.8 µs : | 850 + 14 | e-/pF | 245 µW | (150+95) |
|---|---|---|---|---|---|
| | 130nm @ 2 µs : | 625 + 9 | e-/pF | | |
| | [ 180nm @ 3 µs : | 375 + 10.5 | e-/pF | 210 µW | (70+140) ] |

# Digitized analog pipeline output




**Simulation of the analog pipeline (analog)** **Measured output of the ADC (pulser)**

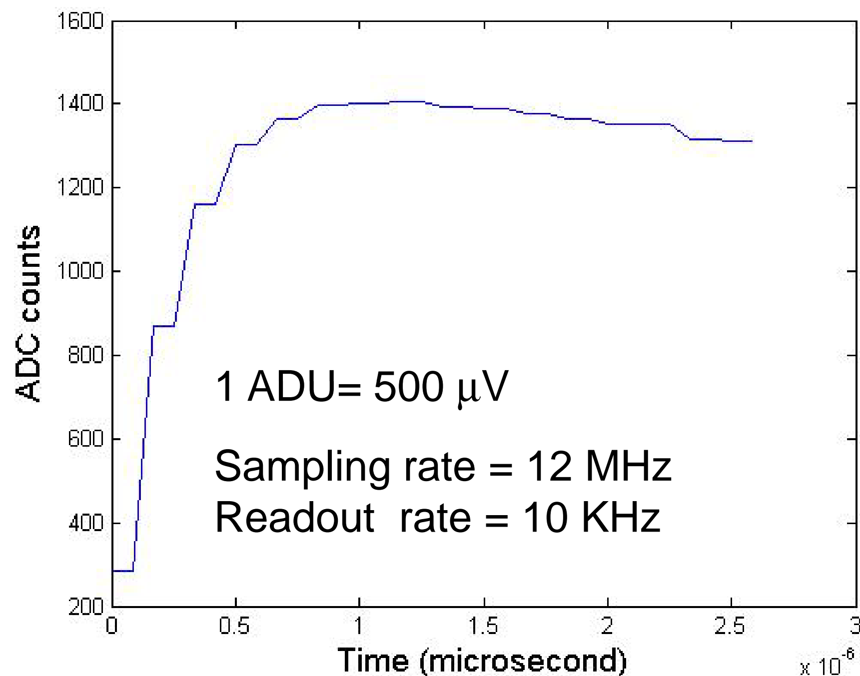
**Waveform distorted due to 1pF parasitic capacitance of the output pad connected for analog diagnostics on 2 out of four channels**

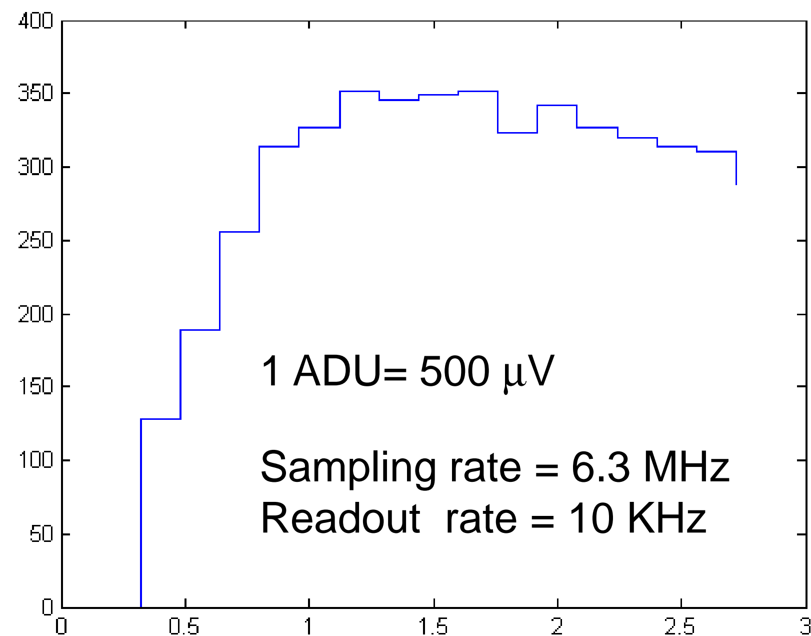
**Traces cut using IFB to get all shaper channels operational to ADC for beam tests**

**Chip 2 includes a voltage buffer between shaper and ADC**

# Digitized analog pipeline output
# Laser response of detector + 130nm chip

Digitized shaper output

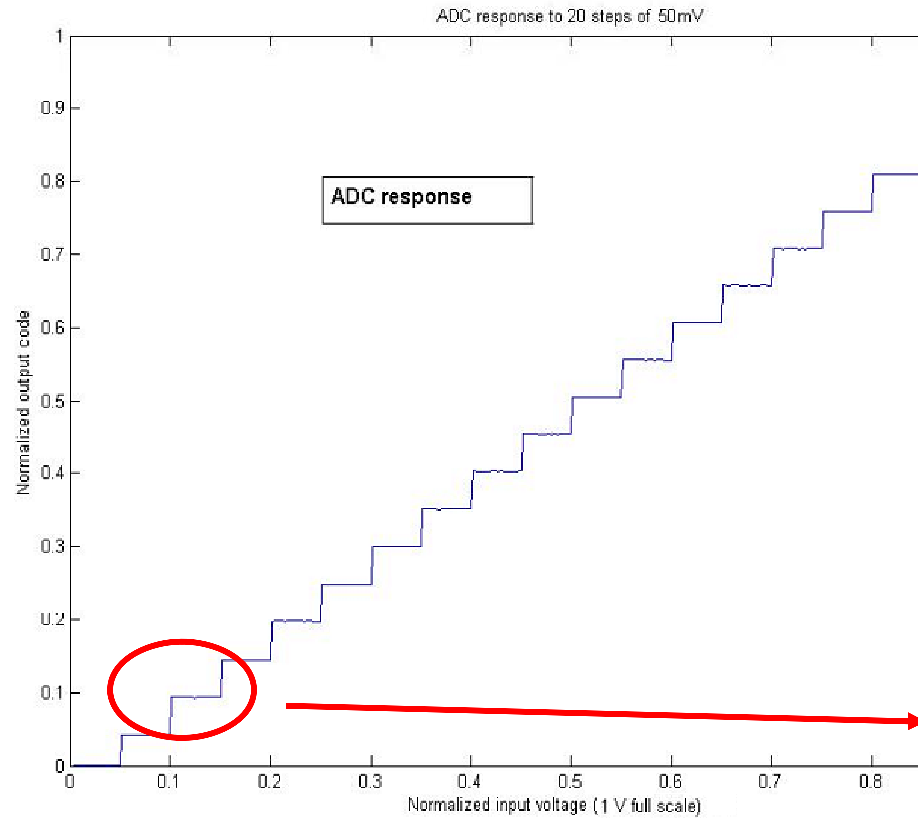


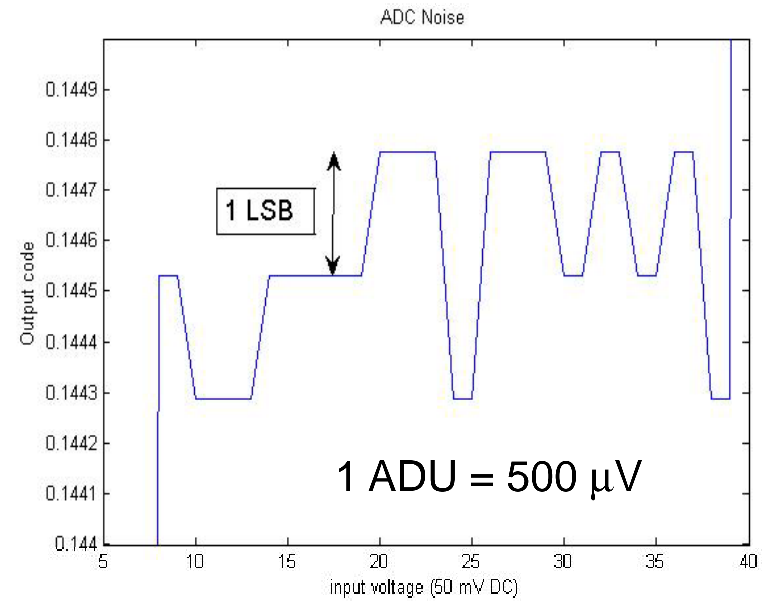




From pulser

From Laser diode + Silicon detector

# ADC evaluation




Noise= 4 LSBs

10 bits OK

# 130-1 chip's tests to come

- Lab tests: Measure ADC extensively

| | |
|---|---|
| Linearities | Integral, differential |
| Noise | Fixed pattern, random |
| Speed | Maximum clock rate |
| Accuracy | Effective number of bits |

- Beam tests at CERN next week

# 130 nm-2

LAPP Annecy le Vieux R. Hermel, D. Fougeron
LPNHE Paris T-H. Pham, R. Sefri

One channel test version in 130nm including:

- Preamp + shaper
- Improved pipeline (output buffer)
- Calibration channel (calibration caps)
- Calibration DAC

Presently under test at LAPP Annecy:

If OK, all analog blocks will be validated for a multi-channel version in 130nm aiming to read a full detector in 2008

# 130-2 tests under work (LAPP Annecy)

## Measure improved pipeline extensively

Denis Fougeron's (LAPPAnnecy) design

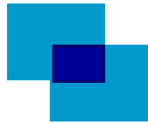
- Linearities
  - Integral, differential
- Noise
  - Pedestal fixed pattern, random noise
  - Maximum clock rate
- Droop
  - Hold data for 1 ms at the ILC
- ADC Driving

# Some issues with 130nm design

- Noise likely modeled pessimistic, but measured quite acceptable
  90nm could be less noisy (Manghisoni, Perugia 2006)
- Lower power supplies voltages reducing dynamic range
- Design rules more constraining
- Some (via densities) not available under Cadence
  Calibre (Mentor) required.
- Low Vt transistors leaky (Low leakage option available at regular Vt)

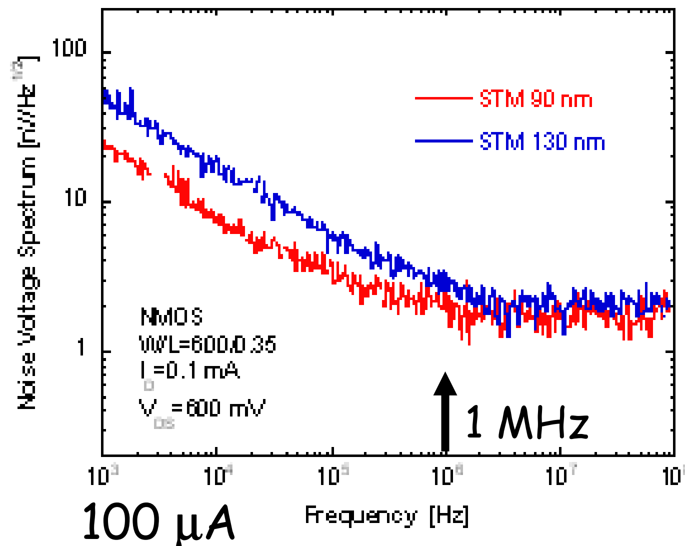
Manageable, UMC design kits user friendly,
Europractice very helpful.

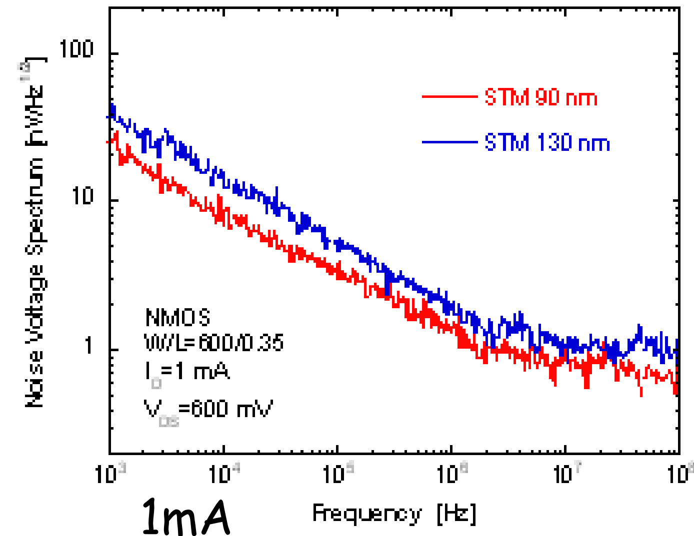
# 130-90nm noise evaluation (STM process)



## Noise and inversion region

*Manghisoni et al FE2006 Perugia*




- At low drain current both devices work in the weak inversion region → channel thermal noise is roughly the same for both devices
- At high drain current, a significant difference in the channel thermal noise can be detected ← device from the 90 nm technology works closer to weak inversion region
- Better 1/f noise performance provided by the STM 90 nm technology

VI International Meeting on Front-End Electronics, Perugia, May 18th 2006 12

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# 128-channel chip

## Goal: Equip a full detector

- Experience from lab test bench + laser/source and 2007 beam-tests
- Full 128-channels with :
  - Preamp-shapers
  - Sparsifier
  - Pipeline (8-sampling + 8-deep event buffer)
  - 12bits ADC
  - Digital
  - Calibration
  - Power cycling

# 128-channel chip

Improvments wrt chip 130-1:

- Increase order of the shaper to 3
  should reduce noise by 20-30% at a moderate increase in DC power.
- Pipeline (8-sampling + 8-deep event buffer) includes a buffer to drive the ADC.
- Full digital control
- Full calibration and channel disable
- Power cycling

# 128-channel chip

Paris, September 27-28th 2007 A. Comerma (Barcelone), Thanh Hung Pham, JFG

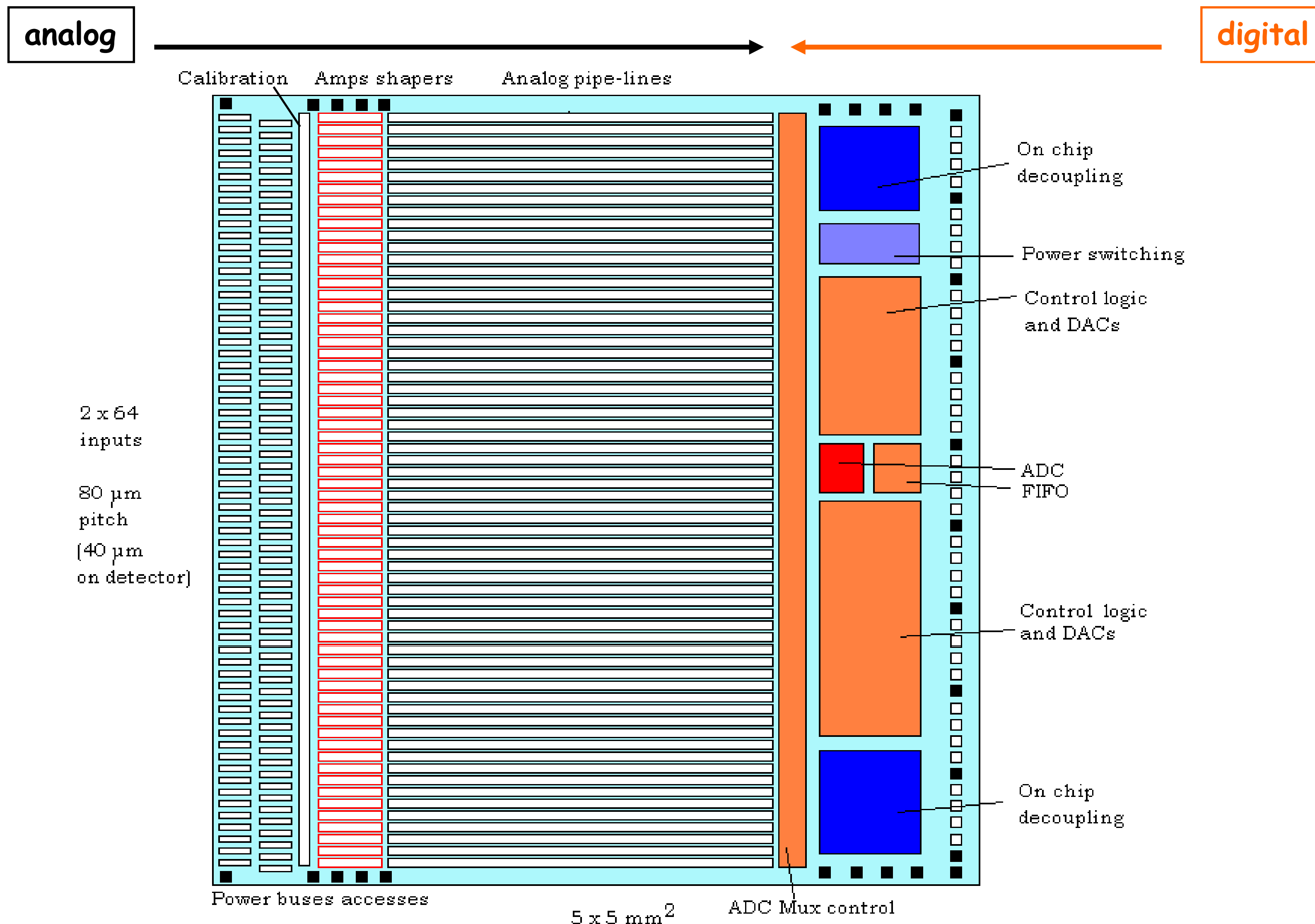
Tentative specs for a Silicon strips 128-channel readout chip

| | | | | I/O |
|---|---|---|---|---|
| **Preamp** | | | | |
| 128 | Inputs | | | 128 |
| 128 | Outputs | | | |
| 1 | Bias_preamp | Control DAC | 6 bits | |
| 1 | V_ref | “ | “ | 1 |
| 1 | Bias_buf “ | “ | “ | 1 |
| **Shaper** | | | | |
| | Inputs | | | |
| 128 | Outputs | | | |
| 1 | Bias_shaper | “ | “ | 1 |
| 2 | V_pole, v_zero | “ | “ | 1 |
| **Sparsifier** | | | | |
| 3 x 128 | Inputs | | | |
| 128 | Outputs | | | |
| 1 | Auto-zero control | | | |
| 1 | Bias_sum_1 | “ | “ | 1 |
| 1 | Bias_sum_2 | “ | “ | 1 |
| 1 | Bias_comp | “ | “ | 1 |
| 1 | Threshold | “ | “ | 1 |
| 128 | Outputs | | | |

***4 more pages…***

Chip splits in 14 functional blocks

# 128-channel chip



# Connexion to detector and external

Layout allows :

- Wire-bonding
- Stud-bonding
- Bump-bonding
- Even 3D interconnect…

# Planned Digital Front-End

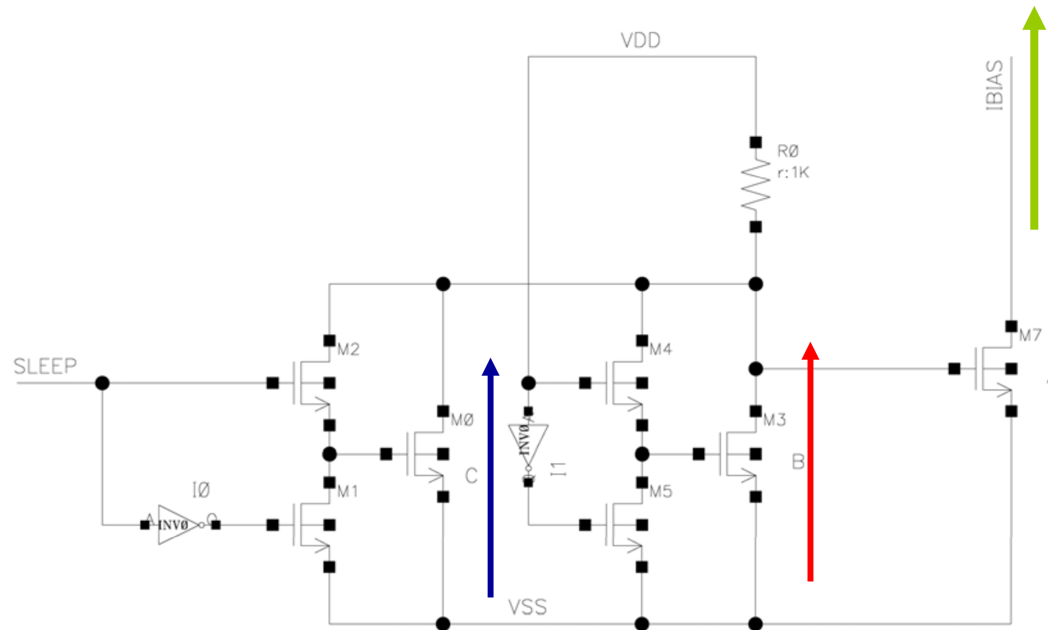
- Chip control
- Buffer memory
- Processing for
  - Calibrations
  - Amplitude and time least squares estimation, centroids
  - Raw data lossless compression

- Tools
  - Cadence DSM Place and Route tool
  - Digital libraries in 130nm CMOS available
  - Synthesis from VHDL/Verilog
  - SRAM
  - Some IPs: PLLs

Need for a mixed-mode simulator

# Power cycling

Switch the current sources between zero and a small fraction ($10^{-2}$ to $10^{-3}$ ) of their nominal values




This option switches the current source feeding both the preamplifier & shaper between 2 values:

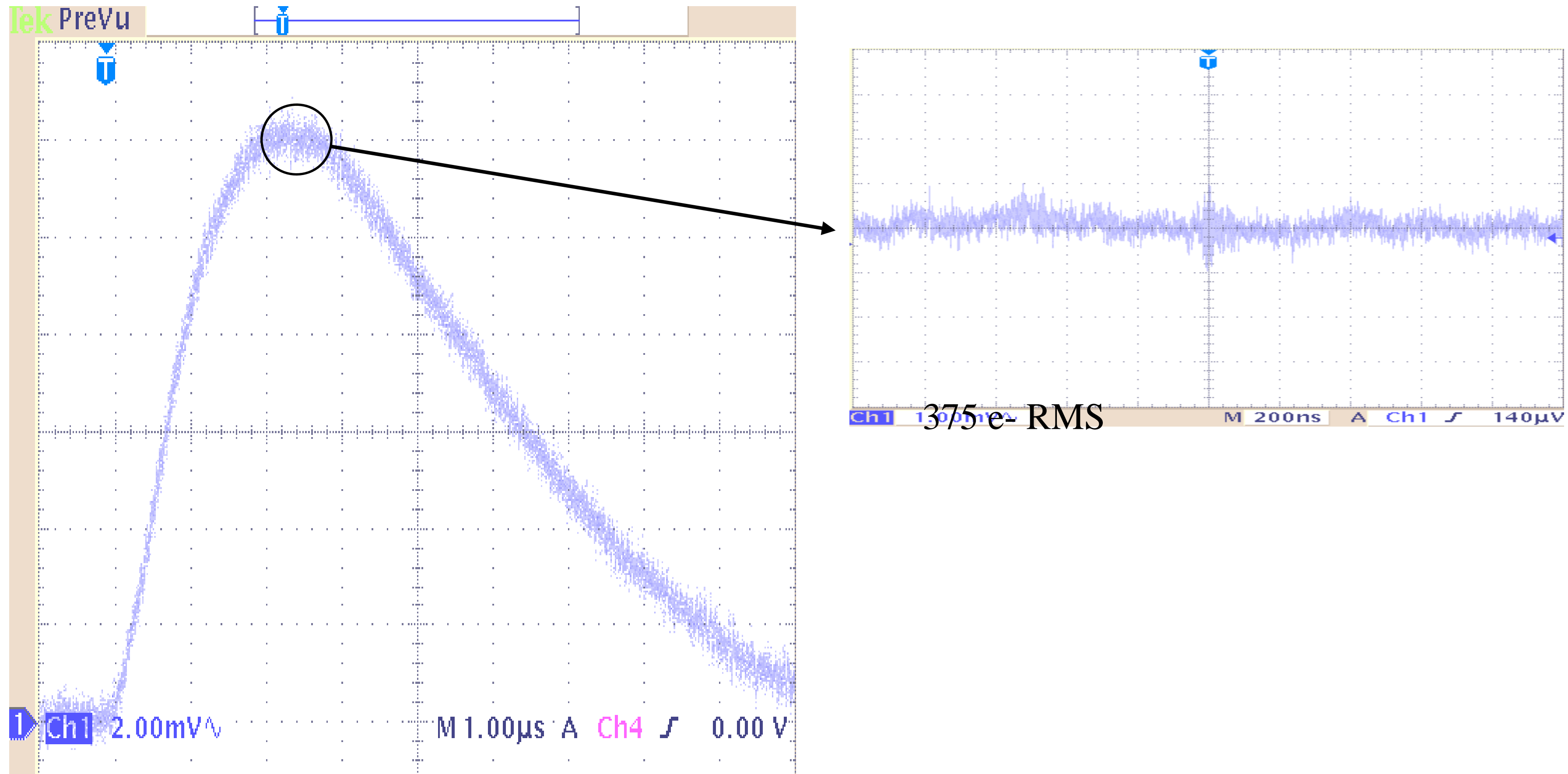
*Zero* or a *small fraction* (0.1% - 1%) of biasing current is held during « power off ».

Zero-power option tested on 180nm chip (slow, but works)

# Schedule

| | |
|---|---|
| Nov '07 | - Complete 130-1 and -2 chips tests |
| December '07 | - Complete analog and digital blocks |
| January '07 | - Merge |
| February '08 | - Submission, test bench development |
| | - Card development for TPC+Silicon tests |
| May '08 | - Tests: lab |
| July '08 | - Connexion to HPK detectors<br>- Tests with HPK detectors: laser, source<br>- Beam tests. |
| September '08 | - OK |

# Shaper output noise




375 e- +10.4 e-/pF input noise with chip-on-board wiring
275 + 8.9/pFsimulated

# Tests Conclusions

12 chips tested ('05)

The UMC CMOS 180nm process is mature and reliable:

- Models mainly OK
- Only one transistor failure over 12 chips
- Process spreads of a few %

Beam tests in October '06 at DESY

Encouraging results regarding CMOS DSM

→ go to 130nm

# Conclusion

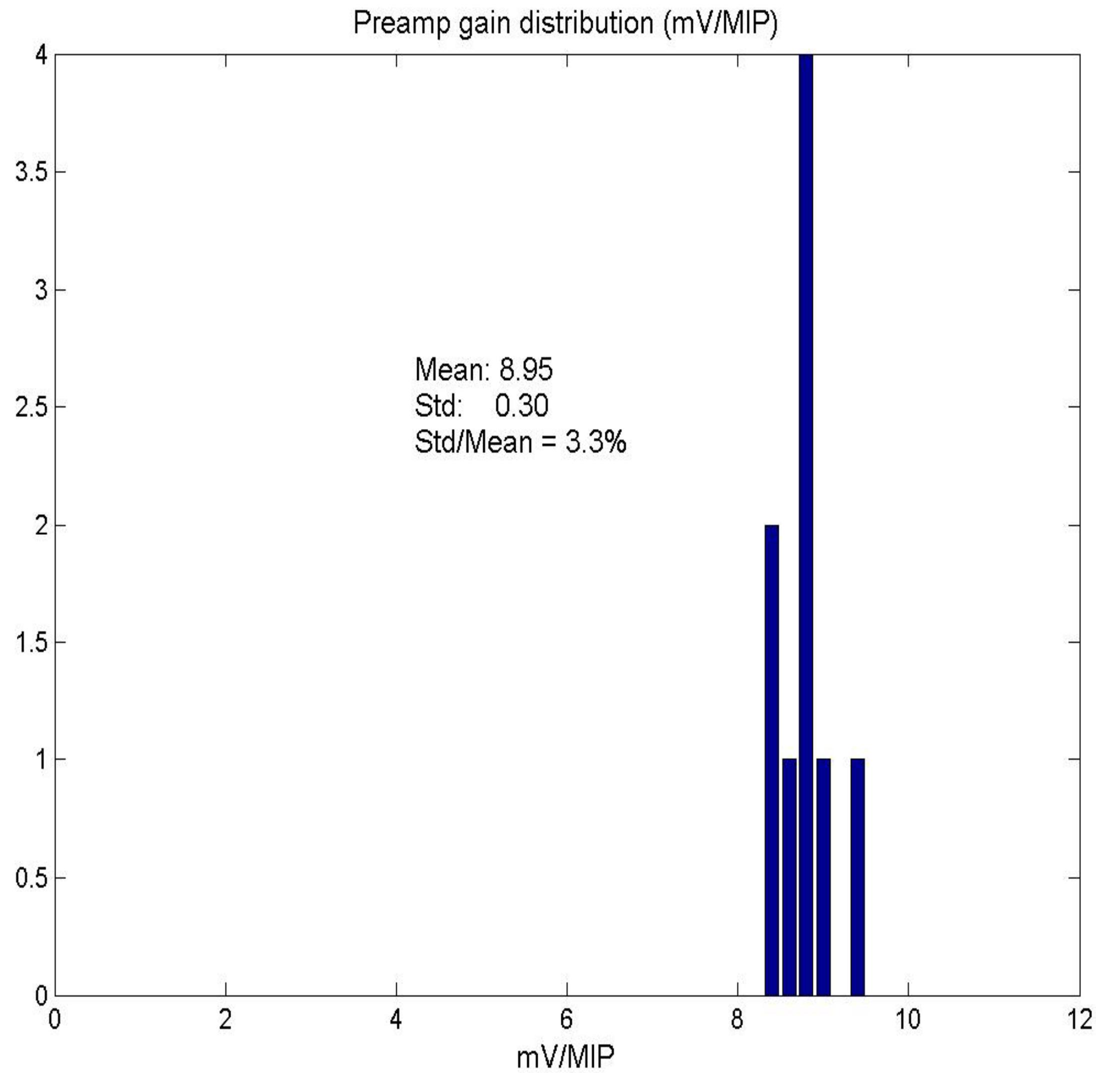
These CMOS 130 designs and first test results demonstrate the feasibility of a highly integrated front-end for Silicon strips (or large pixels) with

- DC power under 500μW/ch
- Silicon area under 50 x 1000 $\mu^2$/ch

*The End …*

# Backup

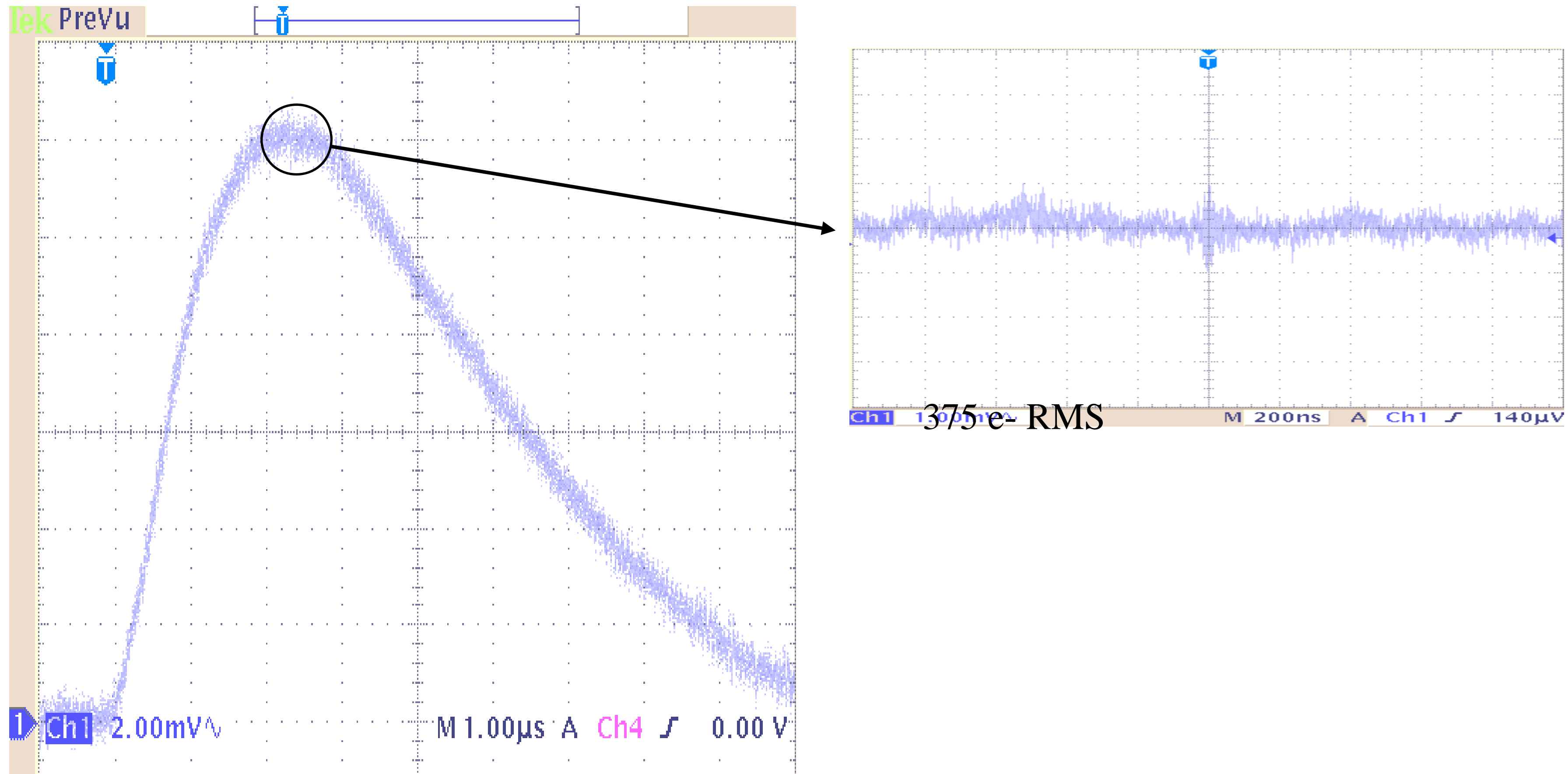
# Process spreads




Preamp gains statistics

**Process spreads within a wafer: 3.3 %**

# Shaper output noise

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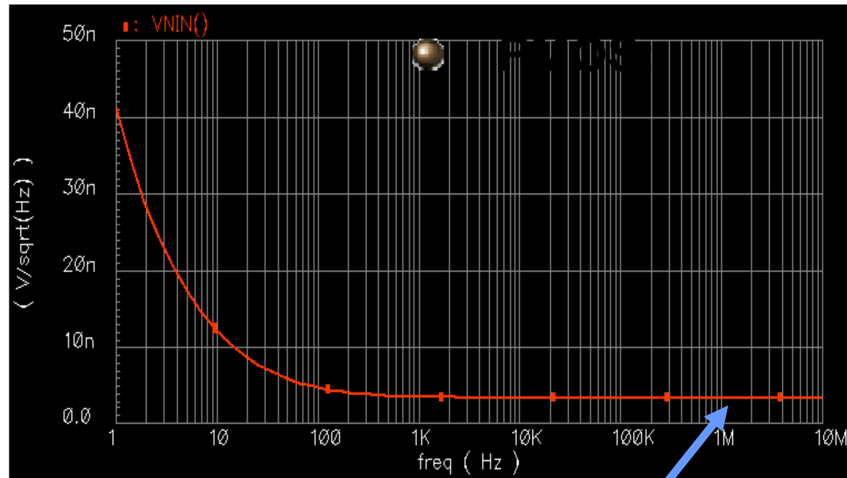
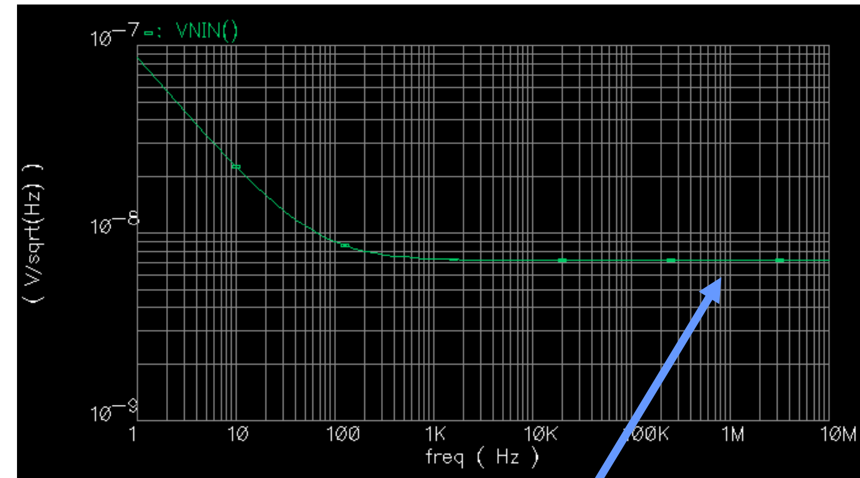
# Possible issues: noise: 130nm vs 180nm (simulation)

**PMOS**




180nm

gm=944.4uS
***1MHz → 3.508nV/sqrt(Hz)***

Thermal noise hand calculation = 3.42nV/sqrt(Hz)

130nm

gm=815.245uS
***1MHz → 7.16nV/sqrt(Hz)***

Thermal noise hand calculation = 3.68nV/sqrt(Hz)

**Thermal noise measured by Wladimir Gromov (NIKHEF) with IBM130nm OK**

# Transistors leaks

- Gate-channel due to tunnel effect
- Through channel when transistor switched-off

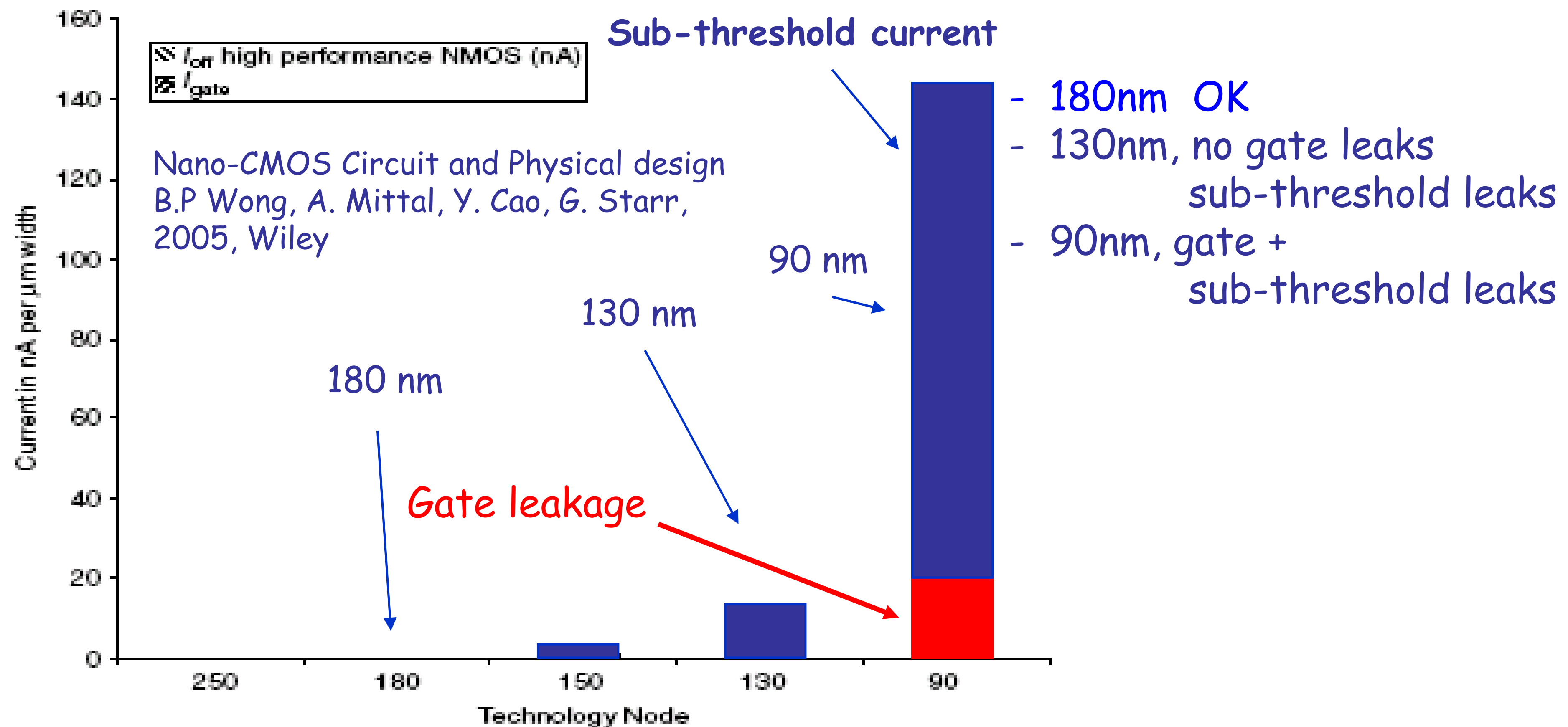


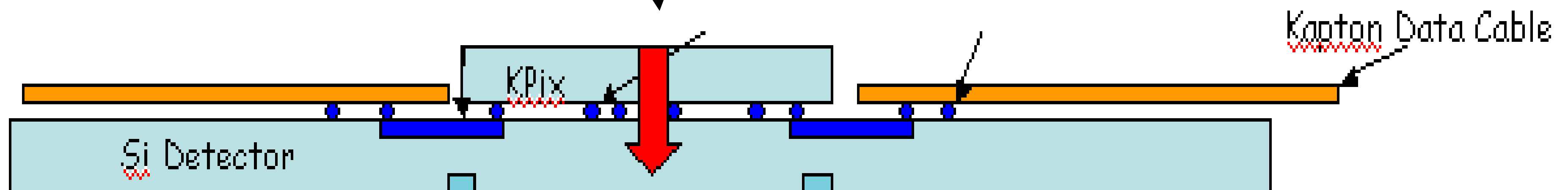

Figure 1.2 $I_{gate}$ and subthreshold leakage versus technology.

- 180nm OK
- 130nm, no gate leaks
  sub-threshold leaks
- 90nm, gate +
  sub-threshold leaks

# Wiring Detector to FE Chips

~~Wire bonding~~

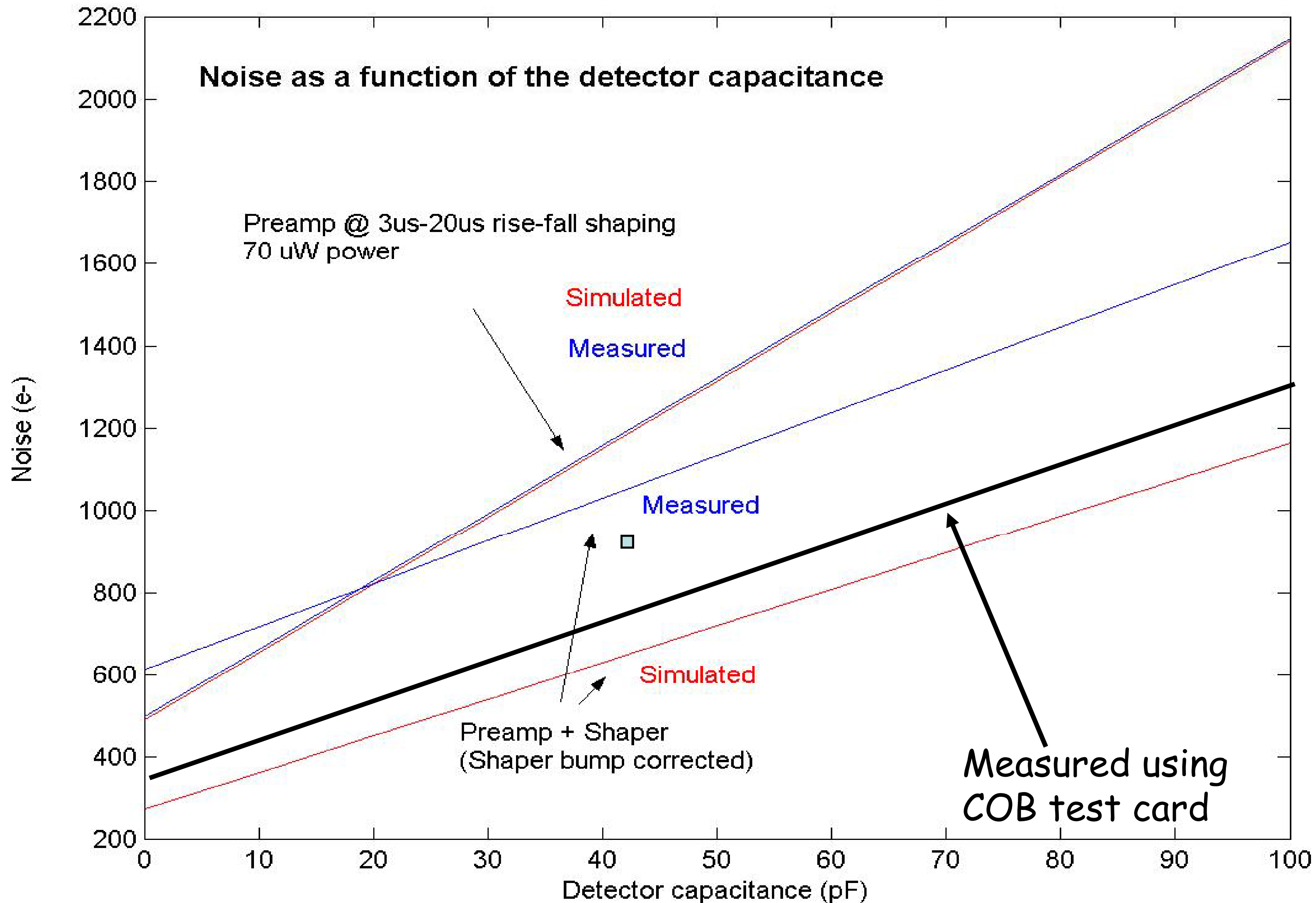
Flip Chip Technology




**Courtesy: Marty Breidenbach (Cal SiD)**

**OR (later)**

# Noise summary (180nm)



# 3D Wiring

## Process flow for 3D Chip

- 3 tier chip (tier 1 may be CMOS)
  - 0.18 um (all layers)
  - SOI simplifies via formation
- Single vendor processing

1) Fabricate individual tiers

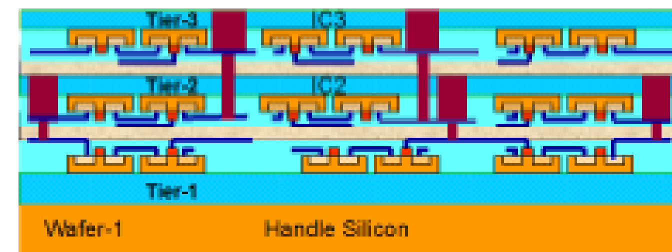
2) Invert, align, and bond wafer 2 to wafer 1

Oxide bond

3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten

3D Via

4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



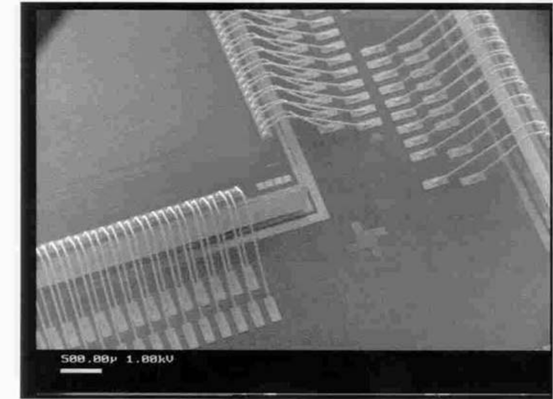

May 2006 FEE 2006 38

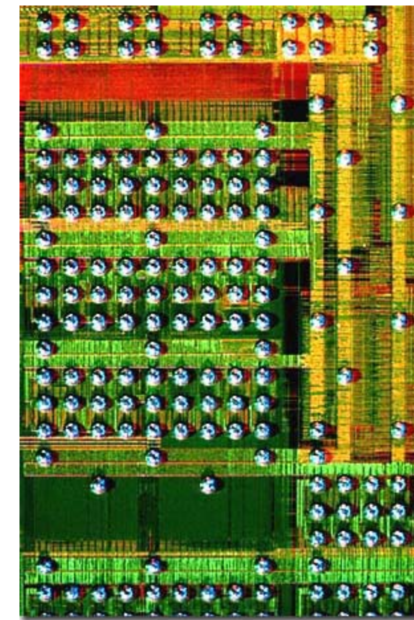
**Courtesy: Ray Yarema, FEE 2006, Perugia**

*Manuel Lozano (CNM Barcelona)*

# Chip connection

- Wire bonding
  - Only periphery of chip available for IO connections
  - Mechanical bonding of one pin at a time (sequential)
  - Cooling from back of chip
  - High inductance (~1nH)
  - Mechanical breakage risk (i.e. CMS, CDF)
- Flip-chip
  - Whole chip area available for IO connections
  - Automatic alignment
  - One step process (parallel)
  - Cooling via balls (front) and back if required
  - Thermal matching between chip and substrate required
  - Low inductance (~0.1nH)

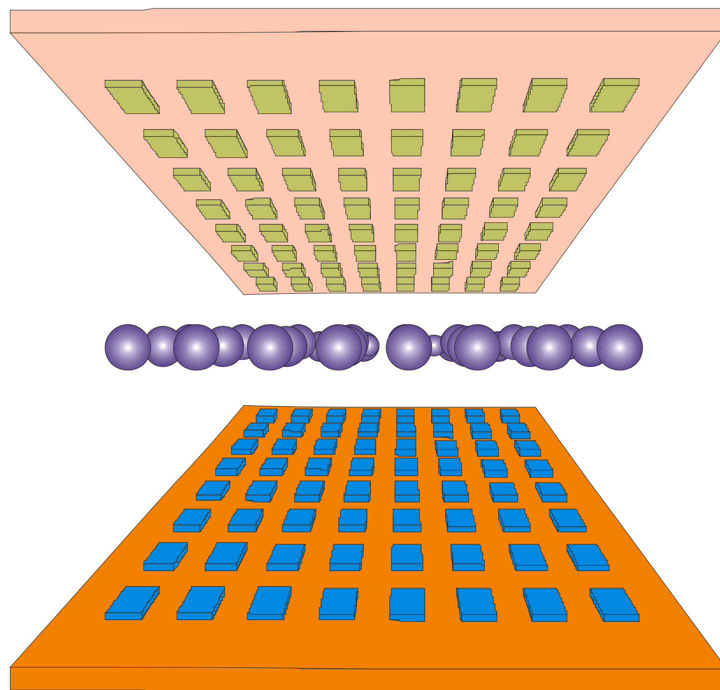


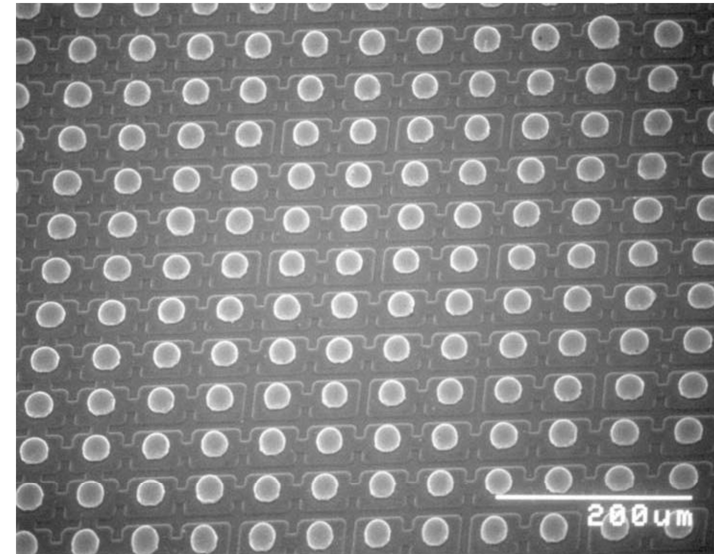


*Manuel Lozano (CNM Barcelona)*

# Bump bonding flip chip technology

- Electrical connection of chip to substrate or chip to chip face to face
  flip chip
- Use of small metal bumps
  bump bonding






CNM

- Process steps:
  - Pad metal conditioning: Under Bump Metallisation (UBM)
  - Bump growing in one or two of the elements
  - Flip chip and alignment
  - Reflow
  - Optionally underfilling

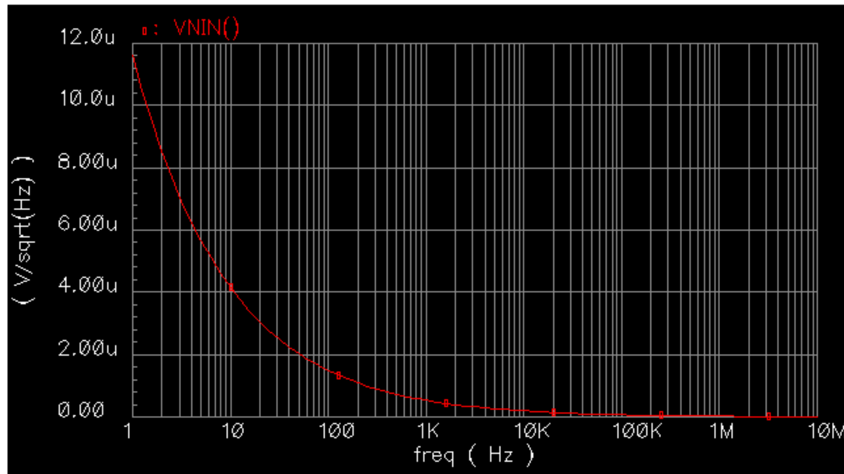
# *Manuel Lozano (CNM Barcelona)*
# Bump bonding flip chip technology

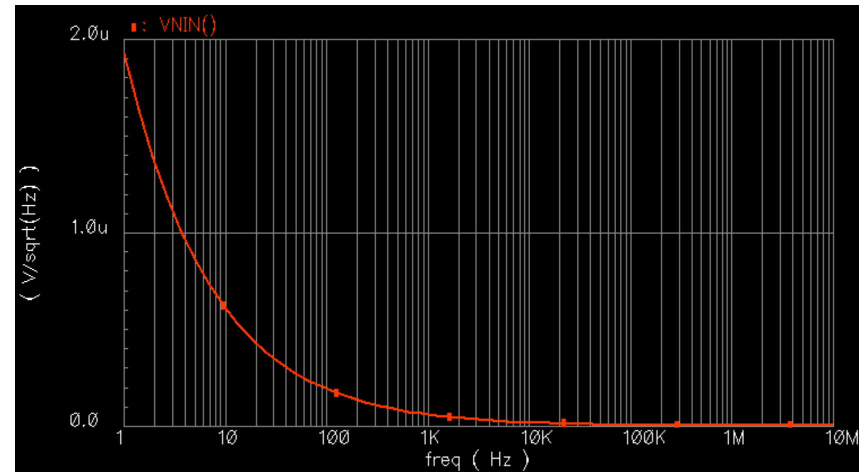
- Expensive technology
  - Especially for small quantities (as in HEP)
  - Big overhead of NRE costs
- Minimal pitch reported: 18 μm but ...
- Few commercial companies for fine pitch applications (< 75 μm)

- Bumping technologies
  - Evaporation through metallic mask
  - Evaporation with thick photoresist
  - Screen printing
  - Stud bumping (SBB)
  - Electroplating
  - Electroless plating
  - Conductive Polymer Bumps
  - Indium evaporation

# Noise: 130nm vs 180nm (simulation)

**NMOS :**




130nm
W/L = 50u/0.5u
Ids=48.0505u,Vgs=260mV,Vds=1.2V
gm=772.031uS,gms=245.341uS,gds=6.3575uS
***1MHz --> 24.65nV/sqrt(Hz)***
100MHz --> 5nV/sqrt(Hz)
Thermal noise hand calculation = 3.78nV/sqrt(Hz)

180nm
W/L=50u/0.5u
Ids=47uA,Vgs=300mV,Vds=1.2V
gm=842.8uS,gms=141.2uS,gds=16.05uS
***1MHz --> 4nV/sqrt(Hz)***
10MHz --> 3.49nV/sqrt(Hz)
Thermal noise hand calculation = 3.62nV/sqrt(Hz)